

SPECIFICATION FOR APPROVAL

- () Preliminary Specification
- (●) Final Specification

Title	TFT-LCD Timing Controller
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BUYER	
MODEL	BULL_REV(HS353149)

SUPPLIER	LG.Philips LCD Co., Ltd.
*MODEL	BULL_REV(HS353149)
LG Part Number	0IHYL-0045A

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Please return 1 copy for your confirmation with your signature and comments.

**Products Engineering Dept.
LG. Philips LCD Co., Ltd**

TFT-LCD Timing Controller

P/N : 0IHYL-0045A

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RECORD OF REVISIONS 1/2

Revision No	Revision Date	Page	Description
1.0	Apr. 21. 2003	-	First Draft (Preliminary)
2.0	May. 20. 2003	8 15 19	1. Option change : No signal Selection “H”→ Must be “L” 2. GOE Waveform Change 3. Application Circuit Change : PLL Block Application Analog Decoder IC parts delete
3.0	May. 20. 2003	3 4,7,8 8 19	1. Function Change 2. 10 2. Output Pin Change : VSY → NP_O (pin10) 3. Option Pin Change : - FSEL : Add to No Signal Black Function(pin21) - ATMN : Add to NTSC/PAL Auto Detection Function (Pin39) 4. Application Circuit Change
3.1	May. 28. 2003	16,19 18~20	1. TQFP 48pin Package Drawing Change 2. Application Circuit Change
3.2	June. 03. 2003	8,9 15,16	1. Signal description Change (Page 8 → Page8,9) 2. Add to Vertical Display Method (Page 15,16)
3.3	June. 09. 2003	10	Signal description Change : MP15 (L ↔ H)
3.4	July. 18. 2003	1 22 23 24 25~28 29~30	1. Contents item change 2. Application Circuit Change*1 - Add to SIGNAL IN/OUT BLOCK, Add to -5V circuit in DC-DC CONVERTER BLOCK, VCOM BLOCK change all, Capacitance(C75, C80) & resistance(R127,R133) change in VGL BLOCK. - Add to VCO circuit & C90(100pF → 150pF) change in PLL BLOCK. HPOSI circuit change in TIMING CONTROLLER BLOCK, Resistance(R170, R173) change in VSM BLOCK. - Reset resistance R177(68K Ω→10K Ω) change, Some ports(NP, MODE1, MODE2,MODE3) delete. [*1] Reference number of resistance & capacitor base on Ver. 3.4 circuit diagrams. For more detail changed description, please refer to the application notes and Ver.3.3 circuit diagrams. 3. Add to Application Circuit Notes 4. Add to Component List

1. General description

BULL_REV IC, which is developed by LG.Philips LCD is timing controller for controlling 7" wide TFT-LCD Module. It is improved LG first ASIC version BULL(0IHYL-0041A) of minor problem.

2. Function

It is using **19.4MHz input clock**, and create the divide signal for comparing PLL phase.

- (1) Outside of Controller IC, it is composed PLL circuit with additional VCO, LPF, pulls the sync signal of PAL, NTSC into CSY pin and it is used for creating MCLK by PDP signal with DIV signal which is created inside of IC.
- (2) It creates signal for driving Source drive IC, Gate drive IC by using Horizontal Sync 'HSY', Vertical Sync 'VSY', input signal.
 - 1) The signal for Source Drive IC : SSPL, SSPLR, LRO, SRESET, SOE, SSC, SSC1, SSC2
 - 2) The signal for Gate Drive IC : UDO, GSP, GSC, GOE
 - 3) The signal for driving VCOM : VCAC
 - 4) The signal for controlling polarity change of display : FRP
- (3) MODE1, MODE2, MODE3 is for selecting of display mode.
- (4) It is for controlling the reverse of signal, left/right, up/down by using LRS, UDS.
- (5) Synchronous, Successive Data Sampling is possible by controlling MP15.
- (6) It is shown the start of Horizontal Line over ODD, EVEN input signal by STRN controlling.
- (7) It can be changed a position of horizontal Start Pulse by SSP_S1, SSP_S2.
- (8) It can be changed the vertical Start Pulse as 1H by GSP_S.
- (9) At NTSC Vertical wide mode 2nd GSC controlled by GSS_S
- (10) Use input signal N_P it can be controlled NTSC/PAL Mode.

If you set NTSC/PAL auto detection selection ATMN "H", it operates internal detection signal. If ATMN is "L", NTSC/PAL selected by N_P input Signal.

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5. Block Diagram

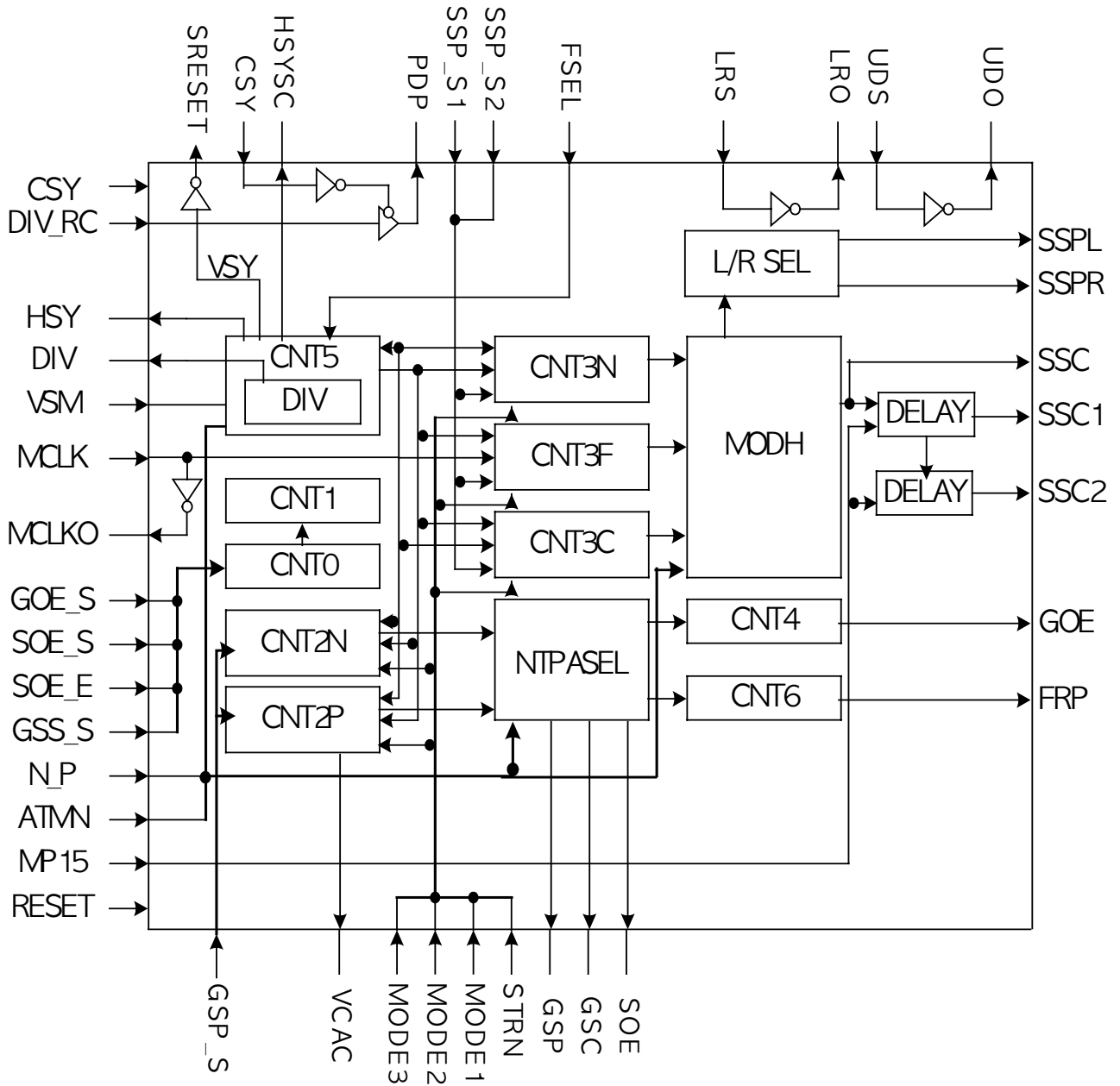


Fig. 2 Block Diagram

6. Main function description

It makes all of control signal which is needed at external input signal MCLK that is from external PLL Block.

CNT0 : Set up the timing of output signal(GOE, SOE,GSC,GSS) which is based on Hsync. input signal of each control is GOE_S, SOE_S,GSC_E,GSS_S, it is based on 'H', 'L' setting.

CNT1 : Set up the timing as taking the signal value which is set up at CNT0(GOE_R,GOE_F, SOE_R, SOE_F, GSC_R,GSS_F), set up Vertical Reset signal.

CNT2N : Block of setting the vertical control signal when input NTSC signal.
Set up the Vertical control signal by taking MODE1,2,3 signal from outside and GSC_VW, GOE_IN,SOE_IN, GSS_IN from CNT1.

CNT2P : Block of setting the vertical control signal when input PAL signal.
Set up the Vertical control signal by taking MODE1,2,3 signal from outside and GSC_VW, GOE_IN,SOE_IN, GSS_IN from CNT1.

CNT3N : Set up Source Start Pulse(SSP) and Source Sampling Clock(SSC) of Normal mode by taking HSY from CNT 5 Block.

CNT3F : Set up Source Start Pulse(SSP) and Source Sampling Clock(SSC) of Full mode by taking HSY from CNT 5 Block.

CNT3C : Set up Source Start Pulse(SSP) and Source Sampling Clock(SSC) of wide mode by taking HSY from CNT 5 Block.

CNT4 : Change Gate Output Enable(GOE) at NTPASEL to 'L' by taking RESET at power on and FVSY

CNT6 : Make several clock delayed FRP ,which is from NTPASEL.

NTPASEL : Choose Vertical Control Signal of NTSC/PAL Mode

MODH : Choose Horizontal Control Signal of each MODE

Delay : Make SSC1, SSC2 output signal delay certain timing as following MP15

CNT5 : Set up the output signal to meet the synchronous of PLL.
The block of sensing NTSC/PAL signal and sensing of no-signal.

L/R SEL : Decide the SSPL and SSPR by the external input L/R signal.

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7. Pin Configuration

Table 1. Pin Configuration

Pin No.	Name	Type	I/O Pad
1	CSY	In	Normal
2	VSM	In	Normal
3	VDD	Power	-
4	LRS	In	Pull Down
5	UDS	In	Pull Down
6	MODE3	In	Pull Up
7	MODE2	In	Pull Up
8	MODE1	In	Pull Up
9	HSY	Out	4mA
10	NP_O	Out	4mA
11	GND	GND	-
12	DIV	Out	4mA
13	DIV_RC	In	Normal
14	PDP	Out	Tri-state(4mA)
15	RESET	In	Normal
16	SOE_S	In	Pull Down
17	SOE_E	In	Pull Down
18	MCLK	In	Normal
19	VDD	Power	-
20	MCLKO	Out	4mA
21	FSEL	In	Pull Up
22	UDO	Out	4mA
23	GSP	Out	4mA
24	GSC	Out	4mA

Pin No.	Name	Type	I/O Pad
25	GOE	Out	4mA
26	SSPL	Out	Tri-state(4mA)
27	GND	GND	-
28	LRO	Out	4mA
29	SRESET	Out	4mA
30	SOE	Out	4mA
31	SSC	Out	8mA
32	SSC1	Out	8mA
33	SSC2	Out	8mA
34	SSPR	Out	Tri-state(4mA)
35	VDD	Power	-
36	GSP_S	In	Pull Down
37	STRN	In	Pull Up
38	N_P	In	Pull Up
39	ATMN	In	Pull Up
40	SSP_S2	In	Pull Down
41	SSP_S1	In	Pull Down
42	GOE_S	In	Pull Down
43	GND	GND	-
44	GSS_S	In	Pull Down
45	VCAC	Out	4mA
46	HSYSC	Out	4mA
47	FRP	Out	4mA
48	MP15	In	Pull Down

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8. Signal Description

Table 2. Signal Description

No.	Name	PIN	Function	Description
1	CSY	I	Sync Signal Input	Composite Sync Signal or Horizontal Sync Signal Input (Synchronization Period : Hi time)
2	VSM	I	Sync Signal Input	Vertical Modulated Signal from Composite Signal or Vertical Sync Signal Input (Synchronization Period : Hi time)
3	VDD	-	Power	3.3V DC Voltage (± 10%)
4	LRS	I	Horizontal Scanning Direction Select	When LRS "H" : SSPL"Enable", SSPR "Hi-Z", LRO"L" (Right → Left Direction Scan) When LRS "L" : SSPL"Hi-Z", SSPR "Enable", LRO"H" (Left → Right Direction Scan)
5	UDS	I	Vertical Scanning Direction Select	When UDS "H" : UDO="L" (Down → Up Direction Scan) When UDS "L" : UDO="H" (Up → Down Direction Scan)
6	MODE3	I	Screen Display Mode Selection 3	Refer to table 5, fig 3-1 ~ 3-5
7	MODE2	I	Screen Display Mode Selection 2	Refer to table 5, fig 3-1 ~ 3-5
8	MODE1	I	Screen Display Mode Selection 1	Refer to table 5, fig 3-1 ~ 3-5
9	HSY	O	Horizontal sync Output(Negative)	Horizontal sync Output(Negative)
10	NP_O	O	NTSC/PAL Selection output	When ATMN "H" : NP_O = "H" at NTSC, NP_O = "L" at PAL input (Auto detect mode) When ATMN "L" : NP_O output depends on input NTSC/PAL select signal N_P. [N_P="H" (NTSC), N_P="L" (PAL)]
11	GND	-	Ground	Ground
12	DIV	O	Horizontal Display Position Control	Horizontal Display Position is controlled by DIV. PDP signal synchronized DIV. PLL Circuit block makes MCLK. (refer to application circuit Fig.12)
13	DIV_RC	I	Horizontal Display Position Control Input	For external horizontal display position control. DIV output adopted external circuit and DIV_RC synchronized PDP Signal. (refer to application circuit Fig.12)
14	PDP	O	Phase detect Pulse	It is made by CSY and DIV. External PLL circuit was synchronized by PDP Signal. (refer to Fig.4, Fig.12)
15	RESET	I	Reset	Logic Initial Reset
16	SOE_S	I	SOE Rising Selection	SOE(INH) Rising position Control. Refer to Fig.8, Table 4.

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No.	Name	PIN	Function	Description
17	SOE_E	I	SOE Falling Selection	SOE(INH) falling position selected by this pin. Refer to Fig.8, Table4.
18	MCLK	I	Main Clock	It's a synchronized Clock which is made by PLL circuit. It is used timing controller main clock.(typ : 19.4MHz) Refer to circuit diagram Fig.12.
19	VDD	-	Power	3.3V DC Voltage ($\pm 10\%$)
20	MCLKO	O	Clock output	For synchronizing PLL MCLKO inverted output MCLK (typ : 19.4MHz) Refer to circuit diagram Fig.12.
21	FSEL	I	No Signal Detect Selection Pin	FSEL"H" : Black Screen Display when No Signal. FSEL"L" : none use
22	UDO	O	Gate Drive IC Up/Down Selection Output	When UDS "H" : UDO="L" (Down \rightarrow Up Direction Scan) When UDS "L" : UDO="H" (Up \rightarrow Down Direction Scan)
23	GSP	O	Gate Drive IC Start Pulse	It is synchronized GSC falling edge which is 1 Horizontal High time Period width and 1 Vertical Frequency. The wave form refer to Fig.6-1~Fig.7-3 .
24	GSC	O	Gate Drive IC Shift Clock	It's used Gate Drive IC Shift Clock. Timing Diagram refer to Fig.8.
25	GOE	O	Gate Drive IC Output Enable	Gate Drive IC Output is disabled when GOE Low time. Timing Diagram refer to Fig.8.
26	SSPL	O	Horizontal Start Pulse(Left)	When LRS "H" : SSPL"Enable", SSPR "Hi-Z", LRO"L" (Right \rightarrow Left Direction Scan) When LRS "L" : SSPL"Hi-Z", SSPR "Enable", LRO"H" (Left \rightarrow Right Direction Scan)
27	GND	-	Ground	Ground
28	LRO	O	Horizontal Scanning Direction Output (Source Drive IC Input)	When LRS "H" : SSPL"Enable", SSPR "Hi-Z", LRO"L" (Right \rightarrow Left Direction Scan) When LRS "L" : SSPL"Hi-Z", SSPR "Enable", LRO"H" (Left \rightarrow Right Direction Scan)
29	SRESET	O	Source Drive IC Reset	It is used for reset of Source Driver IC which is generated the same as positive Vsync. If you need Vsync you can use SRESET signal.
30	SOE	O	Source Drive IC Output Enable	Image Data enter into Liquid Crystal Panel data line from Source Drive IC when SOE rising and falling time. Source Drive IC output moves to Hi-Z When SOE High Period. The wave form refer to Refer to Fig.6-1~Fig.7-3 and Fig.8.
31	SSC	O	Source D-IC Shift Clock	It is used for Source Drive IC Shift Clock which is differ from Image Display Mode.
32	SSC1	O	Source D-IC Shift Clock 1	SSC1 is delayed Clock from SSC which delay time is 17ns(typ) It's used for successive sampling mode when MP15= "H" .

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No.	Name	PIN	Function	Description
33	SSC2	O	Source D-IC Shift Clock 2	SSC2 is delayed Clock from SSC1 which delay time is 17ns(typ) It's used for successive sampling mode when MP15= "H" .
34	SSPR	O	Horizontal Start Pulse(Right)	When LRS "H" : SSPL "Enable", SSPR "Hi-Z", LRO "L" (Right → Left Direction Scan) When LRS "L" : SSPL "Hi-Z", SSPR "Enable", LRO "H" (Left → Right Direction Scan)
35	VDD	-	Power	3.3V DC Voltage (± 10%)
36	GSP_S	I	GSP Position Control	GSP Signal outputs referred to page 17-1~18-3 timing Diagram when GSP_S is "L" If GSP_S is "H" above GSP shifted 1 Horizontal Period.
37	STRN	I	ODD/EVEN GSP Position Control	Referred to Fig.6-1~ Fig.7-3.
38	N_P	I	Manual NTSC/PAL Selection	When ATMN "H" : NP_O = "H" at NTSC, NP_O = "L" at PAL input (Auto detect mode) When ATMN "L" : NP_O output depends on input NTSC/PAL select signal N_P. [N_P= "H" (NTSC), N_P= "L" (PAL)]
39	ATMN	I	NTSC/PAL Auto Selection	When ATMN "H" : NTSC/PAL Automatically detect. When ATMN "L" : NTSC/PAL manually detect.
40	SSP_S2	I	SSP Start Position Control	Horizontal Screen Display Position controlled by SSP_S2, SSP_S1 which is change SSPL,SSPR position. Refer to Fig.5.
41	SSP_S1	I	SSP Start Position Control	Horizontal Screen Display Position controlled by SSP_S2, SSP_S1 which is change SSPL,SSPR position. Refer to Fig.5.
42	GOE_S	I	GOE Width Control	This option control GOE Width which is control Gate Drive IC Output High Period. Refer to Fig.8.
43	GND	-	Ground	Ground
44	GSS_S	I	GSC(GSS) Control at NTSC Mode	It is Control GSC output when NTSC Vertical expand mode(Cinema,Wide2), which is refer to Fig6-2~6-3 and page 19.
45	VCAC	O	Common Voltage Control Signal	It's used for Liquid Crystal Panel Common Voltage Control Signal. Refer to Fig.6-1~ Fig.7-3.
46	HSYSC	O	Hsync Output for IR3Y29B (Negative)	It's used for CHROMA IC Hsync Input.
47	FRP	O	Video Signal Polarity Control	It's used for Video image Signal Polarity Control input.
48	MP15	I	Sampling Mode selection	Selection of Source Driver IC Data Sampling Mode. MP15 "H" : Successive Mode (sampling clock : SSC,SSC1,SSC2) MP15 "L" : Simultaneous Mode (sampling clock : SSC), (SSC1,SSC2 = "L")

9. Electrical SPECIFICATION

(1) Absolute Maximum Rating

Item	Parameter	Min	Typ	Max	Unit	Notes
V _{DD}	Input Voltage	-0.3	-	3.8	V	
V _I	CMOS input Signal Voltage	-0.3	-	V _{DD} +0.3	V	
V _O	CMOS output Signal Voltage	-0.3	-	V _{DD} +0.3	V	
T _{STG}	Storage temperature	-40	-	+125	°C	
T _{LSTG}	Lead Temperature(Soldering, 4sec)	-	-	+260	°C	

※ Notes : This can be destroyed over the maximum rating, LPL didn't assure the secure of component. All function of this component must be operated under normal operating condition

(2) Normal Operating Condition

Item	Parameter	Min	Typ	Max	Unit	Notes
V _{DD}	Input Voltage	3.0	3.3	3.6	V	
V _{IH}	CMOS Input Signal Voltage	2.0	-	V _{DD}	V	
V _{IL}	CMOS Output Signal Voltage	0	-	0.8	V	
T _{OPR}	Operating Temperature	-30	25	85	°C	
T _{REOPR}	Reliability Operating Temperature	-10	25	85	°C	

10. Screen Display range

1) NTSC (N_T = 'H', ATMN = 'L')

(1) Horizontal Direction (Refer to Fig.5)

- a1) FULL Display MODE : Display 480 Pixel
- a2) Normal Display MODE : Display 376 Pixel
- a3) WIDE Display MODE : Display 480 Pixel

(2) Vertical Direction (Refer to page 17-1~17-3)

- b1) FULL Display MODE : Display 23H ~ 256H
- b2) CINEMA Display MODE : Display 54H ~ 229H
- b3) WIDE2 Display MODE : Display 50H ~ 236H

2) PAL (N_T = 'L', ATMN = 'L')

(1) Horizontal Direction (Refer to Fig.5)

- a1) FULL Display MODE : Display 480 Pixel
- a2) Normal Display MODE : Display 376 Pixel
- a3) WIDE Display MODE : Display 480 Pixel

(2) Vertical Direction (Refer to page 18-1~18-3)

- b1) FULL Display MODE : Display 28H ~300H [eliminate (14n +1, 14n + 7)].
- b2) CINEMA Display MODE : Display 47H ~ 280H
- b3) WIDE2 Display MODE : Display 35H ~303H [eliminate (22n +1, 22n +16)].

11. MODE Setting

Table 3. Mode Setting

MODE3	MODE2	MODE1	MODE	Description	Source	Notes
H	H	H	FULL MODE	Display evenly by controlling frequency evenly of whole display under vertical, horizontal range of input signal. It uses 16:9 wide input. Display wide horizontally in case of the display ratio 4:3.	16:9 image	Fig. 3-1
H	H	L	WIDE MODE	Change horizontal Clock to make image output of center display similar with image input to loose incompatibility with center display under 4:3 Full mode.	16:9 image	Fig. 3-2
L	H	H	NORMAL MODE	Display to make same with real display size under input 4:3 display signal, which Left/right side displayed black.	4:3 Image	Fig. 3-3
H	L	L	CINEMA MODE	The main display area of wide signal(16:9) such like Letter focus size. Use Full mode horizontally, use more wide than usual vertically to make similar with real image	Letter Focus Wide Input	Fig. 3-4
L	L	H	WIDE2 MODE	Make the display same with WIDE horizontally and use CINEMA vertically to control center display under 4:3 display mode. Sort of vertical signal can't be seen.	16:9 image	Fig. 3-5
L	L	L	test	Test mode	test	test
L	H	L	test	Test mode	test	test
H	L	H	test	Test mode	test	test

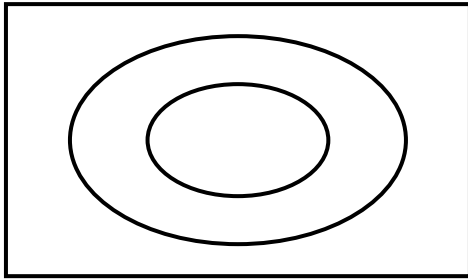


Fig. 3-1 FULL Display MODE

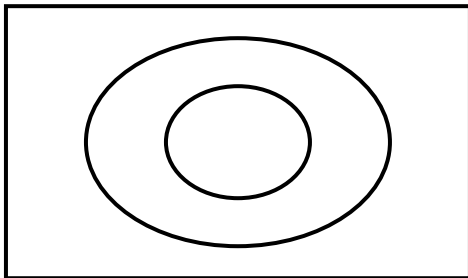


Fig. 3-2 WIDE Display MODE

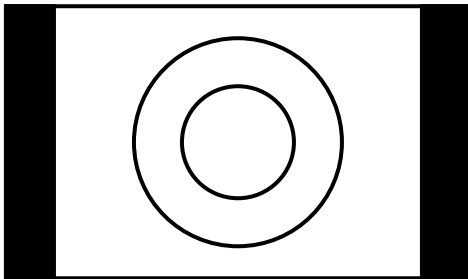


Fig. 3-3 NORMAL Display MODE

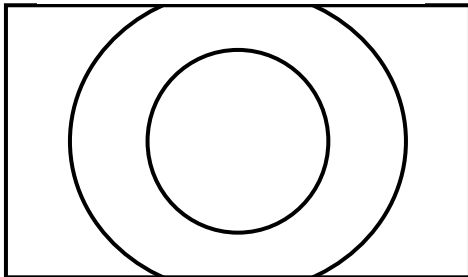


Fig. 3-4 CINEMA Display MODE

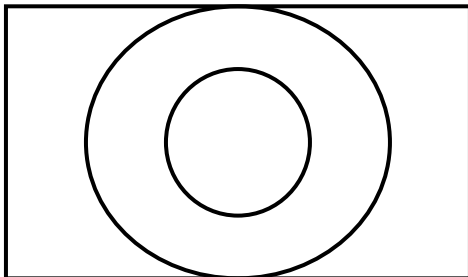


Fig. 3-5 WIDE2 Display MODE

12. DIV, HSY, HSYSC Generation

Internal DIV, HSY, HSYSC Timing Description

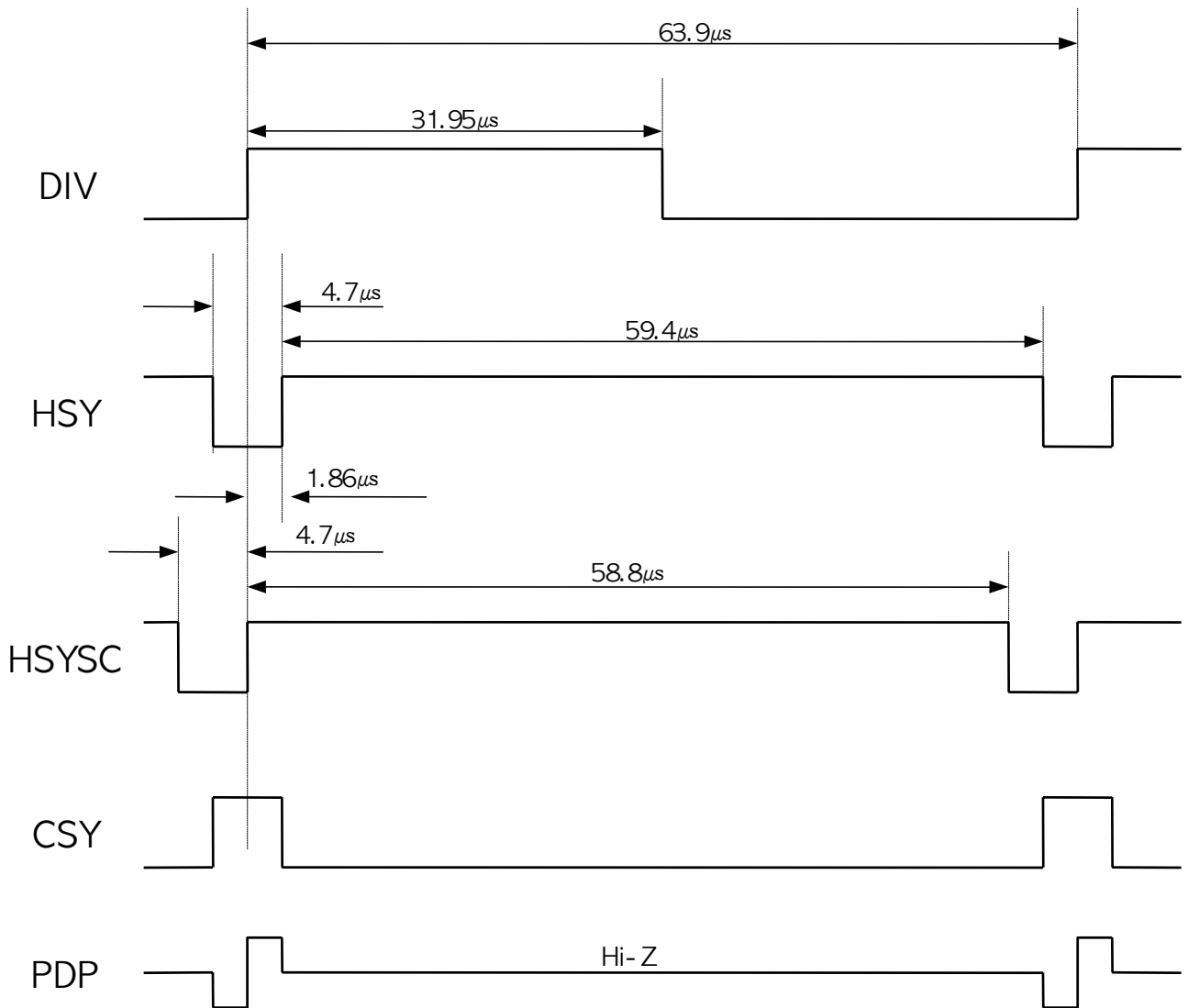


Fig. 4 DIV, HSY, HSYSC Generation

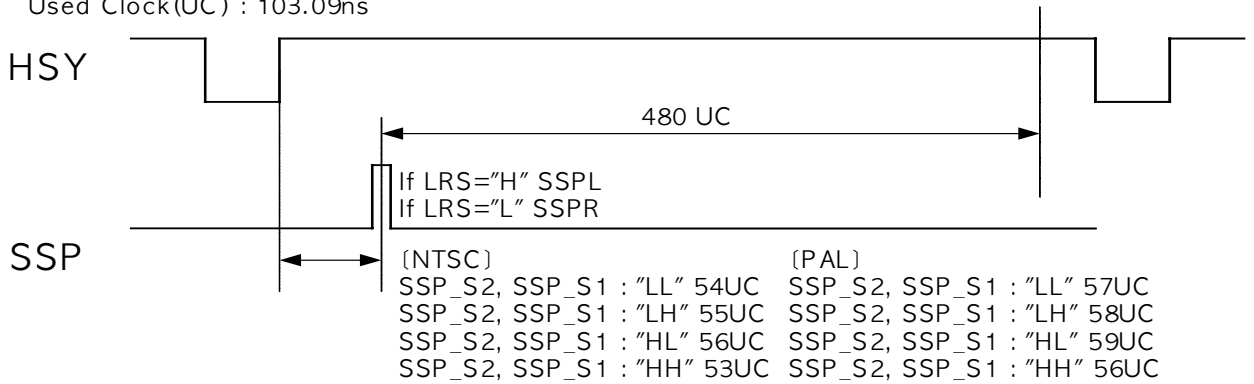
TFT-LCD Timing Controller

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13. Horizontal Display Position

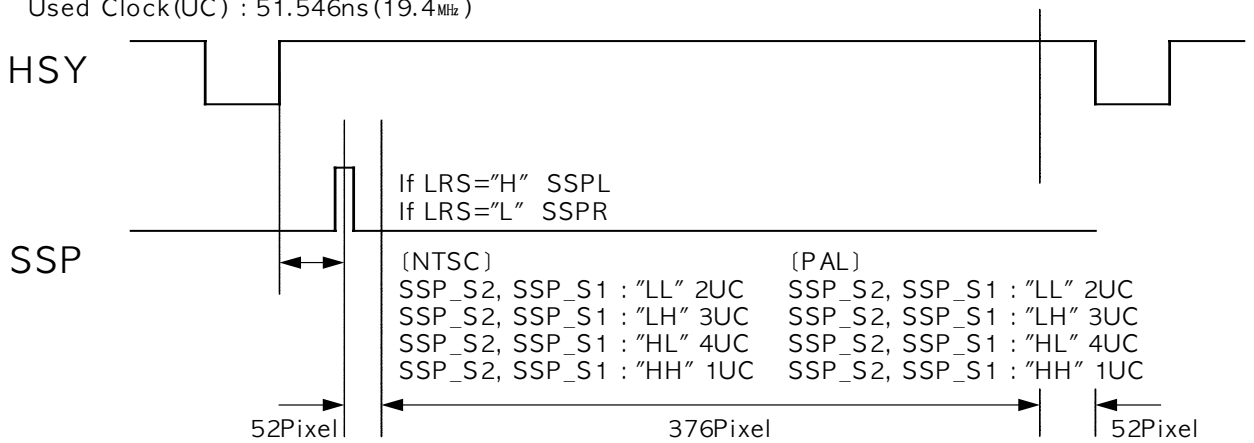
1) Full Mode

MCLK : 51.546ns (19.4MHz)
Used Clock(UC) : 103.09ns



2) Normal Mode

MCLK : 51.546ns (19.4MHz)
Used Clock(UC) : 51.546ns (19.4MHz)



3) Wide Mode

MCLK : 51.546ns (19.4MHz)
Used Clock(UC) : Five kinds of Clock (92.78ns, 96.64ns, 103.09ns, 108.8ns, 113ns)

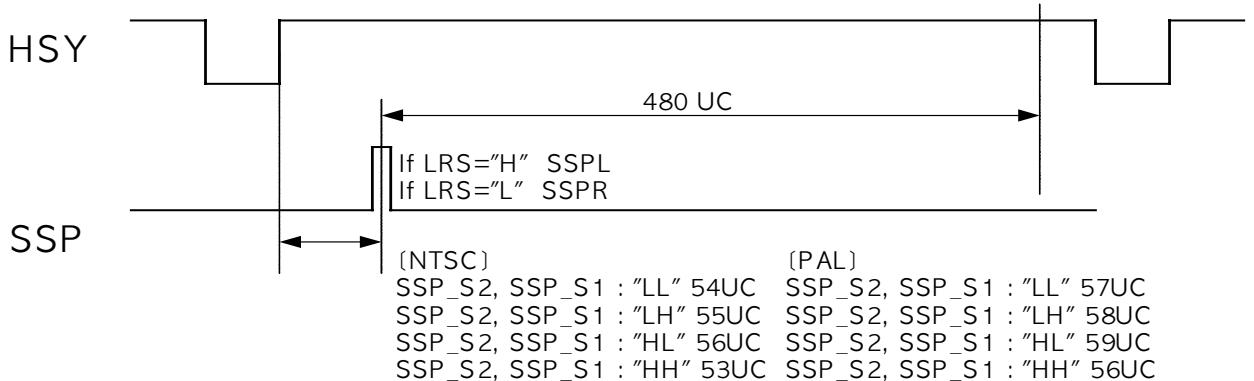


Fig. 5 Horizontal Display Position

14. Vertical Display Method(NTSC)

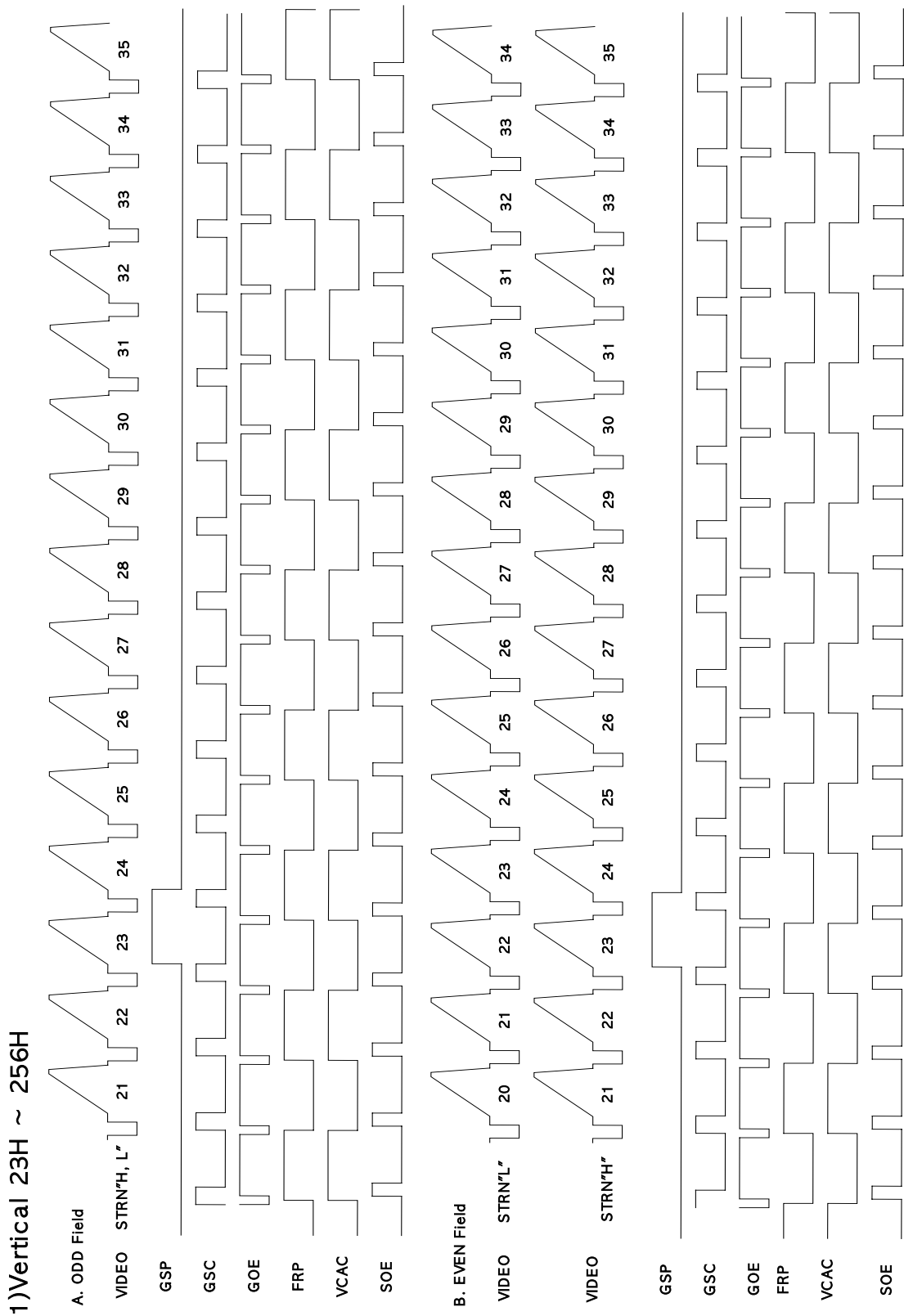


Fig. 6-1 Vertical Display Position1 (NTSC)

14. Vertical Display Method(NTSC)

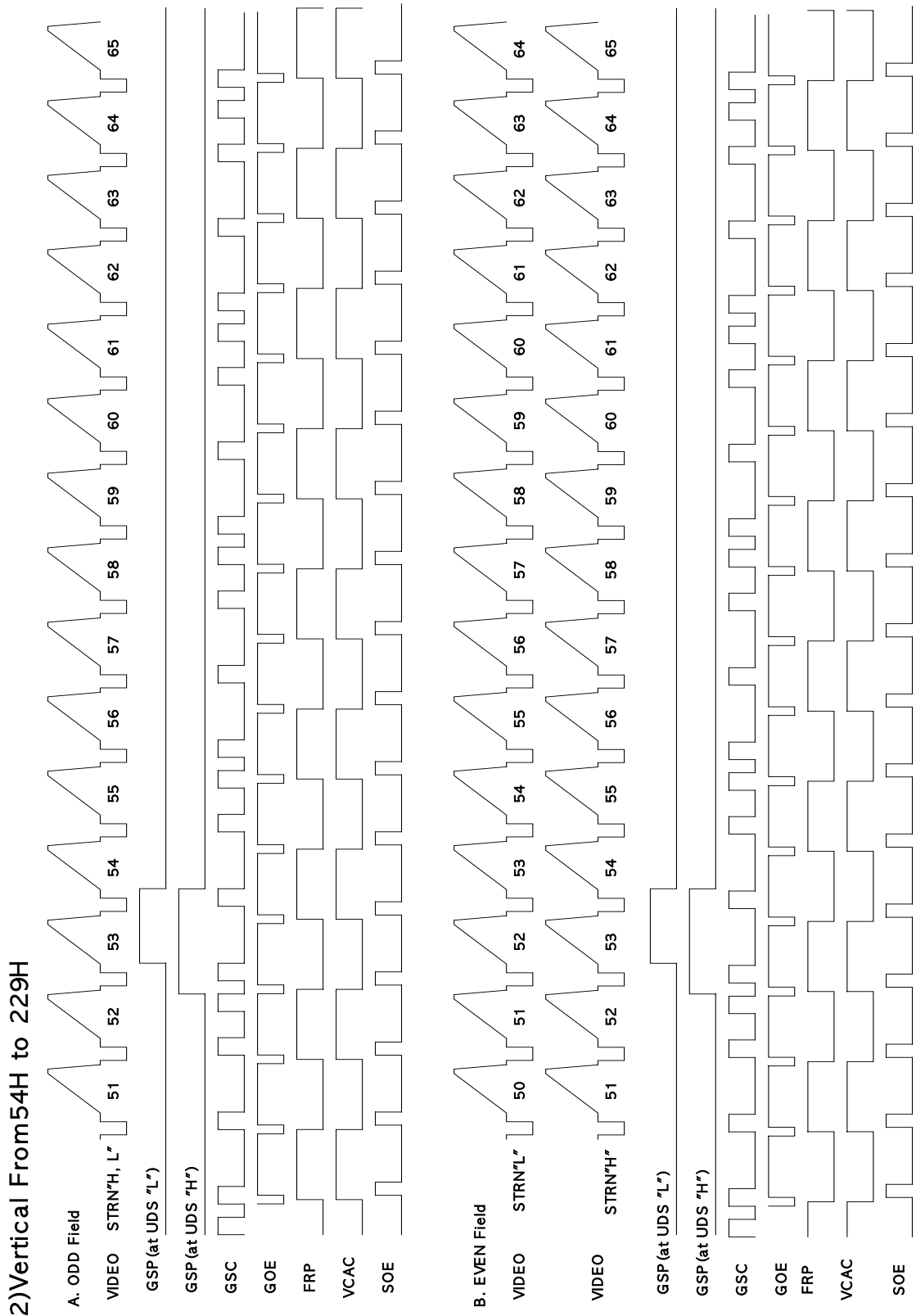


Fig. 6-2 Vertical Display Position2 (NTSC)

14. Vertical Display Method(NTSC)

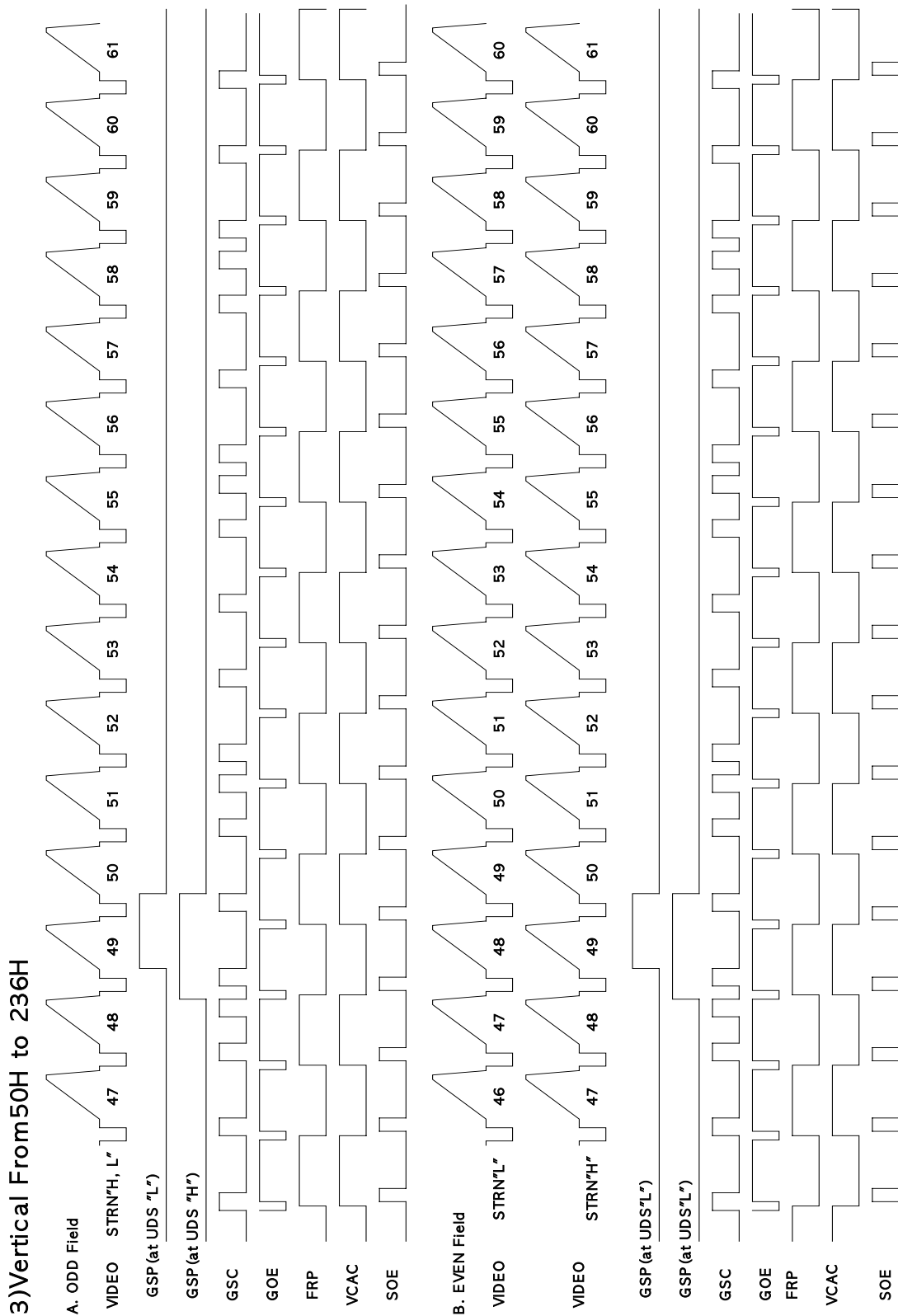


Fig. 6-3 Vertical Display Position3 (NTSC)

15. Vertical Display Method(PAL)

1) Vertical 28H ~ 300H

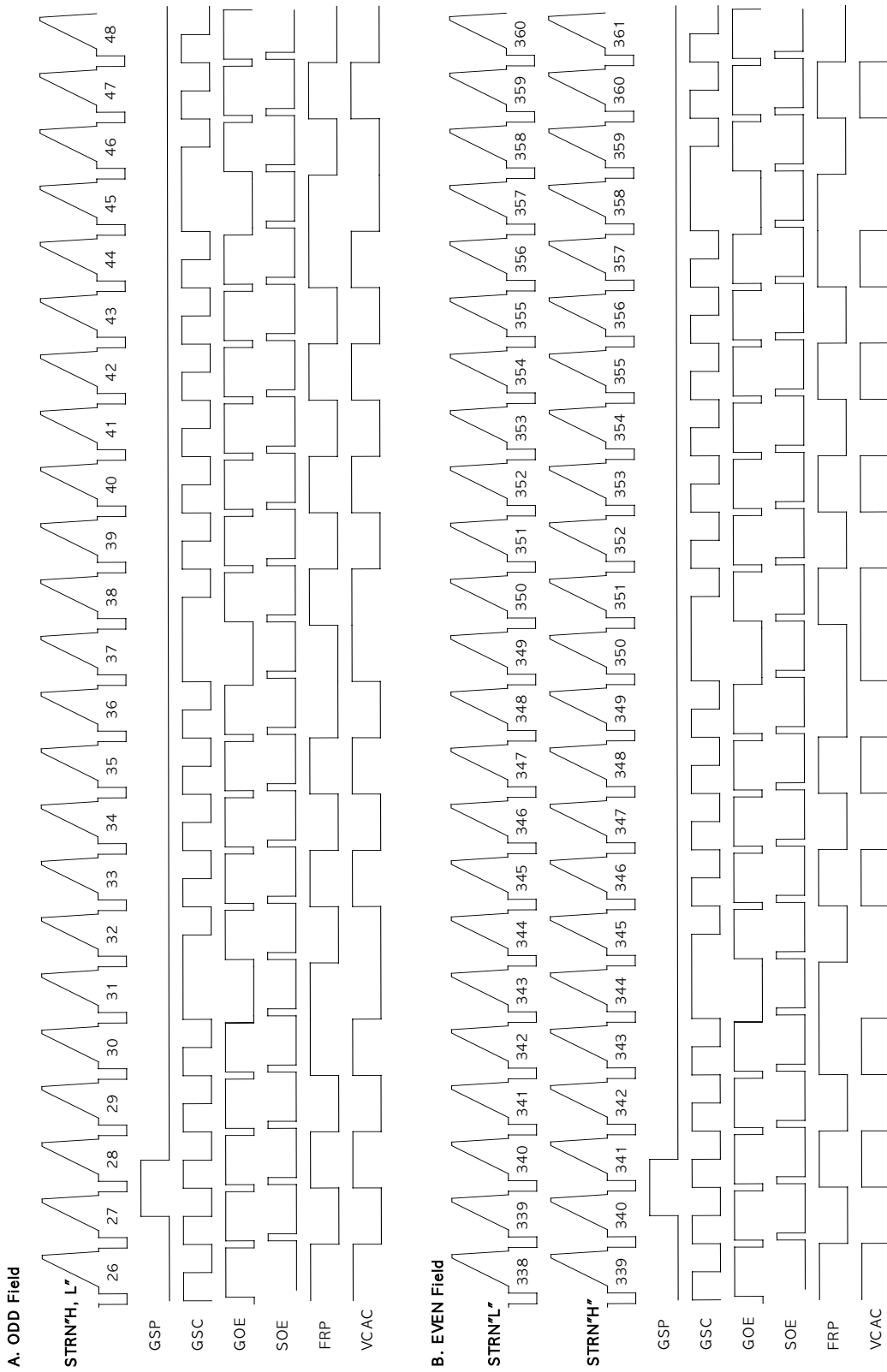


Fig.7-1 Vertical Display Position1 (PAL)

15. Vertical Display Method(PAL)

2) Vertical 35H ~ 303H

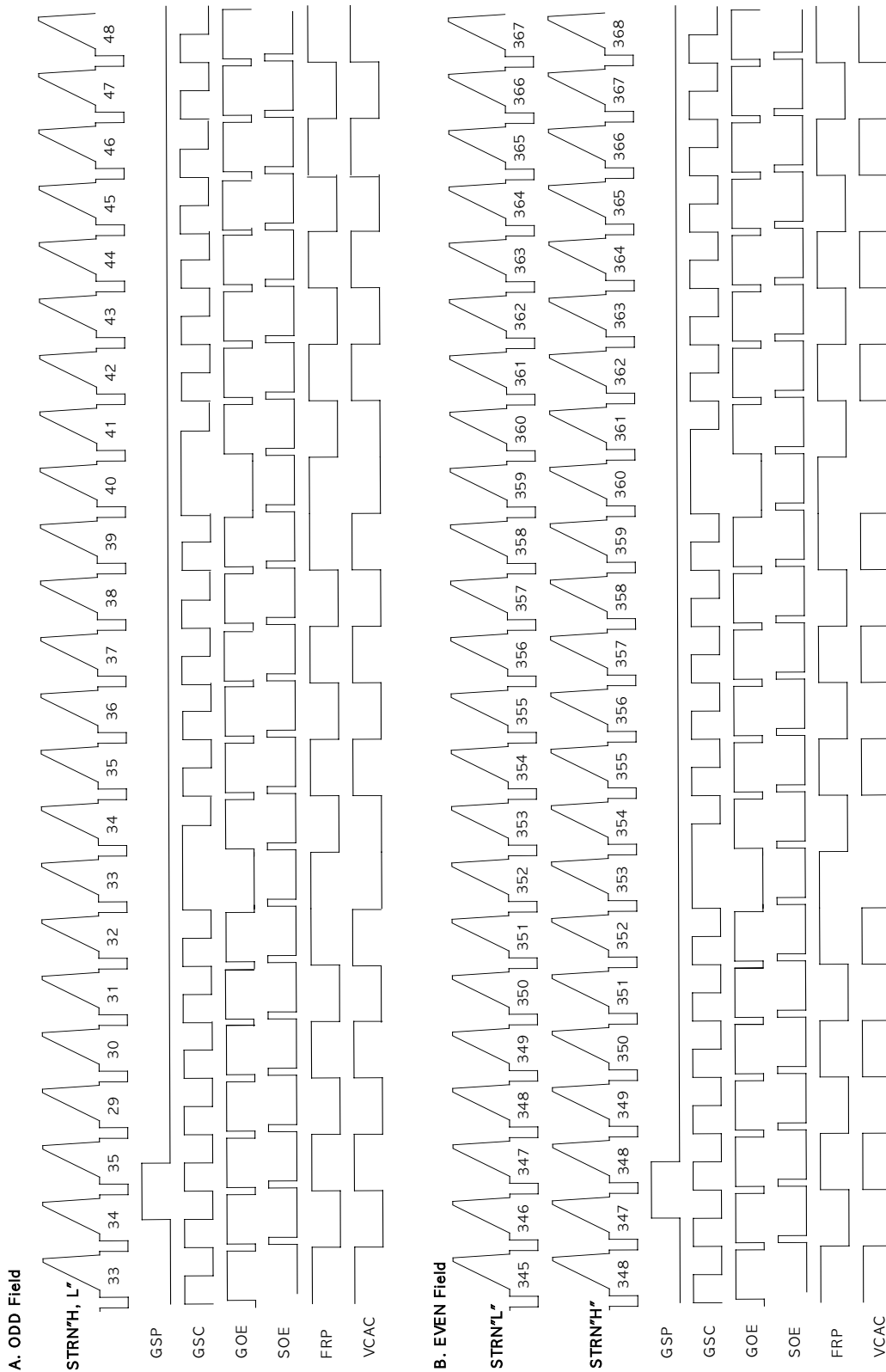


Fig.7-2 Vertical Display Position2 (PAL)

15. Vertical Display Method(PAL)

3) Vertical 47H ~ 280H

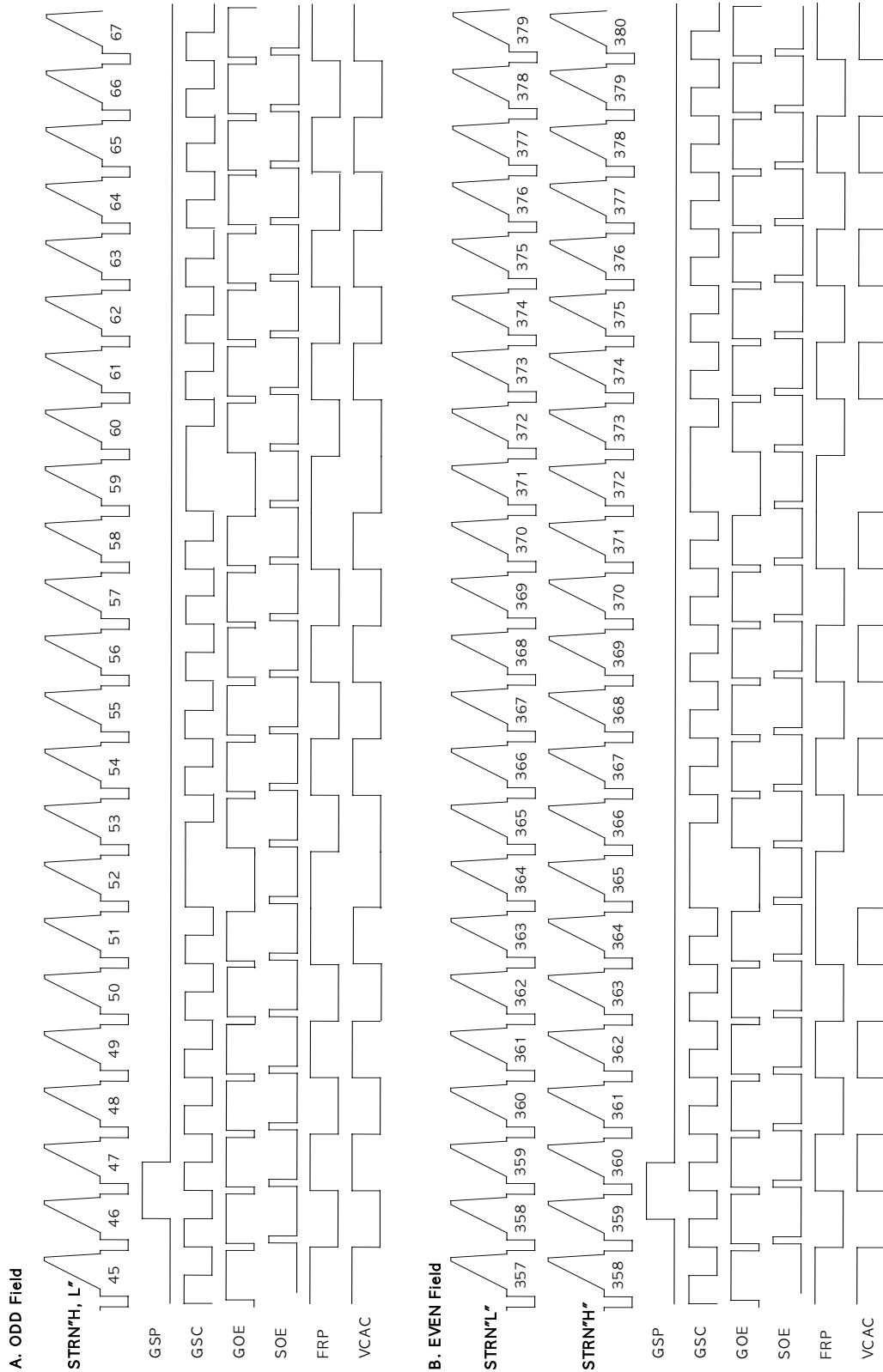


Fig.7-3 Vertical Display Position3 (PAL)

16. Control Option

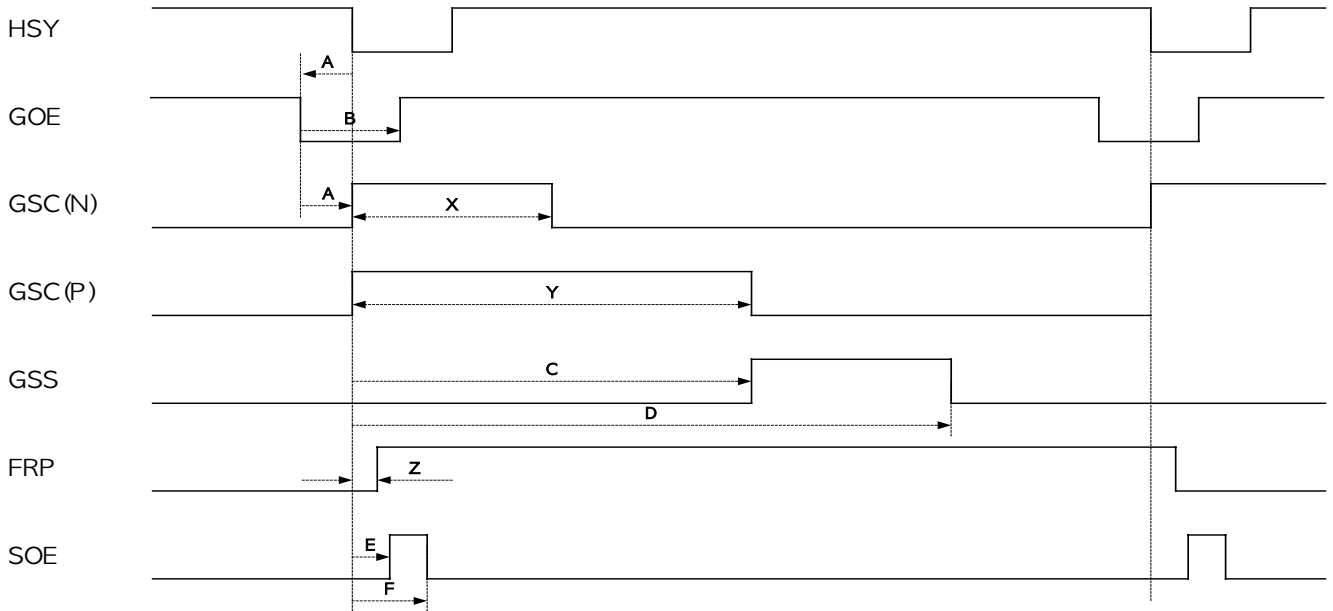


Fig. 8 Control Option

Table 4. Control Option

GOE_S	L	H	Unit	Notes
A	15	25	MCLK	-
B	30	50	MCLK	-
GSS_S	L	H	Unit	Notes
C	950	970	MCLK	1)
D	1150	1150	MCLK	-
SOE_S	L	H	Unit	Notes
E	85	85	MCLK	2)
SOE_E	L	H	Unit	Notes
F	100	100	MCLK	2)

※ Notes : 1) This value used at UDS “L”. Internal modulated GSS rising time used at UDS”H”.

2) SOE rising and falling time is set appropriate timing so fix it at SOE_S, SOE_E “H” “L” .

Others)

- “X : 1/4H”, “Y : 1/2H”, “Z : 36tMCLK”

- Above Timing Control option is normal conditional control option.

- SSP_S2, SSP_S1 refer to page 16.

- GSP_S “L” refer to page 17-1~18-3, if GSP_S “H” when this case GSP runs 1H shift.

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17. Package

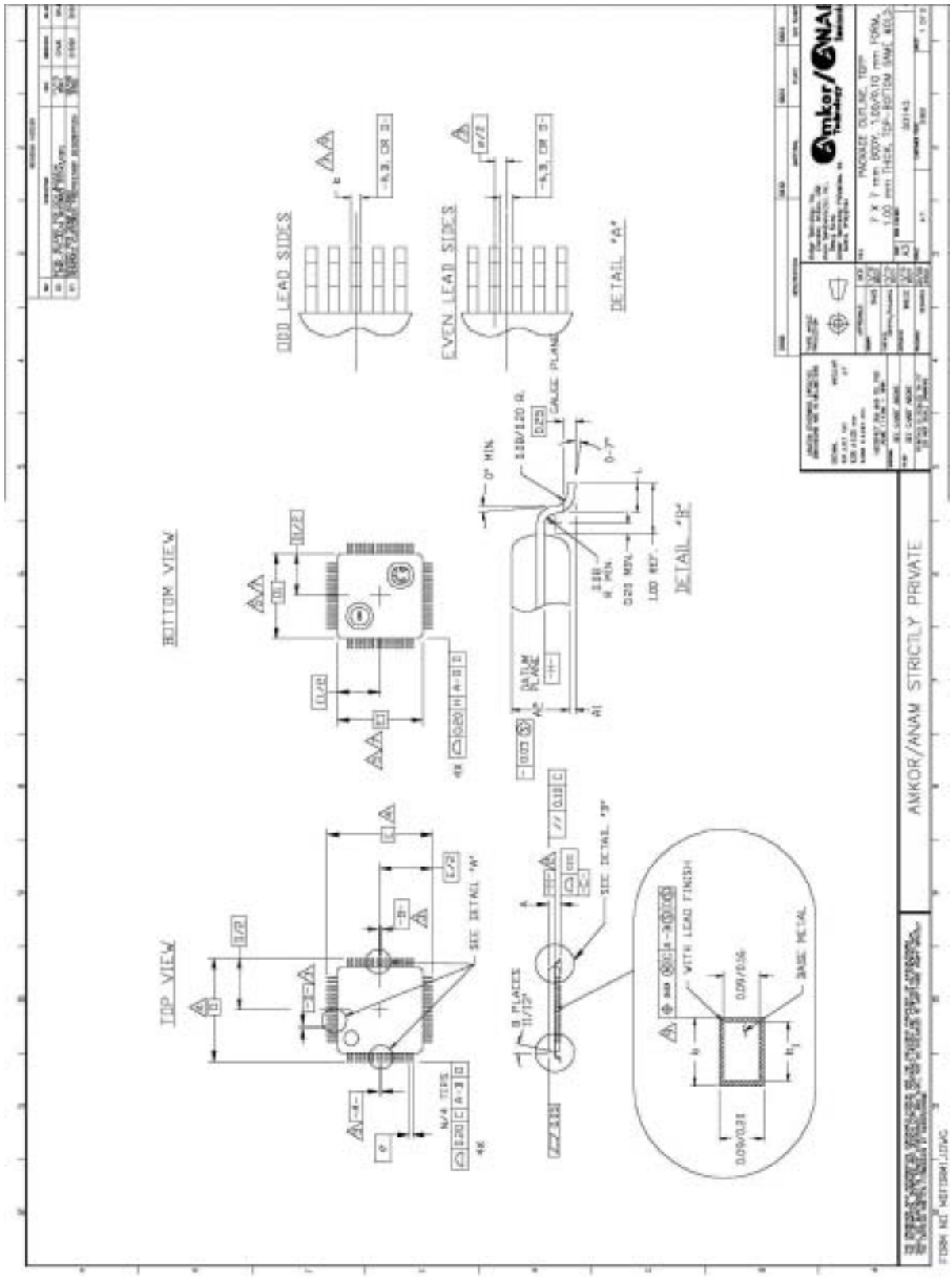


Fig. 9 Package

TFT-LCD Timing Controller

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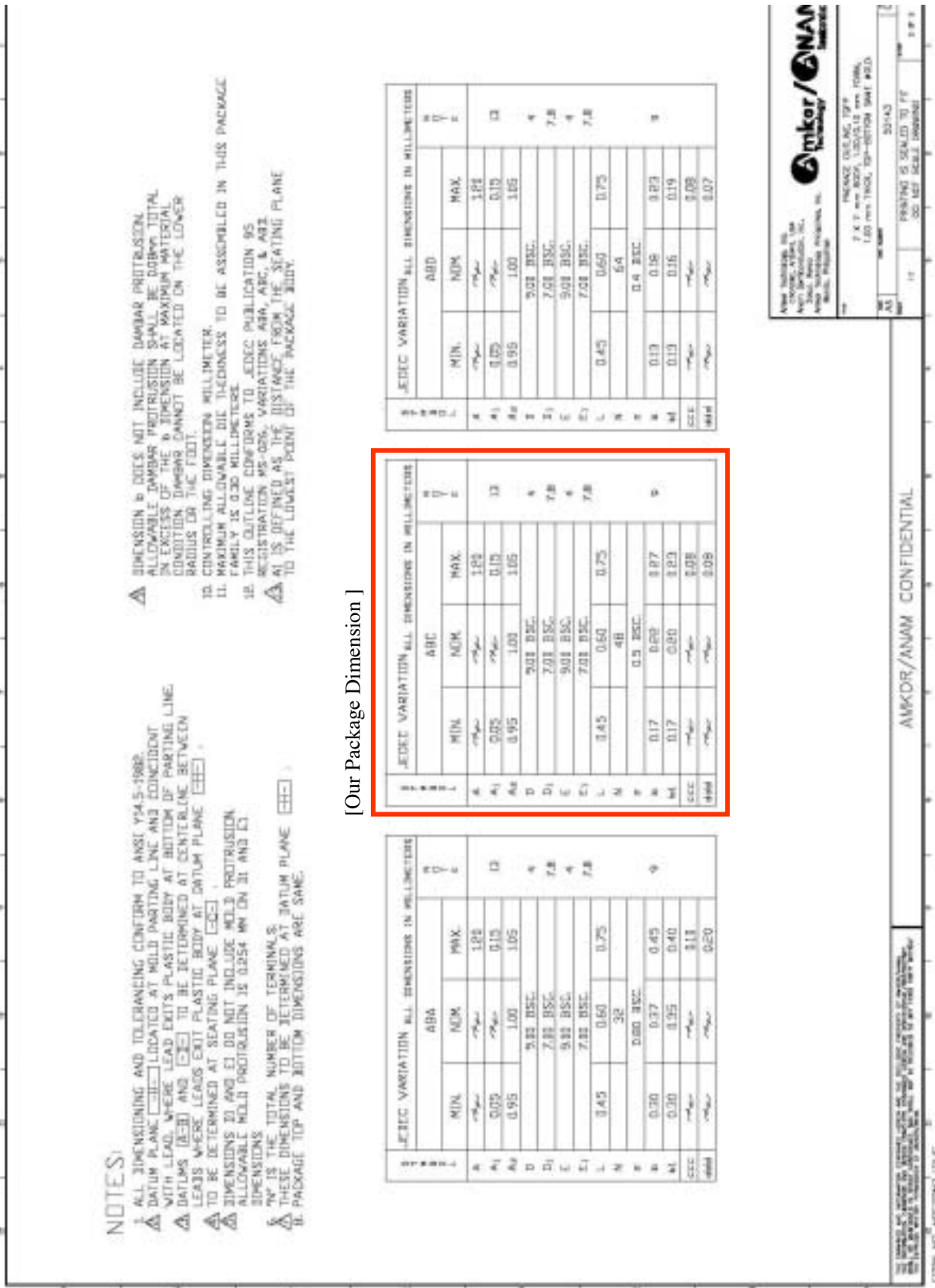


Fig. 10 Package

TFT-LCD Timing Controller

P/N : 0IHYL-0045A

18. Application Circuit

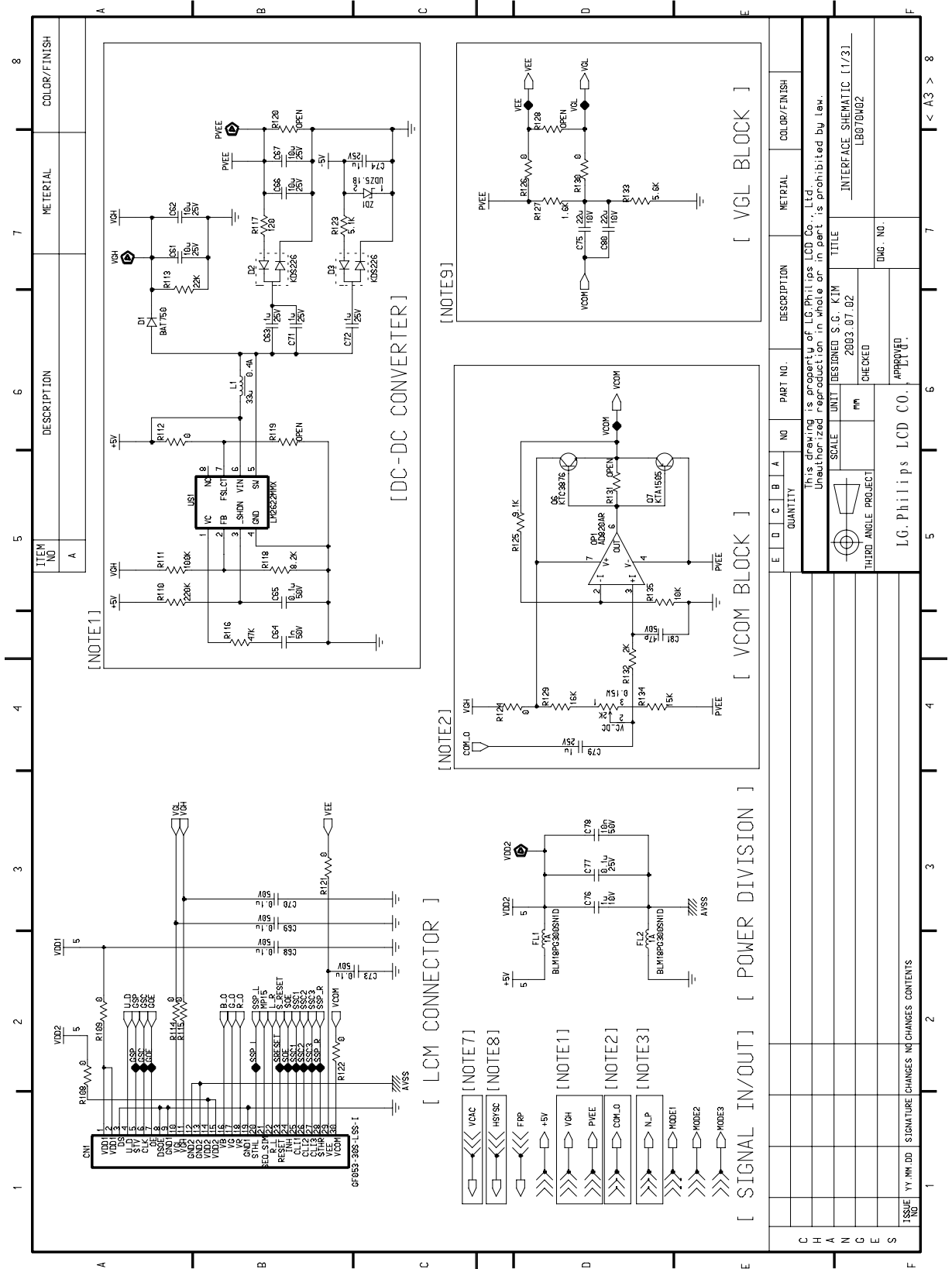


Fig. 11 Application Circuit 1/3

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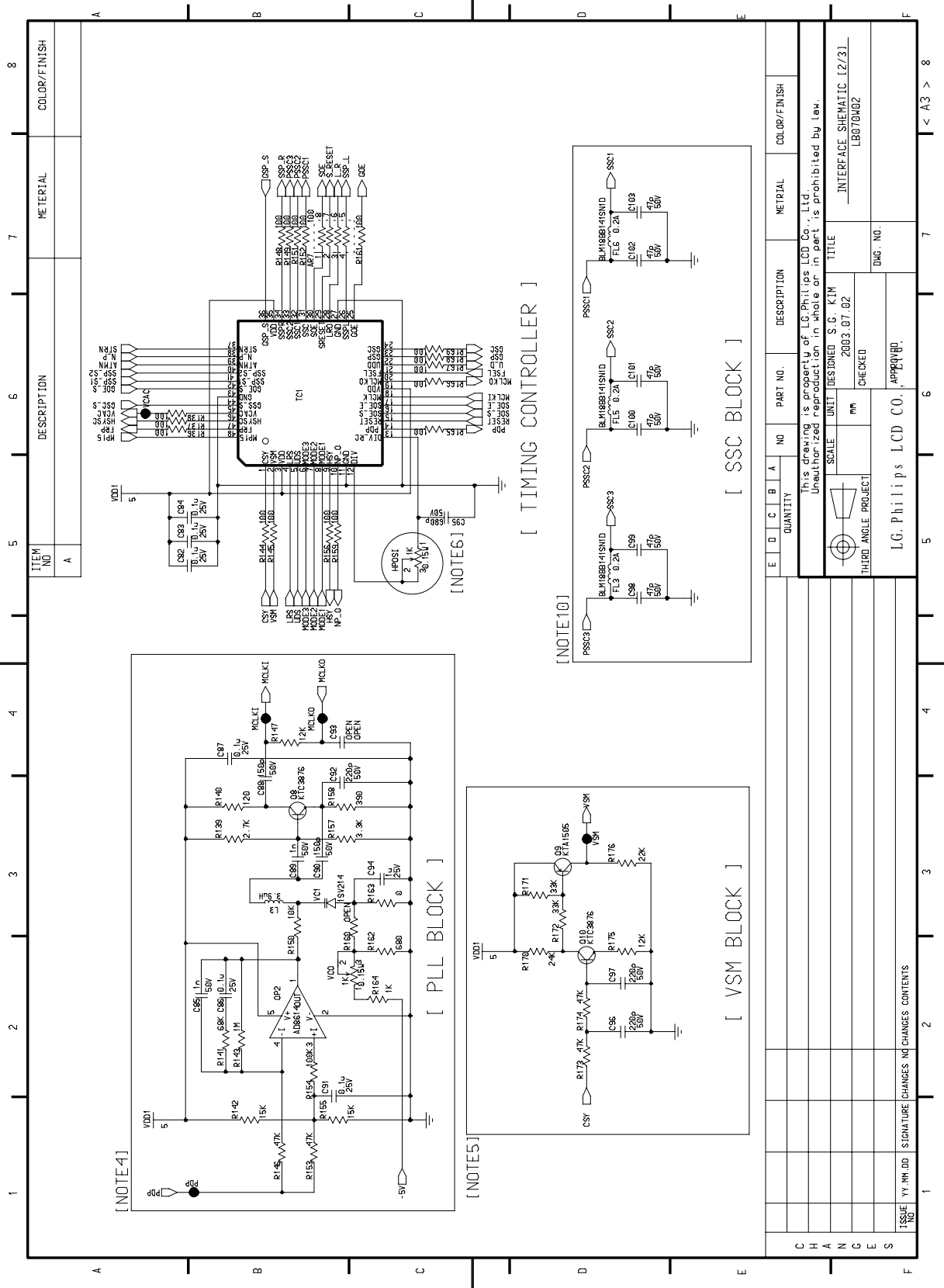


Fig. 12 Application Circuit 2/3

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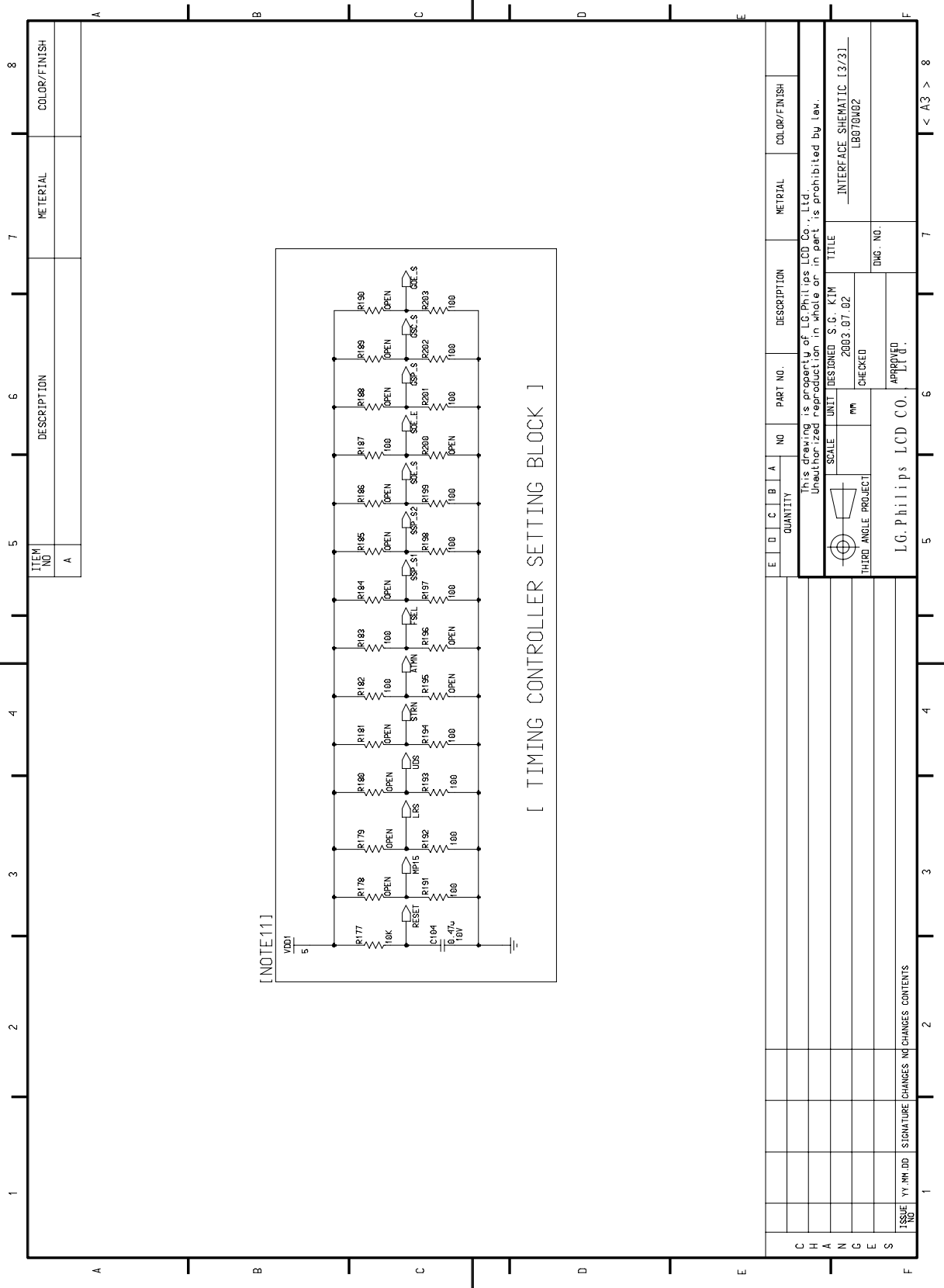


Fig. 13 Application Circuit 3/3

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Application Notes

(NOTE) This is for your reference and it could need to optimize R, C values according to the system.

(NOTE 1) This is DC/DC Converter circuit for supply the power of LCM. If there is another power supplier for LCM, this circuit don't need.

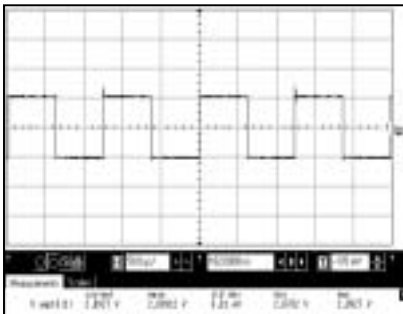
notice) If PVEE is stable enough based on 1H time, it can be used for “-5V”, the source of power for VCO of PLL circuit - which is for revised T-con - after divided it directly

(NOTE 2) COM_O must satisfy the range which is confined in (Table 1).

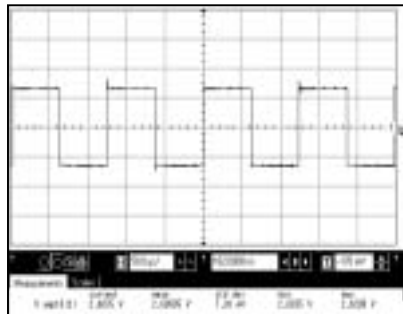
notice) VCOM circuit of this specification is recommended to your circuit for improving performance. (Improving quantity of display and reducing stabilized time of display when power on)

(Table 1)

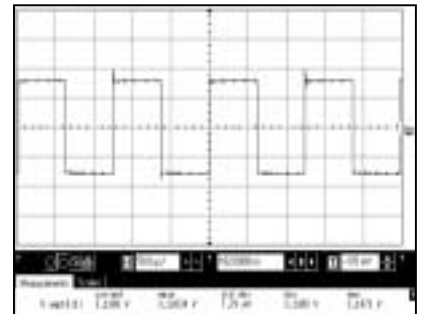
COM_O	MIN	TYP	MAX
V _{DC} (Volts)	+1.5	-	+3.5
V _{AC} (Volts)	+2.1	+2.6	+3.1



(MIN)



(TYP)



(MAX)

(NOTE 3) “N_P” is for choice of NTSC or PAL. In case of setting “H” on the 39th Pin “ATM”,

It is automatically selected NTSC or PAL according to Video input signal, without regard to “N_P” choice.

But if the automatic mode is unstable on your system, you can use “N_P” after setting “ATM” Low.

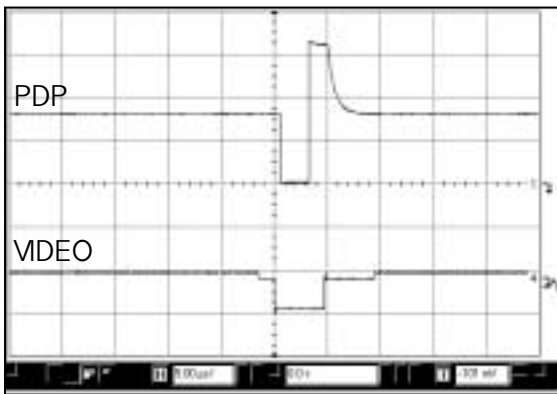
TFT-LCD Timing Controller

P/N : 0IHYL-0045A

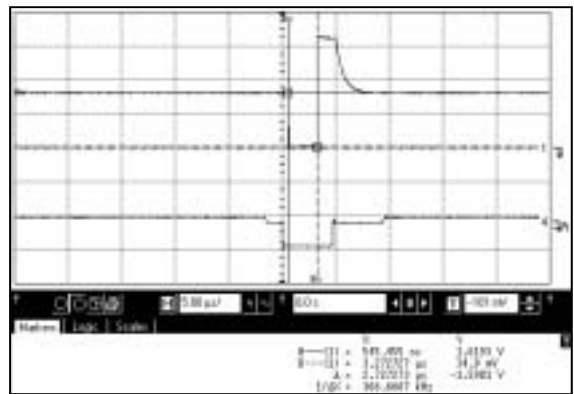
[NOTE 4- 1] PDP signal, which is input signal of PLL circuit, must be satisfied within the range as [Table 2] when no video signal. It must be same with below wave form when you check PDP signal on 25th line of “Odd Frame” when video signal is supplied.

[Table 2]

PDP signal	MIN	TYP	MAX
No Video signal	1.60V	1.65V	1.70V



[PDP signal of 25th line of Odd Frame]

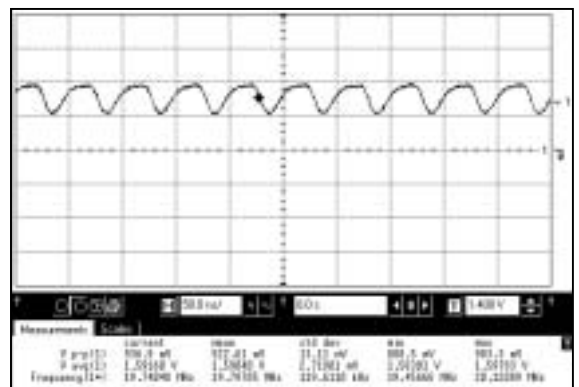


[PDP Low range, Timing 2.7uS]

[NOTE 4- 2] “MCLKI” which is final output of PLL circuit, have to meet [Table 3]. If it can't, you should control R, C values on PLL circuit to meet it.

[Table 3]

MCLKI signal	MIN	TYP	MAX
DC level	1.4V	1.5V	1.6V
AC level	0.8V	1.0V	3.3V



[MCLKI wave form when no video signal of reference circuit]

[NOTE 4- 3] Setting method of PLL Circuit

1st proposal) In case of fixing resistor of VCO, Refer PLL circuit of Fig.12

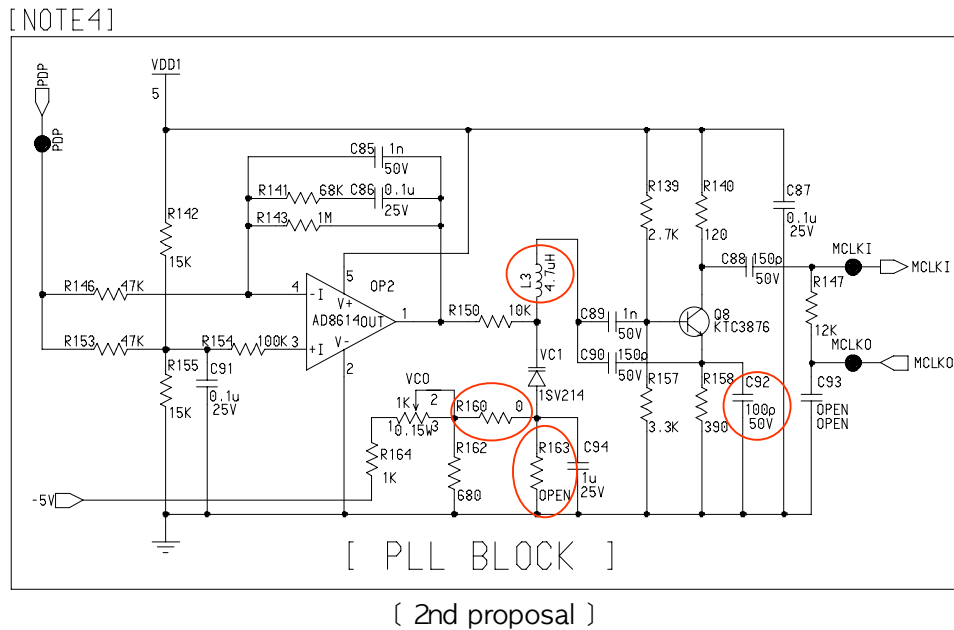
L3=3.9uH, R160=Open, R163=0Ω, C92=220pF

2nd proposal) In case of using the variable resistor of VCO, Refer PLL circuit at Page 27.

L3=4.7uH, R160=0Ω, R163=Open, C92=100pF

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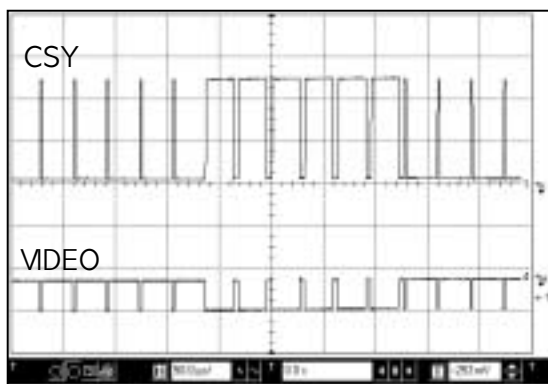
※ 2nd proposal) Notice

As mentioned at (NOTE 1), If you substitute PVEE for “- 5V” power, R164 and R162 must be optimized to keep the voltage ,which is lower side of 1SV214, to “- 1V” and VCO resistor must be controlled to keep the frequency of MCLKO to 19.4MHz.

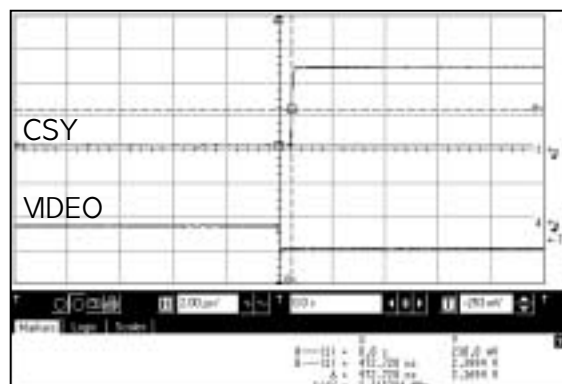
[NOTE 5- 1] CSY , which put in VSM signal, must meet [Table 4].

[Table 4]

CSY signal	MIN	TYP	MAX
Voltage level	3.0V	5.0V	5.5V
Delay time against input SYNC	0us	0.5us	1.0us



[Video signal and CSY signal]



[Delay time of REFERENCE circuit]

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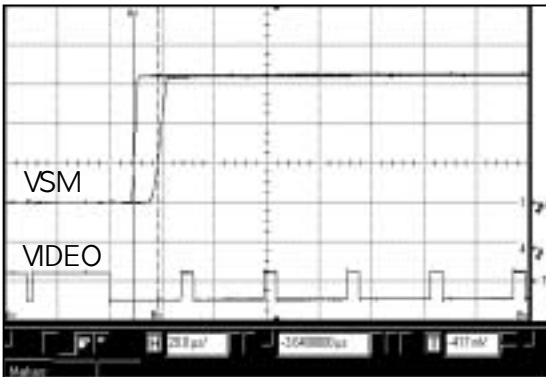
[NOTE 5- 2] “VSM” which is output of VSM circuit must meet [Table 5].

If it can't, it's possible to appear noise on display.

When you check delay time of VSM signal, the basis of voltage level is 1.5V.

[Table 5]

VSM signal	MIN	TYP	MAX
Delay time against VSY falling time	9.5us	-	18.5us



Notice)

If VSM signal is delayed due to using IC of “SYNCHRONOUS SEPARATOR” such like NJW1303, VSM meet at least [Table 6] through optimizing R59 and R95.

[VSM signal margin]

[Table 6]

VSM signal	MIN	TYP	MAX
VSY falling time against delay time	44.0us	-	52.8us

[NOTE 6] Control variable resistor, “HPOSI” when vertical white line occurred at right black area in NORMAL DISPLAY MODE.

[NOTE 7] “VCAC” signal have to be connected with “COMMON FRP”, 32th pin in case of using SHARP DECODER IC (IR3Y29BM) and connected with “VCOMIN”, 64th pin in case of using JRC DECODER IC (NJM2529).

[NOTE 8] “HSYSC” signal have to be connected with “SYNC IN”, 34th pin in case of using SHARP DECODER IC (IR3Y29BM) and connected with “HSYIN”, 57th pin in case of using JRC DECODER IC (NJM2529).

[NOTE 9] Total capacitance using at VGL circuit such like C75, C80 have to keep over 40uF. If it is lower than that, the horizontal line is possible to occur at PAL display.

[NOTE 10] Filter used at SSC circuit will be optimized according to EM and SSC wave form.

[NOTE 11] The noise can occur at certain area because of the difference of resolution between LCM and TV. It need to be optimized condition through changing STRN option.

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※ Component List (Fig. 11 ~ 13)

NO	DESCRIPTION & SPECIFICATION	REFERENCE	Qty.
1	CAPACITOR,CHIP[CERAMIC M/L HDRF/S], 1NF 50V K X 1608 R/TP, S	C64 C85 C89	3
2	CAPACITOR,CHIP[CERAMIC M/L HDRF/S], 10NF 50V Z F 1608 R/TP, S	C78	1
3	CAPACITOR,CHIP[CERAMIC M/L HDRF/S], 0.1UF 25V Z F 1608 R/TP, S	C77 C82 C83 C84 C86 C87 C91	7
4	CAPACITOR,CHIP[CERAMIC M/L HDRF/S], 0.1UF 50V K X7R 1608 R/TP, S	C65 C68 C69 C70 C73	5
5	CAPACITOR,CHIP[CERAMIC M/L HDRF/S], 1UF 10V Z F 1608 R/TP, S	C76	1
6	CAPACITOR,CHIP[CERAMIC M/L HDRF/S], 1UF 25V Z F 2012 R/TP, S	C63 C71 C72 C74 C79 C94	6
7	CAPACITOR,CHIP[CERAMIC M/L HDRF/S], 22UF 10V Z F(Y5V) 3216 R/TP, S	C75 C80	2
8	CAPACITOR,CHIP[CERAMIC M/L HDRF/S], 0.47UF 10V Z F 1608 R/TP, S	C104	1
9	CAPACITOR, HIGH-DIELECTRIC, 10U F, 25 Volt, K PER, (X5R,JB), 3225 R/TP, 20MM(TYP), S	C61 C62 C66 C67	4
10	CAPACITOR,CHIP[CERAMIC M/L TCRF/S], 150PF 50V J NP0 1608 R/TP, S	C88 C90	2
11	CAPACITOR,CHIP[CERAMIC M/L TCRF/S], 220PF 50V J NP0 1608 R/TP, S	C92 C96 C97	3
12	CAPACITOR,CHIP[CERAMIC M/L TCRF/S], 47PF 50V J NP0 1608 R/TP, S	C81 C98 C99 C100 C101 C102 C103	7
13	CAPACITOR,CHIP[CERAMIC M/L TCRF/S], 680PF 50V J NP0 1608 R/TP, S	C95	1
14	DIODE, KDS226-RTK, SOT-23, S	D2 D3	2
15	DIODE, Schottky, BAT750(Q75A), DIODES, R/TP, SOT-23, S	D1	1
16	DIODE,ZENER, UD2S TE-17 5.1B, TP ROHM-K SOD323 0.2W 5.1V 0.005A -PF, S	ZD1	1
17	IC,ANALOG DEVICE, AD820AR-REEL, S	OP1	1
18	IC,ANALOG DEVICE, AD8614ART-REEL7, 5PIN SOT-23 TP OPAMP 1.45[Max], S	OP2	1
19	IC,NATIONAL SEMICONDUCTOR, LM2622MMX-ADJ, 8P,MSOP R/TP PWM IC(DC/DC), S	US1	1
20	INDUCTOR,CHIP,39uH	L3	1
21	INDUCTOR,CHIP, PLN6012T-100MR8PLN6012T-330MR42 TDK R/TP (33uH, 0.4A)	L1	1
22	RESISTOR,CHIP, 0 OHM 1/16W 1608 5% D R/TP, S	R108 R109 R112 R114 R115 R121 R122 R124 R126 R130 R160	11
23	RESISTOR,CHIP, 100 OHM 1/16W 1608 1% D R/TP, S	R136 R137 R138 R144 R145 R148 R149 R151 R152 R156 R159 R161 R165 R166 R167 R168 R169 R182 R183 R187 R191 R192 R193 R194 R197 R198 R199 R201 R202	29
24	RESISTOR,CHIP, 1K OHM 1/16W 1608 1% D R/TP, S	R164	1
25	RESISTOR,CHIP, 10K OHM 1/16W 1608 1% D R/TP, S	R135 R150 R177	3
26	RESISTOR,CHIP, 100K OHM 1/16W1608 1% D R/TP, S	R111 R154	2
27	RESISTOR,CHIP, 1M OHM 1/16W 1608 1% D R/TP, S	R143	1
28	RESISTOR,CHIP, 120 OHM 1/16W 1608 1% D R/TP, S	R117 R140	2
29	RESISTOR,CHIP, 12K OHM 1/16W 1608 1% D R/TP, S	R147 R175	2
30	RESISTOR,CHIP, 15K OHM 1/16W 1608 1% D R/TP, S	R134 R142 R155	3
31	RESISTOR,CHIP, 1.6K OHM 1/16W1608 1% D R/TP, S	R127	1
32	RESISTOR,CHIP, 16K OHM 1/16W 1608 1% D R/TP, S	R129	1
33	RESISTOR,CHIP, 2K OHM 1/16W 1608 1% D R/TP, S	R132	1
34	RESISTOR,CHIP, 22K OHM 1/16W 1608 1% D R/TP, S	R113 R176	2
35	RESISTOR,CHIP, 220K OHM 1/16W1608 1% D R/TP, S	R110	1
36	RESISTOR,CHIP, 24K OHM 1/16W 1608 1% D R/TP, S	R170	1
37	RESISTOR,CHIP, 27K OHM 1/16W1608 1% D R/TP, S	R139	1
38	RESISTOR,CHIP, 33K OHM 1/16W1608 1% D R/TP, S	R157	1
39	RESISTOR,CHIP, 33K OHM 1/16W 1608 1% D R/TP, S	R171 R172	2
40	RESISTOR,CHIP, 390 OHM 1/16W 1608 1% D R/TP, S	R158 R116 R146 R153 R173 R174	6

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NO	DESCRIPTION & SPECIFICATION	REFERENCE	Qty.
41	RESISTOR,CHIP, 5,1K OHM 1/16W1608 1% D R/TP, S	R123	1
42	RESISTOR,CHIP, 5,6K OHM 1/16W1608 1% D R/TP, S	R133	1
43	RESISTOR,CHIP, 680 OHM 1/16W 1608 1% D R/TP, S	R162	1
44	RESISTOR,CHIP, 68K OHM 1/16W 1608 1% D R/TP, S	R141	1
45	RESISTOR,CHIP, 8,2K OHM 1/16W1608 1% D R/TP, S	R118	1
46	RESISTOR,CHIP, 9,1K OHM 1/16W1608 1% D R/TP, S	R125	1
47	RESISTOR,CHIP, 100OHM 5% 1/16W 3216 R/TP, S	AR7	1
48	TRANSISTORR, PNP KTA1505S-Y-RTK, S	Q7 Q9	2
49	TRANSISTORR, KTC3876S-Y-RTK ,NPN, S	Q6 Q8 Q10	3
50	VARACTOR, 1SV214 SMD, S	VC1	1
51	VOLUME, PANASONIC, 2K ohm, EVM3WSX80B23, S	VC_DC	1
52	VOLUME, PANASONIC, 1K ohm, EVM3WSX80B13, S	HPOSI VCO	2
53	FILTER(CIRC), BLM18PG300SN1D,S	FL1 FL2	2
54	FILTER(CIRC), BLM18BB141SN1D,S	FL3 FL5 FL6	3
55	CHROMA IC (SHARP) IR3Y298M	IC1	1
56	T-CON IC, HS353149	TC1	1
57	CONNECTOR(LGC) GF053-30S-LSS	CN1	1