RECORD OF REVISIONS

Revision No	Revision Date	Page	Description
1.0	Mar.22, 2011	-	Final specification

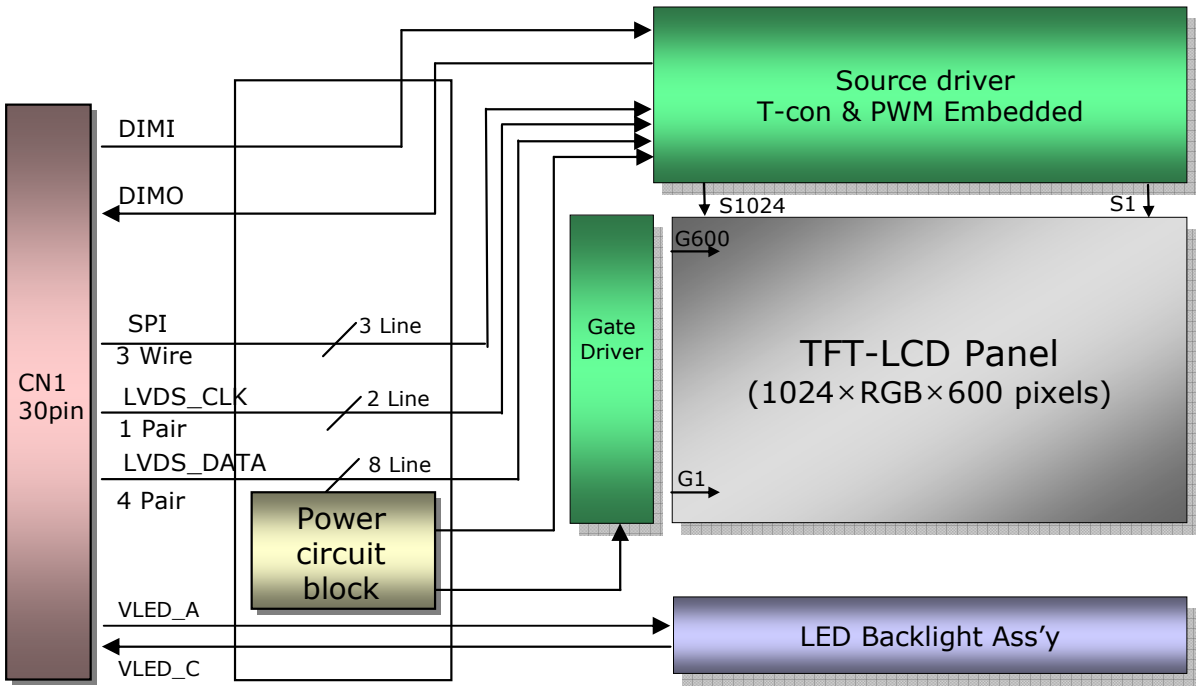
Product Specification

1. General Description

The LD070WS2 is a Color Active Matrix Liquid Crystal Display with an integral Light Emitting Diode(LED) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally Black mode. This TFT-LCD has 7.0 inches diagonally measured active display area with WSVGA resolution(1024 horizontal by 600 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit + 2-bit FRC gray scale signal for each dot, thus, presenting a palette of more than 16,772,216 colors.

The LD070WS2 has been designed to apply the interface method that enables low power, high speed, low EMI.

The LD070WS2 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LD070WS2 characteristics provide an excellent flat display.



General Features

Active Screen Size	7.0 inches diagonal
Outline Dimension	162.8mm x102.9mm x 2.47mm (Typ.)
Dot Pitch	0.050mm × 0.150mm
Pixel Format	1024 horiz. By 600 vert. Pixels RGB strip arrangement
Color Depth	6-bit + 2-bit FRC, 16,7M colors
Luminance, White	400 cd/m^2 (Typ.)
Weight	95g(Max.)
Display Operating Mode	Transmitting type, normally Black
Surface Treatment	Hard coat on the polarizer

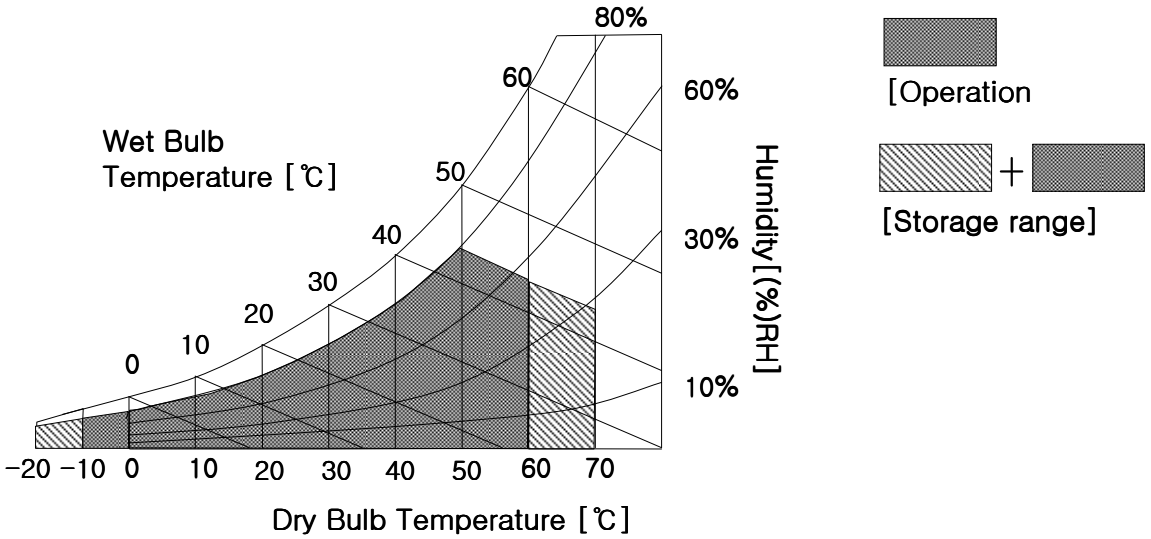
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.5	5.0	Vdc	at 25 ± 5°C
Operating Temperature	TOP	-10	60	°C	[Note 2-1,2,3,4]
Storage Temperature	HST	-20	70	°C	[Note 2-1,2]

[Note 2-1] This rating applies to all parts of the module and should not be exceeded.
[Note 2-2] Maximum wet-bulb temperature is 46℃. Condensation of dew must be avoided as electrical current leaks will occur, causing a degradation of performance specifications.
[Note 2-3] The operating temperature only guarantees operation of the circuit and doesn't guarantee all the contents of Electro-optical specification.
[Note 2-4] Ambient temperature when the backlight is lit (reference value).



3. Electrical Specifications

3-1. Electrical Characteristics

The LD070WS2 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the LED, is typically generated by an LED Driver. The LCD don't include LED Driver.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
LCD :						
Power Supply Input Voltage	VCC	3.0	3.3	3.6	V_{DC}	
Input High-Level Voltage	V_{IH}	0.7VCC	-	VCC	V_{DC}	
Input Low-Level Voltage	V_{IL}	0	-	0.3VCC	V_{DC}	
Power Supply Input Current	I_{CC}	-	250	288	mA	[Note 1]
Power Consumption	Pc	-	0.83	0.95	Watt	[Note 1]

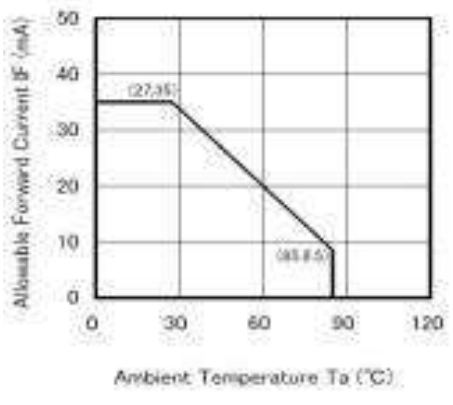
[Note 1] The specified current and power consumption are under the Vcc = 3.3V , 25℃, fv = 60Hz condition whereas "Mosaic Pattern" is displayed and fv is the frame frequency.

Table 3. Backlight Unit

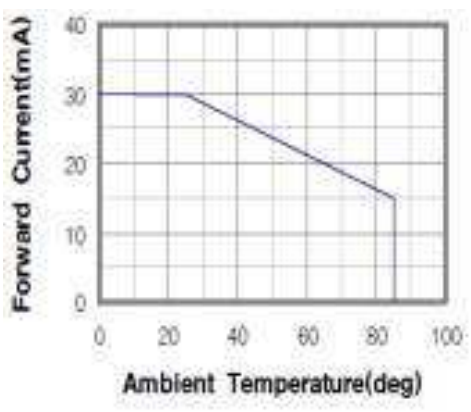
PARAMETER	SYMBOL	LED	MIN.	TYP.	MAX.	UNIT	REMARK
LED forward Current	I_f	Nichia S-LED	-	20	25	mA	Ta=25℃ (per chain)
LED forward Voltage	V_f	Nichia	-	15	16.5	V	Ta=25℃ (per chain)
		S-LED	-	16	17		
Power Consumption	P_{BL}	Nichia	-	1,200	1,320	mW	Ta=25℃ (@ typ. current)
		S-LED	-	1,280	1,360		

[Note 1] The permissible forward current of LED vary with environmental temperature.

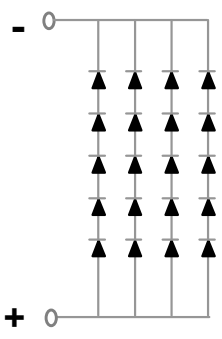
[Nichia LED]



[S-LED]



[LED Array Structure]



3-2. Interface (Input Terminal)

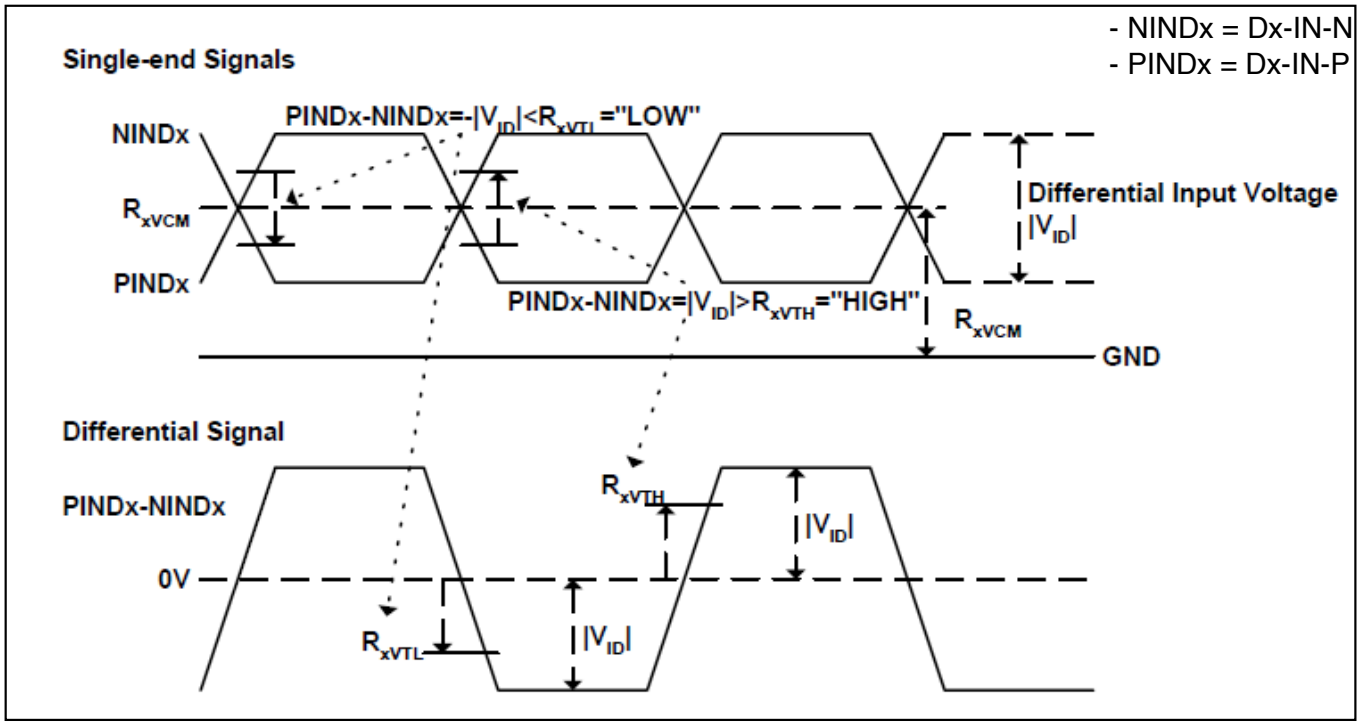
This LCD employs one interface connections, a 30 pin connector is used for the module electronics interface. (Connector Type : 30Pin 0.5mm pitch, Matching Connector : JAE AA01B-S030VA1)

Table 4. Module Connection Pin Configuration(cn1)

No.	Symbol	Description	Notes
1	VCC	+3.3V Power Supply	
2	GND	Ground	
3	VCC	+3.3V Power Supply	
4	CLK-IN-N	LVDS Clock Input (Negative)	
5	VCC	+3.3V Power Supply	
6	CLK-IN-P	LVDS Clock Input (Positive)	
7	GND	Ground	
8	GND	Ground	
9	LEDP	Power Supply For LED [Anode]	
10	D0-IN-N	LVDS differential data input	
11	LEDN	Power Supply For LED [Cathode]	
12	D0-IN-P	LVDS differential data input	
13	GND	Ground	
14	GND	Ground	
15	NC	No Connection	
16	D1-IN-N	LVDS differential data input	
17	NC	No Connection	
18	D1-IN-P	LVDS differential data input	
19	CSB	Serial Communication Chip Select	
20	GND	Ground	
21	SCL	Serial Communication Clock Input	
22	D2-IN-N	LVDS differential data input	
23	SDA	Serial Communication Data Input	
24	D2-IN-P	LVDS differential data input	
25	GND	Ground	
26	GND	Ground	
27	BL-PWM-IN	Brightness Control Signal	
28	D3-IN-Nt	LVDS differential data input	
29	BL-PWM-OUT	Backlight Dimmer Signal	
30	D3-IN-P	LVDS differential data input	

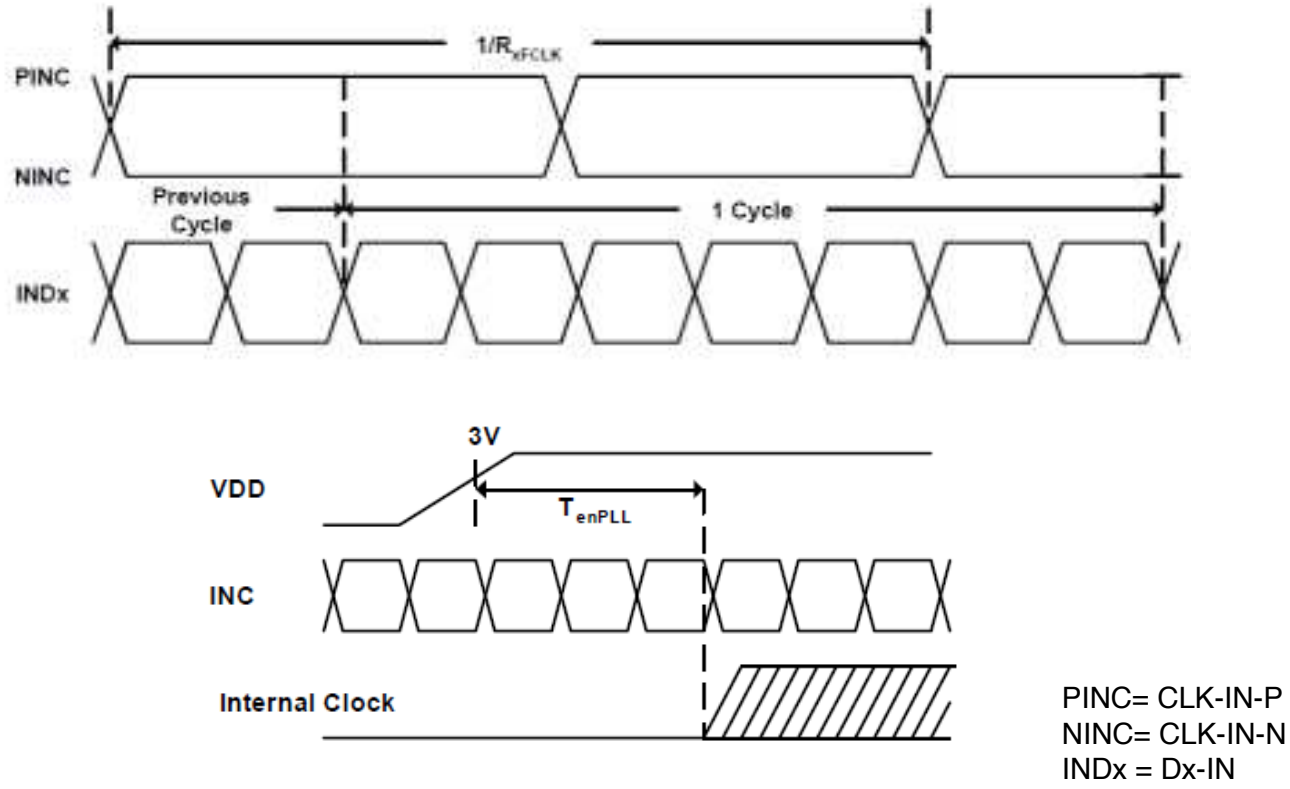
3-3. LVDS Signal Timing Specification

3-3-1. DC Specification



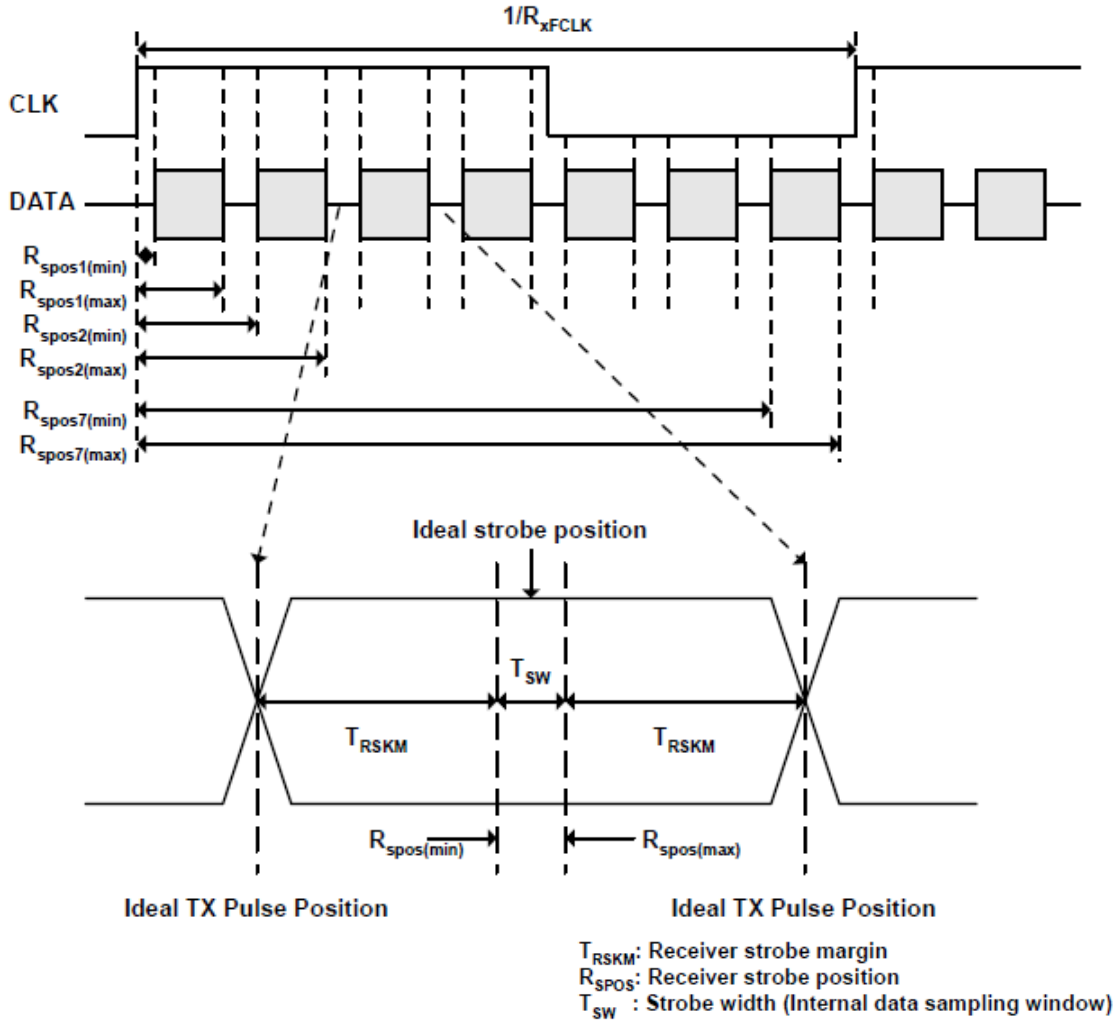
Description	Symbol	Min	Max	Unit	Notes
Differential input high threshold voltage	R_{xVTH}		0.1	V	R_{xVCM} =1.2V
Differential input low threshold voltage	R_{xVTL}	-0.1		V	
Input voltage range (singled-end)	R_{XVIN}	0	2.4	V	
Differential input common mode voltage	R_{xVCM}	IVIDI/2	2.4-IVIDI/2	V	
Differential input voltage	I VIDI	0.2	0.6	V	
Differential input leakage current	RV_{xliz}	-10	10	uA	

3-3-2. AC Specification



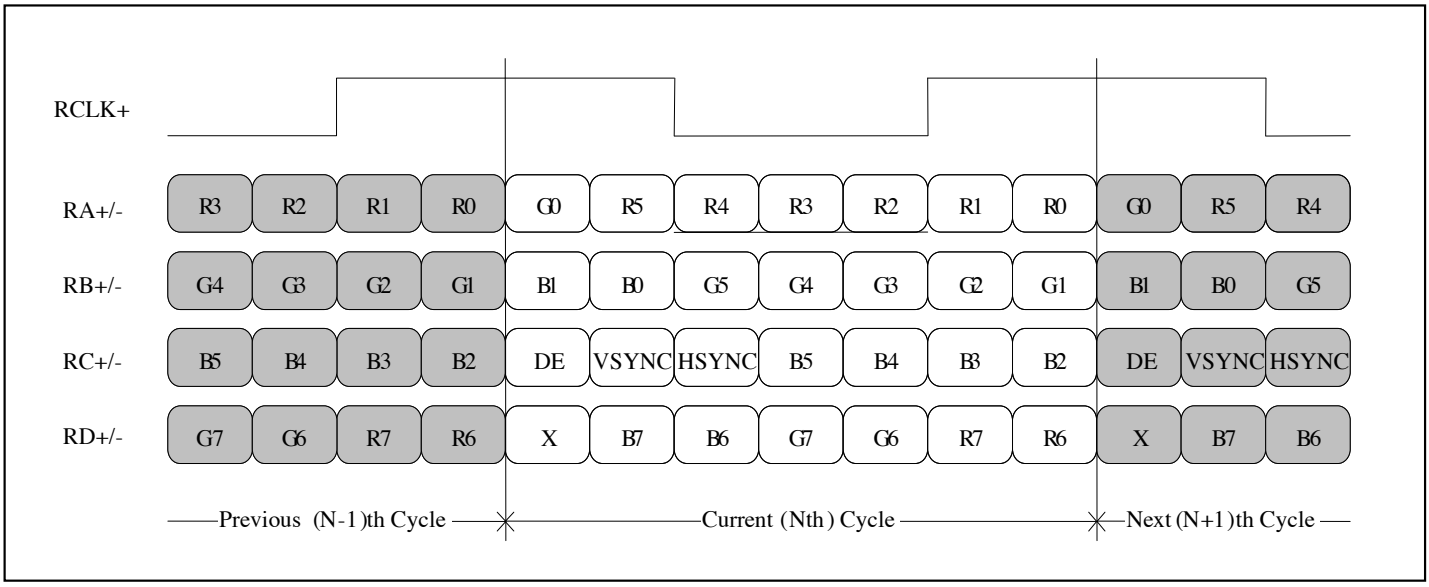
Ta=25°C, VCC=3.3V

Description	Symbol	Min	Typ	Max	Unit	Notes
Clock Frequency	R_{XFCLK}	45.9	-	59.1	MHz	
Input Data Skew Margin	T_{RSKM}	500	-		ps	l VIDl = 400mV RxVCM = 1.2V RxFCLK = 71 MHz
Clock high time	T_{LVCH}		4/(7* R_{xFCLK})		ns	-
Clock low time	T_{LVCL}		3/(7* R_{xFCLK})		ns	-
PLL wake-up time	T_{enPLL}	-		150	us	-



3-3-3. Data Format

-. LVDS 1 Port



< LVDS Data Format >

3-4. Signal Timing Specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of LVDS Tx/Rx for its proper operation.

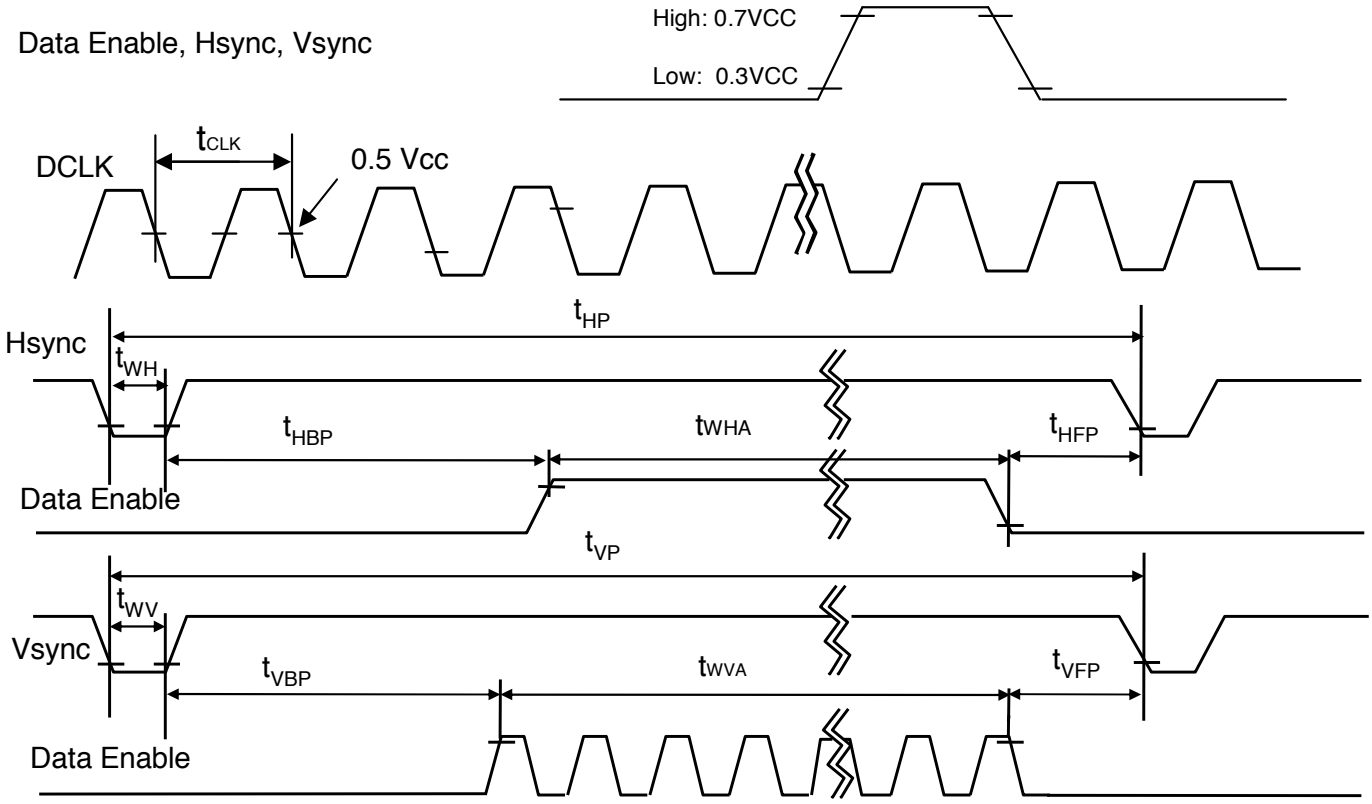
*** HV Mode**

Table 5. TIMING TABLE

ITEM	Symbol		Min	Typ	Max	Unit	Note
DCLK	Frequency	f_{CLK}	45.9	51.2	59.1	MHz	
Hsync	Period	Thp	1229	1344	1372	tCLK	
	Width	t_{WH}	1	-	140		
	Width-Active	t_{WHA}	1024	1024	1024		
Vsync	Period	t_{VP}	623	635	718	tHP	
	Width	t_{WV}	1	-	10		
	Width-Active	t_{WVA}	600	600	600		
Data Enable	Horizontal back porch	t_{HBP}	160	160	160	tCLK	
	Horizontal front porch	t_{HFP}	16	160	216		
	Vertical back porch	t_{VBP}	23	23	23	tHP	
	Vertical front porch	t_{VFP}	1	12	127		

3-5. Signal Timing Waveform

Condition : VCC =3.3V



3-6. Color Input Data Reference

The brightness of each primary color (red,green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 6. COLOR DATA REFERENCE

Colors & Gray Scale	Gray Scale Levels	Data Signal																							
		RED								GREEN								BLUE							
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Black	--	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Blue	--	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Green	--	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Cyan	--	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	--	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Magenta	--	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Yellow	--	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
White	--	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Black	R0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Darker	R1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Brighter	R253	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R254	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Red	R255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Black	G0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Darker	G1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	G2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Brighter	G253	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	G254	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Green	G255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Black	B0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Darker	B1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	B2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Brighter	B253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	B254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
Blue	B255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

3-7. Power Sequence

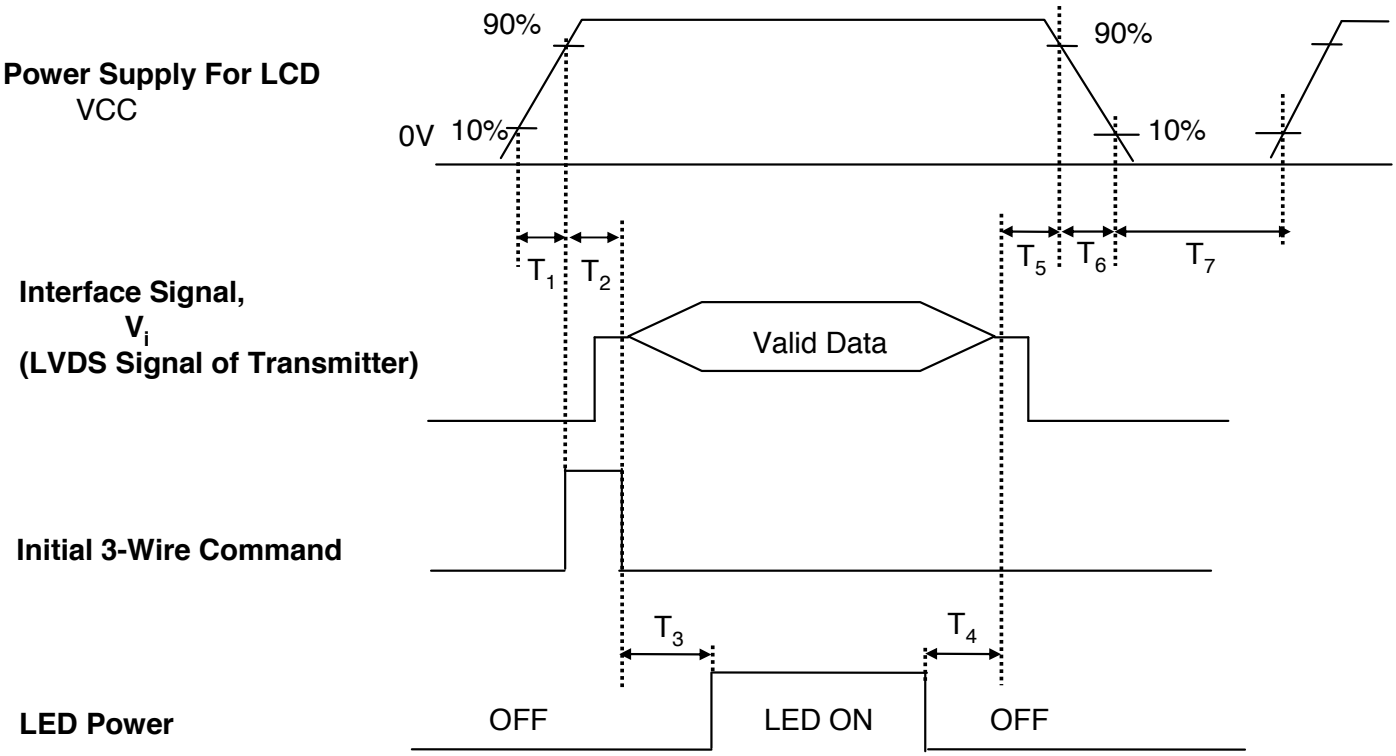


Table 7. POWER SEQUENCE TABLE

Parameter	Value			Units	Remark
	Min.	Typ.	Max.		
T_1	0.5	-	10	(ms)	-
T_2	0	-	16	(ms)	-
T_3	200	-	-	(ms)	-
T_4	200	-	-	(ms)	-
T_5	0	-	50	(ms)	-
T_6	3	-	10	(ms)	-
T_7	400	-	-	(ms)	-

[Note 1] Valid Data is Data to meet “3-3. LVDS Signal Timing Specifications”
[Note 2] Please avoid floating state of interface signal at invalid period.
[Note 3] When the interface signal is invalid, be sure to pull down the power supply for LCD VCC to 0V.
[Note 4] LED power must be turn on after power supply for LCD and interface signal are valid.

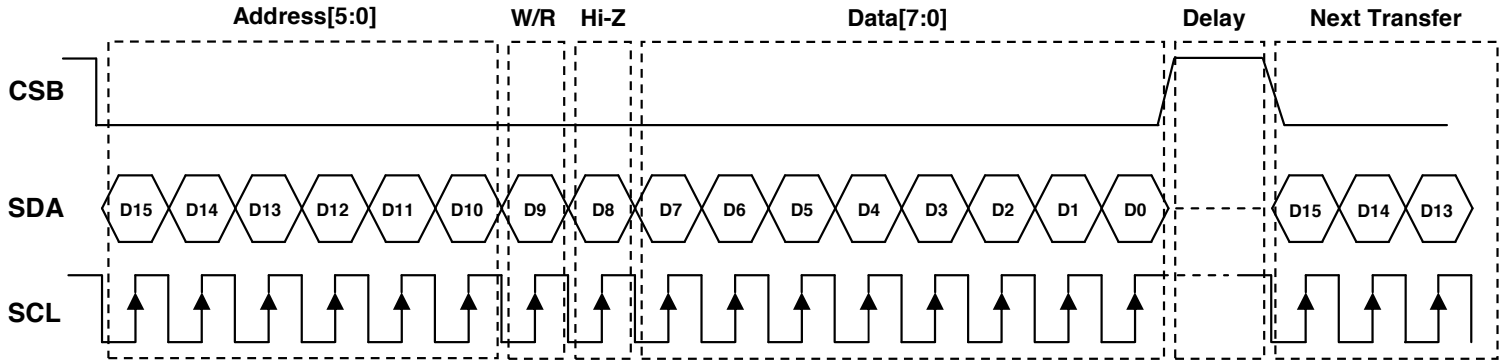
3-8. 3-Wire Serial Port Interface

3-8-1. 3-Wire Command Format

LD070WS2 use the 3-wire serial port as communication interface for all the function and parameter setting. 3-Wire communication can be bi-directional controlled by the “R/W” bit in address field.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.



3-Wire Commend Format

Bit	Description
D15-D10	Register Address [5:0]
D9	W/R control bit. “0” for Write; “1” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7-D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						0	X	Data (Issue by external controller)							

3-Wire Read Format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						1	Hi-Z	Data (Issue by 3-Wire engine)							

3-8-2. 3-Wire Control Register

R00: System Control Register

Designation	Address	Description
MODE	R0[0]	DE / SYNC mode select. MODE="0", HSD/VSD mode. MODE="1", DE mode. (Default)
DCLKPOL	R0[1]	DCLK polarity control bit. DCLKPOL="0": Data sampling at DCLK falling edge. (Default) DCLKPOL="1": Data sampling at DCLK rising edge.
GRB	R0[2]	Global reset bit. GRB="0", The controller is in reset state. GRB="1", Normal operation. (Default)
STBYB	R0[3]	Standby mode selection bit. STBYB="0", Timing control, driver and DC-DC converter, are off, and all outputs are High-Z. STBYB="1", Normal operation. (Default)
UPDN	R0[4]	G Gate Up or Down scan control. UPDN = "0", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver. (Default) UPDN = "1", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.
SHLR	R0[5]	Right/Left sequence control of source driver. SHLR="0", Shift left: Last data=S1<-S2<-S3 … <-S960=First data. SHLR="1", Shift right: First data=S1->S2->S3 … ->S960=Last data. (Default)
-	R0[6]	Reserved
PWR_EN	R0[7]	POWER enable. PWR_EN = H , enable PWM , Charge pump and VCOM buffer PWR_EN = L , disable PWM , Charge pump and VCOM buffer (Default)

R01: System Control Register

Designation	Address	Description
	R1[0]	Reserved
RES[1:0]	R1[2:1]	Display resolution selection. RES[1:0] = "01", for 1024(RGB)*768 display resolution(dual or cascade) RES[1:0] = "00", for 1024(RGB)*600 display resolution(dual or cascade) (Default) RES[1:0] = "10", for 800(RGB)*600 display resolution(dual or cascade) (601~936 channel disable) RES[1:0] = "11", for 800(RGB)*480 display resolution(dual or cascade) (601~936 channel disable)
BIST	R1[3]	Normal Operation/BIST pattern select. BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation (Default)
DITHER	R1[4]	Dithering function enable control. DITHER = "1", Enable internal dithering function DITHER = "0", Disable internal dithering function (Default)
HFRC	R1[5]	H-FRC selection. Normally pull low HFRC = H : H-FRC enable HFRC = L : H-FRC disable (Default) If DITHER = H and HFRC = L : enable only FRC/dithering function If DITHER = L , disable dithering function(H-FRC and FRC both disable)
CABC_EN[1:0]	R1[7:6]	CABC H/W enable pin. Normally pull low. When CABC_EN="00", CABC OFF. (Default mode) When CABC_EN="01", User interface Image. When CABC_EN="10", Still Picture. When CABC_EN="11", Moving Image.

3-8-2. 3-Wire Control Register

R02: System Control Register

Designation	Address	Description
-	R2[5:0]	Reserved
NBW	R2[6]	Normally black or normally white setting. NBW = H : Normally black NBW = L : Normally white (Default)
-	R2[7]	Reserved

R03: Gate on sequence Controller Register

Designation	Address	Description
SEL[1:0]	R3[1:0]	Gate on sequence select SEL[0] / SEL[1] / Pin control function 1 / 1 / Z + ⊐ 1 / 0 / ⊐ 0 / 1 / ⌋ 0 / 0 / Z(Default)
Frame	R3[2]	Frame inverse or not select. FRAME = “1”, Uniform FRAME = “0”, Frame inverse (Default)
-	R3[7:3]	Reserved

R0E:Test mode (1)

Designation	Address	Description
TEST_mode(1)	R0E[7:0]	Enter test mode(1) TEST_mode = 8’h5F, enter TEST_mode = other exit (Default)

R0F: Test mode (2)

Designation	Address	Description
TEST_mode(2)	R0F[7:0]	Enter test mode(2) TEST_mode = 8’hA4, enter TEST_mode = other exit (Default)

R0D:Charing time control (3)

Designation	Address	Description
OE_WIDTH	R0D[7:0]	Inversion type select. Enter Test mode(1) and (2) first. Then R0D setting will be active TEST_mode = 8’h00, increase charging time

R02:Charge sharing control (4)

Designation	Address	Description
EQC_ADJ	R02[7:0]	Inversion type select. Enter Test mode(1) and (2) first. Then R10 setting will be active EQC_ADJ = 8'h43, adjust charge sharing time

R0A: BIAS current control (5)

Designation	Address	Description
BIAS_TRIG	R0A[7:0]	Inversion type select. Enter Test mode(1) and (2) first. Then R10 setting will be active BIAS_TRIG = 8'h28, trigger bias reduction

R10: Inversion architecture

Designation	Address	Description
INV	R10F[7:0]	Inversion type select. Enter Test mode(1) and (2) first. Then R10 setting will be active 2line / 1dot = 8'h41 1line / 1dot = 8'h01 (Default)

※ Recommend Register Setting (CABC Off Mode)

Register write sequence : R00→R00→R01→R02→R0E→R0F→R0D→R02→R0A→R10 →R00
If you don't use register write sequence, it may cause faulty operation.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
R00	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	Reset
R00	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	1	Into Standby mode
R01	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	Enable FRC/Dither (CABC Off Mode)
R02	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	Enable Normally Black
R0E	0	0	1	1	1	0	0	0	0	1	0	1	1	1	1	1	Enter Test mode(1)
R0F	0	0	1	1	1	1	0	0	1	0	1	0	0	1	0	0	Enter Test mode(2)
R0D	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	Increase line charging time
R02	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	1	Adjust charge sharing time
R0A	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	Trigger bias reduction
R10	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	Adopt 2 Line / 1 Dot
R00	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1	PWM On, Released standby mode

4. Optical Specifications

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 5 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

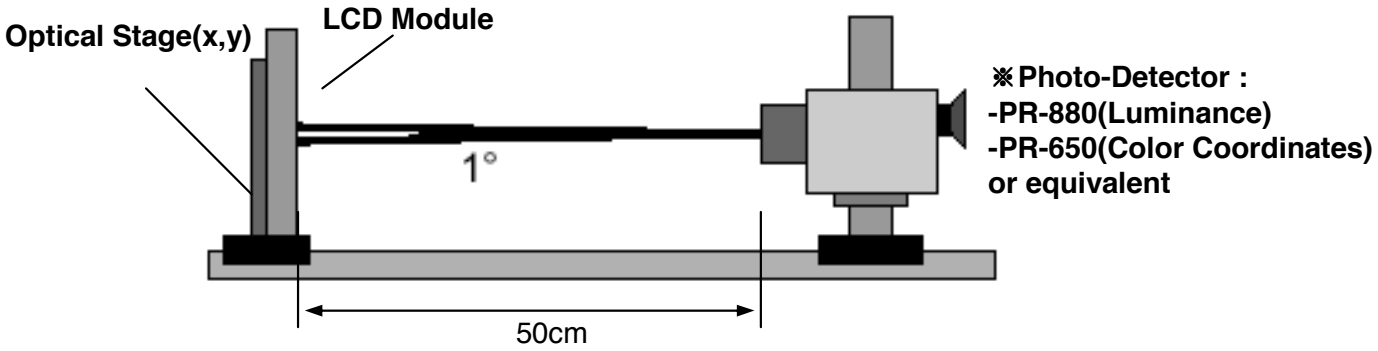


Table 8. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, f_{CLK}= 51.2MHz, **I_{LED} = 80.0mA**

Parameter		Symbol	Values			Units	Notes
			Min	Typ	Max		
Contrast Ratio		CR	640	800	-		1
Surface Luminance, white		L_{WH}	320	400	-	cd/m^2	2
Luminance Variation		δ_{WHITE}	-	1.25	1.4		3
Response Time							4
	Rise Time + Decay Time	$Tr_R + Tr_D$	-	-	50	ms	
Color Coordinates							2
	White	Wx	0.270	0.310	0.350		
		Wy	0.300	0.340	0.380		
Viewing Angle							5
	x axis, right(Φ=0°)	Θr	75	85	-	degree	3 o'clock
	x axis, left (Φ=180°)	Θl	75	85	-	degree	9 o'clock
	y axis, up (Φ=90°)	Θu	75	85	-	degree	12 o'clock
	y axis, down (Φ=270°)	Θd	75	85	-	degree	6 o'clock

[Note 4-1] Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

[Note 4-2] Surface luminance is measured at the center point(L_1) of the LCD with all pixels displaying white at the distance of 50cm by PR-880. Color Coordinates are measured at the center point(L_1) of the LCD with all pixels displaying red, green, blue and white at the distance of 50cm by PR-650. For more information, refer to the FIG 1 and FIG 2.

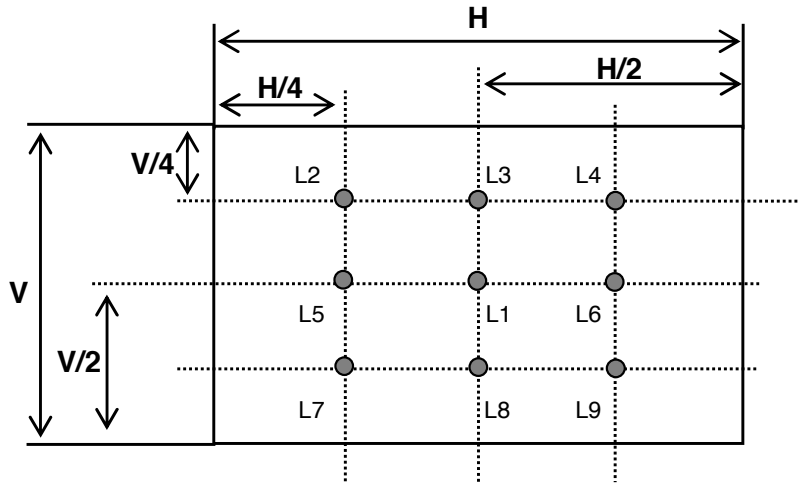
[Note 4-3] Luminance % uniformity is measured for 9 point For more information see FIG 2.
δ_{WHITE} = Maximum(L1,L2, ….. L9) ÷ Minimum(L1,L2, ….. L9)

[Note 4-4] Response time is the time required for the display to transition from white to black (Rise Time, Tr_R) and from black to white(Decay Time, Tr_D). For additional information see FIG 3.

[Note 4-5] Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

FIG. 2 Luminance

<measuring point for surface luminance & measuring point for luminance variation>



***H,V : ACTIVE AREA**

FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.`

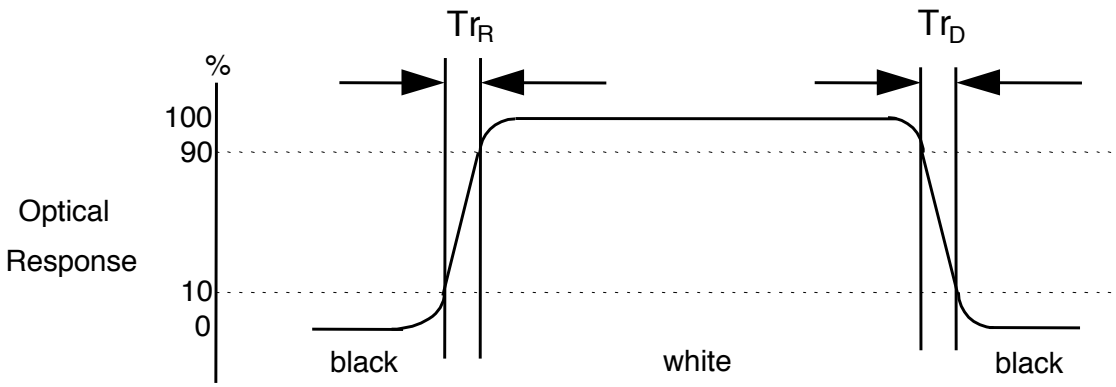
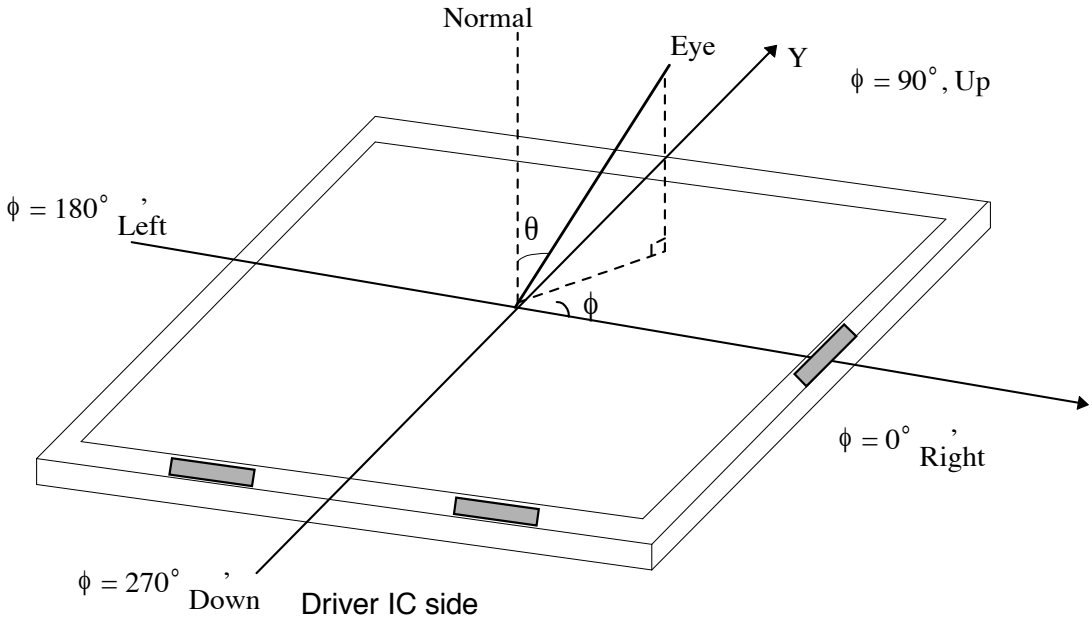


FIG. 4 Viewing angle

<Dimension of viewing angle range>



5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LD070WS2. In addition the figures in the next page are detailed mechanical drawing of the LCD.

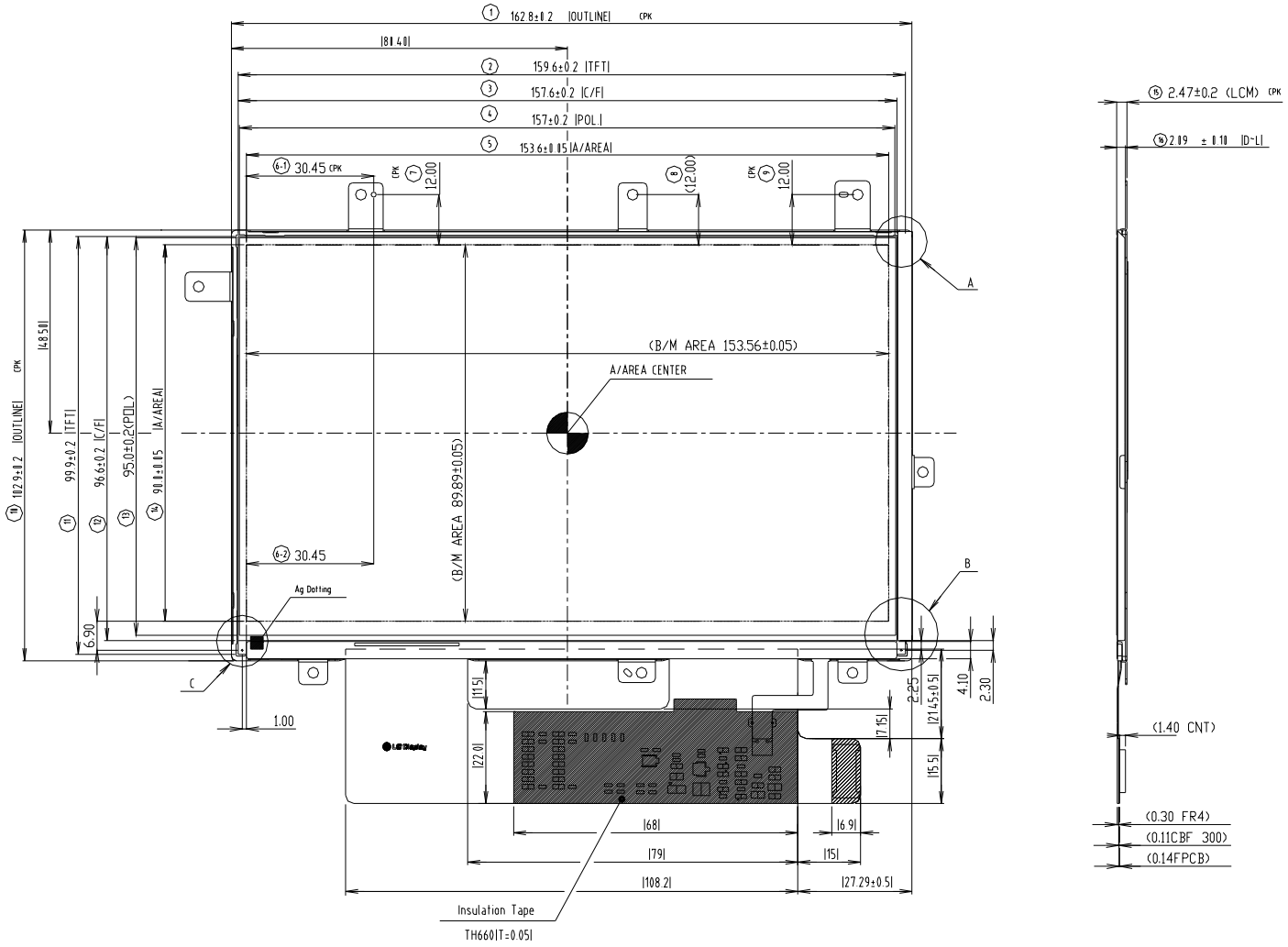
Outline Dimension	Horizontal	162.8 mm(Typ)
	Vertical	102.9 mm(Typ)
	Depth	2.47 mm (Typ.)
Active Display Area	Horizontal	153.6 mm (Typ.)
	Vertical	90.0 mm (Typ.)
Weight	94(Typ.) / 95g (Max.)	
Surface Treatment	Hard coat on the polarizer	

Product Specification

<FRONT VIEW>

Unit:[mm], General tolerance: ± 0.3mm

" FOR REFERENCE ONLY "

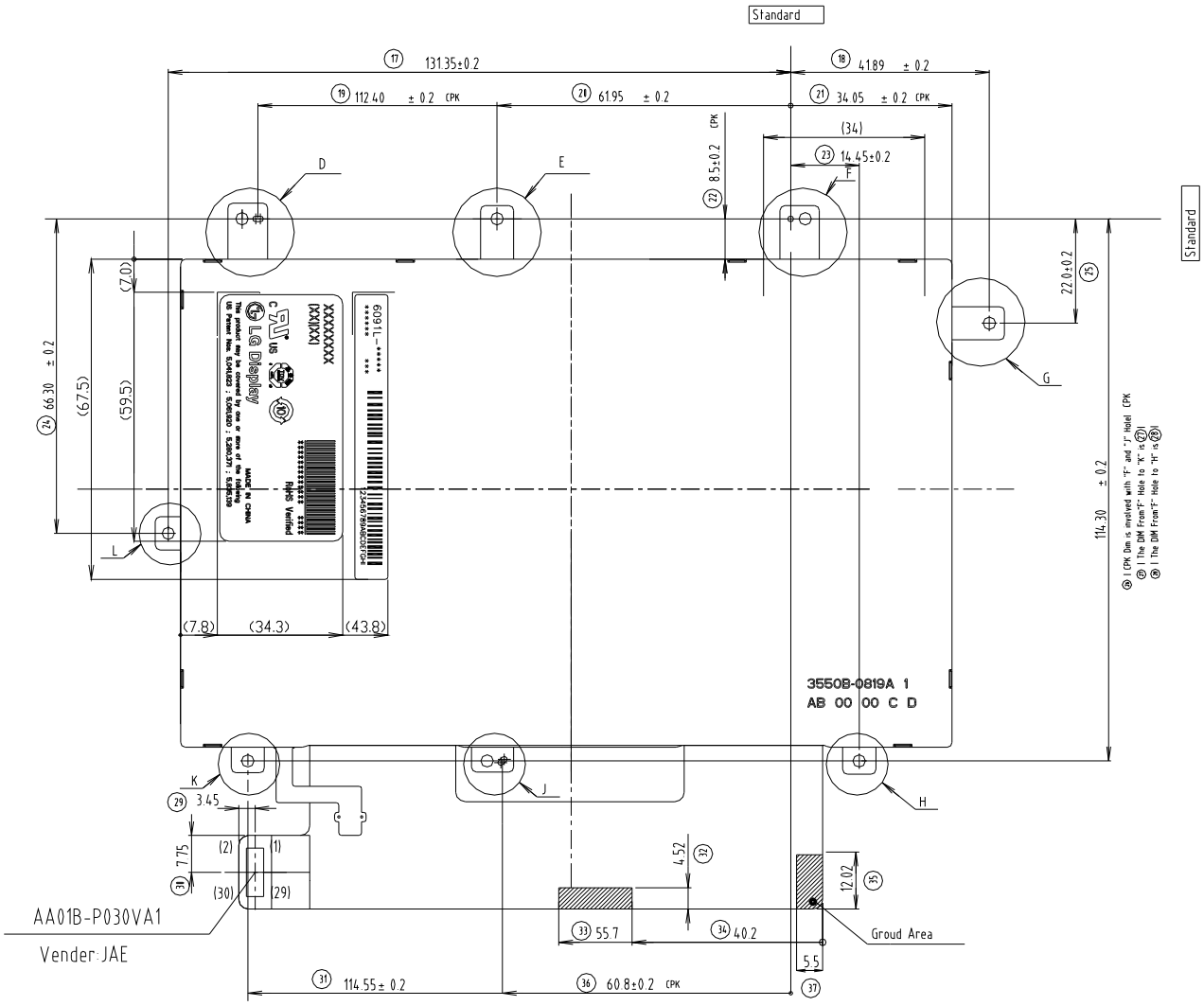


Product Specification

<REAR VIEW>

Unit:[mm], General tolerance: ± 0.3mm

" FOR REFERENCE ONLY "



6. International Standards

6-1. Safety

a) UL 60950-1, Second Edition, Underwriters Laboratories Inc.
Information Technology Equipment - Safety - Part 1 : General Requirements.

b) CAN/CSA C22.2 No.60950-1-07, Second Edition, Canadian Standards Association.
Information Technology Equipment - Safety - Part 1 : General Requirements.

c) EN 60950-1:2006 + A11:2009, European Committee for Electrotechnical Standardization(CENELEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.

6-2. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

7. Packing

7-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	A	B	C	D	E	F	G	H	J	K

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

7-2. Packing Form

a) Package quantity in one box : 44 pcs

b) Box Size(mm) : 478 mm × 365 mm × 244 mm

8. Precautions

Please pay attention to the followings when you use this TFT LCD module.

8-1. Mounting precautions

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

8-2. Operating precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(7) This module is not designed to attach TSP(touch screen panels). If TSP is applied, LPL can't guarantee the ‘Ripple’ related problems.

9-3. Electrostatic discharge control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. Precautions for strong light exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. Handling precautions for protection film

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.