LG.PHILIPS LCD

Display Specification for

13.3” Wide (1280x800) TFT-LCD

With LED Backlight

Revision History

DATE	REV #	Section #	CHANGE DESCRIPTION
8/15/2008	A	All	Release

Table of Content

1. General Description

This document establishes the requirements for the display device for the M97 project.

Category	***Parameter***	***Specification***
General	Manufacturer	LGD
	Mfg. P/N	LP133WX2-TLC1 (for Heesung backlight) LP133WX2-TLC1 (for Radiant backlight)
	LCD TYPE	Normally-White, Transmissive TN TFT-LCD
	Diagonal	13.282" (33.74cm)
	Pixel Format	1280 (RGB stripe, H) x 800 (V)
	Pixel Pitch	0.2235(V) x 3x0.0745(H) mm
	Color Depth	18-bits (6R, 6G, 6B), 262144 colors
	Pooling requirement	Rigid Post Spacer with strong pooling resistance
	Packaging	Protective film on front polarizer. Displays packaged and air-tight sealed in anti-static bags.
Electrical	Interface	3.3V single-channel LVDS
	Power Consumption	4.3 W @ Black (typical, the logic plus the backlight @95% duty cycle @20mA, 3.3V forward bias voltage)
Optical	Luminance	275 nits @ 95% duty cycle @20 mA (typical center)
	White LED Backlight	6 strings, 9 LED per string. Nichia NNSW108T-S1, TG E1S62-YW1D7-08
	Hot Spots	No visible hot spot at any angle
	Viewing Direction	6:00 for worst dark inversion (pcb driver on the bottom)
	Contrast	500 typical
	Top Polarizer	Glossy Surface, 3H Hard Coating, LT4/ARC7 AR coating
	Diffuser Sheet	Tsujiden D153GS (top) & Tsujiden D120 (Bottom)
	BEF Sheet	2 X BEF2-G2 MR (Halogen free)

	Reflector	E6SR (sulfur free)
	LGP	PMMA
Mechanical	Active Area	286.08 mm (H) x 178.80 mm (V)
	Minimum Viewing Area	288.08 mm (H) x 180.80 mm (V)
	Module Outline Size	297.150 mm (H) x 192.150 mm (V)
	Connector	IPEX 20474-030E-12
	Mating Connector	IPEX 20472-030T-10
	Weight	300 grams typical
Environmental	Operating Temperature	0°C ~ +50°C
	Storage Temperature	-25°C ~ +65°C
Pre-Aging	Before shipment	Minimum 2 hours at 50°C, panel on

2. ORDER OF PRECEDENCE OF DOCUMENTATION AUTHORITY

In the case of any conflict in any specification related to these parts, this order of precedence of authority shall apply:

2.1. The Purchase Order

2.2. This Specification

2.3. Reference Documents

3. PHYSICAL DESCRIPTION

3.1. Display Mode

Normally White, Transmissive, Twisted Nematic Liquid Crystal Displays

3.2. Pixel Configuration

RGB Vertical Stripe

3.3. Pixel Pitch

0.2235 mm x 0.2235 mm

3.4. Resolution

1280 (RGB stripe, H) x 800 (V)

3.5. Aperture Ratio

Minimum > TBD

3.6. Optimum Viewing Cone

6 o'clock worst dark inversion direction (PCB on the bottom)

3.7. Interface & Driving Scheme

3.3V single-channel LVDS (Flat Link) interface, requiring Hsync and Vsync signals, along with DE (Data Enable) mode, 2-dot inversion

3.8. Front Surface Treatment

Low-reflection gloss surface, ~1% Reflectance, ≥3H hardness (Sumitomo LT4, or Nitto Denko ARC7)

3.9 Environmental Requirements:

Any homogeneous component must meet Apple Halogen-Free Specification, 069-1857.

Display assembly shall not contain arsenic in the glass, in accordance with the Apple Regulated Substances Specification, 069-0135. Restrictions on arsenic are not applicable to semiconductor materials.

Display assembly shall not contain mercury, in accordance with the Apple Regulated Substances Specification, 069-0135.

4. MECHANICAL REQUIREMENTS

4.1. Dimensions and Tolerances

Refer to Apple MCO 069-2659, which include height, width, and thickness, mounting details, bulb location, cable length, and connectors. The LCD module outline is described in the following table.

Dimension	Min	Typ	Max	Unit
Horizontal (H)	296.85	297.15	297.45	mm
Vertical (V)	191.85	192.15	192.45	mm
Depth (D)	3.00	3.30	3.60	mm

4.2. Weight

300 g (typical), 310 g (max)

4.3. Stack-up (tentative)

Mechanical Stack-up	**Part #**	**Thickness /mm**
Top Polarizer (glossy, LT4 or ARC7)	LGC, 6308L-1543A	0.215
LCD Glass CF		0.5
LCD Glass TFT		0.5
Bottom Polarizer		0.135
Total Design Gap	-	0.135
Upper Diffuser	Tsujiden D153GS	0.095
Upper BEF (Halogen Free)	BEF II-GII MR	0.155
Lower BEF (Halogen Free)	BEF II-GII MR	0.155
Lower Diffuser	Tsujiden D120	0.12
Light Guide	PMMA	0.72
White Reflector (Sulfur-free reflector for PMMA backlight)	E6SR	0.188
Rear Bezel	SUS 304	0.3
Tape		0.1
Total Typical Thickness	w/o PCB	3.30
Maximum Tolerance		0.3

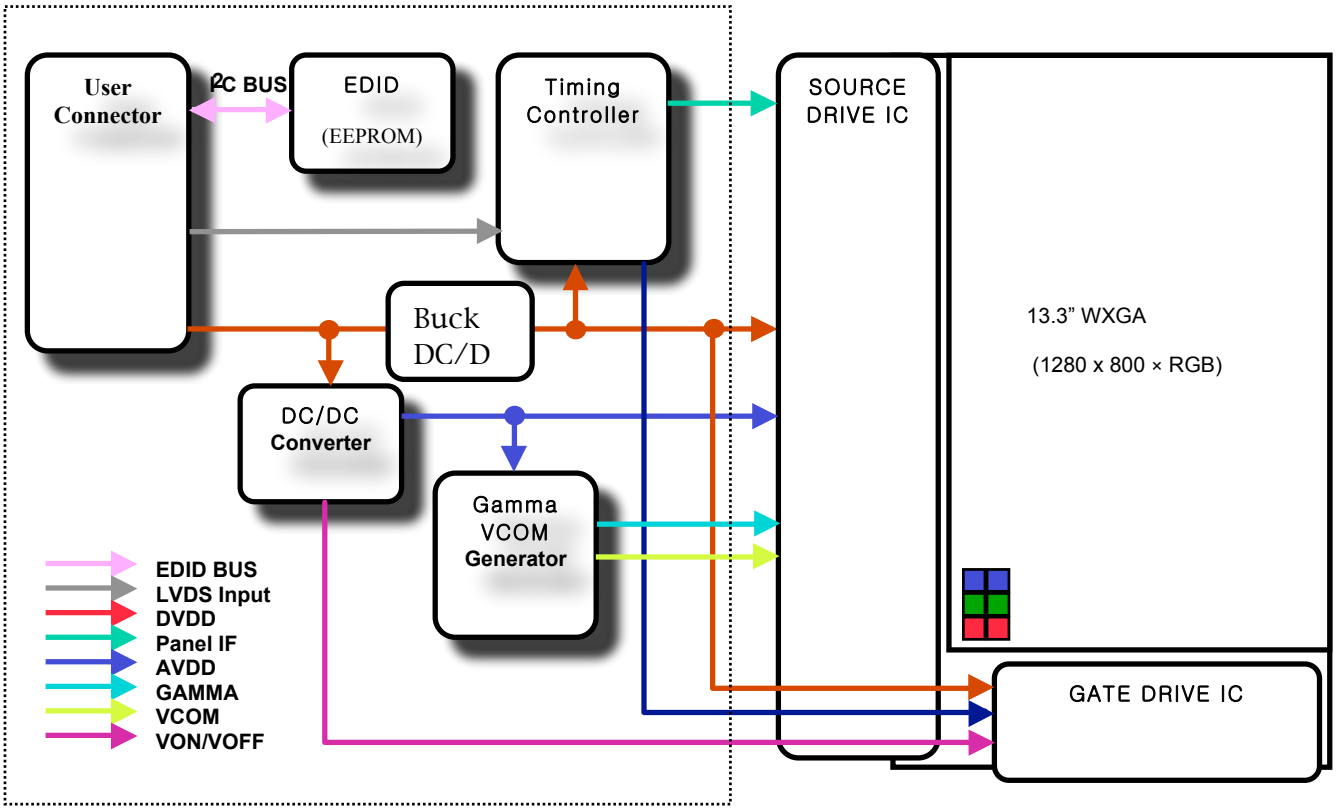
Total Maximum Thickness	(w/o PCB)	3.60
PCB Thickness (8 Layer PCB)		0.8
Maximum Component - 1 side (include Solder)		1.15
Maximum Component - 2 side (include Solder)		0.2
Total Maximum PCB Thickness		2.15

4.4. Exposed Areas and Restrictions

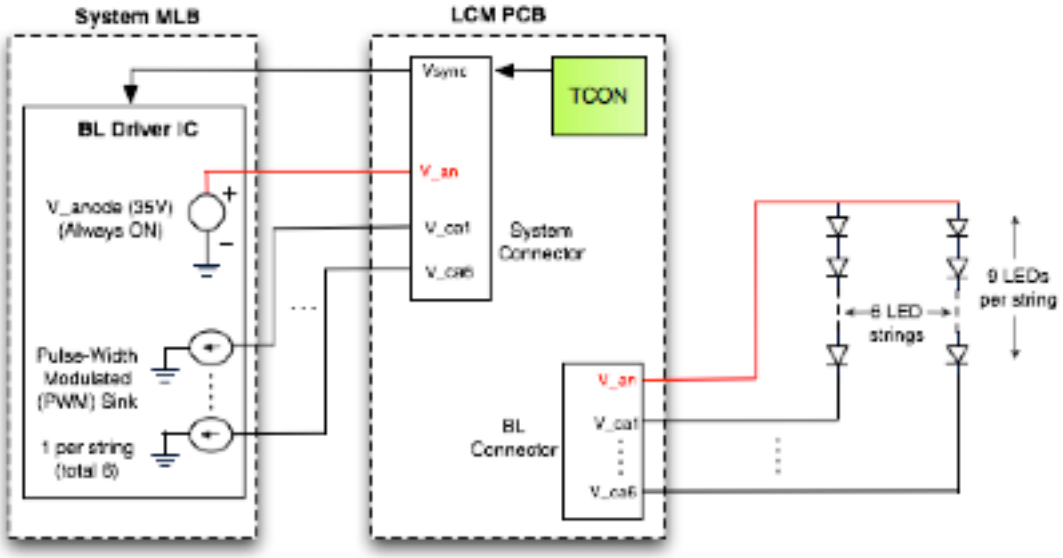
The display module shall not have exposed edges or components, which may cause injury or damage during handling, inspection, assembly, and service. Exposed areas of the display module (those not protected or shielded by construction) must be insulated and otherwise protected to eliminate the possibility of electrical shorting or destructive ESD discharges (per Section 7.2) during handling, inspection, assembly, and service. The Supplier shall identify all such areas prior to the Design Review and work with Apple Engineering to ensure the above criteria have been addressed.

5. ELECTRICAL REQUIREMENTS

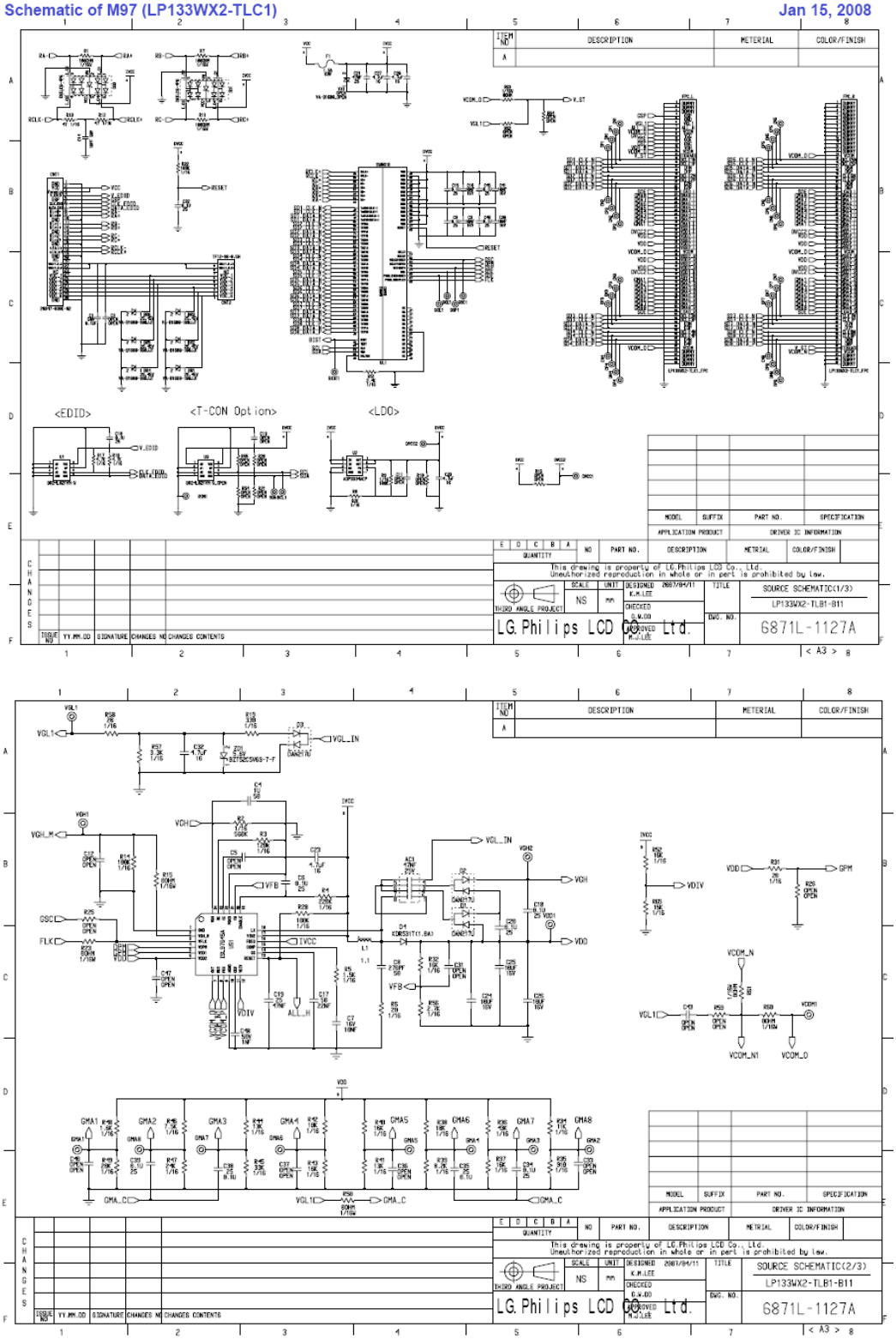
5.1. Block Diagram

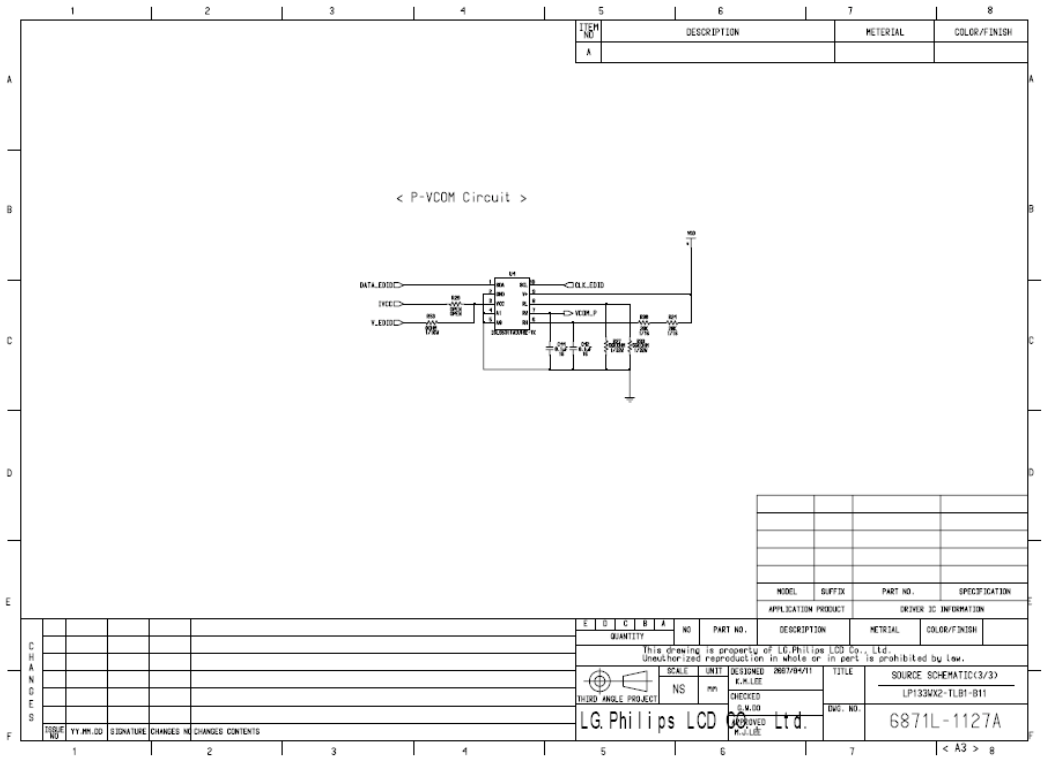


Backlight Driving Architecture



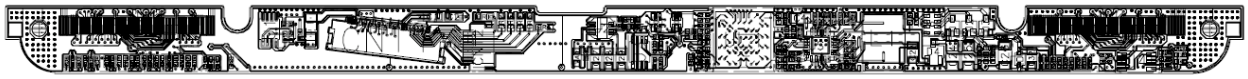
5.2. Display PCB Schematics



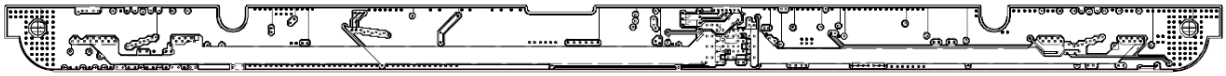


5.3. Display PCB Layout

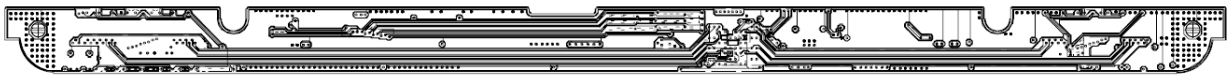
Layer 1:



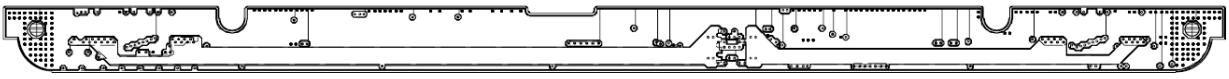
Layer 2:



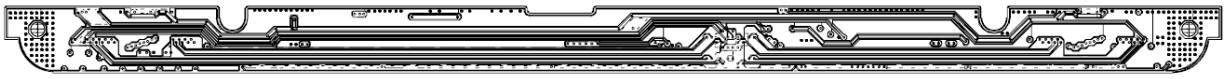
Layer 3:



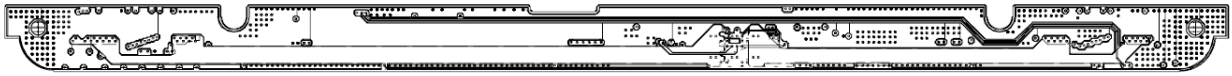
Layer 4:



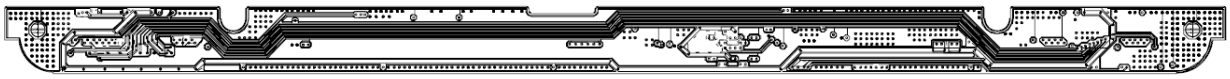
Layer 5:



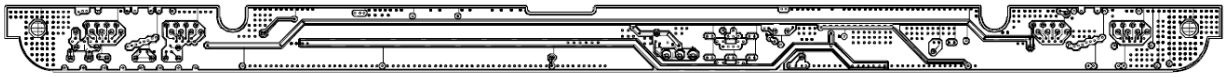
Layer 6:



Layer 7:



Layer 8:



5.4. Display Subsystem (PCB & TFT Panel)

5.4.1. Pin-Out (Single Channel LVDS Interface)

Connector: IPEX 20474-030E-12 or equivalent (1.0 mm thickness, lock-in type, pin 1 starts from left on the front)

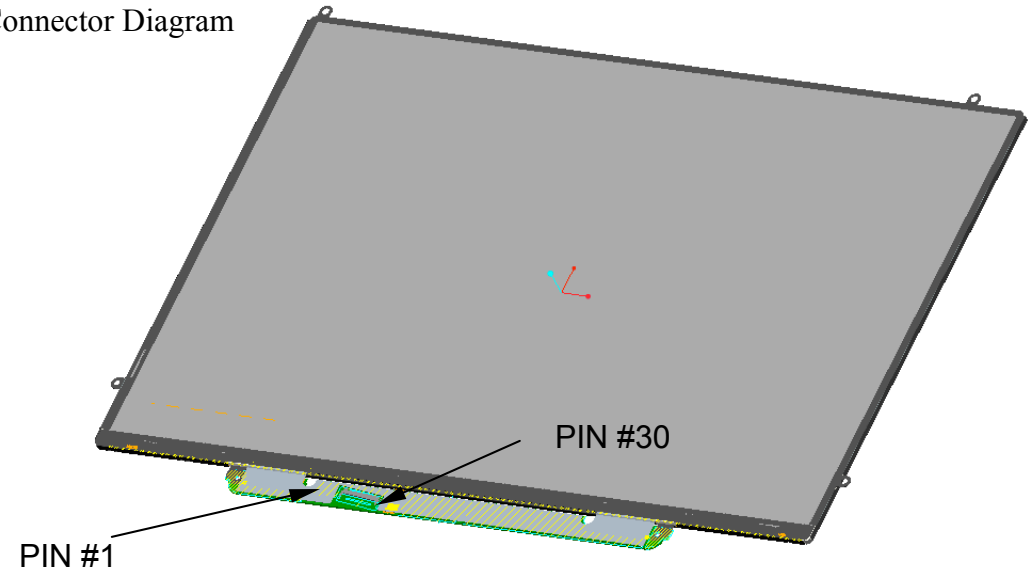
Matching Connector: IPEX 20472-030T-10 or equivalent (micro-coax type)

Interface Chips: (need update according the latest Configuration Sheet), integrated LVDS and timing controller)

Single Channel LVDS Configuration			
Pin	Symbol	Description	Micro-coax cable gauge (AWG)
1	GND	Ground	40
2	Vcc	Power Supply (+3.3V)	**36**
3	V_{analog}	Power Supply (+3.3V)	**36**
4	V_{EDID}	DDC Power +3.3V	40
5	Vsync	Vsync	40
6	Clk_{EDID}	DDC Clock	40
7	$DATA_{EDID}$	DDC Data	40
8	Rin0-	Differential Data Input	40
9	Rin0+	Differential Data Input	40

10	GND	Ground	40
11	Rin1-	Differential Data Input	40
12	Rin1+	Differential Data Input	40
13	GND	Ground	40
14	Rin2-	Differential Data Input	40
15	Rin2+	Differential Data Input	40
16	GND	Ground	40
17	Clkin-	Differential Clock Input	40
18	Clkin+	Differential Clock Input	40
19	GND	Ground	40
20	NC	NC	40
21	Vdc(1 &2)	LED Annold (Positive)	40
22	Vdc(3&4)	LED Annold (Positive)	40
23	NC	NC	40
24	Vdc1	LED Cathode (Negative)	40
25	Vdc2	LED Cathode (Negative)	40
26	Vdc3	LED Cathode (Negative)	40
27	Vdc4	LED Cathode (Negative)	40
28	Vdc5	LED Cathode (Negative)	40
29	Vdc6	LED Cathode (Negative)	40
30	NC	NC	40

5.4.2. Connector Diagram



5.4.3. Color Input Data Reference

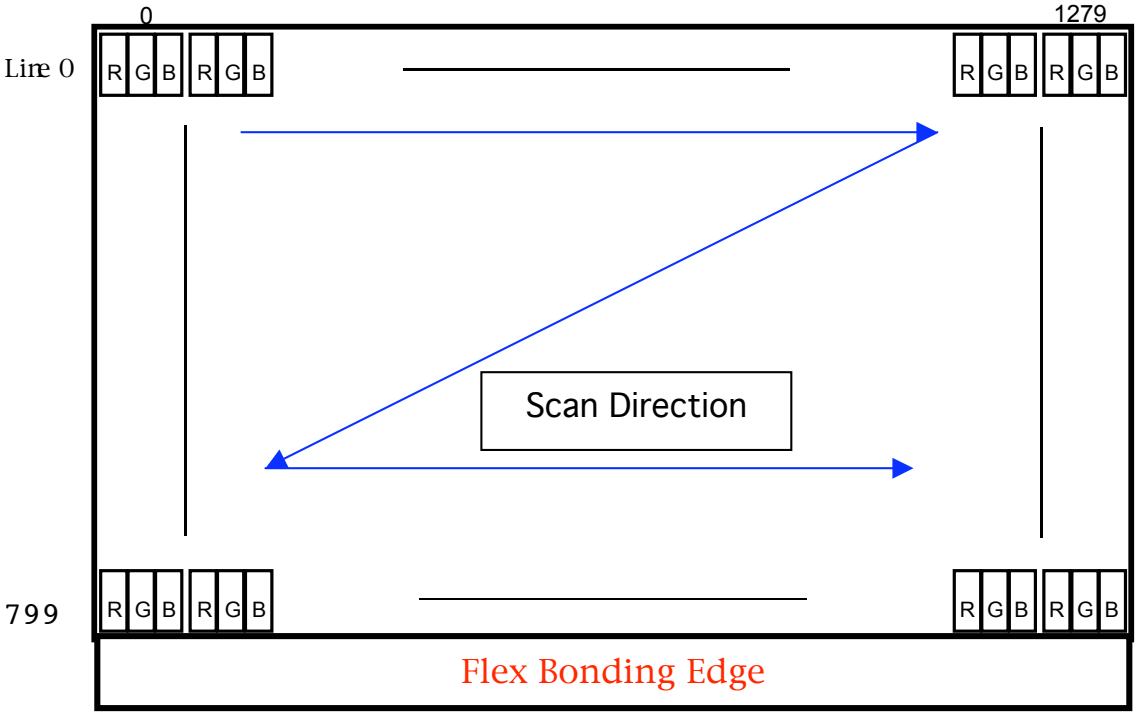
The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																	
		Red						Green						Blue					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(00) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63) Bright	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(00)Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0

	Green(63)Bright	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue(00) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63) Bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Pixel Format on the Display



5.4.4. EDID Interface (Per Vesa EDID 1.x standard requirements)

Ver0.3

LP133WX2-TLC1 EDID Data

2008.07.12

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)		Value (binary)	
0	00	Header	0	0	0000 0000	**Header**
1	01	Header	F	F	1111 1111	
2	02	Header	F	F	1111 1111	
3	03	Header	F	F	1111 1111	
4	04	Header	F	F	1111 1111	
5	05	Header	F	F	1111 1111	
6	06	Header	F	F	1111 1111	
7	07	Header	0	0	0000 0000	
8	08	EISA manufacturer code(3 Character ID) = APP	0	6	0000 0110	**Vender/ Product ID**
9	09	Compressed ASCII	1	0	0001 0000	
10	0A	Product code(Refer to Apple's request) = M97(0x9c89)	8	9	1000 1001	
11	0B	(Hex, LSB first)	9	C	1001 1100	
12	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	0	0	0000 0000	
13	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	0	0	0000 0000	
14	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	0	0	0000 0000	
15	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	0	0	0000 0000	
16	10	Week of Manufacture = Jan 15th 3week	0	3	0000 0011	
17	11	Year of Manufacture = 2008	1	2	0001 0010	
18	12	EDID Structure version # = 1	0	1	0000 0001	**EDID Version/ Revision**
19	13	EDID Revision # = 3	0	3	0000 0011	
20	14	Video Input Definition = Digital I/P,non TMDS CRGB	8	0	1000 0000	**Display Parameter**
21	15	Max H image size(㎝)=28.608cm(29)	1	D	0001 1101	
22	16	Max V image size(㎝)=17.880cm(18)	1	2	0001 0010	
23	17	Display gamma =2.2	7	8	0111 1000	
24	18	Feature support(DPMS) = Active off, RGB Color	0	A	0000 1010	
25	19	Red/Green low Bits	D	A	1101 1010	**Color Characteristic**
26	1A	Blue/White Low Bits	E	0	1110 0000	
27	1B	Red X = 0.597	9	8	1001 1000	
28	1C	Red Y = 0.349	5	9	0101 1001	
29	1D	Green X = 0.319	5	1	0101 0001	
30	1E	Green Y = 0.549	8	C	1000 1100	

31	1F	Blue X = 0.144	2	4	0010	0100	
32	20	Blue Y = 0.135	2	2	0010	0010	
33	21	White X = 0.313	5	0	0101	0000	
34	22	White Y = 0.329	5	4	0101	0100	
35	23	Established Timing I = 00h(If not used)	0	0	0000	0000	**Established Timings**
36	24	Established Timing II = 00h(If not used)	0	0	0000	0000	
37	25	Manufacturer's Timings = 00h(If not used)	0	0	0000	0000	
38	26	Standard Timing Identification 1 was not used	0	1	0000	0001	
39	27	Standard Timing Identification 1 was not used	0	1	0000	0001	
40	28	Standard Timing Identification 2 was not used	0	1	0000	0001	
41	29	Standard Timing Identification 2 was not used	0	1	0000	0001	
42	2A	Standard Timing Identification 3 was not used	0	1	0000	0001	
43	2B	Standard Timing Identification 3 was not used	0	1	0000	0001	
44	2C	Standard Timing Identification 4 was not used	0	1	0000	0001	**Standard**
45	2D	Standard Timing Identification 4 was not used	0	1	0000	0001	**Timing ID**
46	2E	Standard Timing Identification 5 was not used	0	1	0000	0001	
47	2F	Standard Timing Identification 5 was not used	0	1	0000	0001	
48	30	Standard Timing Identification 6 was not used	0	1	0000	0001	
49	31	Standard Timing Identification 6 was not used	0	1	0000	0001	
50	32	Standard Timing Identification 7 was not used	0	1	0000	0001	
51	33	Standard Timing Identification 7 was not used	0	1	0000	0001	
52	34	Standard Timing Identification 8 was not used	0	1	0000	0001	
53	35	Standard Timing Identification 8 was not used	0	1	0000	0001	

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)		Value (binary)		
54	36	Pixel Clock/10,000 (LSB) 72.5 MHz @ 60.2Hz	5	2	0101	0010	
55	37	Pixel Clock/10,000 (MSB)	1	C	0001	1100	
56	38	Horizontal Active (lower 8 bits) 1280 Pixels	0	0	0000	0000	
57	39	Horizontal Blanking(Thp-HA) (lower 8 bits) 143 Pixels	8	F	1000	1111	

58	3A	Horizontal Active / Horizontal Blanking(Thp-HA) (upper 4:4bits)	5	0	0101 0000	
59	3B	Vertical Avtive 800 Lines	2	0	0010 0000	
60	3C	Vertical Blanking (Tvp-HA) (DE Blanking typ.for DE only panels) 46 Lines	2	E	0010 1110	
61	3D	Vertical Active : Vertical Blanking (Tvp-HA) (upper 4:4bits)	3	0	0011 0000	**Timing**
62	3E	Horizontal Sync. Offset (Thfp) 48 Pixels	3	0	0011 0000	**Descriptor**
63	3F	Horizontal Sync Pulse Width (HSPW) 32 Pixels	2	0	0010 0000	**#1**
64	40	Vertical Sync Offset(Tvfp) : Sync Width (VSPW) 3 Lines : 6 Lines	3	6	0011 0110	
65	41	Horizontal Vertical Sync Offset/Width (upper 2bits)	0	0	0000 0000	
66	42	Horizontal Image Size = 286.08mm(286)	1	E	0001 1110	
67	43	Vertical Image Size = 178.80cm(179)	B	3	1011 0011	
68	44	Horizontal & Vertical Image Size	1	0	0001 0000	
69	45	Horizontal Border = 0	0	0	0000 0000	
70	46	Vertical Border = 0	0	0	0000 0000	
71	47	Non-interlaced,Normal display,no stereo,Digital separate sync,H/V pol negatives	1	8	0001 1000	
72	48	Detailed Timing Descriptor #2	0	0	0000 0000	
73	49		0	0	0000 0000	
74	4A		0	0	0000 0000	
75	4B		0	1	0000 0001	
76	4C	Version	0	0	0000 0000	
77	4D	Apple edid signature	0	6	0000 0110	
78	4E	Apple edid signature	1	0	0001 0000	
79	4F	Link Type	2	0	0010 0000	**Timing**
80	50	Pixel and link component format(6-bit panel interface)	0	0	0000 0000	**Description**
81	51	Panel features(Inverter NA, no inverter)	0	0	0000 0000	**#2**
82	52		0	0	0000 0000	
83	53		0	0	0000 0000	
84	54		0	0	0000 0000	
85	55		0	0	0000 0000	
86	56		0	0	0000 0000	
87	57		0	0	0000 0000	
88	58		0	A	0000 1010	
89	59		2	0	0010 0000	
90	5A	Detailed Timing Descriptor #3	0	0	0000 0000	
91	5B		0	0	0000 0000	
92	5C		0	0	0000 0000	
93	5D		F	E	1111 1110	
94	5E		0	0	0000 0000	
95	5F	L	4	C	0100 1100	

96	60	P	5	0	0101	0000	**Timing Description #3**
97	61	1	3	1	0011	0001	
98	62	3	3	3	0011	0011	
99	63	3	3	3	0011	0011	
100	64	W	5	7	0101	0111	
101	65	X	5	8	0101	1000	
102	66	2	3	2	0011	0010	
103	67	-	2	D	0010	1101	
104	68	T	5	4	0101	0100	
105	69	L	4	C	0100	1100	
106	6A	C	4	3	0100	0011	
107	6B	1	3	1	0011	0001	

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)		Value (binary)		
108	6C	Detailed Timing Descriptor #4	0	0	0000	0000	**Timing Description #4**
109	6D		0	0	0000	0000	
110	6E		0	0	0000	0000	
111	6F		F	E	1111	1110	
112	70		0	0	0000	0000	
113	71	C	4	3	0100	0011	
114	72	o	6	F	0110	1111	
115	73	l	6	C	0110	1100	
116	74	o	6	F	0110	1111	
117	75	r	7	2	0111	0010	
118	76	SPACE	2	0	0010	0000	
119	77	L	4	C	0100	1100	
120	78	C	4	3	0100	0011	
121	79	D	4	4	0100	0100	
122	7A	LF	0	A	0000	1010	
123	7B	SPACE	2	0	0010	0000	
124	7C	SPACE	2	0	0010	0000	
125	7D	SPACE	2	0	0010	0000	
126	7E	Extension flag = 00	0	0	0000	0000	**Extension Flag**
127	7F	Checksum	**A**	**7**	1010	0111	**Checksum**

5.4.5. Electrical Ratings

PARAMETER	SYMBOL	VALUES			UNIT	NOTES
		Min.	Typ.	Max.		

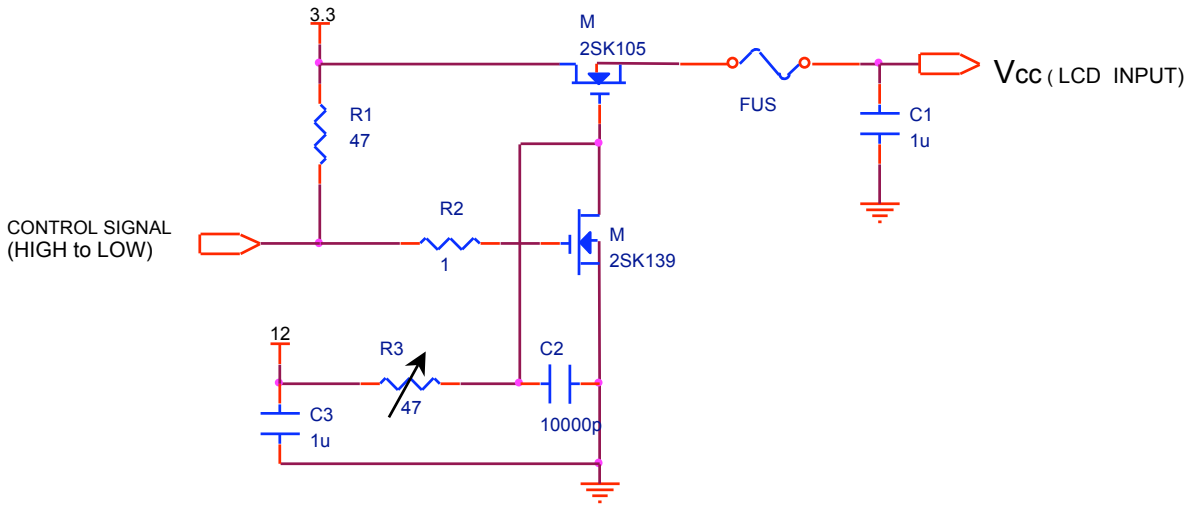
Power Supply Input Voltage	V_{CC}	3.0	3.3	3.6	V (DC)	
Power Supply Ripple			50		mV_{p-p}	1
Power Supply Input Current	I_{CC}	-	242	273	mA	2
Differential Impedance	Z_m	90	100	110	Ω	3
Power Consumption	P_c	-	0.8	0.9	W	2
Rush current	I_{RUSH}	-	-	1.5	A	4

Notes: (1) The power supply ripple is measured whereas a black pattern is displayed;

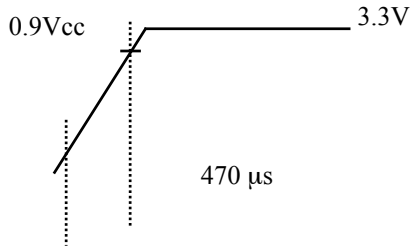
(2) The specified current and power consumption are under the conditions at V_{cc} = 3.3 V, T = 25ºC, and f_v = 60 Hz, f_{CLK}=72.5MHz, whereas a mosaic pattern (typical) is displayed;

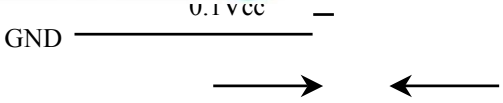
(3) This impedance value is needed to a proper display and is measured from LVDS mating connector to LVDS Rx

(4) The following is a typical Vcc circuit on the system side



<u>V_{cc} rise time is about 470 µs</u>





The duration of the rush current is about 20 ms.

5.4.6. Signal Timing

5.4.6.1. Signal Impedance

Defined in VESA standard for LVDS FPDI 2

5.4.6.2. Timing Data

This is the signal timing required at the input of the control ASIC concerned with LVDS as a FlatLink or equivalent. All of the interface signal timing should be satisfied with the following specifications based on the VESA timing guideline (1280x800 @ 60 Hz) for its proper operation.

Video Timing Data

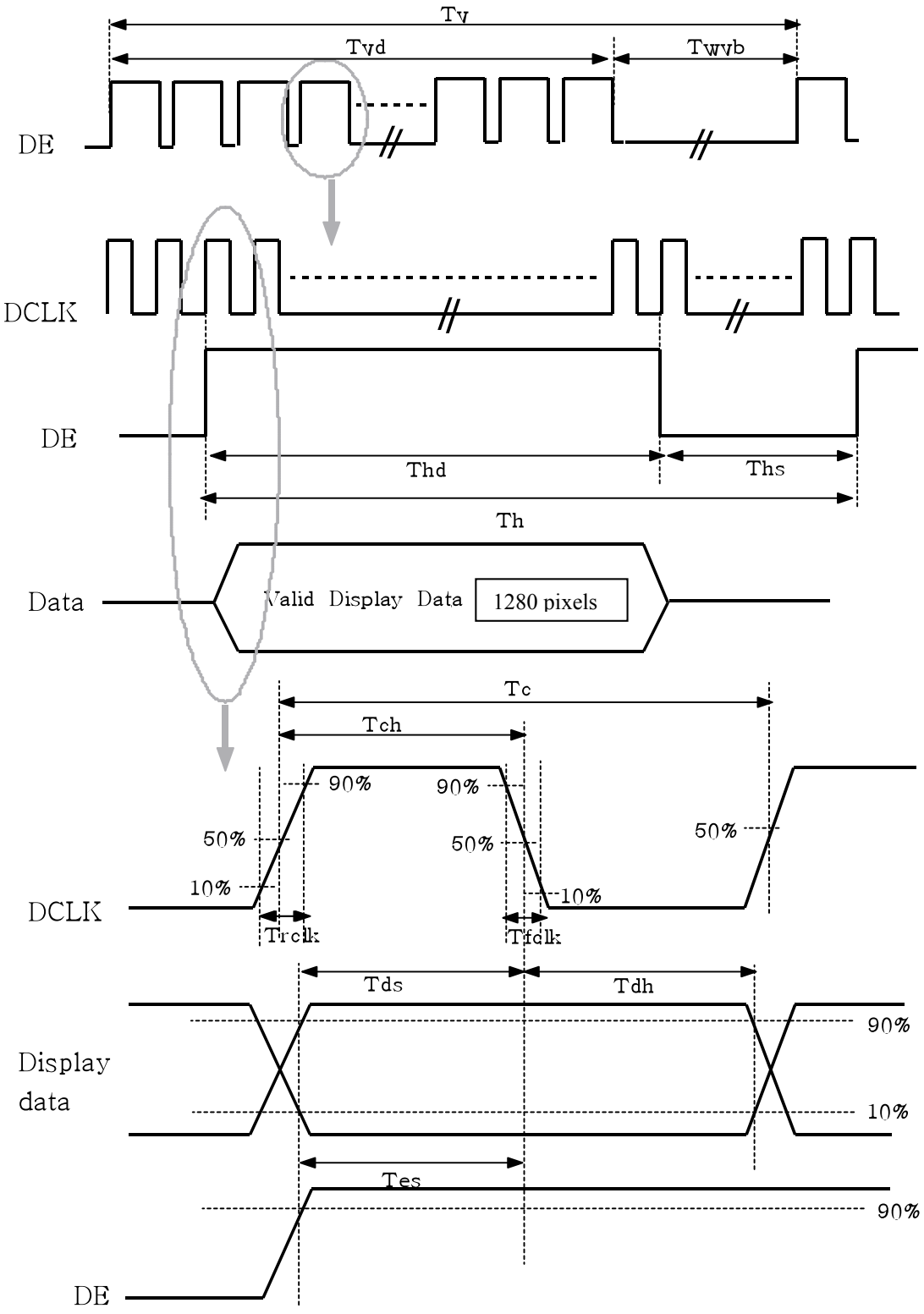
Signal	Parameter	Symbol	Min	Typ	Max	Unit	Note
D_{CLK}	Clock Period	T_C		13.79		ns	1
	Clock Frequency	f_C		72.50		MHz	$1/T_C$
	Duty Ratio (% High)	K_{dr}	40	50	60	%	T_{Ch}/T_C
	Rise Time	$T_{R\ CLK}$	-	4.42	-	ns	
	Fall Time	$T_{F\ CLK}$	-	4.42	-	ns	
DE	DE Setup Time	T_{se}	4	-	-	ns	
(Data Enable	Data Setup Time	T_{sd}	4	-	-	ns	
Only)	Data Hold Time	T_{hd}	2	-	-	ns	
(DTMG)	Horizontal Period	T_H		1440		T_C	2
Data	Horizontal Blank Period	T_{ha}		160		T_C	
	Vertical Period	T_V		823		T_H	f_V=59.94 Hz, 3
	Vertical Blank Period	T_{wvb}		23		T_H	
H_{sync}	H_{sync} Back Porch	H_{bp}		80		T_C	
	H_{sync} Pulse Width	T_{WH}		32		T_C	
	H_{sync} Front Porch	H_{fp}		48		T_C	
	Horizontal Active Period	T_{HD}	1280	1280	1280	T_C	Display Period
V_{sync}	V_{sync} Back Porch	V_{bp}		14		T_H	
	V_{sync} Pulse Width	T_{WV}		6		T_H	
	V_{sync} Front Porch	V_{fp}		3		T_H	
	Vertical Active Period	T_{VD}	800	800	800	T_H	Display Period

Note: (1) When the WXGA+ controller sets DE Mode, and H_{sync} and V_{sync} are required. The duration of DE (DTMG) signal must be longer than 1 clock period (T_C) at every horizontal sync period;

(2) Horizontal Period = One Line Scanning Time;

(3) The vertical period T_V is related to the frame frequency f_V, *i.e.*, 60 Hz.

5.4.6.3. Video Timing Diagram



5.4.7. Power Measurements (W/O backlight)

Pattern	Min	Typ	Max	Unit
White	To be updated			mA
Mosaic		242	273	mA
V. Stripe	To be updated			mA
Black		273	303	mA

Note: (1) Display data pins and timing signal pins should be connected (GND = 0V);

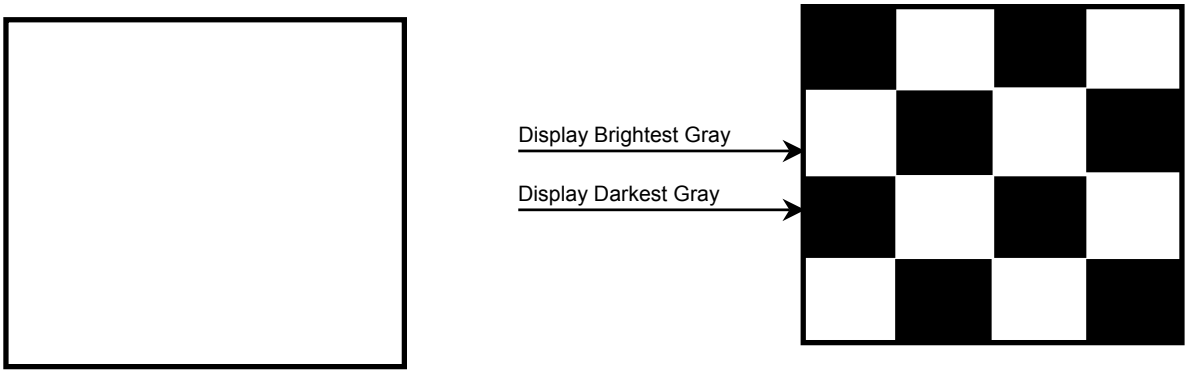
(2) Operation conditions: f_V = 60 Hz, f_{CLK} = 72.5 MHz, V_{cc} = 3.3 V;

(3) Power dissipation patterns are as follows.

(a) White screen

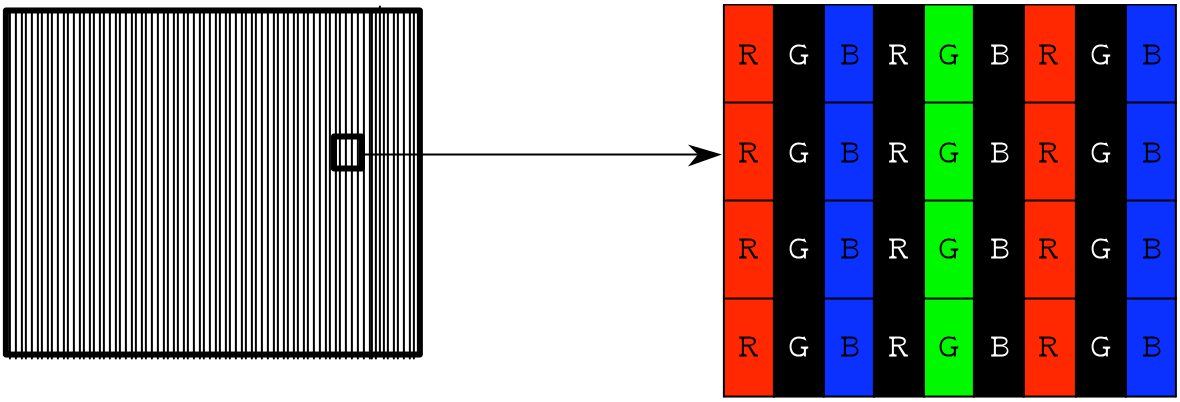
(b) Mosaic (or checker) pattern

20x20 pixel black and white boxes



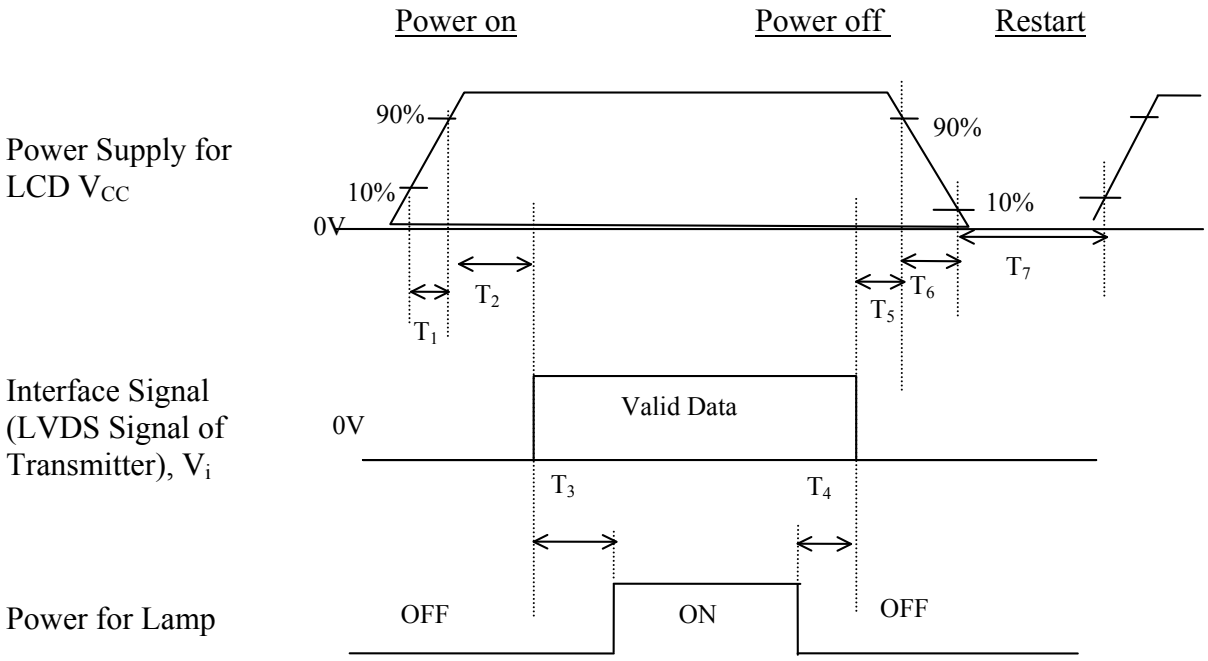
(c) Vertical Stripe Pattern

sub-pixel vertical line on/off alternation,



5.4.8. Power on-off sequence

Power-on includes both MacBook system starting from power-off state and wake from sleep state; power-off includes both MacBook system shutdown and entering sleep state.



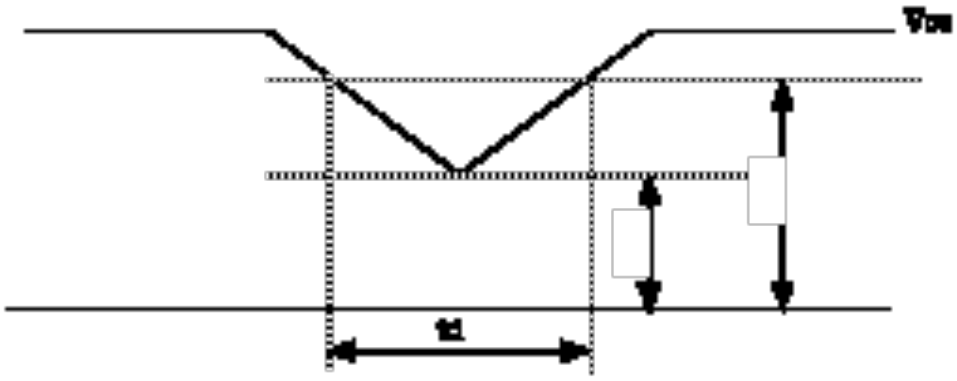
Parameter	Values			Unit
	Min.	Typ.	Max.	
T_1	0.15	-	10	ms
T_2	1	20	50	ms
T_3	200	250	-	ms
T_4	200	250	-	ms
T_5	0	20	50	ms
T_6	5	-	20	ms
T_7	500	-	-	ms

5.4.9. Vcc Dip Condition

The V_{cc} dip is the Vcc voltage drop during panel start-up.

(1) $2.5V \leq V_{cc} < 3.0$ V, $T_d \leq 20$ ms;

(2) For $V_{cc} < 2.5V$, V_{cc} should follow the power on-off sequence defined in 5.4.8



5.5. Near-Field Noise

The RF emissions from the panel (especially the LVDS input and Tcon) interfere with Wifi operation. The panel vendor shall follow the noise characterization process outlined in Apple's near field noise spec 069-2794, and comply with noise emission limits.

Note that this spec compliance requirement is in addition to the legal EMI compliance requirements.

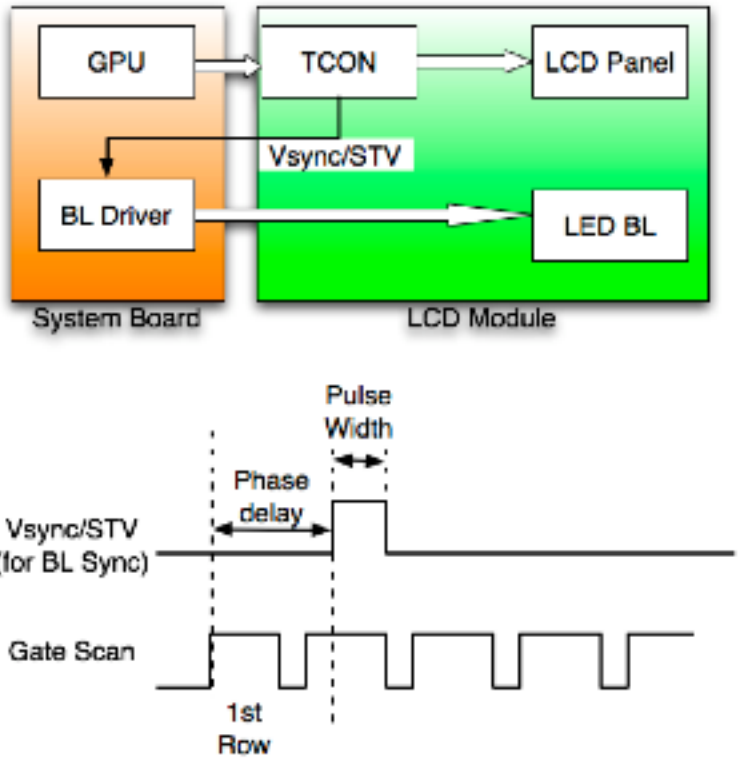
5.6. Backlight Subsystem

5.6.1. General Information

LED Manufacturer	Nichia
LED Manufacturer Assembly P/N	NNSWT108-S1 (HS backlight) 62-YW2D7-08 (ROE backlight)
Number of LEDs	54
LED Bin	TBD
LED Ranks	TBD

LED Brightness Bin	
LED Vf Bin	0.2 V per bin
LED Forward Voltage Range for All 6 LED Series Lines	MAX: 30.6 V (Characterized at LVDS Connector for 20 mA)

5.6.2. Backlight Synchronization Requirement (to avoid BL shimmering)



The Vsync/STV signal is a once-per-frame pulse that has a constant phase delay with respect to the start of the frame. This signal is used by the backlight LED driver to synchronize BL PWM with the frame update to avoid shimmering (waterfall) artifacts in the image.

The minimum pulse width is 1 us.

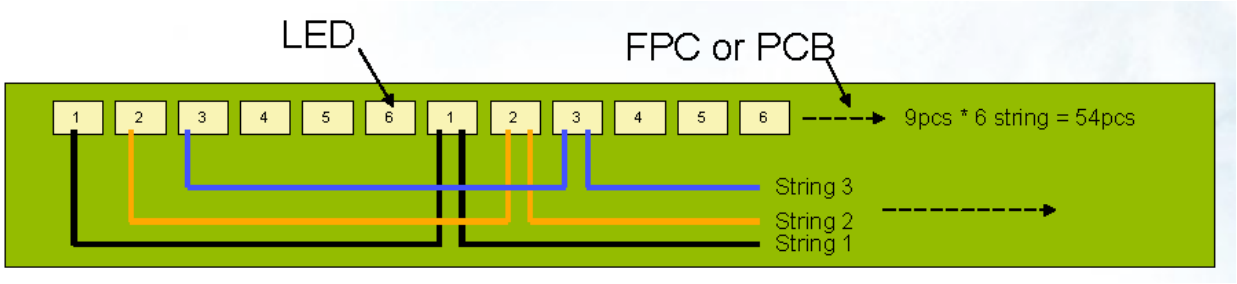
5.6.3. Backlight Electrical Characteristics

The backlight brightness test shall be tested at 600Hz PWM cycle & 20mA peak current with following percentage duty cycle

LED Current (% duty cycle)	LED Forward Voltage for any LED string	Power (W) Assuming 3.3V average forward bias	Display Minimum Luminance (nits)	Display Typical Luminance (nits)	Display Maximum Luminance (nits)
100%	30.6 V	3.56	261	290	319
95%	30.6 V	3.38	248	275	303
22.8%	30.6 V	0.81	57	66	72
3.8%	30.6 V	0.14	10	11	12

5.6.4. LED Connection

String	LED1	LED2	LED3	LED4	LED5	LED6	LED7	LED8	LED9
1	1	7	13	19	25	31	37	43	49
2	2	8	14	20	26	32	38	44	50
3	3	9	15	21	27	33	39	45	51
4	4	10	16	22	28	34	40	46	52
5	5	11	17	23	29	35	41	47	53
6	6	12	18	24	30	36	42	48	54



6. OPTICAL REQUIREMENTS

6.1. Optical Specifications

Supplier must submit optical measurement data from 20 samples for items marked critical in Table 6.1.1. The optical performance will be approved by Apple based on supplier's measurement data, visual inspection of the samples, verification measurements, and specification correlation.

Table 6.1.1: Optical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Iso-Contrast Viewing Angle CR ≥ 10	θ	up	15	20	--	Degrees	1,2,3
		down	30	35			
		left/right	40/40	50/50			
Contrast ratio	CR	Optimal	400	500	--	--	1,2,3
Luminance	Y	I_{LED}=20mA @95% duty cycle	248	275	--	cd/m^2	1,2,4
Global Luminance Uniformity		Optimal	50		--	%	1,2
Worst Neighbor Luminance Uniformity		Optimal	65		--	%	1,2
Gamma	γ	--	--	2.2	--	--	1,2,3
Flicker	F	No Visual Flicker	--	--	-30	dB	1,2,3
Cross Talk	D_{SHA}	Optimal	--		2.0	%	1,2,3
Worst Low Level (dark) Inversion Viewing Direction		PCB on the bottom	--	6:00	--	o'clock	1,2
Response (rise+fall time)	τ_{on+off}	θ = 0°, Ta=25°C	--	16	25	ms	1,2,3
Gray to Gray Response time	τ_{G2G}	θ = 0°, Ta=25°C	--		40	ms	1,2,3
White Chromaticity (all panels)	x	CIE 1931	0.297	0.313	0.329	--	1,2,3
	y		0.313	0.329	0.345	--	1,2,3
White Chromaticity (Within one panel)	delta x	max			0.005		
	delta y	max			0.008		

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Red Chromaticity	x	CIE 1931	0.575	0.595	0.615	--	1,2,3
	y		0.325	0.345	0.365	--	1,2,3
Green Chromaticity	x	CIE 1931	0.300	0.320	0.340	--	1,2,3
	Y		0.535	0.555	0.575	--	1,2,3
Blue Chromaticity	X	CIE 1931	0.135	0.155	0.175	--	1,2,3
	Y		0.125	0.145	0.165	--	1,2,3
Max color difference within one panel	du'v'	white			0.005		1,2
Max color difference w.r.t. Center within one panel	du'v'	white			0.003		1,2
Max color difference from panel to panel	du'v'	white			0.008		
Max color difference between neigbors	du'v'	white			0.0025		1,2

Note 1: The testing conditions are specified in 6.2.

Note 2: The definitions of optical characteristics are shown in 6.3.

Note 3: Measured at center point. Equivalent performance over the entire panel required.

Note 4: Both center point and average of 160 points.

6.2. Measuring Conditions

The optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes at the maximum brightness, in a dark environment at an ambient temperature at 25°C ± 2°C. The electrical conditions include V_{cc} = 3.3 V, f_v = 60 Hz, f_{CLK} = 72.5 MHz, I_{BL} = 20.0 mA @95% duty cycle with 600Hz. Recommended measuring equipments for luminance and color are CCD based imaging systems such as Radiant Imaging Prometric 1400 system, or Colorimeter such as Photo Research PR650, TOPCON BM-5A or similar. The measuring distance should be about 50 cm from the LCD surface at normal unless otherwise specified. Measurements should be done on the 160 grid points as shown in the following figures. The measurement spot at

the center is approximately 12 mm in diameter from a distance of 400 mm by TOPCON BM-5A or 15 mm in diameter from a distance of 500 mm by PR 650.

Viewing angle measurements should be done by an Eldim EZ Color system or similar.

The CIE 1931 or 1976 Standards will be used.

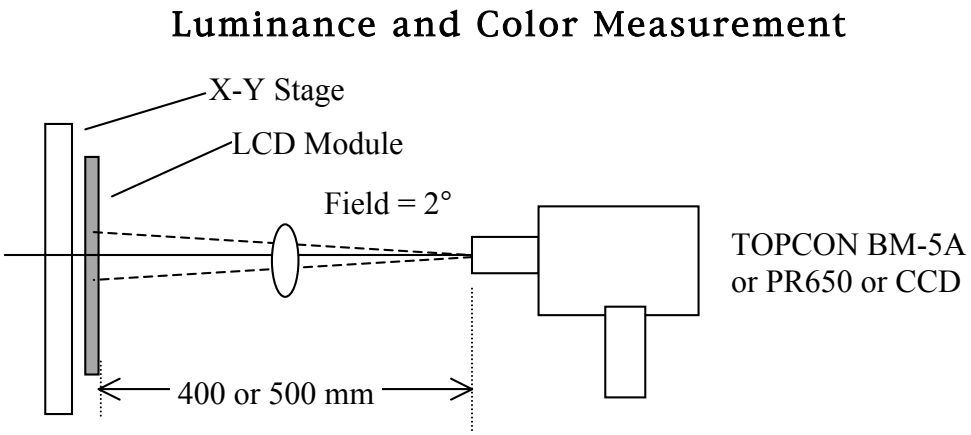


Figure 6-1: Optical Measurement Set-up

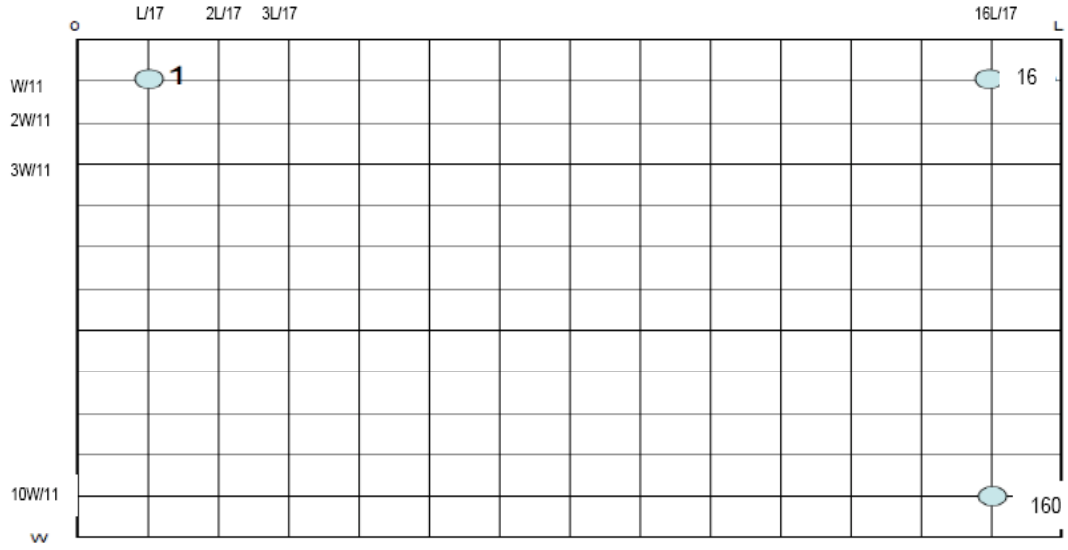


Figure 6-2: Measurement point location. L and W are the length and width of Active Area respectively.

6.3. Definition

6.3.1. Center Point Luminance

L_{ct} =(L_{72+} L_{73+} L_{88+} L_{89})/4{Average Luminance value at point #72, 73, 88, 89}

6.3.2. Average Luminance

L_{Ave} = SUM(L_1:L_{160}) / 160

where L_1 to L_{160} are the luminance values measured at point #1 to #160.

6.3.3. Luminance Uniformity

The entire display active area shall be scanned with the luminance measurement with white screen set full brightness.

Apple requires two kinds of data for brightness uniformity: Luminance Uniformity, and Worst Neighbor Luminance Uniformity. The definitions are shown in below:

6.3.3.1. Global Luminance Uniformity:

$U = 100\% - (L_{max}-L_{min})/L_{max}$

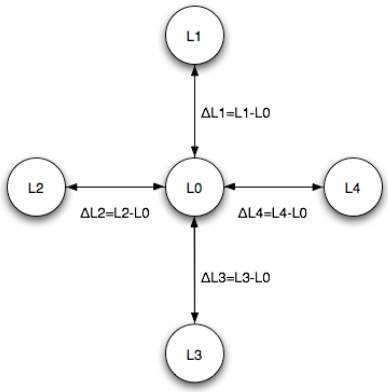
where, L_{max} = max {Luminance values at 160 points},

L_{min} = min {Luminance values at 160 points}

6.3.3.2. Worst Neighbor Luminance Uniformity (The 4 points that are closest to the test point)

WNU=100%-Max(ΔL1, ΔL2, ΔL3, ΔL4)/L0

Global WNU = min (WNU1, …WNU160)



6.3.4. Contrast Ratio

CR = Luminance at G_{max} / Luminance at G_{min} {Average contrast value at point #72, 73, 88, 89}

6.3.5. White Color Uniformity

The entire display active area shall be scanned with the color coordinate measurement with white screen set full brightness.

6.3.5.1. Panel to Panel White Color Uniformity

The center point (as defined by the average value at point #72, 73, 88, 89) white color coordinate of any panel shall be within the box with 4 corners coordination boundary listed in Table 6.1.

6.3.5.2. Max Color Difference with respect to the center within a panel

On each panel, the maximum color difference between any of the 160 points and the center point (defined as the average value at point #72, 73, 88, 89), represented in delta u'v'.

6.3.5.3. Max Color Difference between any two points within the panel

On each panel, the maximum color difference between any two of the 160 points, represented in delta u'v'.

6.3.5.4. Max Color Difference between two neighbors

On each panel, the maximum color difference between any two neighboring points on the panel, represented in delta u'v'

6.3.6. RGB Color Chromaticity

The entire display active area shall be scanned with the color coordinate measurement with screen set to full brightness and solid R, G, B color respectively. The measured color coordinate of any panel shall be within the box with 4 corners coordination boundary listed in Table 6.1.

6.3.7. Viewing Angle

The viewing angle is defined as the viewing angle range under the condition at CR $\geq$ 10:1 .

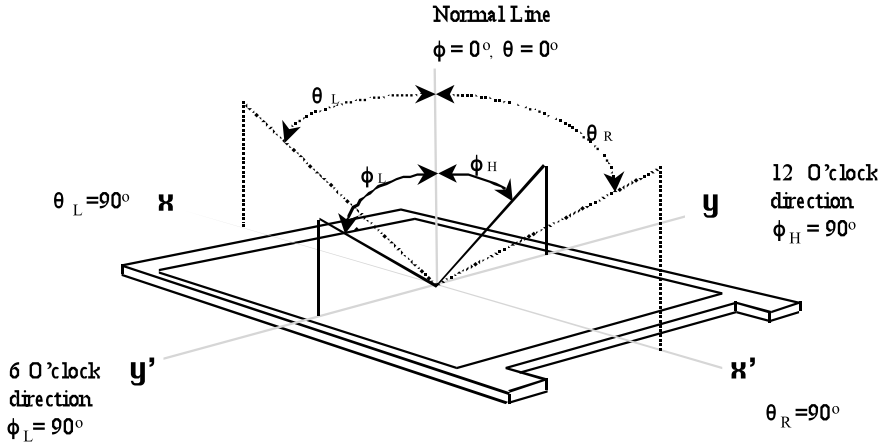


Figure 6-4: Viewing angle definition

6.3.8. Gray Scale Inversion

Luminance vs. viewing angle curves are measured based on gray level 255, 223, 191, 159, 127, 95, 63, 32 and 0, in the viewing angle of left, right, up, down, with PCB on the bottom side. Gray scale inversion happens when a higher gray scale measures the same luminance or lower luminance than any of the lower gray scale.

6.3.9. Response Time

6.3.9.1. On and Off Response Time

The On/Off response time, $t_R + t_F$, is defined in the following figure and shall be measured by switching the input signal for "black" and "white".

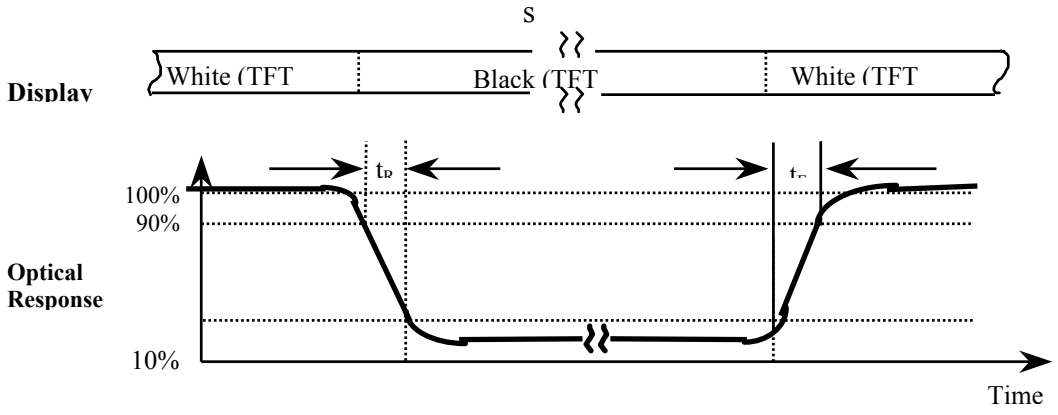


Figure 6-5: Response Time Measurement

6.3.9.2. Gray to Gray Response Time

Gray to Gray Response Time is measured in a similar method. But instead of switching display between black and white, panel is switched between two gray scales. The maximum gray-to-gray response time is based on 9 levels of gray scales. The 9 levels are: gray level 255, 223, 191, 159, 127, 95, 63, 32 and 0. Figure 6-6 shows an example of Gray to Gray Response Time measurement data.

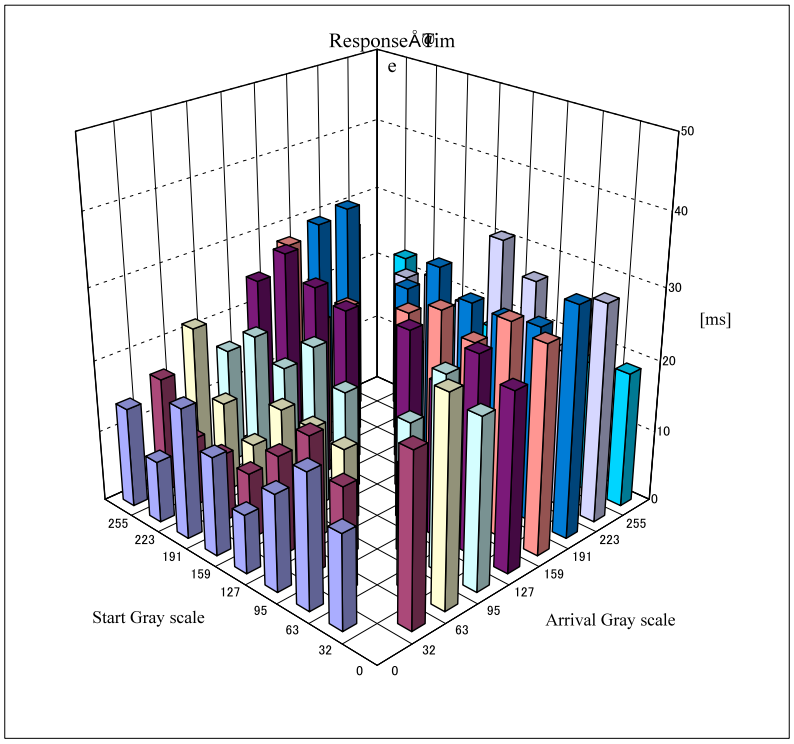


Figure 6-6: Gray to Gray Response Time

6.3.10. Gray Scale Linearity or Gamma Value

The display luminance, L_G, is measured at the different gray scales, G_{min}, …, G_{max}. The exponential fitting is used to determine the gamma (γ) value, which should be an intrinsic or uncorrected characteristic.

$$L_G \sim G^{\gamma}.$$

6.3.11. Flicker

No visual flicker will be allowed. The flicker level should be measured with either vertical stripes or a checker pattern, defined in Sec. 5.3.6. The output signal of a photometer is sent to an FFT analyzer. The flicker is essentially a ratio of the powers in the frequency spectrum at 30 Hz (P_x) and 0 Hz (P_0), *i.e.*,

$$F = 10 \text{ Log } (P_x / P_0).$$

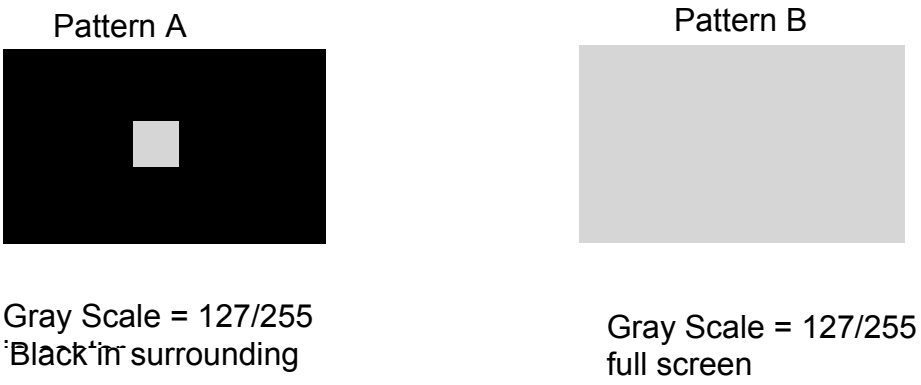
6.3.12. Cross-talk

No visual cross-talk will be allowed. Two luminance values are measured at center spot with 50 x 50 pixels. The cross-talk, D_{SHA}, is defined as,

$$D_{SHA} = (L_B - L_A)/L_B \bullet 100\%,$$

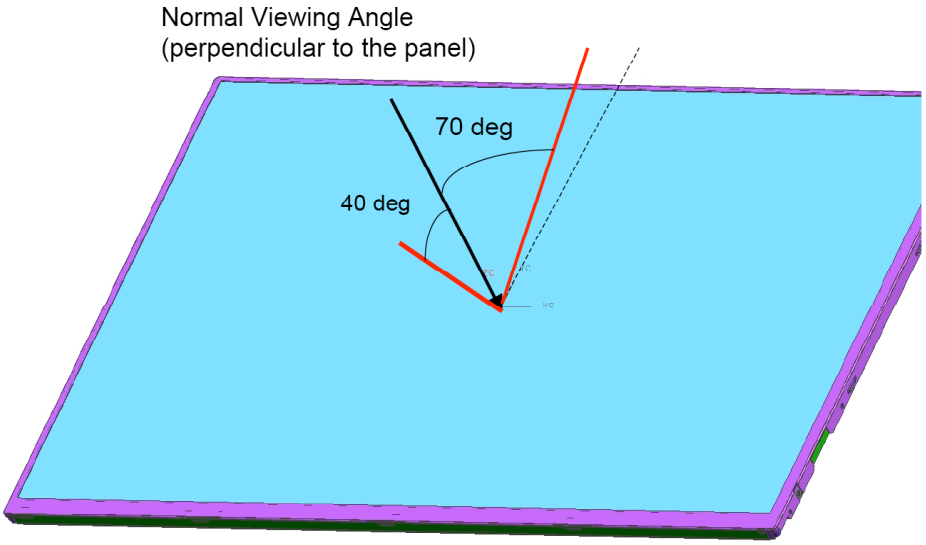
Where, L_A = Luminance in Pattern A

L_B = Luminance in Pattern B.



6.4. Hot Spot Specifications:

The LED hot spot shall be inspected from 70 degree to -40 degree per the drawing below. There shall be no visible hot spot or no worse than “limited sample” hot spot (if there is a “limited sample” set up.



6.5. FOS Shimmering Specifications

Shimmering is defined as moving bands on the front of the screen in the appearance of water-fall, waves, and etc. Shimmering needs to be tested under the following conditions:

-Test Fixture should read Apple approved EDID from panel and drive the panel based on EDID setting

-LVDS Pixel Clock Frequency: 72502443 Hz

-LED PWM Frequency: 542 Hz

-LED PWM Duty Cycle: 2%, 25% 50%, 100%

-Test Image: Full screen R,G,B, White at gray scale 255, 223, 191, 159, 127, 95, 63, 32 and 0 (8 bits)

-Viewing direction: 80deg w.r.t. normal axis in any viewing direction

No shimmering is allowed under any of the inspection conditions.

7. ENVIRONMENTAL

The display modules shall meet all functional and cosmetic specifications after testing to the environmental quality standards listed in this section. Additionally, the LCD modules in Apple's products shall pass all the system testing requirements listed in the end of this document.

7.1. Shock and Vibration

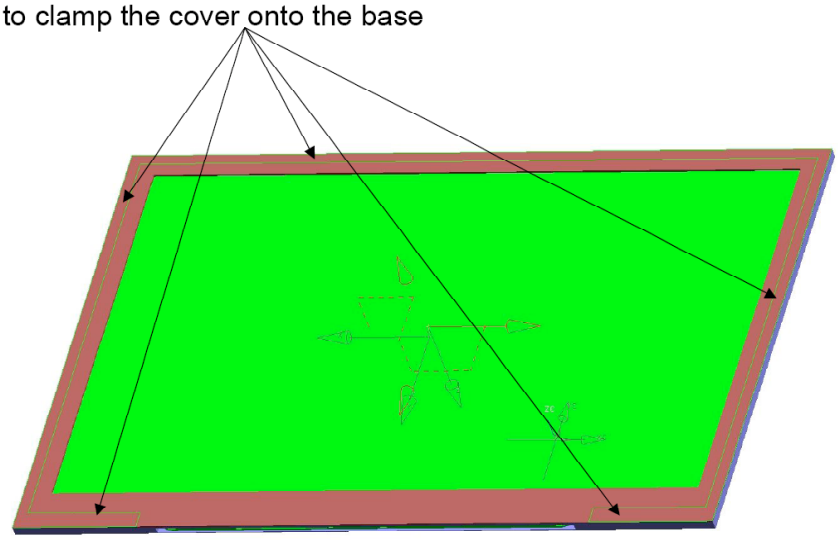
7.1.1 There will be no functional or cosmetic defects following a shock to all 6 sides delivering at least 200 G in a half sine pulse no longer than 2 ms to the display module, secured by its designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.

7.1.2 There will be no functional defects following a shock delivering at least 260 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays. The displays are secured by designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.

7.1.3 There will be no functional or cosmetic defects following a shock delivering at least 60 G in a pulse 11 msec or longer to the display module, secured by its designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.

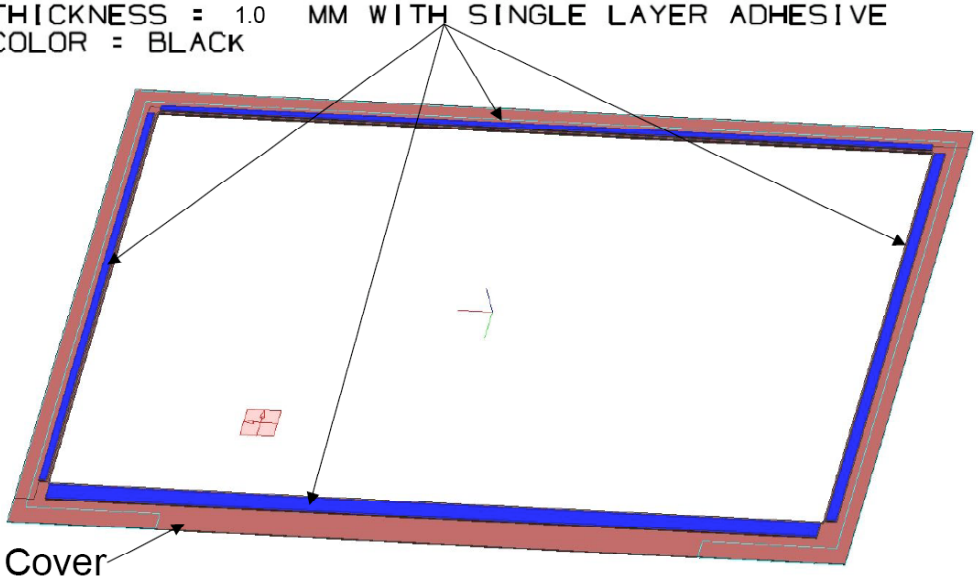
7.1.4 There shall be no functional or cosmetic defects following a vibration test, conducted at **3.0** G from 5–150 Hz, 0.37 Oct/min with sine wave for 30 min./axis, with the display secured by its designated mounting details, and conducted in accordance with MIL-STD-202F, method 201A.

Area to clamp the cover onto the base

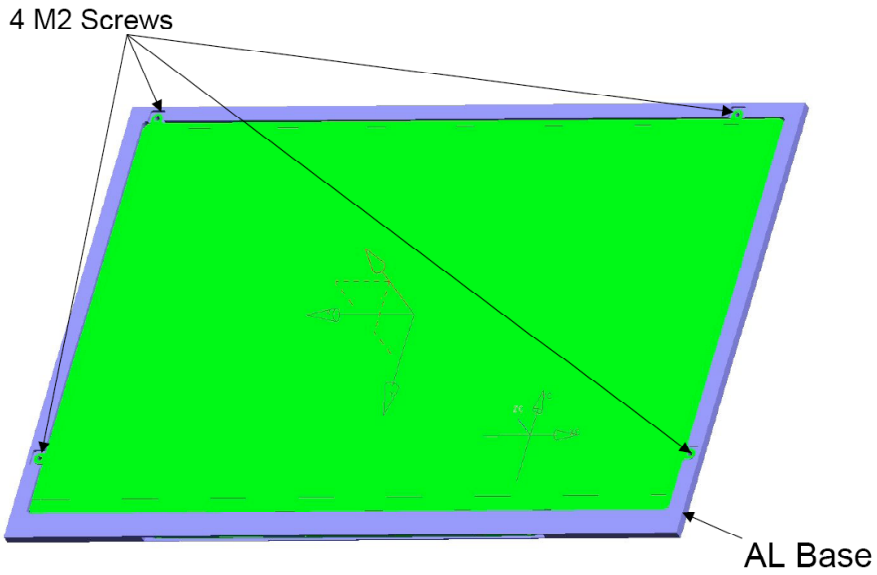


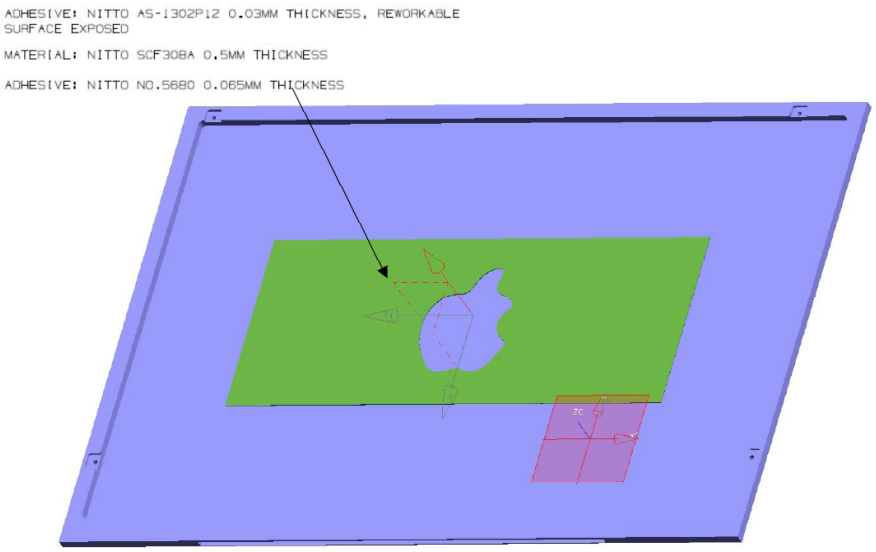
Poron Gaskets

MATERIAL: PORON S-RS 40P
COMPRESSIVE LOAD (AT 50%) = 2.2 N/CM^2
THICKNESS = 1.0 MM WITH SINGLE LAYER ADHESIVE
COLOR = BLACK



AL Cover



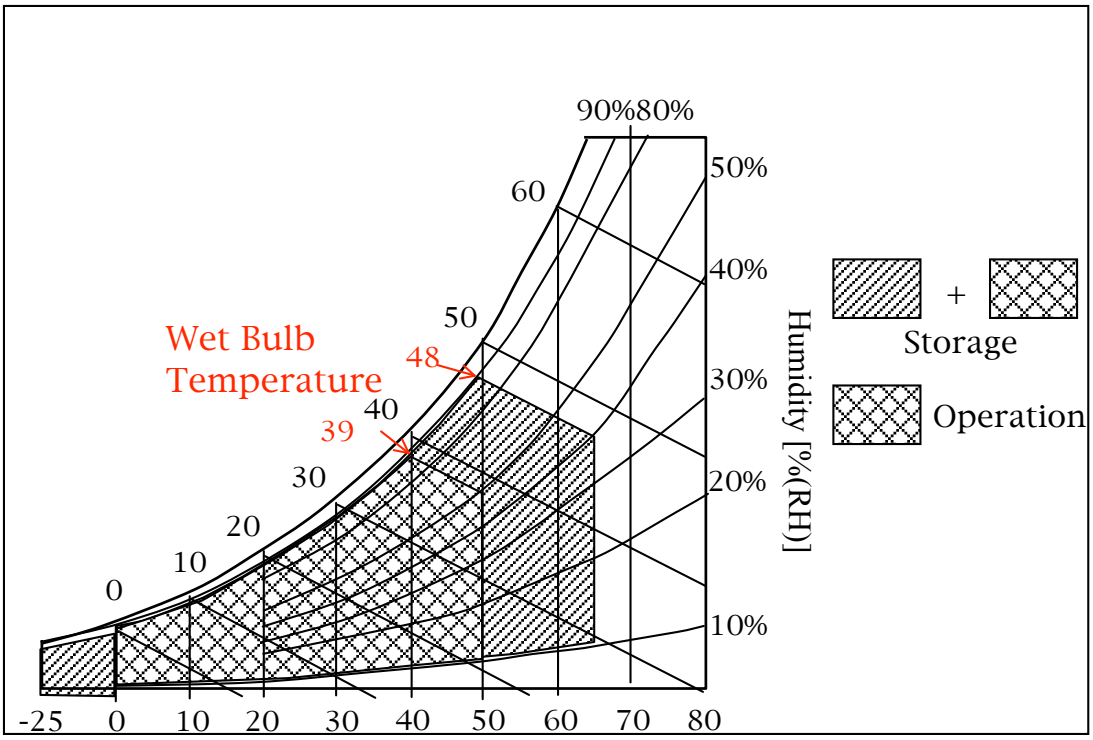


7.2. Temperature and Humidity

Unless otherwise stated in this specification, the display module must meet functional and cosmetic requirements after testing in accordance with Apple Spec. # 080-0859, non-operating and operating conditions.

For these tests, the following limits set forth in Specification #080-0859 shall be altered to read.

7.2.1. General Performance Requirements



Note:

1) Maximum wet bulb temp operating temperature is 39°C.

2) Maximum wet bulb temp storage temperature is 48°C.

7.2.2. Non-operational Testing

7.2.2.1. Low Temperature

-25°C @ 500 hrs

7.2.2.2. High Temperature

65°C @ 500 hrs

7.2.2.3. High Temperature and High Humidity

60°C @ 500 hrs, R.H. = 75% ± 10%

7.2.2.4. Thermal Shock

Cycle display from -25°C to 65°C with 5-minute transfer time,

100 cycles at -25°C/65°C/-25°C.

7.2.3. Operational Testing

7.2.3.1. Low Temperature

0°C for 500 hours

7.2.3.2. High Temperature

50°C for 500 hours

7.2.3.3. High Temperature and High Humidity

50°C and 90% R.H. for 240 hours (Functional Check)
Maximum wet-bulb temperature at 39°C or lower without condensation.

7.2.3.4. Four Corner Test (72 hrs – operating)

40°C @ 10% RH
40°C @ 90% RH

10°C @10% RH

10°C @ 90% RH

7.3. Altitude

72 hour storage	
Operational:	15,000 Ft.
Non-Operational:	40,000 Ft.

8. RELIABILITY

8.1. Resistance to Normal Abuse

8.1.1. Torsion Test

Module is fixed by 4 mounting holes (A, B, & C) on stable supports. Tester is connected to mounting hole on free floating module corner. Push/Pull test is conducted on all four corners.

8.1.2. Test Conditions:

Applied Force	20 N
Cycles	10 K
Frequency (F=push / pull)	1 Hz (1 cycle / sec.)

8.1.3. Test Set-up

8.1.4. Static Load Deflection and Breakage

Supplier shall demonstrate compliance per Apple Specification 062-2208 Static Breakage Test

8.2. Electrostatic Discharge (ESD)

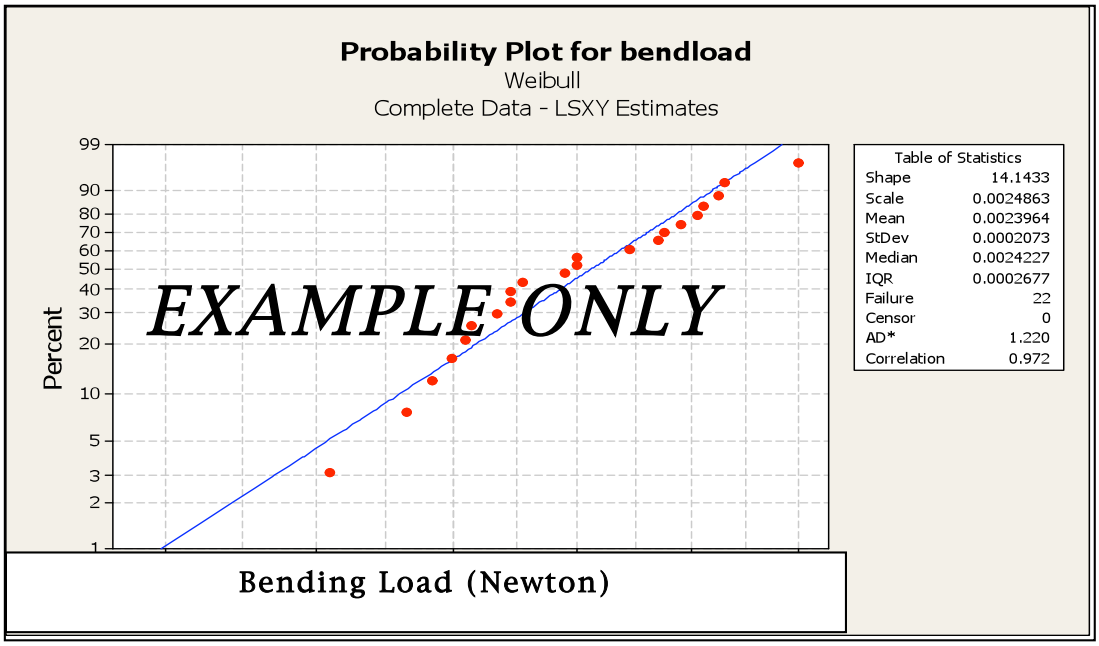
Display modules are to be tested for ESD susceptibility per Apple specification 062-0302. The display modules must meet the Level 1 for the bare module, and Level 1 through III test requirements stated in the above referenced specification, when assembled in a portable computer.

8.3. MTBF

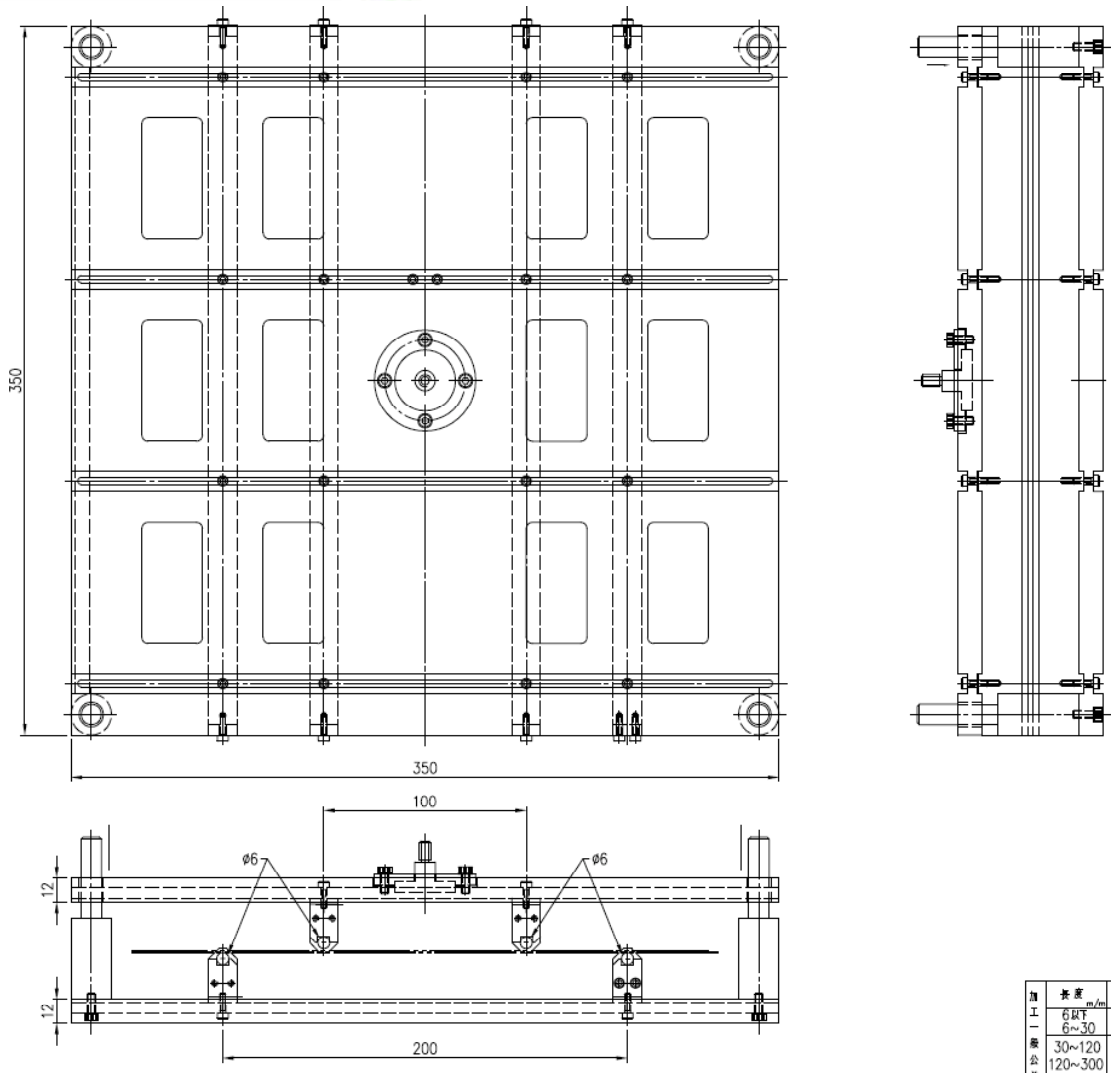
Supplier to demonstrate display module meets minimum 50,000 Hrs.@90% Confidence Supplier to include any acceleration factors included in the calculations. Power cycling frequency during this test is to be approved by Apple.

8.4.LCD Glass Strength

The LCD glass strength (failure load) will be defined at a single 90% survival rate value on Weibull distribution. Please provide the optimized loading performance in the similar chart format below. The failure load of the 90% Weibull survival rate shall be higher than TBD N.

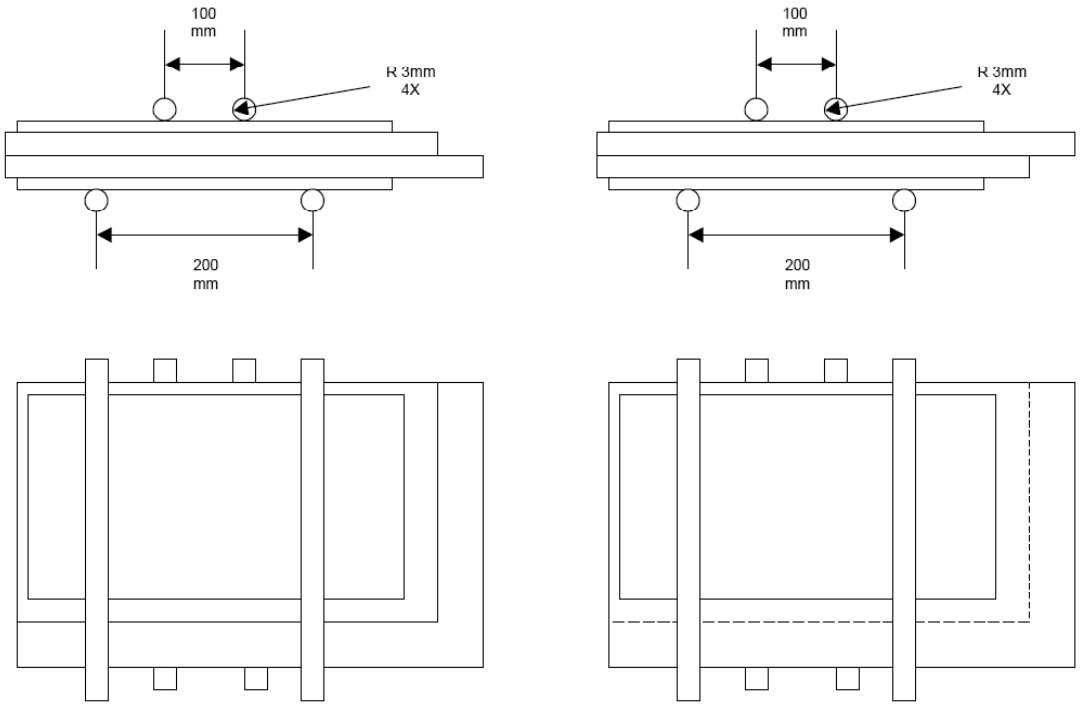


The 4 point bend test shall be used for the LCD glass strength test. The detailed fixture design/ shall follow the **ASTM standard C158-02**. The fixture is used in conduction with a load-displacement machine, commonly known as Instron.



Two orientations must be tested for this specification: orientation A (Figure 2.A) and orientation B (Figure 2.B)

This test shall be performed on 30 samples, **WITH current POLARIZERS** laminated on both top and bottom of the LCD glass, per applicable orientation as a First Article Inspection and when settings, tooling, and equipment are modified. Supplier is responsible for monitoring glass strength on an ongoing production basis. The test shall be conducted with a top rollers velocity of 1 mm/min. As soon as the first plane breaks, the test shall be stopped to prevent the second plane from breaking.



Orientation A. Longer plane parallel to ledge

Orientation B. Shorter plane parallel to ledge

Figure 2. Display orientations measuring strength at edges

LCD glass strength data collection

Failure initiation site must be determined by visual inspection by selecting one of the different cases shown below (Figure 3).

Case A) If the failure is starting from the bottom edge or close to it, enter letter A.

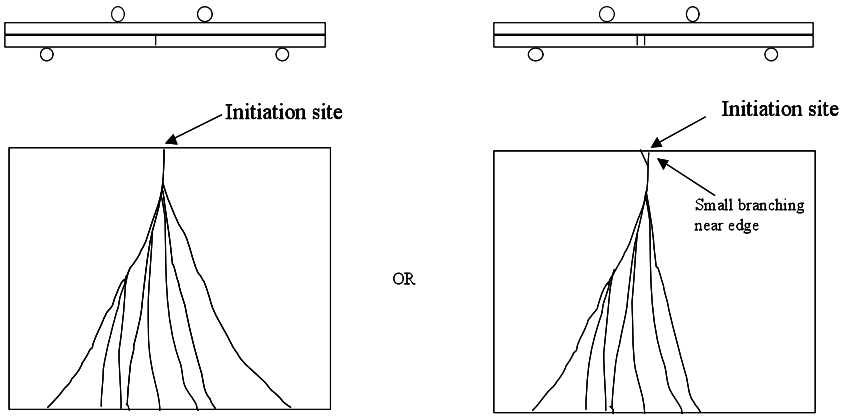
Case B) If the failure is starting from the top edge or close it, enter letter B.

Case C) If the failure is starting from the surface of glass, away from the edges and showing branching in both directions, enter letter C.

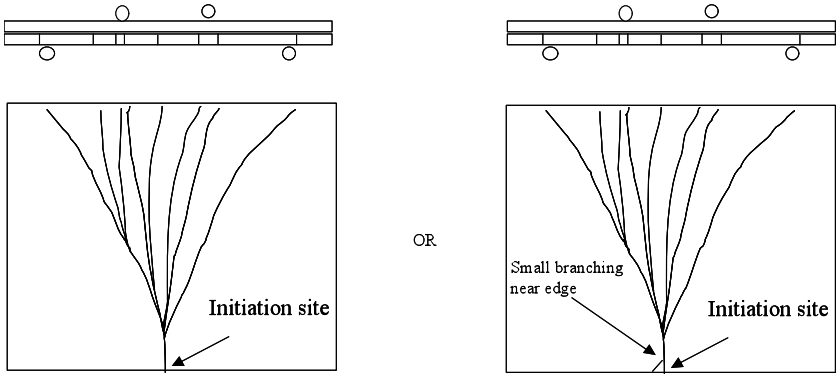
Case D) When testing in orientation D (Figure 1.D), if the failure is starting at the epoxy region between the panes, enter letter C edges of the glass (case D).

Case E) If during testing a snap is heard, but no crack is visible, enter letter E

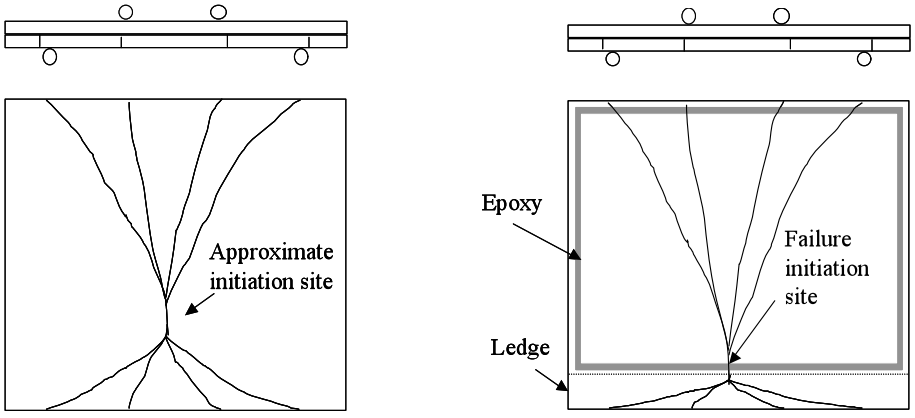
Case O) If the failure does not match any of the above or cannot be easily recognized due to catastrophic breakage, enter letter O.



Case A. Failure from bottom edge (with or without slight branching near edge)



Case B. Failure from top edge (with or without slight branching near edge)



Case C. Initiation on surface of glass

Case D. Failure at surface on epoxy region (Orientation D)

Figure 3 Surface crack initiation.

All failure loads and failure initiation sites will be entered in the following table below.

Orientation a b c d	(Circle one)	
W [mm] =	Llong [mm] =	
Lshort [mm] =	t [mm] =	
a [mm] =		

Unit #	Failure Load [N]	Failure Initiation Site Case (A, B, C, D, E, or O)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		

8.5.Itemized On-going Reliability Test Requirements

8.5.1. Environmental Test

The following environmental tests are required during the period of production of notebook color TFT displays.

Item	Test Conditions	Inspection Instruction	Sample Qty	Test Frequency
Vib.	3Grms, 5~150Hz, 0.37 Oct/min sine wave, 30Min/ axis	Check for functional failures (Electrical failures or drastically cosmetic degradation that can be considered functional)	3	Every Month
Shock	200G, half sine 2ms, 6sides	same as above	3	Every Month
Non-operating, Low Temperature	-25℃, 500Hr	same as above	3	Every Month
Non-operating, High Temperature	65℃,500Hr	same as above	3	Every Month
Non-operating, High temp. High humidity	60℃, 75±10% RH, 500Hr	same as above	3	Every Month
Heat Soak with module mounted in the fixture with cover glass or system clamshell	65C/90% RH for 72 hours	same as above	3	Every Week
Non-operating, Thermal shock	-25 ℃ ~ 65 ℃(5min transfer time), 100cycle	same as above	3	Every Week
Operating, Low Temperature	0℃, 500Hr	same as above	3	Every Month
Operating, High Temperature	50℃, 500Hr	same as above	3	Every Month
Operating, High temp. High humidity	50℃, 90%RH, 240Hr	same as above	3	Every Month
ESD susceptibility	Appe 062-0302, meet level 1	Check for electrical failures. Check EDID.	3	Every Month
Backpack (data collection)	Per Apple spec (TBA)		3	Every Month
Operating, Four Corner	40℃@10%RH, 40℃@90%RH, 10℃@10%RH, 10℃@90%RH, 72Hr	Check for functional failures (Electrical failures or drastically cosmetic degradation that can be	2 for each corner	Every Month

		considered functional)		

8.5.2. Component FAI Measurement

The following mechanical tests are required during the period of production of notebook color TFT displays.

Item	Test Conditions	Inspection Instruction	Sample Qty	Test Frequency
FAI	25edgC	All FAI items	3 per config	Every Month

8.5.3. Optical Test

The following optical tests are required during the period of production of notebook color TFT displays.

Item	Test Conditions	Inspection Instruction	Sample Qty	Test Frequency
White, Red, Green, Blue Color	10min warm up. 20mA LED current. Measure in dark room at 90degree to display surface. Use CIE 1931 x,y diagram, 2degree observer.	Per module engineering spec	3	Every Week
Brightness	The same as above. Center only.	Per module engineering spec	3	Every Week
Contrast	The same as above. Center only.	Per module engineering spec	3	Every Week
Brightness Uniformity	160 points	Per module engineering spec	3	Every Week
Color Uniformity	160 points	Per module engineering spec	3	Every Week
Flicker	25degC. Use Apple specified flicker meter to check	Per module engineering spec	3	Every Week
Image Sticking	Short-term test followed by long-term test. Refer to Apple cosmetic spec 062-7003.	Per module engineering spec	3	Every 2 Weeks

8.5.4. Electrical Test

The following electrical tests are required during the period of production of notebook color TFT displays.

Item	Test Conditions	Inspection Instruction	Sample Qty	Test Frequency
Frequency Margin	Increase the display refresh rate from 60 Hz until display showing	Inform Apple if the frequency margin is	5	Every Month

	distorted image	less than 71Hz		
Near Field Scan	Spec 069 -2794		5	Every Month

9. COSMETIC REQUIREMENTS

The LCD module must meet Specification over the entire viewing

10. REGULATORY

10.1. Product Safety (Environmental, Ergonomics, Safety and Health)

Materials: The vendor is to provide Apple, upon request, specific chemical composition information or certifications necessary for the product to enter countries, markets, and/or for component(s) material identification, or for Apple to respond to customer requests for information. The information may be in the form of, but is not limited to, Material Safety Data Sheets, material specification sheets, health hazard information, certifications, or other forms of documentation.

10.2. RoHS Compliance and other Substance Regulations

This product's components, parts, and packaging shall be manufactured or assembled based upon the following requirements.

10.2.1 The display module must comply with the European RoHS directive, 2002/95/EC and the Apple RoHS Compliance Specification, 069-1111. As evidence of such compliance, the supplier must provide Apple a declaration of conformity in accordance with Apple's RoHS Declaration of Conformity Procedure, 080-2153.

10.2.2 In addition to RoHS compliance, the display module and its manufacturing process shall comply with Apple's Regulated Substances Specification, 069-0135.

10.2.3 The vendor shall provide a written statement declaring the average and maximum amount of mercury in the display module.

10.3 Halogen Free

Flat panel display must be must be halogen-free in accordance with the Apple Halogen-Free Specification, 069-1857

10.3. Environmental Markings and Recycling

10.3.1 Flat panel display must be modular in design so that parts can be easily separated, without any special tools, for ease of proper recycling/disposal at the product's end-of-life.

10.3.2 Flat panel display plastic parts >25 grams must be marked according to ISO 11469 (except for the LGP (light guide panel) and optical films in the backlight).

10.4. Product Safety

Flat panel display assembly shall comply with Apple Specification, 069-0279, Product Safety Requirements for Component Flat Panel Display Assemblies.

10.5. Ergonomics

The flat panel display must comply with the ergonomic requirements of ISO 13406 parts 1 and 2. The vendor shall provide a written statement that the flat panel display, supplied to Apple, is certified to comply with ISO 13406, parts 1 and 2.

10.6. Electromagnetic Compatibility (EMC)

10.6 Emissions

The final product must meet Apple Class B Emission Standards for home electronic device when configured within a system per Apple Spec. #062-0718. The display supplier must provide all necessary support as required to meet this requirement. EMI measurements are taken at the worst-case contrast setting.

10.6.1 Susceptibility

Performance degradation due to external noise or RF will be considered as specified in #062-0718 for Class B products.

10.6.2 Spectrum Spreading Compatibility (SSC)

10.6.2.1 Emissions

The final product must be compatible with spectrum spreading conditions specified in 1.2.2 of this document. No failure or degradation in electronic functionality and optical performance is allowed with the spreading turned ON compared to that when it is turned OFF.

10.6.2.2 Conditions for Spectrum Spreading

Spreading %: 0% (min.), 0.75% (typical), and 1.5% (max.)
Spreading type: center or down

Modulation Rate: 40 to 80 kHz.

11 FACTORY/SERVICE REQUIREMENTS

11.1 SQBR

Factory requirements are outlined in Supplier Quality and Business Requirements,