LG.PHILIPS LCD

Display Specification for

15.4” Wide (1440x900) TFT-LCD

With LED Backlight

LG.PHILIPS LCD

Revision History

DATE	REV #	Section	CHANGE DESCRIPTION
12/11/2007	01	All	Initial Engineering Release
1/23/2008	01	5	All of section 5 updated
3/10/2008	01	5	Power consumption correction
4/1/2008	01	5	Connector diagram update
05/02/2008	02	5	LED and EDID update
05/16/2008	02	5	EVT Engineering Release (EDID Update and Add Module Aging Request)
08/18/08	02	5,6	Electrical and Optical Update

LG.PHILIPS LCD

Table of Content

LG.PHILIPS LCD

1. General Description

This document establishes the requirements for the display device for the M98 project.

Category	***Parameter***	***Specification***
General	Manufacturer	
	Mfg. P/N	LP154WP3-TLA2
	LCD TYPE	Normally-White, Transmissive TN TFT-LCD
	Diagonal	15.383" (390.74 cm)
	Pixel Format	1440 (RGB stripe, H) x 900 (V)
	Pixel Pitch	0.2301 (H)_0.2301(V)
	Color Depth	18-bits (6R, 6G, 6B), 262,144 colors
	Pooling requirement	Rigid Post Spacer with strong pooling resistance
	Packaging	Protective film on front polarizer. Displays packaged and air-tight sealed in anti-static bags.
Electrical	Interface	3.3V dual-channel LVDS
	Power Consumption	4.8 W @ Black (typical, the logic plus the backlight @18 mA)
Optical	Luminance	330 nits @18 mA (typical)
	White LED Backlight	6 strings, 10 LED per string. TG E1S66-YW1D7-08@2.2 cd typical brightness rank
	Hot Spots	No visible hot spot at any angle
	Viewing Direction	6:00 for worst dark inversion (PCB driver on the bottom)
	Contrast	800
	Glass	0.5 t As-free glass E-XG
	Top Polarizer	Glossy Surface, 3H Hard Coating, 1% Reflectance, WV-EA, LT4 AR coating or equivalent

	Bottom Polarizer	WV-EA, Thin APCF or equivalent
	LGP	Conventional PMMA LGP
	Diffuser Sheet	CH192N (bottom) and D134L (top)
	BEF Sheet	BEFII-G2-MR
	Reflector	UX225
Mechanical	Active Area	331.344 mm X 207.090 mm
	Minimum Viewing Area	332.344 mm X 209.090 mm
	Module Outline Size	342.85 mm X 220.84 mm
	Connector	IPEX 20347-140E-12
	Mating Connector	
	Weight	440 grams typical
Environmental	Operating Temperature	0°C ~ +50°C
	Storage Temperature	-25°C ~ +65°C

2. ORDER OF PRECEDENCE OF DOCUMENTATION AUTHORITY

In the case of any conflict in any specification related to these parts, this order of precedence of authority shall apply:

2.1. The Purchase Order

2.2. This Specification

2.3. Reference Documents

3. PHYSICAL DESCRIPTION

3.1. Display Mode

Normally White, Transmissive, Twisted Nematic Liquid Crystal Displays

3.2. Pixel Configuration

RGB Vertical Stripe

3.3. Pixel Pitch

0.2301 mm x 0.2301 mm

3.4. Resolution

1440 (RGB stripe, H) x 900 (V)

3.5. Aperture Ratio

Minimum > 50%

3.6. Optimum Viewing Cone

6 o'clock worst dark inversion direction (PCB on the bottom)

3.7. Interface & Driving Scheme

3.3V dual-channel LVDS interface, requiring Hsync and Vsync signals, along with DE (Data Enable) mode, 2-dot inversion

3.8. Front Surface Treatment

Low-reflection gloss surface, ~1% Reflectance, ≥3H hardness (Sumitomo LT4)

3.9 Environmental Requirements:

Any homogeneous component must meet Apple Halogen-Free Specification, 069-1857.

Display assembly shall not contain arsenic in the glass, in accordance with the Apple Regulated Substances Specification, 069-0135. Restrictions on arsenic are not applicable to semiconductor materials.

Display assembly shall not contain mercury, in accordance with the Apple Regulated Substances Specification, 069-0135.

4. MECHANICAL REQUIREMENTS

4.1. Dimensions and Tolerances

Refer to Apple MCO 069-2659, which include height, width, and thickness, mounting details, bulb location, cable length, and connectors. The LCD module outline is described in the following table.

Dimension	Min	Typ	Max	Unit
Horizontal (H)	342.55	342.85	343.15	mm
Vertical (V)	220.54	220.84	221.14	mm
Depth (D)	3.43	3.73	4.03	mm

4.2. Weight

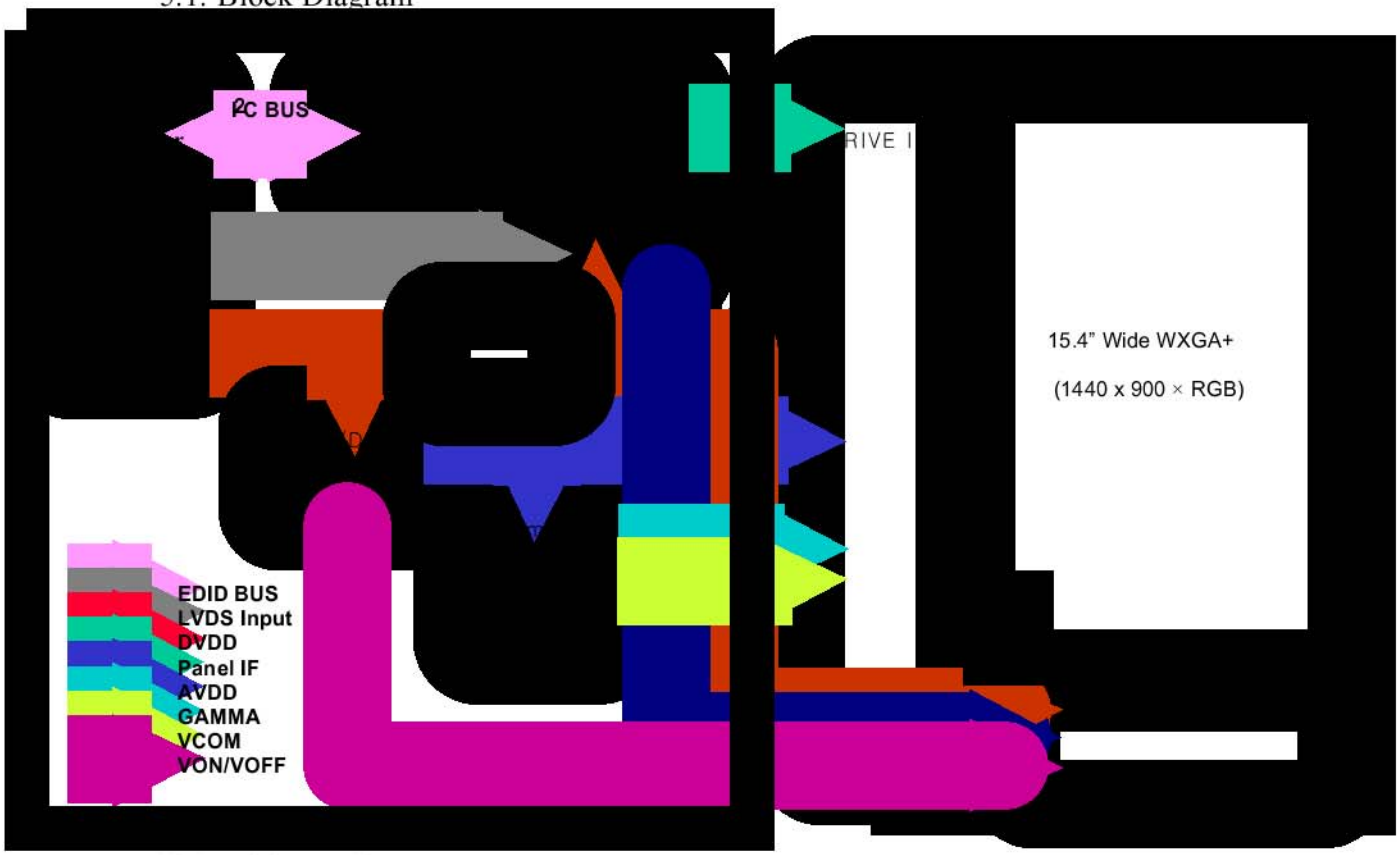
450 g (max), 440 g (typical)

4.3. Exposed Areas and Restrictions

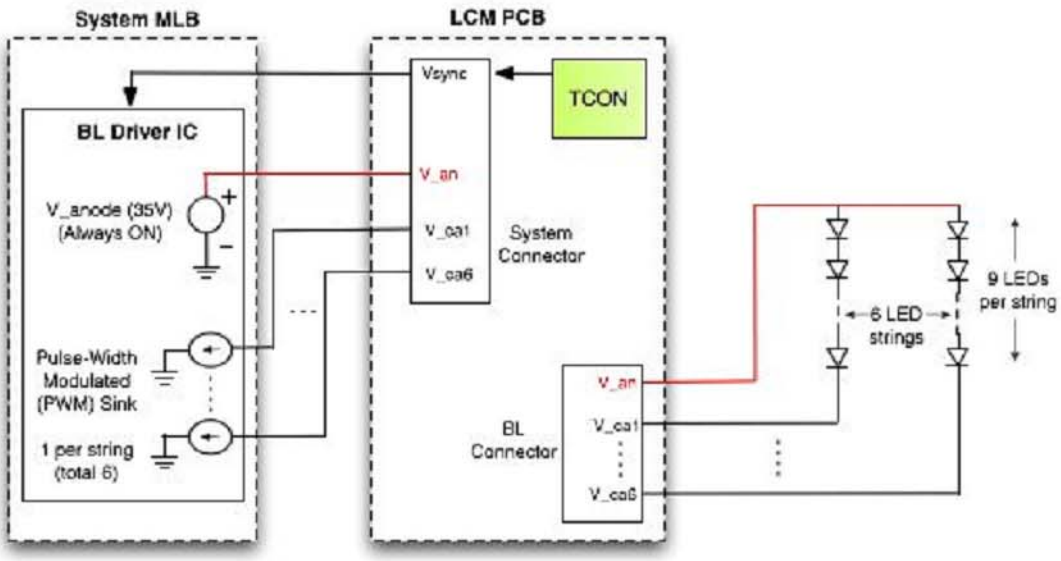
The display module shall not have exposed edges or components, which may cause injury or damage during handling, inspection, assembly, and service. Exposed areas of the display module (those not protected or shielded by construction) must be insulated and otherwise protected to eliminate the possibility of electrical shorting or destructive ESD discharges (per Section 7.2) during handling, inspection, assembly, and service. The Supplier shall identify all such areas prior to the Design Review and work with Apple Engineering to ensure the above criteria have been addressed.

5. ELECTRICAL REQUIREMENTS

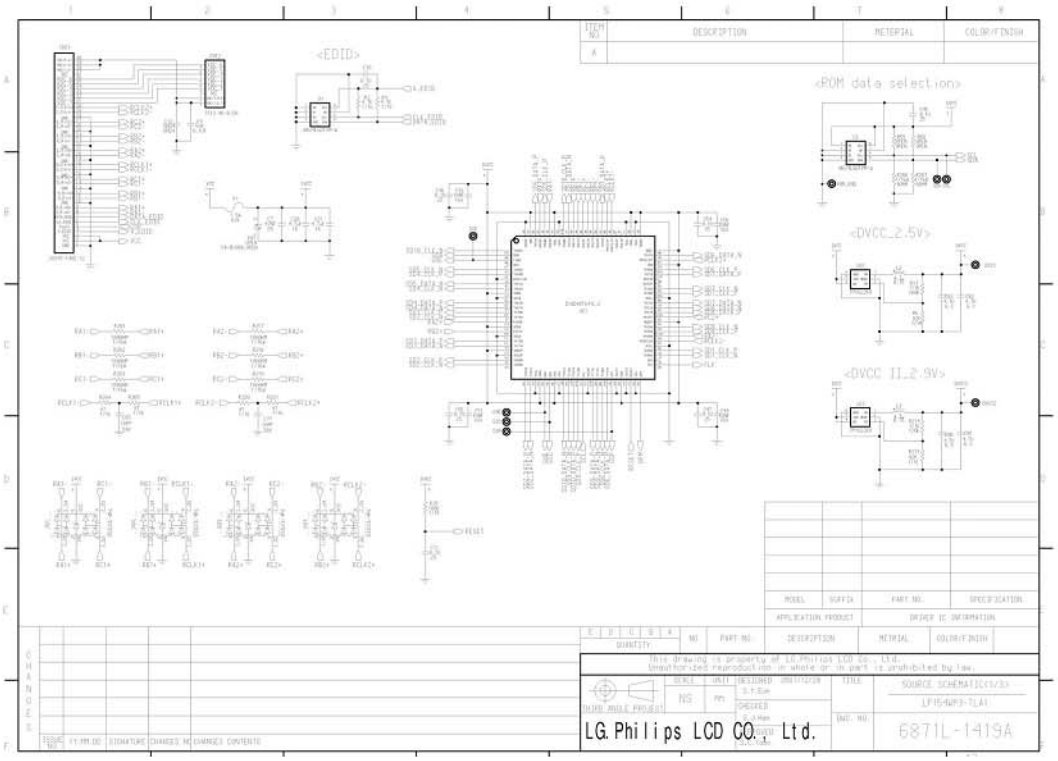
5.1. Block Diagram

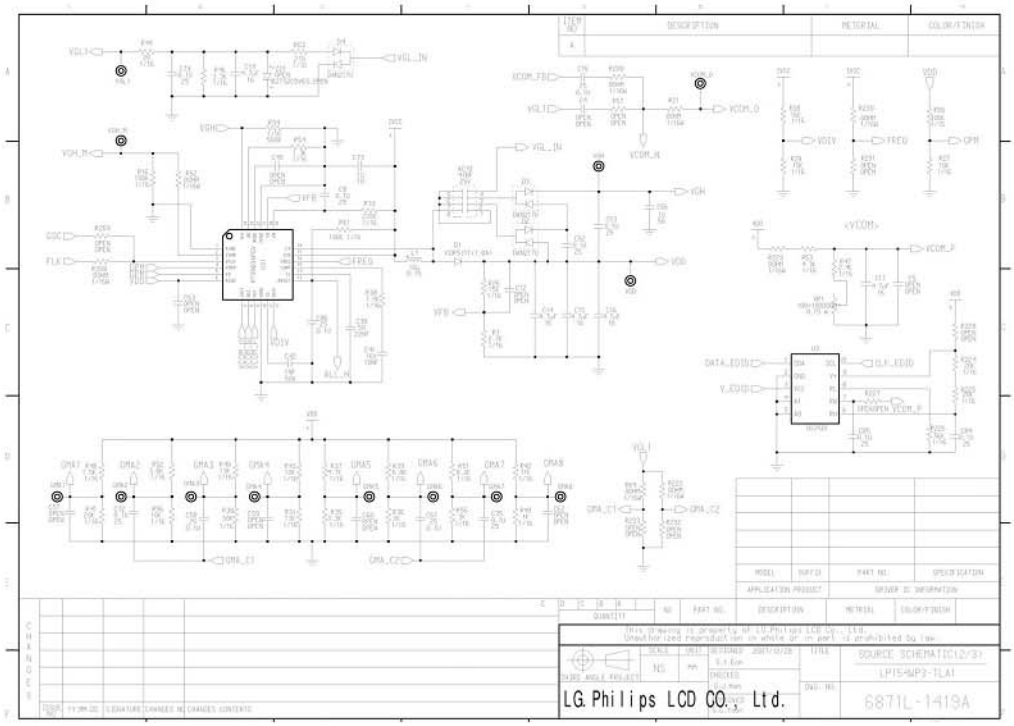


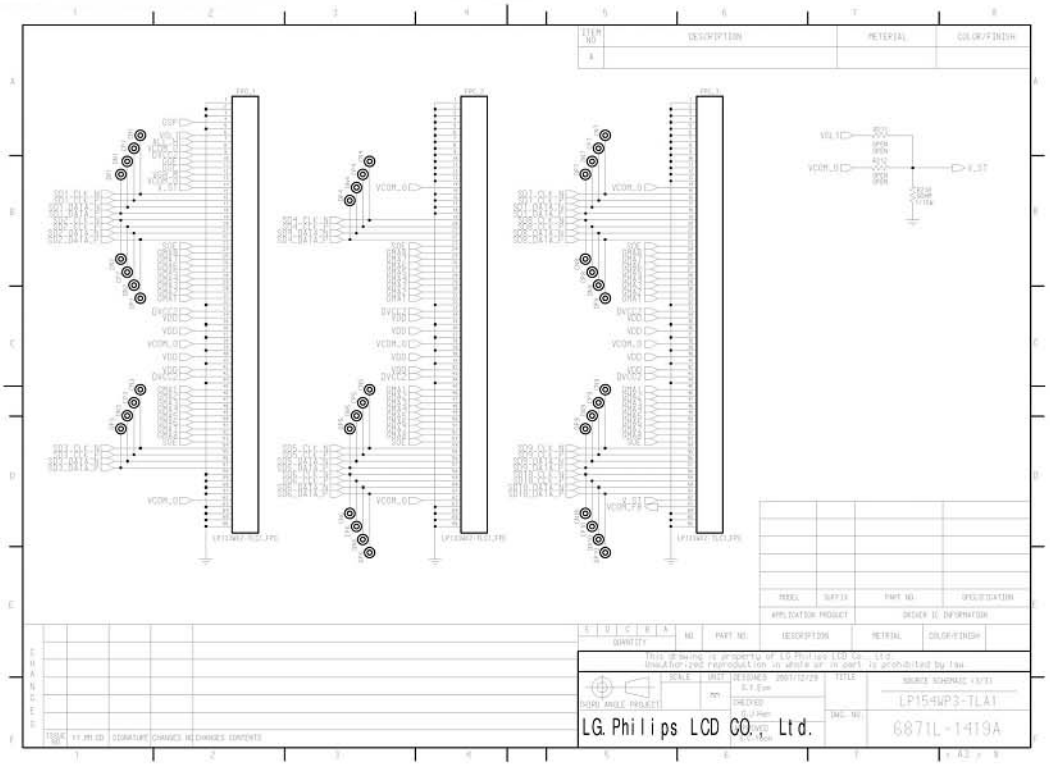
Backlight Driving Architecture



5.2. Display PCB Schematics



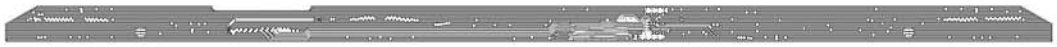




5.3. Display PCB Layout

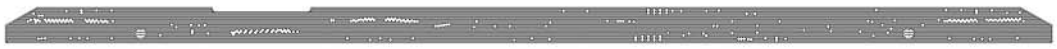
[Layer 1]

[Layer 2]



[Layer 3]

[Layer 4]



[Layer 5]

[Layer 6]

[Layer 7]

[Layer 8]

5.4. Display Subsystem (PCB & TFT Panel)

5.4.1. Pin-Out (Dual Channel LVDS Interface)

Connector: IPEX 20472-140E-12 or equivalent

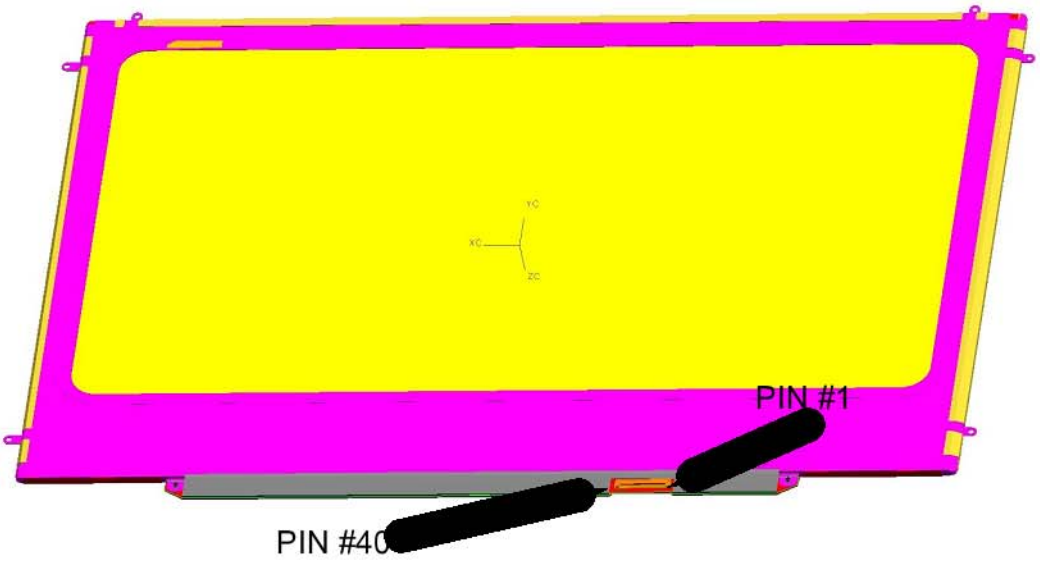
Matching Connector: IPEX 20472-040T-10 or equivalent (refer to MCO 069-2561)

Interface Chips: (need update according the latest Configuration Sheet), integrated LVDS and timing controller)

Pin	Symbol	Description	Micro-coax cable gauge (AWG)
1	GND	Ground	40
2	Vcc	Power Supply (+3.3V)	**32**
3	Vcc	Power Supply (+3.3V)	**32**
4	V_{EDID}	DDC 3.3V Power	40
5	Vsync	Vsync	40
6	Clk_{EDID}	DDC Clock	40
7	$DATA_{EDID}$	DDC Data	40
8	Odd_Rin0-	Odd Channel Differential Data Input	40
9	Odd_Rin0+	Odd Channel Differential Data Input	40
10	GND	Ground	40
11	Odd_Rin1-	Odd Channel Differential Data Input	40
12	Odd_Rin1+	Odd Channel Differential Data Input	40
13	GND	Ground	40
14	Odd_Rin2-	Odd Channel Differential Data Input	40
15	Odd_Rin2+	Odd Channel Differential Data Input	40
16	GND	Ground	40
17	Odd_Clkin-	Odd Channel Differential Clock Input	40
18	Odd_Clkin+	Odd Channel Differential Clock Input	40
19	GND	Ground	40
20	Even_Rin0-	Even Channel Differential Data Input	40
21	Even_Rin0+	Even Channel Differential Data Input	40
22	GND	Ground	40
23	Even_Rin1-	Even Channel Differential Data Input	40
24	Even_Rin1+	Even Channel Differential Data Input	40
25	GND	Ground	40
26	Even_Rin2-	Even Channel Differential Data Input	40

27	Even_Rin2+	Even Channel Differential Data Input	40
28	GND	Ground	40
29	Even_Clkin-	Even Channel Differential Clock Input	40
30	Even_Clkin+	Even Channel Differential Clock Input	40
31	Vdc1	LED Cathode (Negative)	40
32	Vdc2	LED Cathode (Negative)	40
33	Vdc3	LED Cathode (Negative)	40
34	Vdc4	LED Cathode (Negative)	40
35	Vdc5	LED Cathode (Negative)	40
36	Vdc6	LED Cathode (Negative)	40
37	NC	NC	40
38	Vdc(1 &2)	LED Anode (Positive)	40
39	Vdc(3&4)	LED Anode (Positive)	40
40	Vdc(5&6)	LED Anode (Positive)	40

5.4.2. Connector Diagram



5.4.3. Color Input Data Reference

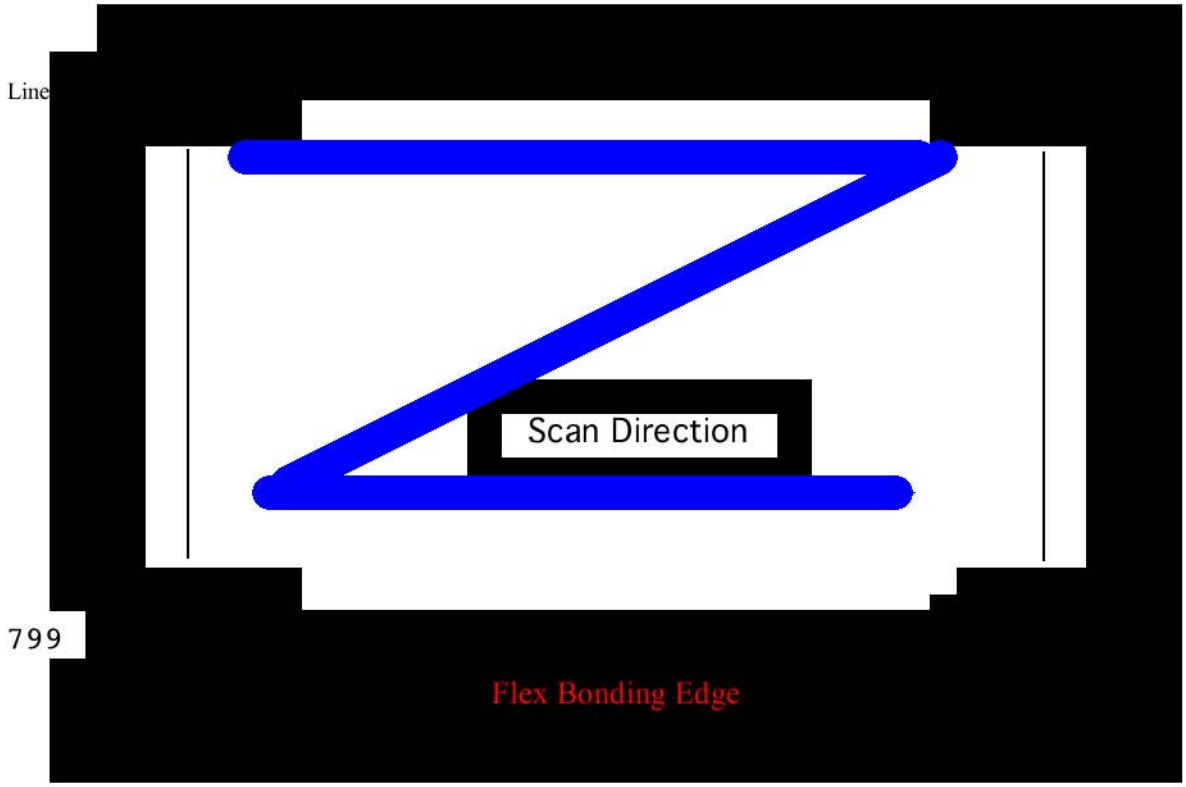
The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																	
		Red						Green						Blue					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(00) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63) Bright	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(00)Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0

	Green(63)Bright	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue(00) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63) Bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Pixel Format on the Display



5.4.4. EDID Interface (Per Vesa EDID 1.x standard requirements)

Byte (dec)	Byte (hex)	Field Name and Comments	Value (hex)
0	**00**	Header	**00**
1	**01**	Header	**FF**
2	**02**	Header	**FF**
3	**03**	Header	**FF**
4	**04**	Header	**FF**
5	**05**	Header	**FF**
6	**06**	Header	**FF**
7	**07**	Header	**00**
8	**08**	EISA manufacture code (3 Character ID) APP	**06**
9	**09**	EISA manufacture code (Compressed ASCI)	**10**
10	**0A**	Panel Supplier Reserved - Product Code 9C84h	**84**
11	**0B**	(Hex. LSB first)	**9C**
12	**0C**	LCD Module Serial No - Preferred but Optional ("0" If not used)	**00**
13	**0D**	LCD Module Serial No - Preferred but Optional ("0" If not used)	**00**
14	**0E**	LCD Module Serial No - Preferred but Optional ("0" If not used)	**00**
15	**0F**	LCD Module Serial No - Preferred but Optional ("0" If not used)	**00**
16	**10**	Week of Manufacture : 00 weeks	**00**
17	**11**	Year of Manufacture 2008 year	**12**
18	**12**	EDID structure version # = 1	**01**
19	**13**	EDID revision # = 3	**03**
20	**14**	Video input Definition = Digital signal	**80**
21	**15**	Max H image size (Rounded cm) = 33 cm	**21**
22	**16**	Max V image size (Rounded cm) = 21 cm	**15**
23	**17**	Display gamma = 2.2 Gamma	**78**
24	**18**	Feature Support (no_DPMS, no_Active Off/Very Low Power, RGB color display, Timing BLK 1,no_ GTF)	**0A**
25	**19**	Red/Green Low Bits (RxRy/GxGy)	**50**
26	**1A**	Blue/White Low Bits (BxBy/WxWy)	**C5**
27	**1B**	Red X Rx = 0.595	**98**
28	**1C**	Red Y Ry =0.345	**58**
29	**1D**	Green X Gx = 0.32	**52**
30	**1E**	Green Y Gy =0.555	**8E**
31	**1F**	Blue X Bx = 0.155	**27**

32	**20**	Blue Y By = 0.145	**25**
33	**21**	White X Wx =0.313	**50**
34	**22**	White Y Wy =0.329	**54**
35	**23**	Established timing 1 (00h if nt used)	**00**
36	**24**	Established timing 2 (00h if nt used)	**00**
37	**25**	Manufacturer's timings (00h if nt used)	**00**
38	**26**	Standard timing ID1 (01h if not used)	**01**
39	**27**	Standard timing ID1 (01h if not used)	**01**
40	**28**	Standard timing ID2 (01h if not used)	**01**
41	**29**	Standard timing ID2 (01h if not used)	**01**
42	**2A**	Standard timing ID3 (01h if not used)	**01**
43	**2B**	Standard timing ID3 (01h if not used)	**01**
44	**2C**	Standard timing ID4 (01h if not used)	**01**
45	**2D**	Standard timing ID4 (01h if not used)	**01**
46	**2E**	Standard timing ID5 (01h if not used)	**01**
47	**2F**	Standard timing ID5 (01h if not used)	**01**
48	**30**	Standard timing ID6 (01h if not used)	**01**
49	**31**	Standard timing ID6 (01h if not used)	**01**
50	**32**	Standard timing ID7 (01h if not used)	**01**
51	**33**	Standard timing ID7 (01h if not used)	**01**
52	**34**	Standard timing ID8 (01h if not used)	**01**
53	**35**	Standard timing ID8 (01h if not used)	**01**
54	**36**	Pixel Clock/10,000 (LSB) 88.75 MHz @ 60Hz	**AB**
55	**37**	Pixel Clock/10,000 (MSB)	**22**
56	**38**	Horizontal Active (lower 8 bits) 1440 Pixels	**A0**
57	**39**	Horizontal Blanking(Thp-HA) (lower 8 bits) 160 Pixels	**A0**
58	**3A**	Horizontal Active / Horizontal Blanking(Thp-HA) (upper 4:4bits)	**50**
59	**3B**	Vertical Active 900 Lines	**84**
60	**3C**	Vertical Blanking (Tvp-HA) (DE Blanking typ.for DE only panels) 26 Lines	**1A**
61	**3D**	Vertical Active : Vertical Blanking (Tvp-HA) (upper 4:4bits)	**30**
62	**3E**	Horizontal Sync. Offset (Thfp) 48 Pixels	**30**
63	**3F**	Horizontal Sync Pulse Width (HSPW) 32 Pixels	**20**
64	**40**	Vertical Sync Offset(Tvfp) : Sync Width (VSPW) 3 Lines : 3 Lines	**36**
65	**41**	Horizontal Vertical Sync Offset/Width (upper 2bits)	**00**
66	**42**	Horizontal Image Size (mm) 331 mm	**4B**
67	**43**	Vertical Image Size (mm) 207 mm	**CF**
68	**44**	Horizontal Image Size / Vertical Image Size	**10**
69	**45**	Horizontal Border = 0 (Zero for Notebook LCD)	**00**
70	**46**	Vertical Border = 0 (Zero for Notebook LCD)	**00**
71	**47**	Non-Interlace, Normal display, no stereo, Digital Separate	**18**

72	**48**	Flag		**00**
73	**49**	Flag		**00**
74	**4A**	Flag		**00**
75	**4B**	Data Type Tag (Descriptor Defined by manufacturer)		**01**
76	**4C**	Flag (Version)		**00**
77	**4D**	Descriptor Defined by manufacturer (Apple EDID signature) APP		**06**
78	**4E**	Descriptor Defined by manufacturer (Apple EDID signature)		**10**
79	**4F**	Descriptor Defined by manufacturer (Link Type)		**30**
80	**50**	Descriptor Defined by manufacturer (Pixel and link component format_6bit panel interface)		**00**
81	**51**	Descriptor Defined by manufacturer (Panel feature_Inverter NA, no Inverter)		**00**
82	**52**	Descriptor Defined by manufacturer		**00**
83	**53**	Descriptor Defined by manufacturer		**00**
84	**54**	Descriptor Defined by manufacturer		**00**
85	**55**	Descriptor Defined by manufacturer		**00**
86	**56**	Descriptor Defined by manufacturer		**00**
87	**57**	Descriptor Defined by manufacturer		**00**
88	**58**	Descriptor Defined by manufacturer		**0A**
89	**59**	Descriptor Defined by manufacturer		**20**
90	**5A**	Flag		**00**
91	**5B**	Flag		**00**
92	**5C**	Flag		**00**
93	**5D**	Data Type Tag (ASCII String)		**FE**
94	**5E**	Flag		**00**
95	**5F**	ASCII String	L	**4C**
96	**60**	ASCII String	P	**50**
97	**61**	ASCII String	1	**31**
98	**62**	ASCII String	5	**35**
99	**63**	ASCII String	4	**34**
100	**64**	ASCII String	W	**57**
101	**65**	ASCII String	P	**50**
102	**66**	ASCII String	3	**33**
103	**67**	ASCII String	-	**2D**
104	**68**	ASCII String	T	**54**
105	**69**	ASCII String	L	**4C**
106	**6A**	ASCII String	A	**41**
107	**6B**	ASCII String	1	**31**
108	**6C**	Flag		**00**
109	**6D**	Flag		**00**
110	**6E**	Flag		**00**

111	**6F**	Data Type Tag (ASCII String)		**FE**
112	**70**	Flag		**00**
113	**71**	ASCII String	C	**43**
114	**72**	ASCII String	o	**6F**
115	**73**	ASCII String	l	**6C**
116	**74**	ASCII String	o	**6F**
117	**75**	ASCII String	r	**72**
118	**76**	ASCII String		**20**
119	**77**	ASCII String	L	**4C**
120	**78**	ASCII String	C	**43**
121	**79**	ASCII String	D	**44**
122	**7A**	ASCII String		**0A**
123	**7B**	ASCII String		**20**
124	**7C**	ASCII String		**20**
125	**7D**	ASCII String		**20**
126	**7E**	Extension flag (# f optional 128 panel ID extension block to follow, Typ = 0)		**00**
127	**7F**	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)		**92**

5.4.5. Electrical Ratings

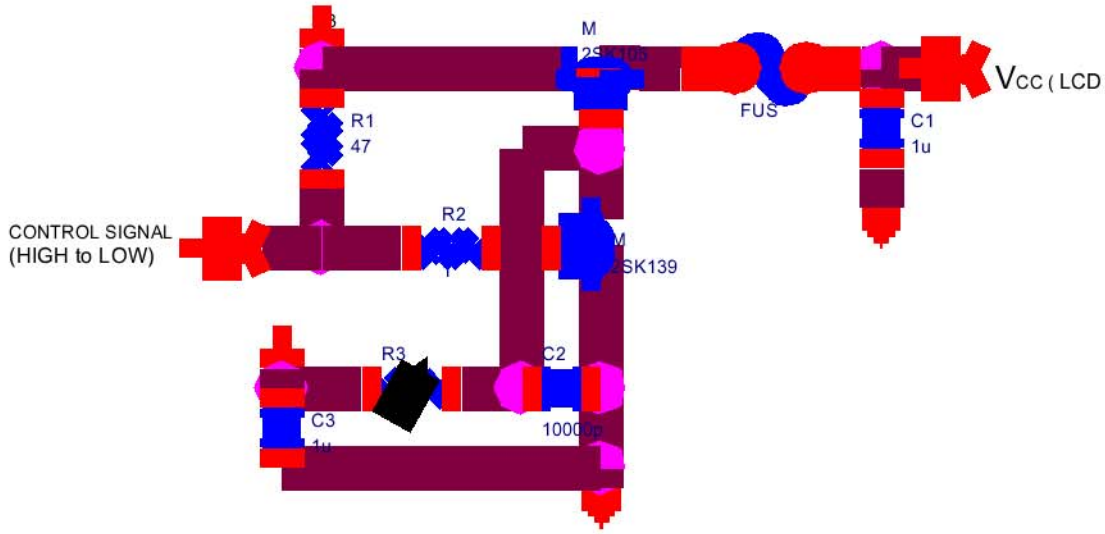
PARAMETER	SYMBOL	VALUES			UNIT	NOTES
		Min.	Typ.	Max.		
Power Supply Input Voltage	V_{CC}	3.0	3.3	3.6	V (DC)	
Power Supply Ripple			50		mV_{p-p}	1
Power Supply Input Current	I_{CC}	-	335	390	mA	2
Differential Impedance	Z_m	90	100	110	Ω	3
Power Consumption	P_c	-	1.1	1.2	W	2
Rush current	I_{RUSH}	-	-	1.5	A	4

Notes: (1) The power supply ripple is measured when a black pattern is displayed;

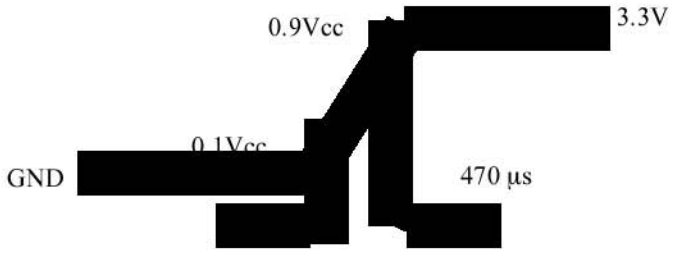
(2) The specified current and power consumption are under the conditions at Operation conditions: f_V = 60 Hz, f_{CLK} = 88.75 MHz, V_{cc} = 3.3 V, whereas a mosaic pattern (typical) is displayed;

(3) This impedance value is needed for proper functioning of the display, and is measured from LVDS mating connector to LVDS Rx

(4) The following is a typical Vcc circuit on the system side.



Vcc rise time is about 470 μs



The duration of the rush current is about 20 ms.

5.4.6. Signal Timing

5.4.6.1. Signal Impedance

Defined in VESA standard for LVDS FPDI 2

5.4.6.2. Timing Data

This is the signal timing required at the input of the control ASIC concerned with LVDS as a FlatLink or equivalent. All of the interface signal timing should be

satisfied with the following specifications based on the VESA timing guideline (1440x900 @ 60 Hz) for it's proper operation.

Video Timing Data

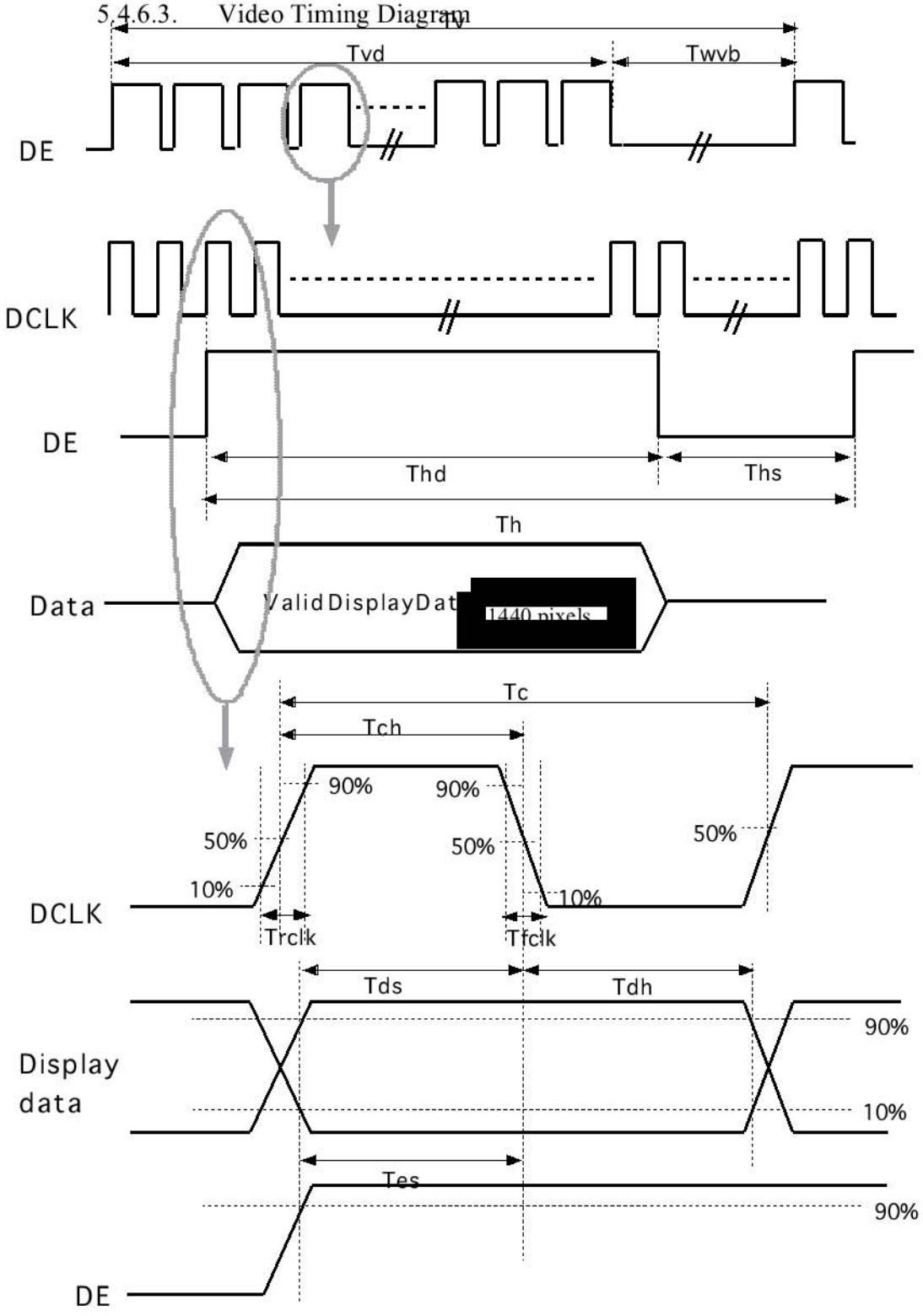
Signal	Parameter	Symbol	Min	Typ	Max	Unit	Note
D_{CLK}	Clock Period	T_C		11.27		ns	1
	Clock Frequency	f_C		88.75		MHz	$1/T_C$
	Duty Ratio (% High)	K_{dr}	40	50	60	%	T_{Ch}/T_C
	Rise Time	$T_{R\,CLK}$	-	4.42	-	ns	
	Fall Time	$T_{F\,CLK}$	-	4.42	-	ns	
DE	DE Setup Time	T_{se}	4	-	-	ns	
(Data Enable	Data Setup Time	T_{sd}	4	-	-	ns	
Only)	Data Hold Time	T_{hd}	2	-	-	ns	
(DTMG)	Horizontal Period	T_H		1600		T_C	2
Data	Horizontal Blank Period	T_{ha}		160		T_C	
	Vertical Period	T_V		926		T_H	f_V=59.90 Hz, 3
	Vertical Blank Period	T_{wvb}		26		T_H	
H_{sync}	H_{sync} Back Porch	H_{bp}	176	224		T_C	
	H_{sync} Pulse Width	T_{WH}	16	32		T_C	
	H_{sync} Front Porch	H_{fp}	16	64		T_C	
	Horizontal Active Period	T_{HD}	1440	1440	1440	T_C	Display Period
V_{sync}	V_{sync} Back Porch	V_{bp}	3	6		T_H	
	V_{sync} Pulse Width	T_{WV}	1	3		T_H	
	V_{sync} Front Porch	V_{fp}	1	3		T_H	
	Vertical Active Period	T_{VD}	900	900	900	T_H	Display Period

Note: (1) When the WXGA+ controller sets DE Mode, and H_{sync} and V_{sync} are required. The duration of DE (DTMG) signal must be longer than 1 clock period (T_C) at every horizontal sync period;

(2) Horizontal Period = One Line Scanning Time;

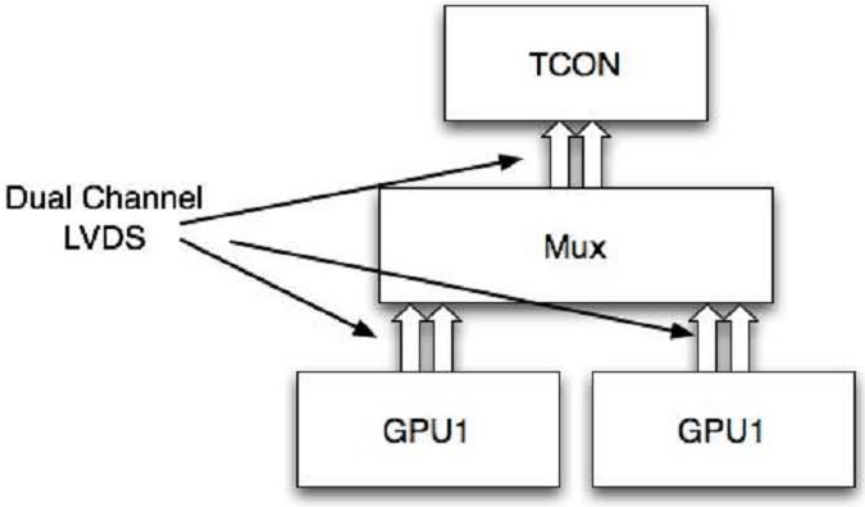
(3) The vertical period T_V is related to the frame frequency f_V, *i.e.*, 60 Hz.

5.4.6.3. Video Timing Diagram



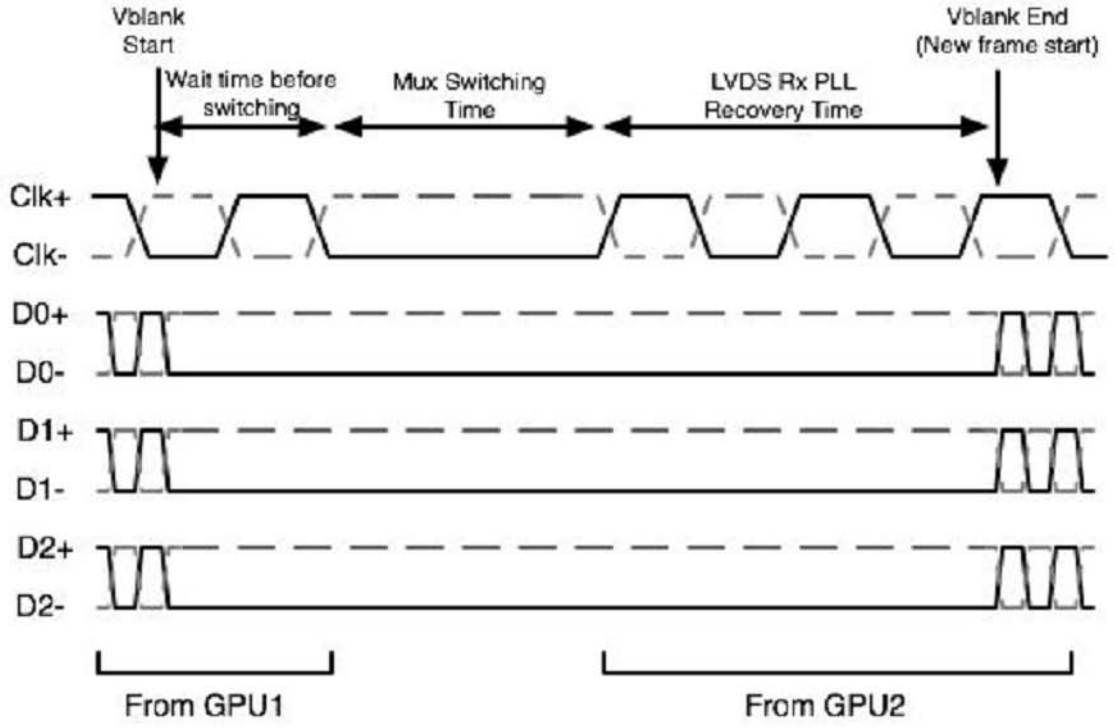
5.4.7. Apple Notebook Graphics Multiplexer Architecture

A part of Apple's notebook image pipeline architecture is shown in the following image. The LVDS outputs of two video sources are digitally multiplexed and then retransmitted to the internal LCD.



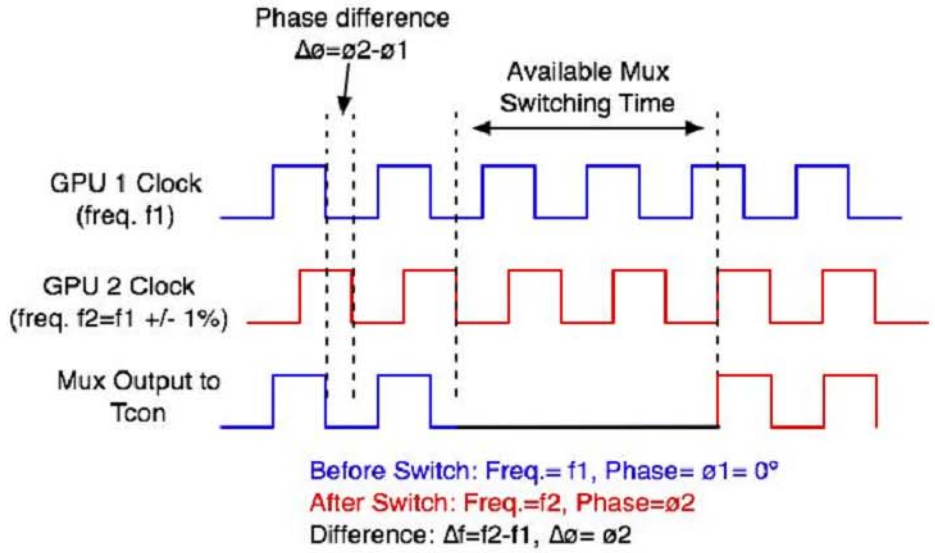
LVDS Mux Description

Since the mux is a digital buffer, the output waveform will not have any glitches or bouncing. However, there is a finite switching time required for the mux, during which time the outputs are held constant. The data is zeroed to ensure that a false DE, Vsync, or Hsync is not triggered, as shown in the following figure (NOT TO SCALE).



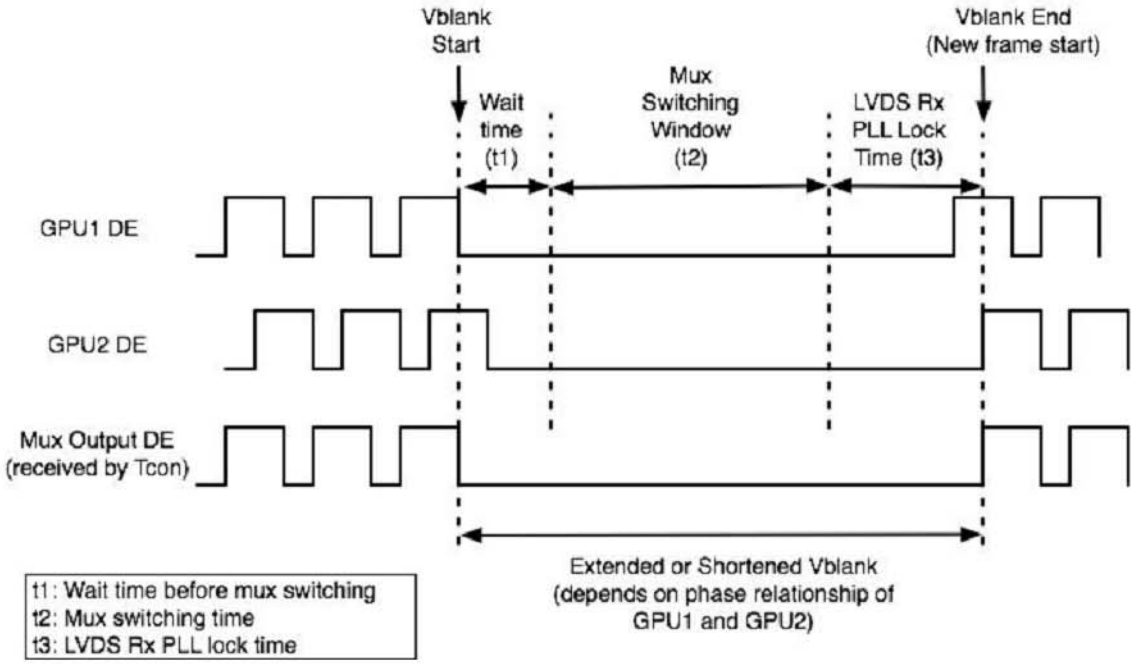
Apple would like to accomplish the switch of LVDS data streams seamlessly (i.e. without a visible impact to the LCD image). Therefore, the switching is done during the Vertical Blanking time.

The LVDS frequencies of GPU 1 and 2 intentionally differ by up to 1%, thereby causing the two waveforms to shift relative to each other. When the blanking periods are roughly aligned, the system will switch the mux. The following example shows switching from GPU 1 to GPU 2.



Apple Requirements

Scenario 1: PLL loses sync due to frequency and phase difference between GPU 1 and GPU 2



The TCON should accommodate Apple's requirement on timing restrictions and ensure that there is no visible 'glitch' on the LCD. This also requires that the failsafe feature in the Tcon should NOT turn on due to mux switching.

Scenario 2: PLL does NOT lose sync - frequency and phase difference between GPU 1 and GPU 2 are within PLL limits

In some cases, the phase difference between GPU 1 and GPU 2, Δø, and frequency difference Δf, may be small enough that the Tcon Rx PLL will not lose sync. Vendors need to specify the maximum values of Δø and Δf that will allow the PLL to stay synced.

Condition	Parameter	Apple Requirement		Vendor Response		Comments
		Min	Max	Min	Max	
PLL loses sync	t1	N/A	3 lines			Wait time after entering blanking before mux switches
	t2	4 LVDS clock cycles	N/A			Mux switching window
	t3	N/A	100 us			LVDS Rx PLL Lock time
	Failsafe start time after Rx detects lost clock	> t2+t3 (adjustable)	1 ms			Wait time before Tcon enters failsafe mode (has to be adjustable by registers)
	Vertical Blanking time	2 lines	1500 lines			Vendor to specify min and max Vblank (this dictates available time for mux switching)
PLL does NOT lose sync	Δf	N/A	N/A	N/A		Vendor to specify max Δf at which PLL remains locked
	Δø	N/A	N/A	N/A		Vendor to specify max phase difference Δø at which PLL remains locked

5.4.8. Power Measurements (W/O backlight)

Pattern	Min	Typ	Max	Unit
White		274	310	mA
Mosaic		333	360	mA
V. Stripe				mA
Black		399	420	mA

Note: (1) Display data pins and timing signal pins should be connected (GND = 0V);

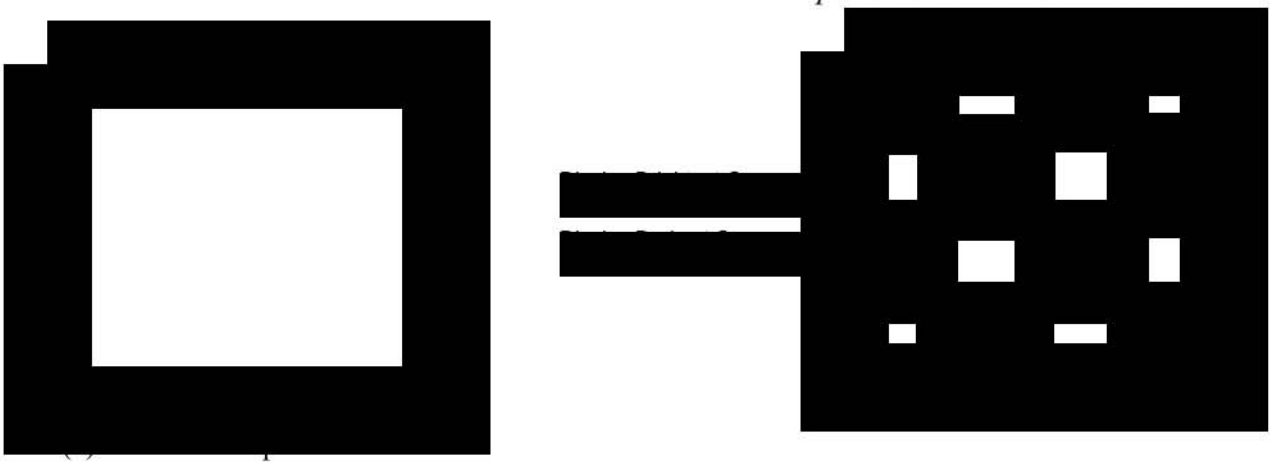
(2) Operation conditions: f_V = 60 Hz, f_{CLK} = 88.75 MHz, V_{cc} = 3.3 V;

(3) Power dissipation patterns are as follows.

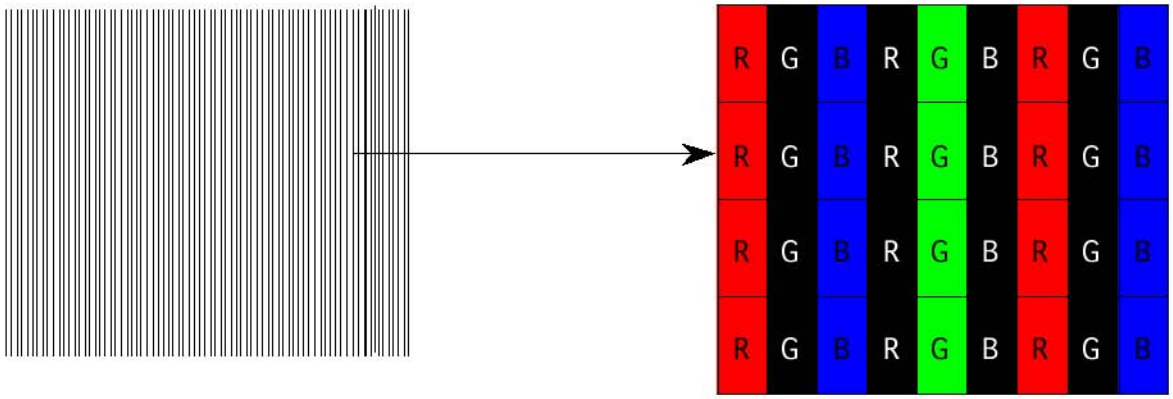
(a) White screen

(b) Mosaic (or checker) pattern

20x20 pixel black and white boxes

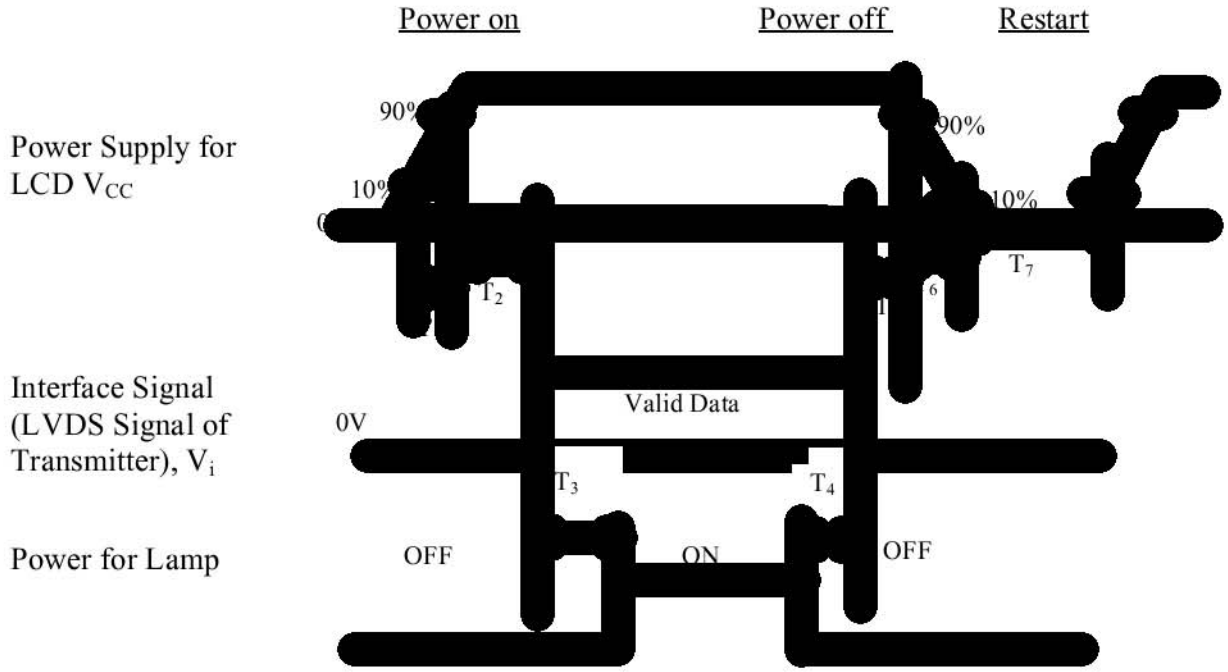


sub-pixel vertical line on/off alternation,



5.4.9. Power on-off sequence

Power-on includes both MacBook system starting from power-off state and wake from sleep state; power-off includes both MacBook system shutdown and entering sleep state



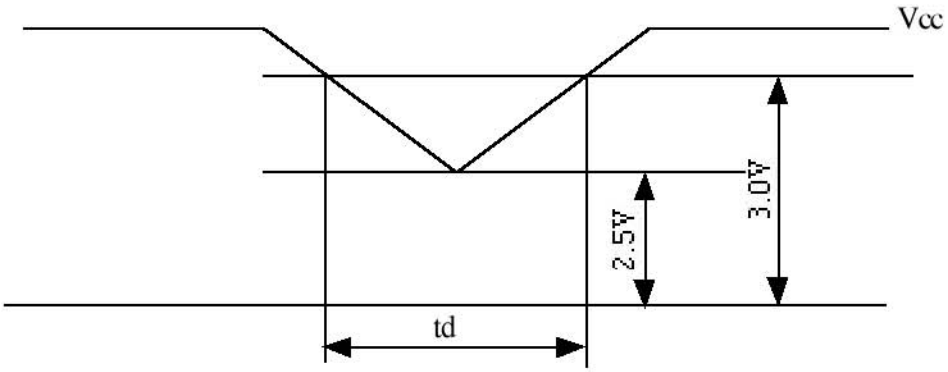
Parameter	Values			Unit
	Min.	Typ.	Max.	
T_1	0.15	-	10	ms
T_2	1	20	50	ms
T_3	200	250	-	ms
T_4	200	250	-	ms
T_5	0	20	50	ms
T_6	5	-	20	ms
T_7	500	-	-	ms

5.4.10. Vcc Dip Condition

The V_{cc} dip is the Vcc voltage drop during panel start-up.

(1) $2.5V \leq V_{cc} < 3.0$ V, $T_d \leq 20$ ms;

(2) For $V_{cc} < 2.5V$, V_{cc} should follow the power on-off sequence defined in 5.4.9.



5.5. Near-Field Noise

The RF emissions from the panel (especially the LVDS input and Tcon) interfere with Wifi operation. The panel vendor shall follow the noise characterization process outlined in Apple's near field noise spec (069-2794), and comply with noise emission limits.

Note that this spec compliance requirement is in addition to the legal EMI compliance requirements.

5.6. Backlight Subsystem

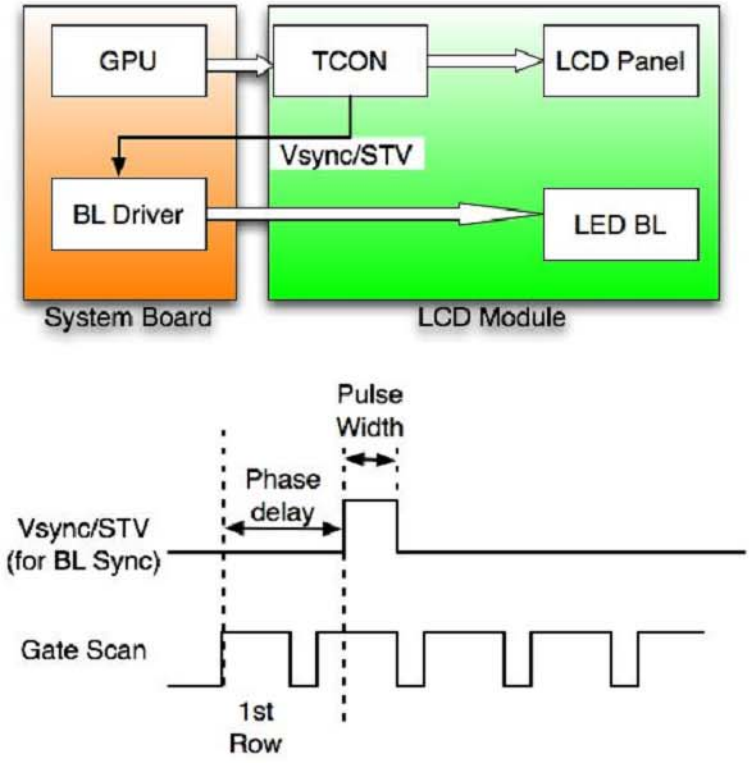
5.6.1. General Information

LED Manufacturer	TG
LED Manufacturer Assembly P/N	TG E1S66-YW1D7-08
Number of LEDs	60
LED Bin	LC,MC,NC (single bin), LB,LD,MB,MD,NB,ND (mixing bin)
LED Ranks	2,3,4,5,6

LED Brightness Bin	70 mcd per bin
LED Vf	Rank 1,2 (0.2 V per bin)
LED Forward Voltage Range for All 6 LED Series Lines	MAX: 34.0 V (Characterized at LVDS Connector for 20 mA)

LCD modules need to be aged for 2 hours minimum at 50 °C.

5.6.2. Backlight Synchronization Requirement (to avoid BL shimmering)



The Vsync/STV signal is a once-per-frame pulse that has a constant phase delay with respect to the start of the frame. This signal is used by the backlight LED driver to synchronize BL PWM with the frame update to avoid shimmering (waterfall) artifacts in the image.

The minimum pulse width is 1 us.

5.6.3. Backlight Electrical Characteristics

The backlight brightness test shall be tested at 600Hz PWM cycle & 20mA peak current with following percentage duty cycle

LED Current (% duty cycle)	LED Forward Voltage	Power (W)	Display Minimum Luminance (nits)	Display Typical Luminance (nits)	Display Maximum Luminance (nits)
100%	34.0 V	3.96	349	388	427
90%	34.0 V	3.56	300	330	363
18%	34.0 V	0.71	60	66	73
3%	34.0 V	0.12	10	11	12

5.6.4. LED Connection

String	LED1	LED2	LED3	LED4	LED5	LED6	LED7	LED8	LED9	LED10
1	1	7	13	19	25	31	37	43	49	55
2	2	8	14	20	26	32	38	44	50	56
3	3	9	15	21	27	33	39	45	51	57
4	4	10	16	22	28	34	40	46	52	58
5	5	11	17	23	29	35	41	47	53	59
6	6	12	18	24	30	36	42	48	54	60

6. OPTICAL REQUIREMENTS

6.1. Optical Specifications

Supplier must submit optical measurement data from 20 samples for items marked critical in Table 6.1.1. The optical performance will be approved by Apple based on supplier's measurement data, visual inspection of the samples, verification measurements, and specification correlation.

Table 6.1.1: Optical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Iso-Contrast Viewing Angle CR ≥ 10	θ	up	50	60	--	Degree	1,2,3
		down	70	80			
		left/right	70/70	80/80			
No Gray Inversion Angle	θ	up		25	--	Degree	1,2,3
	θ	down		30	--	Degree	1,2,3
		left/right		60/60			
Contrast ratio	CR	Optimal	600	800	--	--	1,2,3
Luminance	Lave	90% duty cycle at I_{LED}=20mA	300	330	--	cd/m^2	1,2,4
Global Luminance Uniformity		Optimal	65	75	--	%	1,2
Worst Neighbor Luminance Uniformity		Optimal	85		--	%	1,2
Gamma	γ	--	--	2.2	--	--	1,2,3
Flicker	F	No Visual Flicker	--	--	-30	dB	1,2,3
Cross Talk	D_{SHA}	Optimal	--		2.0	%	1,2,3
Worst Low Level (dark) Inversion Viewing Direction		PCB on the bottom	--	6:00	--	o'clock	1,2
Response (rise+fall time)	τ_{on+off}	θ = 0°, Ta=25°C	--	16	20	ms	1,2,3
Gray to Gray Response time	τ_{G2G}	θ = 0°, Ta=25°C	--		40	ms	1,2,3

White Chromaticity (all panels)	X	CIE 1931	0.297	0.313	0.329	--	1,2,3
	Y		0.313	0.329	0.345	--	1,2,3
White Chromaticity (Within one panel)	delta x				0.005		
	delta y				0.008		
Red Chromaticity	X	CIE 1931	0.575	0.595	0.615	--	1,2,3
	Y		0.325	0.345	0.365	--	1,2,3
Green Chromaticity	X	CIE 1931	0.300	0.320	0.340	--	1,2,3
	Y		0.535	0.555	0.575	--	1,2,3
Blue Chromaticity	X	CIE 1931	0.135	0.155	0.175	--	1,2,3
	Y		0.125	0.145	0.165	--	1,2,3
Max color difference within one panel	du'v'	white			0.0084		1,2
Max color difference w.r.t. Center within one panel	du'v'	white			0.007		1,2
Max color difference from panel to panel	du'v'	white			0.008		
Max color difference between neigbors	du'v'	white			0.0025		1,2

Note 1: The testing conditions are specified in 6.2.

Note 2: The definitions of optical characteristics are shown in 6.3.

Note 3: Measured at center point. Equivalent performance over the entire panel required.

Note 4: Both center point and average of 160 points.

6.2. Measuring Conditions

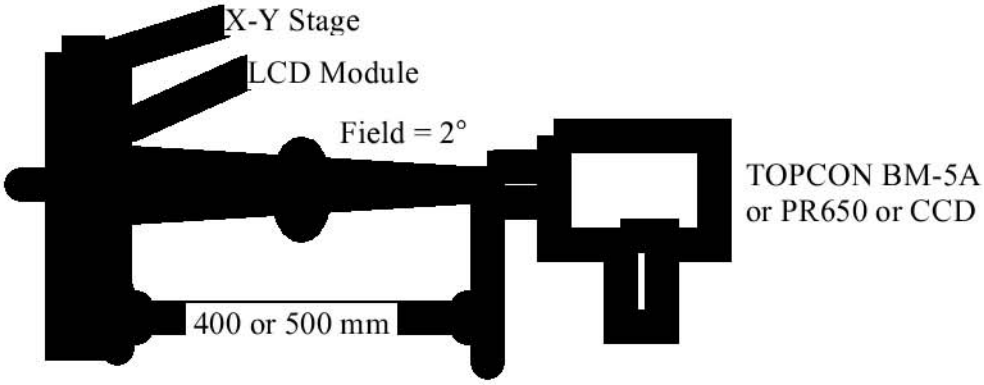
The optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes at the maximum brightness, in a dark environment at an ambient temperature at 25°C ± 2°C. The electrical conditions include V_{cc} = 3.3 V, f_v = 60 Hz, f_{CLK} = 88.75 MHz, I_{BL} = 20.0 mA @ 90% duty cycle with 600Hz. Recommended measuring equipments for luminance and color are CCD based imaging systems such as Radiant Imaging Prometric 1400 system, or Colorimeter such as Photo Research PR650, TOPCON BM-5A or similar. The measuring distance should be about

50 cm from the LCD surface at normal unless otherwise specified. Measurements should be done on the 160 grid points as shown in the following figures. The measurement spot at the center is approximately 12 mm in diameter from a distance of 400 mm by TOPCON BM-5A or 15 mm in diameter from a distance of 500 mm by PR 650.

Viewing angle measurements should be done by an Eldim EZ Color system or similar.

The CIE 1931 or 1976 Standards will be used.

Luminance and Color Measurement



Viewing Angle Measurement

Figure 6-1: Optical Measurement Set-up

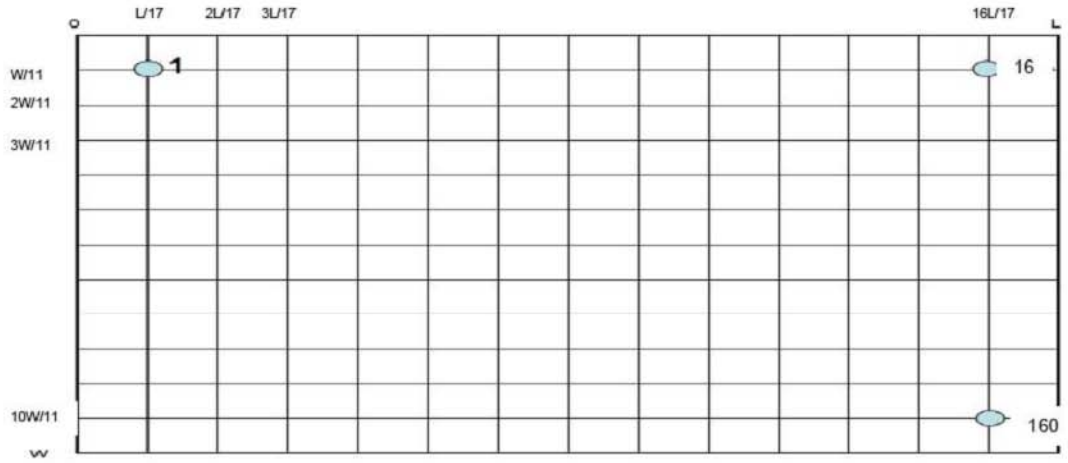


Figure 6-2: Measurement point location. L and W are the length and width of Active Area respectively.

6.3. Definition

6.3.1. Center Point Luminance

$L_{ct} = (L_{72} + L_{73} + L_{88} + L_{89})/4$ {Average Luminance value at point #72, 73, 88, 89}

6.3.2. Average Luminance

$L_{Ave} = SUM(L_1:L_{160}) / 160$

where L_1 to L_{160} are the luminance values measured at point #1 to #160.

6.3.3. Luminance Uniformity

The entire display active area shall be scanned with the luminance measurement with white screen set full brightness.

Apple requires two kinds of data for brightness uniformity: Luminance Uniformity, and Worst Neighbor Luminance Uniformity. The definitions are shown in below:

6.3.3.1. Global Luminance Uniformity:

$U = 100\% - (L_{max} - L_{min})/L_{max}$

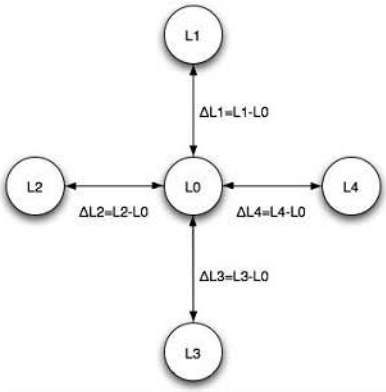
where, L_{max} = max {Luminance values at 160 points},

L_{min} = min {Luminance values at 160 points}

6.3.3.2. Worst Neighbor Luminance Uniformity (The 4 points that are closest to the test point)

WNU=100%-Max(ΔL1, ΔL2, ΔL3, ΔL4)/L0

Global WNU = min (WNU1, …WNU160)



6.3.4. Contrast Ratio

CR = Luminance at G_{max} / Luminance at G_{min} {Average contrast value at point #72, 73, 88, 89}

6.3.5. White Color Uniformity

The entire display active area shall be scanned with the color coordinate measurement with white screen set full brightness.

6.3.5.1. Panel to Panel White Color Uniformity

The center point (as defined by the average value at point #72, 73, 88, 89) white color coordinate of any panel shall be within the box with 4 corners coordination boundary listed in Table 6.1.

6.3.5.2. Max Color Difference with respect to the center within a panel

On each panel, the maximum color difference between any of the 160 points and the center point (defined as the average value at point #72, 73, 88, 89), represented in delta u'v'.

6.3.5.3. Max Color Difference between any two points within the panel

On each panel, the maximum color difference between any two of the 143 points , represented in delta u'v'.

6.3.5.4. Max Color Difference between two neighbors

On each panel, the maximum color difference between any two neighboring points on the panel, represented in delta u'v'

6.3.6. RGB Color Chromaticity

The entire display active area shall be scanned with the color coordinate measurement with screen set to full brightness and solid R, G, B color respectively. The measured color coordinate of any panel shall be within the box with 4 corners coordination boundary listed in Table 6.1.

6.3.7. Viewing Angle

The viewing angle is defined as the viewing angle range under the condition at CR $\geq$ 10:1 .

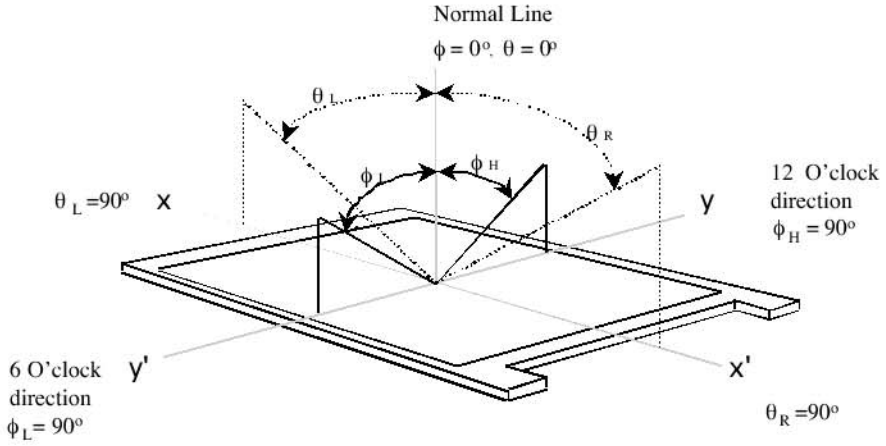


Figure 6-4: Viewing angle definition

6.3.8. Gray Scale Inversion

Luminance vs. viewing angle curves are measured based on gray level 255, 223, 191, 159, 127, 95, 63, 32 and 0, in the viewing angle of left, right, up, down, with PCB on the bottom side. Gray scale inversion happens when a higher gray scale measures the same luminance or lower luminance than any of the lower gray scale.

6.3.9. Response Time

6.3.9.1. On and Off Response Time

The On/Off response time, $t_R + t_F$, is defined in the following figure and shall be measured by switching the input signal for "black" and "white".

Figure 6-5: Response Time Measurement

6.3.9.2. Gray to Gray Response Time

Gray to Gray Response Time is measured in a similar method. But instead of switching display between black and white, panel is switched between two gray scales. The maximum gray-to-gray response time is based on 9 levels of gray scales. The 9 levels are: gray level 255, 223, 191, 159, 127, 95, 63, 32 and 0. Figure 6-6 shows an example of Gray to Gray Response Time measurement data.

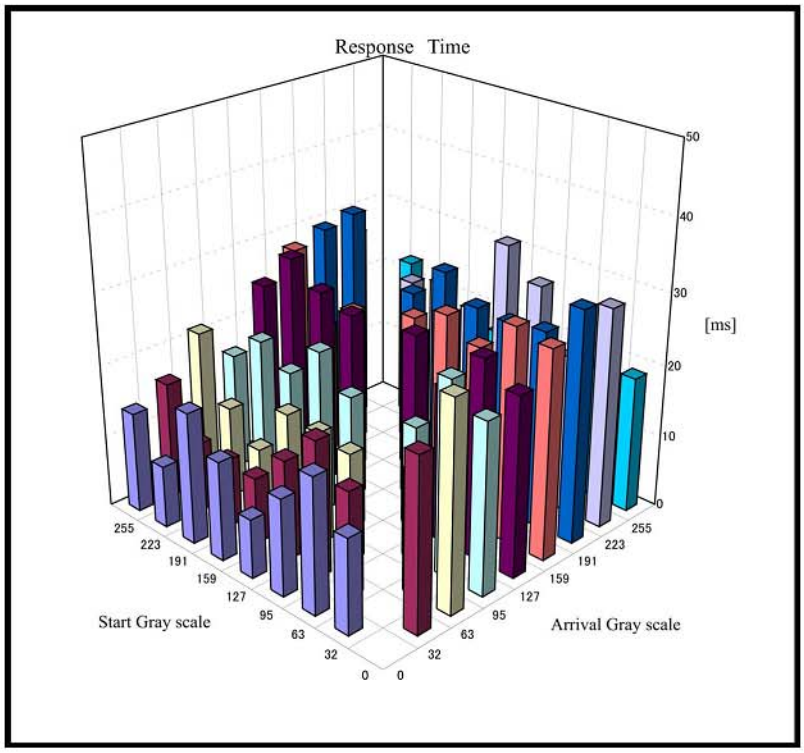


Figure 6-6: Gray to Gray Response Time

6.3.10. Gray Scale Linearity or Gamma Value

The display luminance, L_G, is measured at the different gray scales, G_{min}, …, G_{max}. The exponential fitting is used to determine the gamma (γ) value, which should be an intrinsic or uncorrected characteristic.

$$L_G \sim G^{\gamma}.$$

6.3.11. Flicker

No visual flicker will be allowed. The flicker level should be measured with either vertical stripes or a checker pattern, defined in Sec. 5.3.6. The output signal of a photometer is sent to an FFT analyzer. The flicker is essentially a ratio of the powers in the frequency spectrum at 30 Hz (P_x) and 0 Hz (P_0), *i.e.*,

$$F = 10 \text{ Log } (P_x / P_0).$$

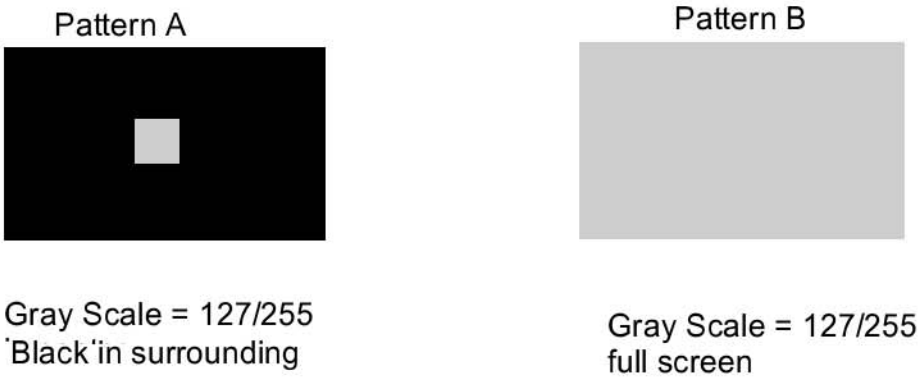
6.3.12. Cross-talk

No visual cross-talk will be allowed. Two luminance values are measured at center spot with 50 x 50 pixels. The cross-talk, D_{SHA}, is defined as,

$$D_{SHA} = (L_B - L_A)/L_B \bullet 100\%,$$

Where, L_A = Luminance in Pattern A

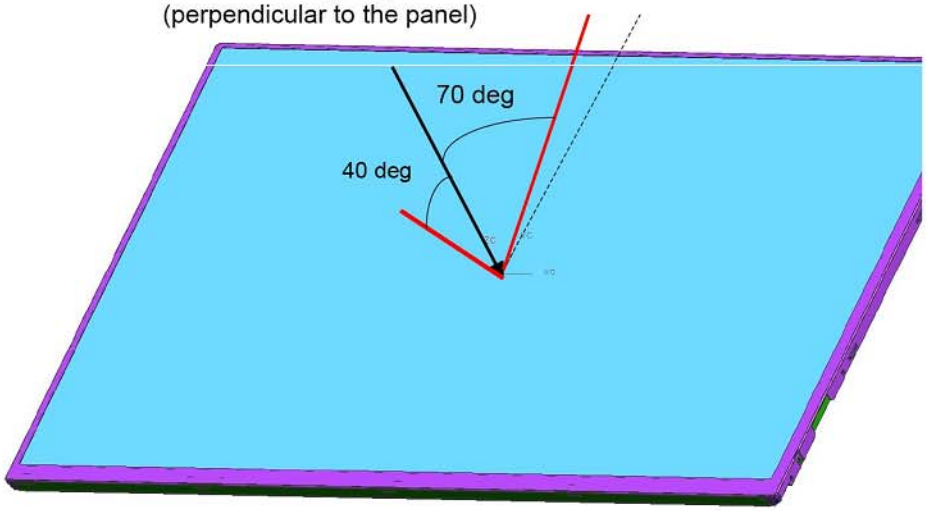
L_B = Luminance in Pattern B.



6.4. Hot Spot Specifications:

The LED hot spot shall be inspected from 70 degree to -40 degree per the drawing below. There shall be no visible hot spot or no worse than "limited sample" hot spot (if there is a "limited sample" set up.

Normal Viewing Angle
(perpendicular to the panel)



7. ENVIRONMENTAL

The display modules shall meet all functional and cosmetic specifications after testing to the environmental quality standards listed in this section. Additionally, the LCD modules in Apple's products shall pass all the system testing requirements listed in the end of this document.

7.1. Shock and Vibration

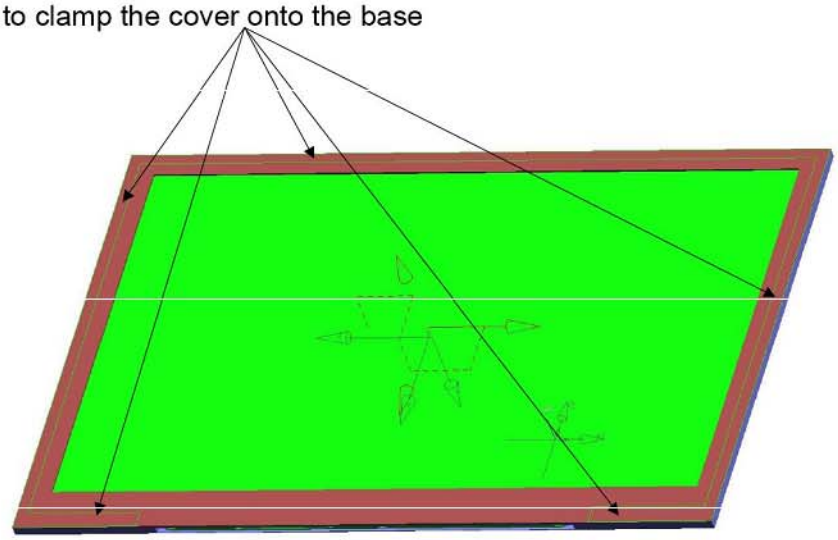
7.1.1 There will be no functional or cosmetic defects following a shock to all 6 sides delivering at least 200 G in a half sine pulse no longer than 2 ms to the display module, secured by its designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.

7.1.2 There will be no functional defects following a shock delivering at least 260 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays. The displays are secured by designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.

7.1.3 There will be no functional or cosmetic defects following a shock delivering at least 60 G in a pulse 11 msec or longer to the display module, secured by its designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.

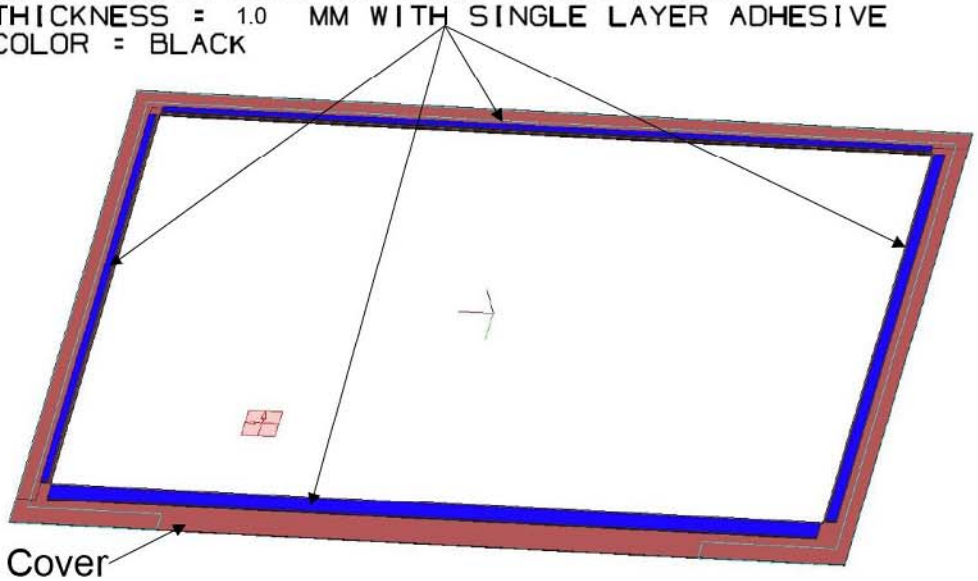
7.1.4 There shall be no functional or cosmetic defects following a vibration test, conducted at **3.0** G from 5–150 Hz, 0.37 Oct/min with sine wave for 30 min./axis, with the display secured by its designated mounting details, and conducted in accordance with MIL-STD-202F, method 201A.

Area to clamp the cover onto the base

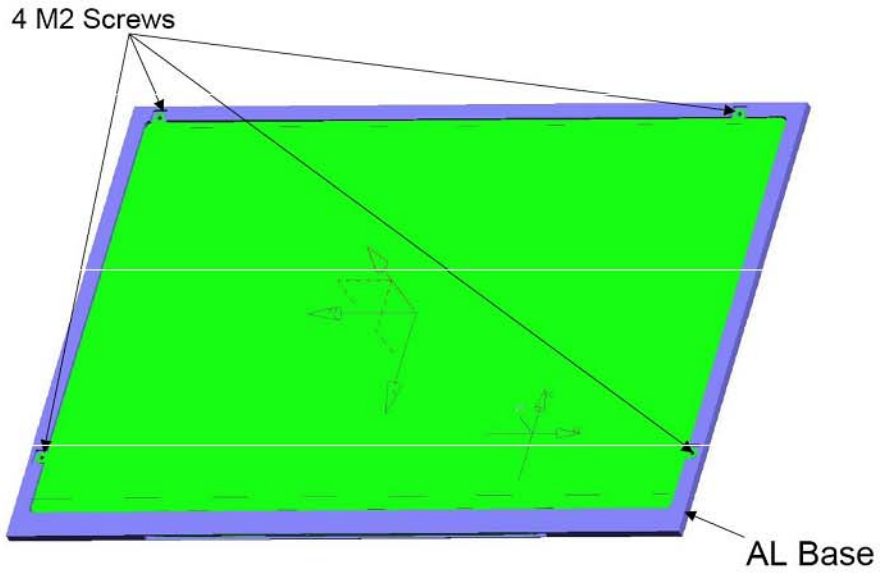


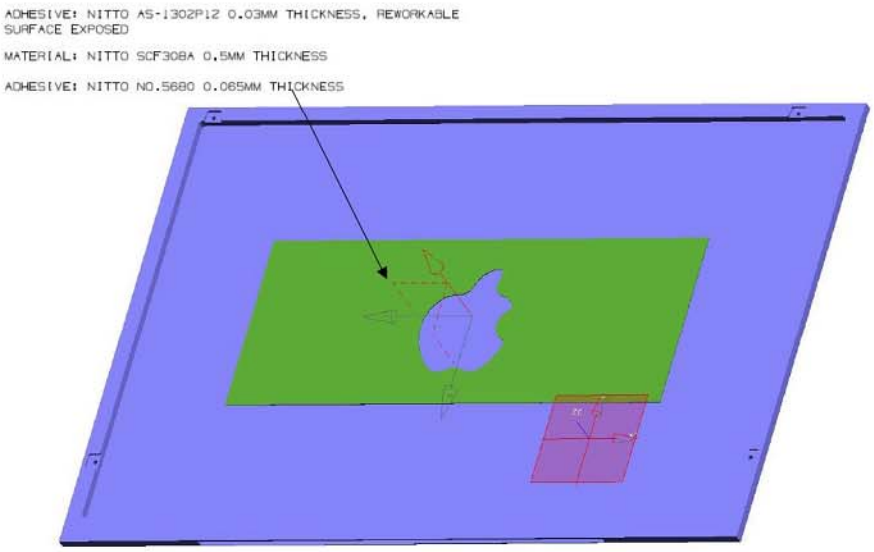
Poron Gaskets

MATERIAL: PORON S-RS 40P
COMPRESSIVE LOAD (AT 50%) = 2.2 N/CM^2
THICKNESS = 1.0 MM WITH SINGLE LAYER ADHESIVE
COLOR = BLACK



AL Cover



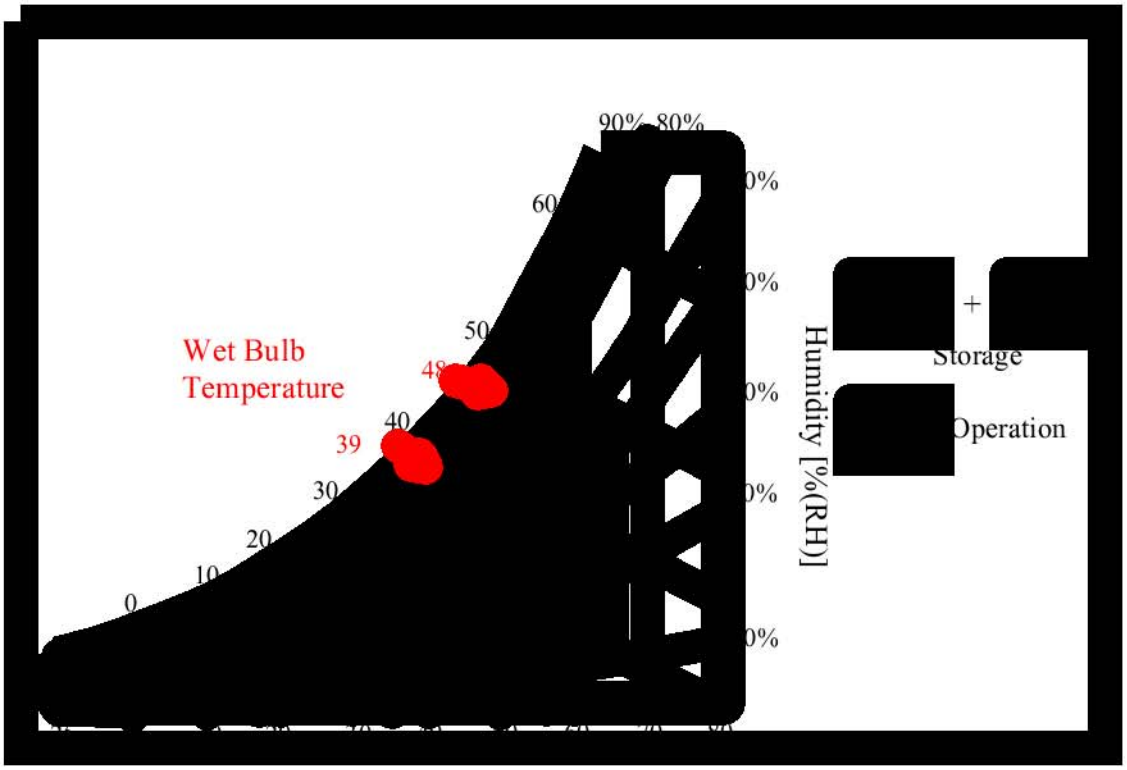


7.2. Temperature and Humidity

Unless otherwise stated in this specification, the display module must meet functional and cosmetic requirements after testing in accordance with Apple Spec. # 080-0859, non-operating and operating conditions.

For these tests, the following limits set forth in Specification #080-0859 shall be altered to read.

7.2.1. General Performance Requirements



Dry Bulb Temperature [˚C]

Note:

1) Maximum wet bulb temp operating temperature is 39°C.

2) Maximum wet bulb temp storage temperature is 48°C.

7.2.2. Non-operational Testing

7.2.2.1. Low Temperature

-25°C @ 500 hrs

7.2.2.2. High Temperature

65°C @ 500 hrs

7.2.2.3. High Temperature and High Humidity

60°C @ 500 hrs, R.H. = 75% ± 10%

7.2.2.4. Thermal Shock

Cycle display from -25°C to 65°C with 5-minute transfer time,

100 cycles at -25°C/65°C/-25°C.

7.2.3. Operational Testing

7.2.3.1. Low Temperature

0°C for 500 hours

7.2.3.2. High Temperature

50°C for 500 hours

7.2.3.3. High Temperature and High Humidity

50°C and 90% R.H. for 240 hours (Functional Check)
Maximum wet-bulb temperature at 39°C or lower without condensation.

7.2.3.4. Four Corner Test (72 hrs – operating)

40°C @ 10% RH
40°C @ 90% RH

10°C @10% RH

10°C @ 90% RH

7.3. Altitude

72 hour storage

Operational:	15,000 Ft.
Non-Operational:	40,000 Ft.

8. RELIABILITY

8.1. Resistance to Normal Abuse

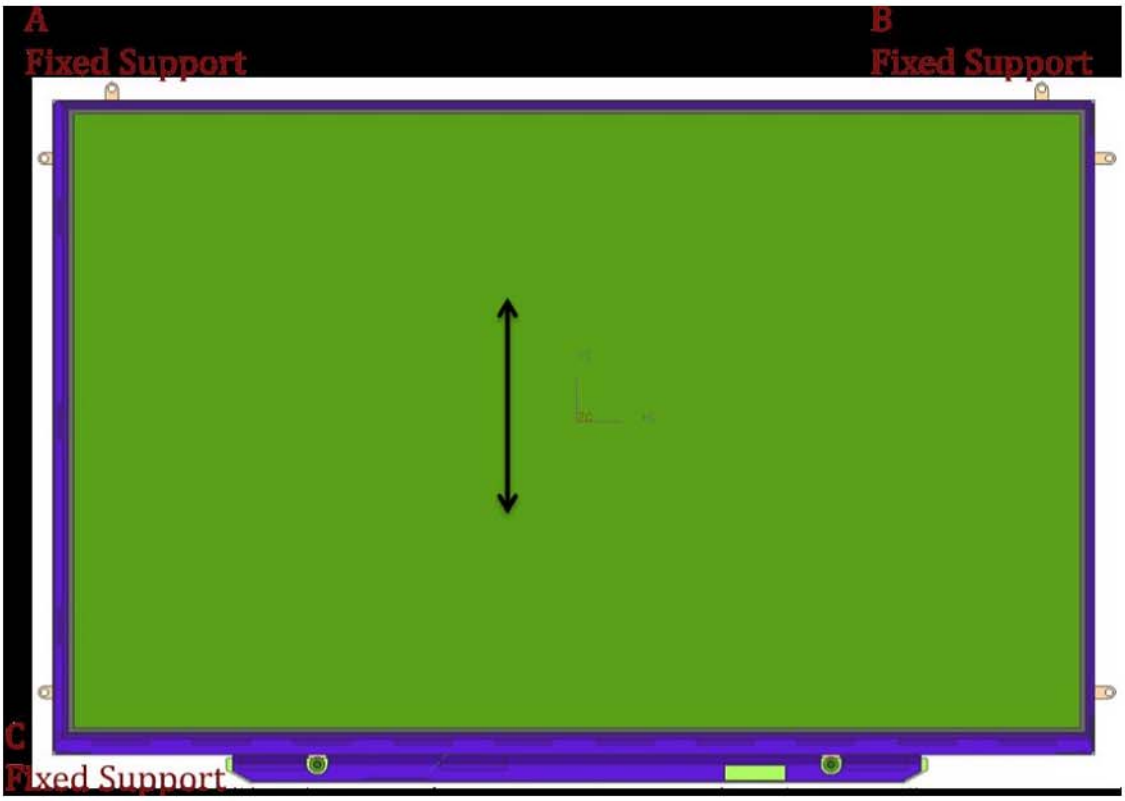
8.1.1. Torsion Test

Module is fixed by 4 mounting holes (A, B, & C) on stable supports. Tester is connected to mounting hole on free floating module corner. Push/Pull test is conducted on all four corners.

8.1.2. Test Conditions:

Applied Force	20 N
Cycles	10 K
Frequency (F=push / pull)	1 Hz (1 cycle / sec.)

8.1.3. Test Set-up



8.1.4. Static Load Deflection and Breakage

Supplier shall demonstrate compliance per Apple Specification 062-2208 Static Breakage Test

8.2. Electrostatic Discharge (ESD)

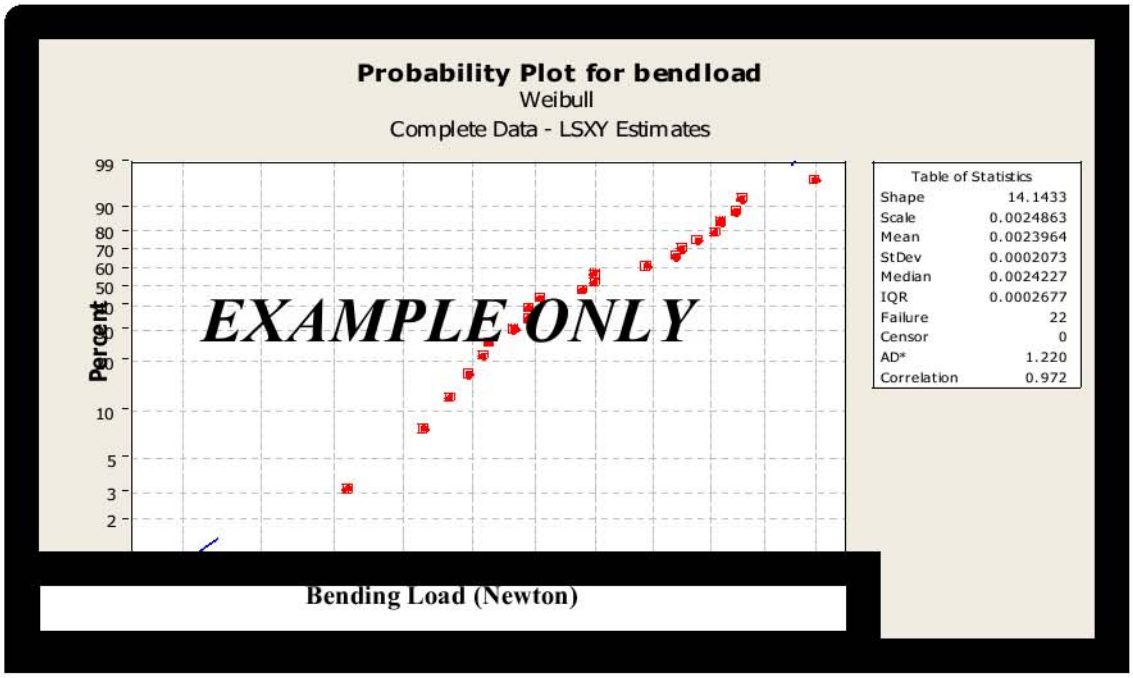
Display modules are to be tested for ESD susceptibility per Apple specification 062-0302. The display modules must meet the Level 1 for the bare module, and Level 1 through III test requirements stated in the above referenced specification, when assembled in a portable computer.

8.3. MTBF

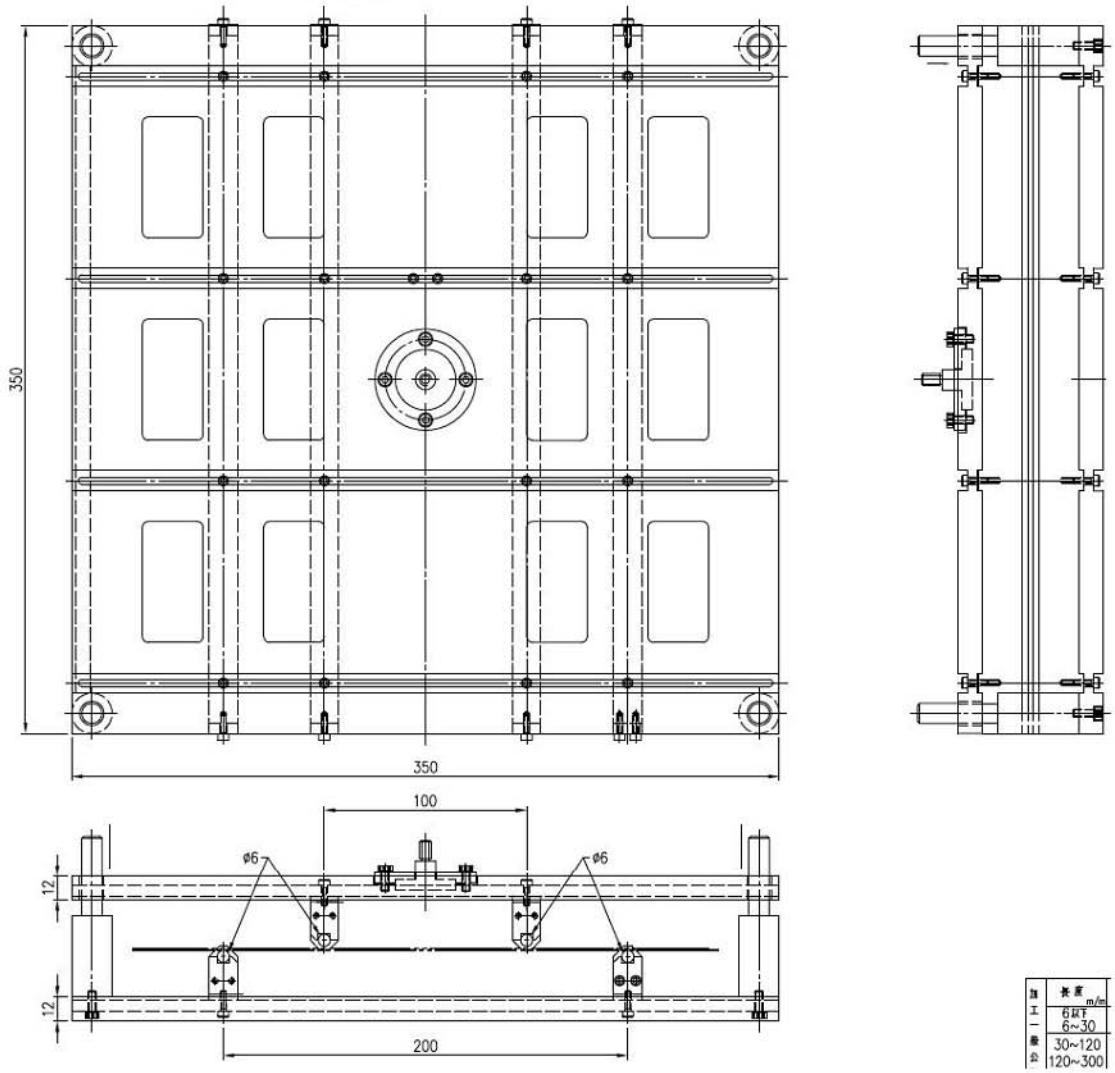
Supplier to demonstrate display module meets minimum 50,000 Hrs.@90% Confidence Supplier to include any acceleration factors included in the calculations. Power cycling frequency during this test is to be approved by Apple.

8.4. LCD Glass Strength

The LCD glass strength (failure load) will be defined at a single 90% survival rate value on Weibull distribution. Please provide the optimized loading performance in the similar chart format below. The failure load of the 90% Weibull survival rate shall be higher than TBD N.

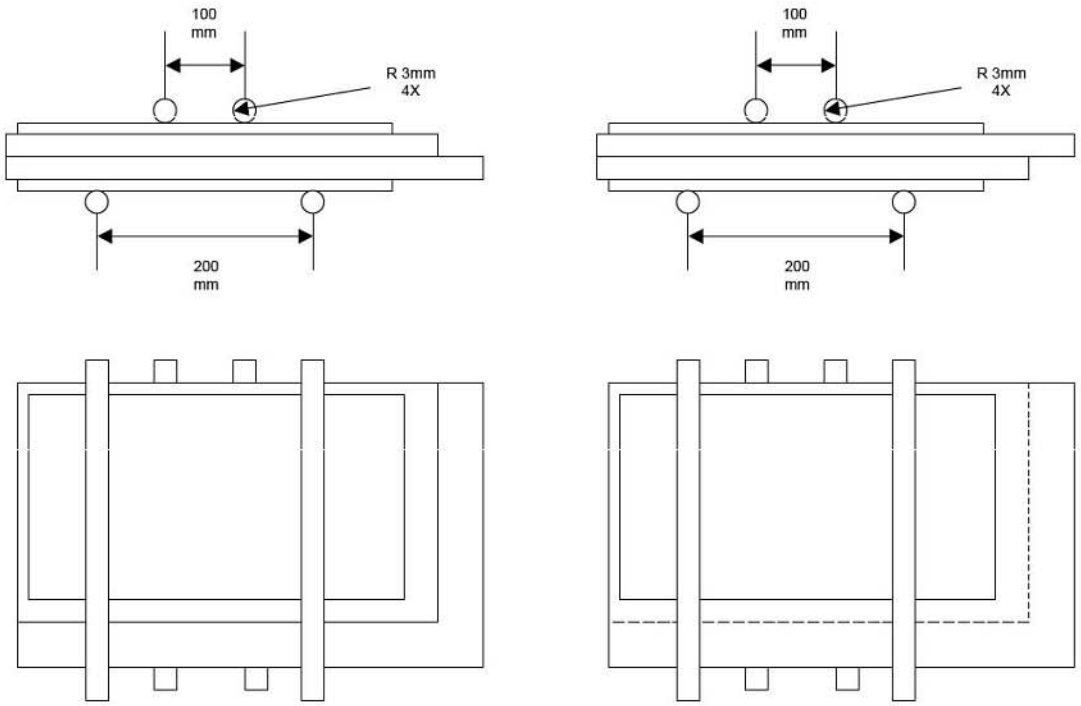


The 4 point bend test shall be used for the LCD glass strength test. The detailed fixture design/ shall follow the **ASTM standard C158-02**. The fixture is used in conduction with a load-displacement machine, commonly known as Instron.



Two orientations must be tested for this specification: orientation A (Figure 2.A) and orientation B (Figure 2.B)

This test shall be performed on 30 samples, **WITH current POLARIZERS** laminated on both top and bottom of the LCD glass, per applicable orientation as a First Article Inspection and when settings, tooling, and equipment are modified. Supplier is responsible for monitoring glass strength on an ongoing production basis. The test shall be conducted with a top rollers velocity of 1 mm/min. As soon as the first plane breaks, the test shall be stopped to prevent the second plane from breaking.



Orientation A. Longer plane parallel to ledge

Orientation B. Shorter plane parallel to ledge

Figure 2. Display orientations measuring strength at edges

LCD glass strength data collection

Failure initiation site must be determined by visual inspection by selecting one of the different cases shown below (Figure 3).

Case A) If the failure is starting from the bottom edge or close to it, enter letter A.

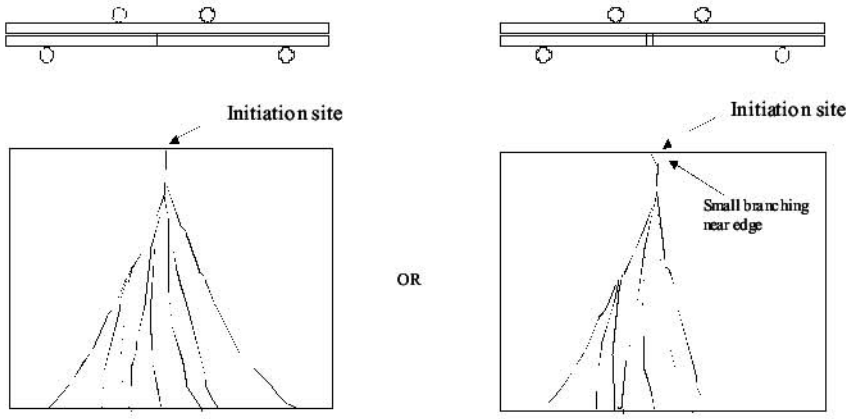
Case B) If the failure is starting from the top edge or close it, enter letter B.

Case C) If the failure is starting from the surface of glass, away from the edges and showing branching in both directions, enter letter C.

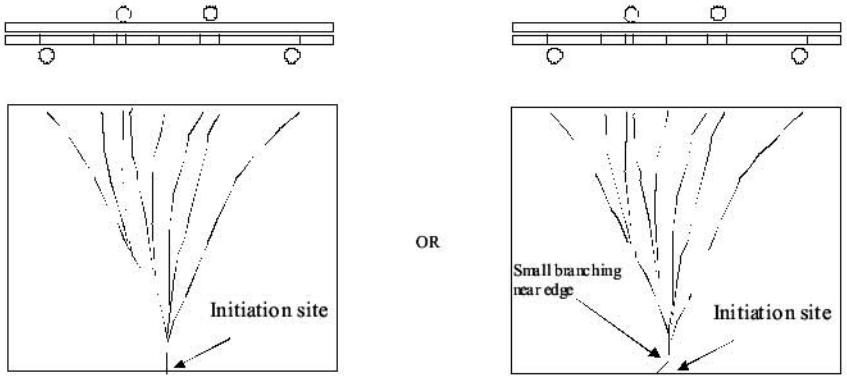
Case D) When testing in orientation D (Figure 1.D), if the failure is starting at the epoxy region between the panes, enter letter C edges of the glass (case D).

Case E) If during testing a snap is heard, but no crack is visible, enter letter E

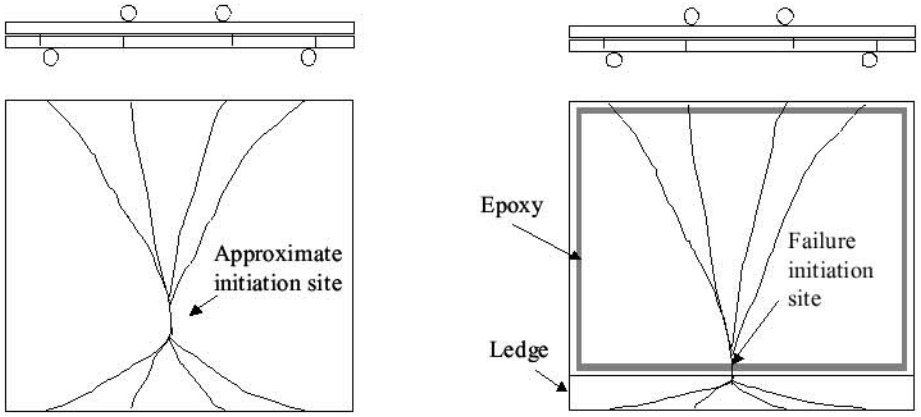
Case O) If the failure does not match any of the above or cannot be easily recognized due to catastrophic breakage, enter letter O.



Case A. Failure from bottom edge (with or without slight branching near edge)



Case B. Failure from top edge (with or without slight branching near edge)



Case C. Initiation on surface of glass

Case D. Failure at surface on epoxy region (Orientation D)

Figure 3 Surface crack initiation.

All failure loads and failure initiation sites will be entered in the following table below.

Orientation	a b c d	(Circle one)	
W [mm] =		Llong [mm] =	
Lshort [mm] =		t [mm] =	
a [mm] =			

Unit #	Failure Load [N]	Failure Initiation Site Case (A, B, C, D, E, or O)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		