

Display Specification for Q41/Q41a Project

LG 17" Wide XGA+ TFT-LCDs

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Revision History

Date	Rev #	Page #	Description
11/10/02	01		Initial Draft
02/06/03	A		1 st Production Release
04/13/04			Black Spot Improvement

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1 GENERAL DESCRIPTION

This document establishes the requirements for the display device for the Q41/Q41a project.

Display Type:	Normally-White, Transmissive, Twisted-Nematic TFT-LCDs With Wide-Viewing Optical Films
Manufacturer:	LG.Philips LCD
Mfg. P/N:	LP171W01-A4K3
Display Active Area:	367.20 mm (H) x 229.50 mm (V), 17.05" (43.30 cm) diagonal
Resolution:	1440 (RGB stripe, H) x 900 (V)
Aspect:	16:10
Module Outline Size:	382.2 mm (W) x 244.5 mm (H) x 6.2 mm (D), typical 6.5 mm (D, max) and 6.2 mm (max) at the cable pass-through
Weight:	760 g (max), 740 g (typical)
Luminance:	160 nits @ 6.0 mA (typical)
Power Consumption:	6.5 W @ Black (typical, the logic plus the backlight, 6 mA lamp current, logic 1.7 W and B/L 4.8 W)
Color Depth:	6 bits/color, 262,144 colors
Surface Treatment:	3H hard coating, anti-glare treatment of the front polarizer

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2 ORDER OF PRECEDENCE OF DOCUMENTATION AUTHORITY

In the case of any conflict in any specification related to these parts, this order of precedence of authority shall apply:

2.1 The Purchase Order

2.2 This Specification

2.3 Reference Documents

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3 PHYSICAL DESCRIPTION

3.1 Display Mode

Normally White, Transmissive, Twisted Nematic Liquid Crystal Displays With
Wide Viewing Films

3.2 Pixel Configuration

RGB Vertical Stripe

3.3 Pixel Pitch

0.255 mm x 0.255 mm, 99.6 ppi

3.4 Resolution

1440 (RGB stripe, H) x 900 (V)

3.5 Aperture Ratio

Minimum > 55%

3.6 Optimum Viewing Cone

6 o'clock direction

3.7 Interface & Driving Scheme

3.3V dual-channel LVDS (Flat Link) interface, DE (Data Enable) only mode, dot
inversion (2 sub-pixels)

3.8 Front Surface Treatment

The display surface must meet 3H based on JIS Pencil Scratch Tester for Coated
Film (JIS K 5400) and must have anti-glare treatment approved by Apple.

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4 MECHANICAL REQUIREMENTS

4.1 Dimensions and Tolerances

Refer to Apple MCO 062-9331, which include height, width, and thickness, mounting details, bulb location, cable length, and connectors. The LCD module outline is described in the following table.

Dimension	Min	Typ	Max	Unit
Horizontal (H)	381.7	382.2	382.7	mm
Vertical (V)	244.0	244.5	245.0	mm
Depth (D)	-	6.2	6.5	mm

Note: 6.2 mm (max) at the LVDS cable path-through.

4.2 Weight

760 g (max), 740 g (typical)

4.3 Exposed Areas and Restrictions

The display module shall not have exposed edges or components, which may cause injury or damage during handling, inspection, assembly, and service. Exposed areas of the display module (those not protected or shielded by construction) must be insulated and otherwise protected to eliminate the possibility of electrical shorting or destructive ESD discharges (per Section 7.2) during handling, inspection, assembly, and service. The Supplier shall identify all such areas prior to the Design Review and work with Apple Engineering to ensure the above criteria have been addressed.

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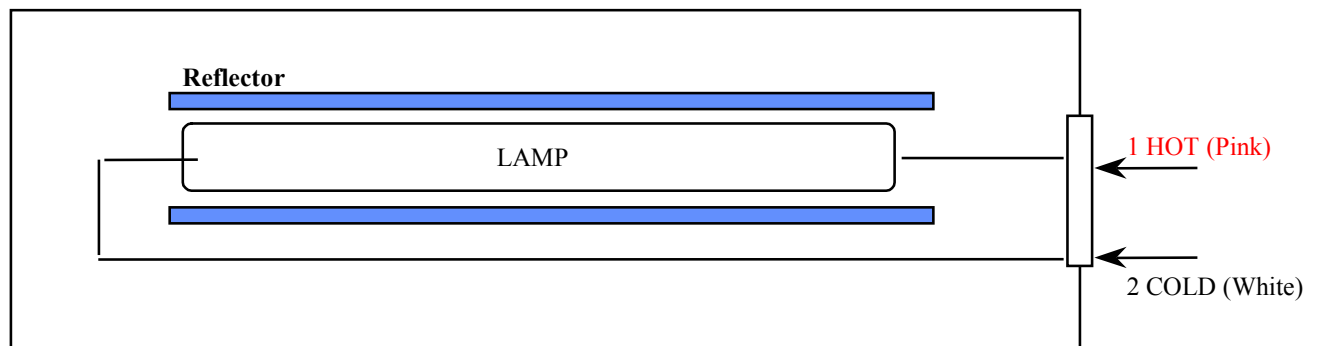
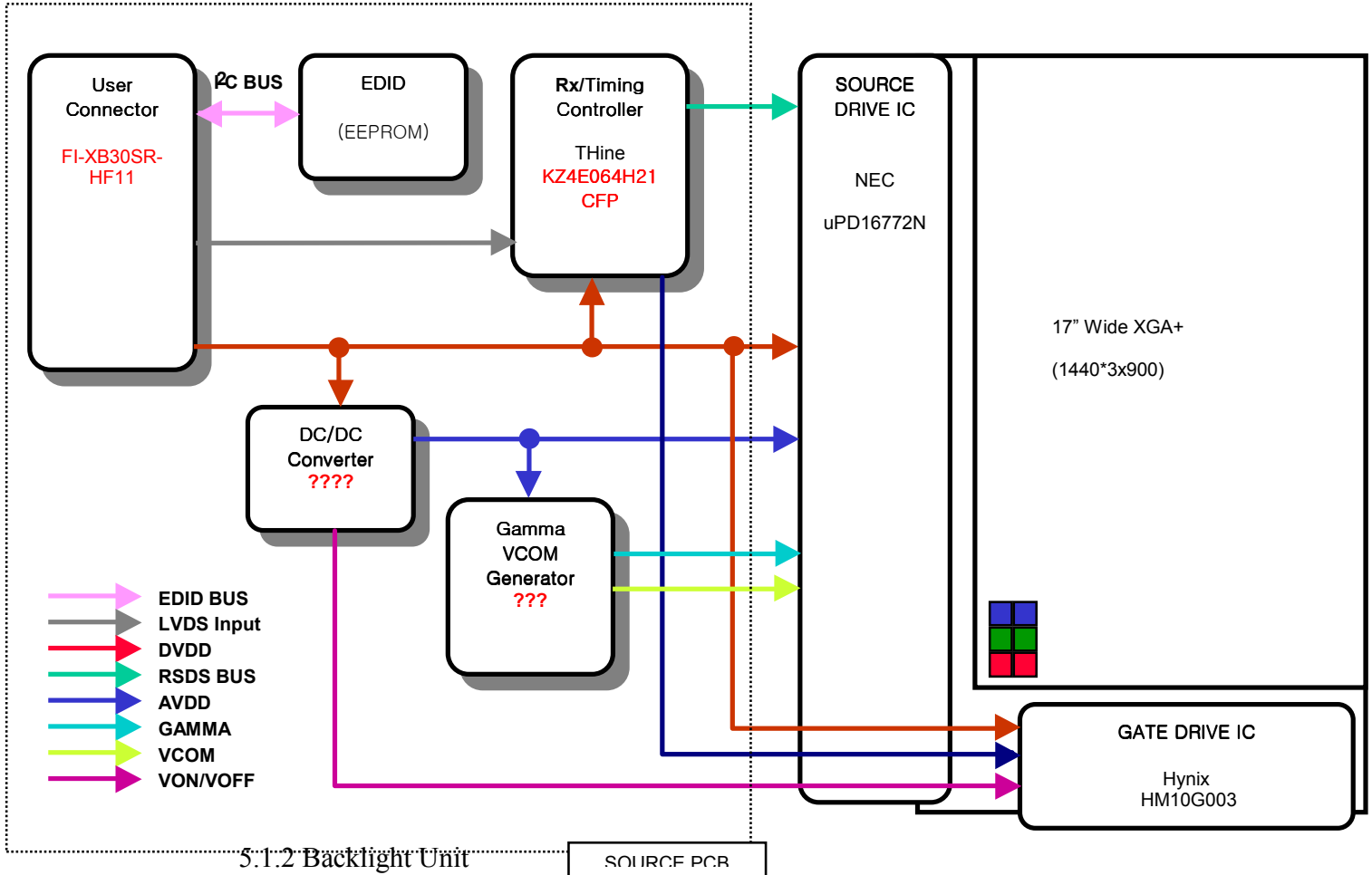
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5 ELECTRICAL REQUIREMENTS

5.1 Block Diagram

5.1.1 TFT LCD Module



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5.2 Display Subsystem (PCB & TFT Panel)

5.2.1 Pin-Out (Dual Channel LVDS Interface)

Connector: JAE FI-XB30SR-HF11 (1.5 mm thickness, normal type, pin 1 starts from left on the front)

Matching Connector: JAE FI-X30M or equivalent (microcoax type)

Interface Chips: Thine KZ4E064H21CFP (integrated LVDS and timing controller)

Pin	Symbol	Description	Micro-coax cable gauge (AWG)
1	GND	Ground	40
2	Vcc	Power Supply (+3.3V)	32
3	Vcc	Power Supply (+3.3V)	32
4	V _{EDID}	DDC 3.3V Power	40
5	NC	No Connection	40
6	Clk _{EDID}	DDC Clock	40
7	DATA _{EDID}	DDC Data	40
8	Odd_Rin0-	Odd Channel Differential Data Input	40
9	Odd_Rin0+	Odd Channel Differential Data Input	40
10	GND	Ground	40
11	Odd_Rin1-	Odd Channel Differential Data Input	40
12	Odd_Rin1+	Odd Channel Differential Data Input	40
13	GND	Ground	40
14	Odd_Rin2-	Odd Channel Differential Data Input	40
15	Odd_Rin2+	Odd Channel Differential Data Input	40
16	GND	Ground	40
17	Odd_Clkin-	Odd Channel Differential Clock Input	40
18	Odd_Clkin+	Odd Channel Differential Clock Input	40
19	GND	Ground	40
20	Even_Rin0-	Even Channel Differential Data Input	40
21	Even_Rin0+	Even Channel Differential Data Input	40
22	GND	Ground	40
23	Even_Rin1-	Even Channel Differential Data Input	40
24	Even_Rin1+	Even Channel Differential Data Input	40
25	GND	Ground	40
26	Even_Rin2-	Even Channel Differential Data Input	40
27	Even_Rin2+	Even Channel Differential Data Input	40
28	GND	Ground	40
29	Even_Clkin-	Even Channel Differential Clock Input	40
30	Even_Clkin+	Even Channel Differential Clock Input	40

NOTE: (1) The 28 40-AWG LVDS signal lines shall have an impedance of 50 Ohms per line;
 (2) Make sure that the odd channel = lower channel and the even channel = upper channel.

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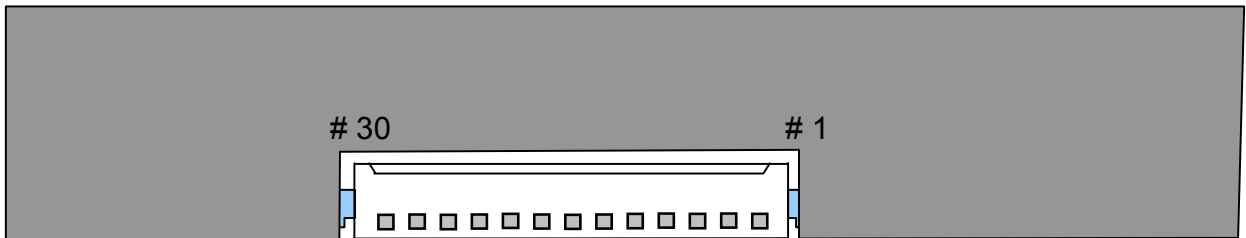
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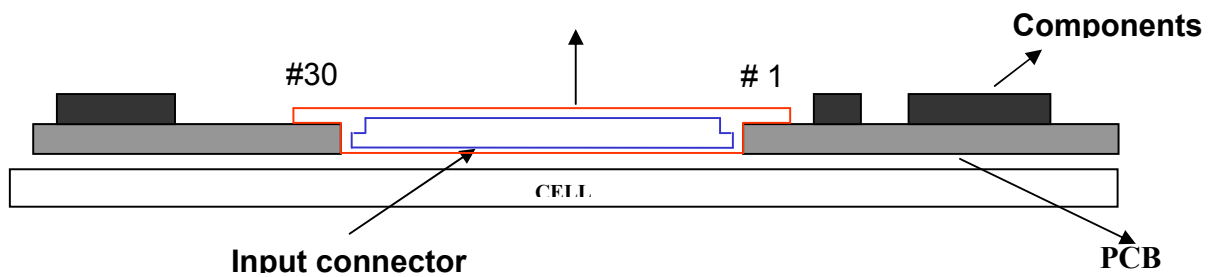
5.2.2 Connector Diagram

On back of display

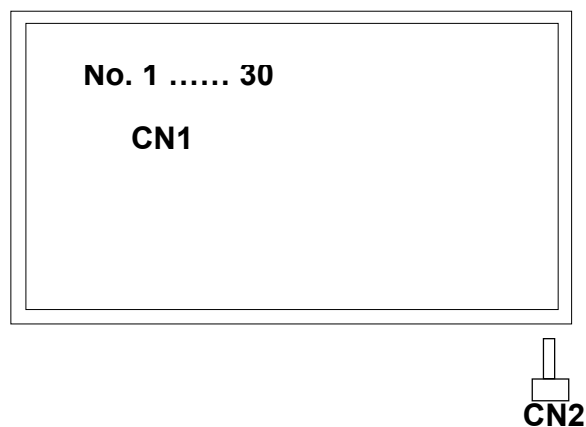


30 pin JAE FI-XB30SR-HF11, or compatible

Mating connector on LVDS cable: JAE FI-X30M or compatible



On front of display



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5.2.3 Logic Level Interface (Per LVDS standard requirements)

REQUIRED SIGNAL ASSIGNMENT FOR Flat Link Transmitter (Per Each Channel, Even or Odd)

Pin #	Pin Name	Require Signals	Pin #	Pin Name	Require Signals
1	D4	R4	48	D3	R3
2	Vcc	Vcc	47	D2	R2
3	D5	R5	46	GND	GND
4	D6	G0	45	D1	R1
5	GND	GND	44	D0	R0
6	D7	G1	43	NC	NC
7	D8	G2	42	LVDS GND	LVDS GND
8	Vcc	Vcc	41	Y0M	A0M
9	D9	G3	40	Y0P	A0P
10	D10	G4	39	Y1M	A1M
11	GND	GND	38	Y1P	A1P
12	D11	G5	37	LVDS Vcc	LVDS Vcc
13	D12	B0	36	LVDS GND	LVDS GND
14	NC	NC	35	Y2M	A2M
15	D13	B1	34	Y2P	A2P
16	D14	B2	33	CLKOUTM	CLKM
17	GND	GND	32	CLKOUTP	CLKP
18	D15	B3	31	LVDS GND	LVDS GND
19	D16	B4	30	PLLGND	PLL GND
20	D17	B5	29	PLLVcc	PLL Vcc
21	Vcc	Vcc	28	PLLGND	PLL GND
22	D18	HSYNC	27	SHDN	SHDN
23	D19	VSYNC	26	CLKIN	Dclk
24	GND	GND	25	D20	DE (Data Enable)

Notes: Refer to LVDS Transmitter Data Sheet for detail descriptions.

Flat Link Interface

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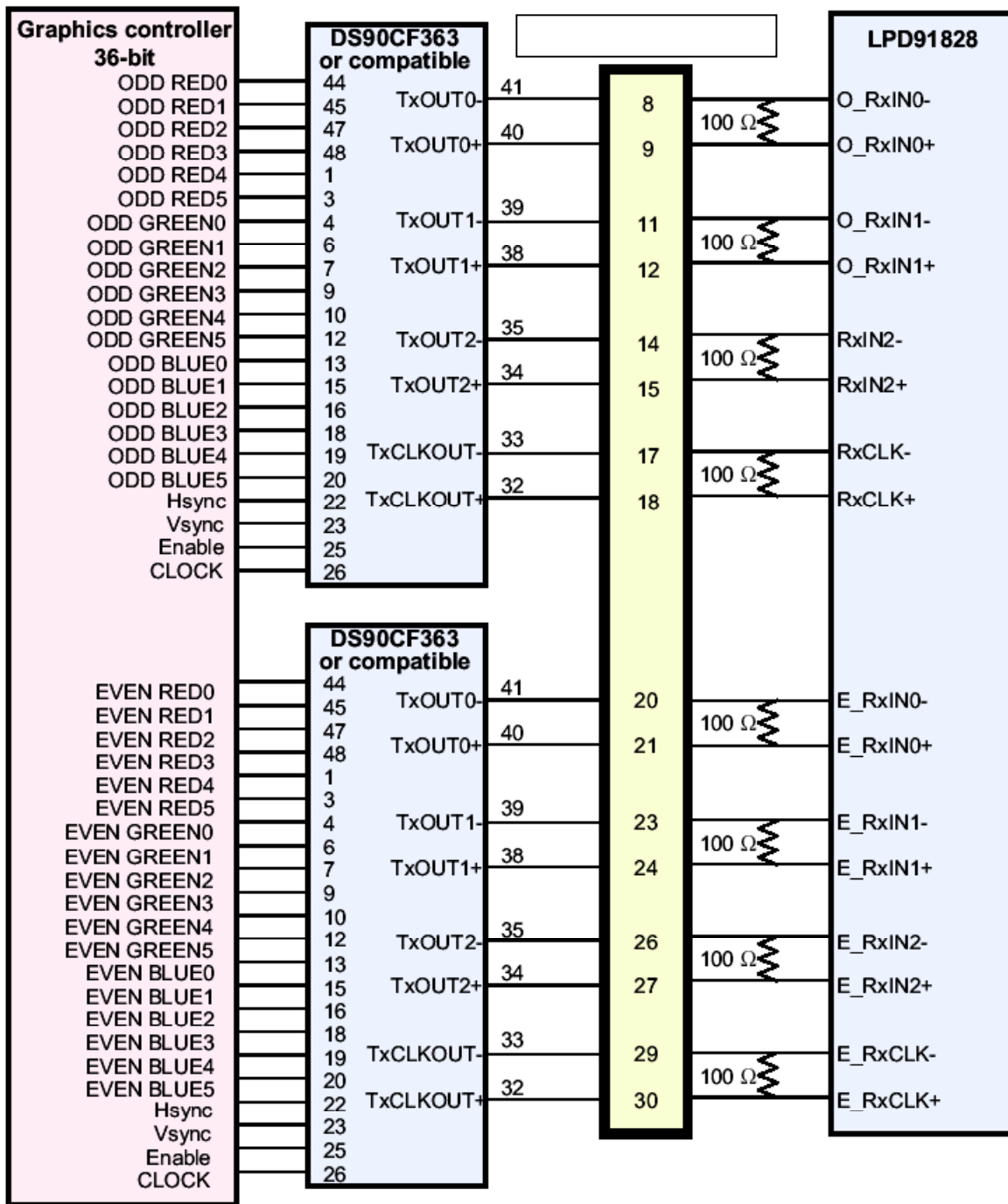
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Note : The LCD Module uses a 100ohm resistor between positive and negative lines of each receiver input.

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5.2.4 EDID Interface (Per VESA EDID 1.x standard requirements)

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)	Value (binary)	
0	00	Header	0 0	000 000 0 0	Header
1	01		F F	111 111 1 1	
2	02		F F	111 111 1 1	
3	03		F F	111 111 1 1	
4	04		F F	111 111 1 1	
5	05		F F	111 111 1 1	
6	06		F F	111 111 1 1	
7	07		0 0	000 000 0 0	
8	08	EISA manufacturer code = APP	0 6	000 011 0 0	Vender/ Product ID
9	09		1 0	000 000 1 0	
10	0A	Product code = refer to Apple's request	2 C	001 110 0 0	
11	0B	(Hex, LSB first)	9 C	100 110 1 0	
12	0C	32-bit serial number	0 0	000 000 0 0	
13	0D		0 0	000 000 0 0	
14	0E		0 0	000 000 0 0	
15	0F		0 0	000 000 0 0	
16	10	Week of manufacture = 1st week	0 1	000 000 0 1	EDID Version/ Revision
17	11	Year of manufacture = 2003	0 D	000 110 0 1	
18	12	EDID Structure version # = 1	0 1	000 000 0 1	
19	13	EDID Revision # = 3	0 3	000 001 0 1	Display Parameter
20	14	Video input definition = Digital I/p,non TMDS CRGB	8 0	100 000 0 0	
21	15	Max H image size(cm)=36.720 cm(37)	2 5	001 010 0 1	
22	16	Max V image size(cm)=22.950 cm(23)	1 7	000 011 1 1	
23	17	Display gamma = 2.20	7 8	011 100 1 0	
24	18	Feature support(DPMS) = Active off, RGB Color	0 A	000 101 0 0	
25	19	Red/Green low Bits	0 3	000 001 0 1	
26	1A	Blue/White Low Bits	1 D	000 110 1 1	
27	1B	Red X Rx =0.610	9 C	100 110	

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						1	0	
28	1C	Red Y	Ry =0.340	5	7	010	011	Color Characteristic
						1	1	
29	1D	Green X	Gx =0.325	5	3	010	001	
						1	1	
30	1E	Green Y	Gy =0.550	8	C	100	110	
						0	0	
31	1F	Blue X	Bx =0.145	2	5	001	010	
						0	1	
32	20	Blue Y	By =0.115	1	D	000	110	
						1	1	
33	21	White X	Wx = 0.320	5	1	010	000	
						1	1	
34	22	White Y	Wy = 0.330	5	4	010	010	
						1	0	
35	23	Established Timing I		0	0	000	000	Established Timings
						0	0	
36	24	Established Timing II		0	0	000	000	
						0	0	
37	25	Manufacturer's Timings		0	0	000	000	
						0	0	
38	26	Standard Timing Identification 1 was not used		0	1	000	000	Standard Timing ID
						0	1	
39	27	Standard Timing Identification 1 was not used		0	1	000	000	
						0	1	
40	28	Standard Timing Identification 2 was not used		0	1	000	000	
						0	1	
41	29	Standard Timing Identification 2 was not used		0	1	000	000	
						0	1	
42	2A	Standard Timing Identification 3 was not used		0	1	000	000	
						0	1	
43	2B	Standard Timing Identification 3 was not used		0	1	000	000	
						0	1	
44	2C	Standard Timing Identification 4 was not used		0	1	000	000	
						0	1	
45	2D	Standard Timing Identification 4 was not used		0	1	000	000	
						0	1	
46	2E	Standard Timing Identification 5 was not used		0	1	000	000	
						0	1	
47	2F	Standard Timing Identification 5 was not used		0	1	000	000	
						0	1	
48	30	Standard Timing Identification 6 was not used		0	1	000	000	
						0	1	
49	31	Standard Timing Identification 6 was not used		0	1	000	000	
						0	1	
50	32	Standard Timing Identification 7 was not used		0	1	000	000	
						0	1	
51	33	Standard Timing Identification 7 was not used		0	1	000	000	
						0	1	
52	34	Standard Timing Identification 8 was not used		0	1	000	000	
						0	1	
53	35	Standard Timing Identification 8 was not used		0	1	000	000	
						0	1	
54	36	1440 X 900 @ 60 Hz mode pixel clock = 96.21 MHz		9	5	100	010	
						1	1	
55	37	(Stored LSB first)		2	5	001	010	
						0	1	
56	38	Horizontal Active = 1440 pixels		A	0	101	000	
						0	0	
57	39	Horizontal Blanking = 320 pixels		4	0	010	000	
						0	0	

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58	3A	Horizontal Active : Horizontal Blanking = 1440 : 320	5	1	010 000 1 1	Detailed Timing Description #1	
59	3B	Vertical Active = 900 lines	8	4	100 010 0 0		
60	3C	Vertical Blanking = 12 lines	0	C	000 110 0 0		
61	3D	Vertical Active : Vertical Blanking = 900 : 12	3	0	001 000 1 0		
62	3E	Horizontal Sync. Offset = 64 pixels	4	0	010 000 0 0		
63	3F	Horizontal Sync Pulse Width = 32 pixels	2	0	001 000 0 0		
64	40	Vertical Sync Offset = 3 lines, Sync Width = 3 lines	3	3	001 001 1 1		
65	41	Horizontal Vertical Sync Offset/Width upper 2bits = 0	0	0	000 000 0 0		
66	42	Horizontal Image Size = 367.20 mm(367)	6	F	011 111 0 1		
67	43	Vertical Image Size = 229.50 mm(230)	E	6	111 011 0 0		
68	44	Horizontal & Vertical Image Size	1	0	000 000 1 0		
69	45	Horizontal Border = 0	0	0	000 000 0 0		
70	46	Vertical Border = 0	0	0	000 000 0 0		
71	47	Non-interlaced, Normal display, no stereo, Digital separate sync, H/V pol negatives	1	8	000 100 1 0		
72	48	Detailed Timing Descriptor #2	0	0	000 000 0 0		Detailed Timing Description #2
73	49		0	0	000 000 0 0		
74	4A		0	0	000 000 0 0		
75	4B		0	1	000 000 0 1		
76	4C	Version	0	0	000 000 0 0		
77	4D	Apple edid signature	0	6	000 011 0 0		
78	4E	Apple edid signature	1	0	000 000 1 0		
79	4F	Link Type	3	0	001 000 1 0		
80	50	Pixel and link component format = 6-bit panel interface	0	0	000 000 0 0		
81	51	Panel features = Inverter NA (no inverter)	0	0	000 000 0 0		
82	52		0	0	000 000 0 0		
83	53		0	0	000 000 0 0		
84	55		0	0	000 000 0 0		
85	55		0	0	000 000 0 0		
86	56		0	0	000 000 0 0		
87	57		0	0	000 000 0 0		
88	58		0	A	000 101	Apple Defined	

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					0 0	
89	59		2	0	001 000 0 0	
90	5A	Detailed Timing Descriptor #3	0	0	000 000 0 0	Detailed Timing Description #3 Ascii Data String: LP171W01
91	5B		0	0	000 000 0 0	
92	5C		0	0	000 000 0 0	
93	5D		F	E	111 111 1 0	
94	5E		0	0	000 000 0 0	
95	5F	L	4	C	010 110 0 0	
96	60	P	5	0	010 000 1 0	
97	61	1	3	1	001 000 1 1	
98	62	7	3	7	001 011 1 1	
99	63	1	3	1	001 000 1 1	
100	64	W	5	7	010 011 1 1	
101	65	0	3	0	001 000 1 0	
102	66	1	3	1	001 000 1 1	
103	67		0	0	000 000 0 0	
104	68		0	0	000 000 0 0	
105	69		0	0	000 000 0 0	
106	6A	LF	0	A	000 101 0 0	
107	6B	SPACE	2	0	001 000 0 0	
108	6C	Detailed Timing Descriptor #4	0	0	000 000 0 0	Detailed Timing Description #4
109	6D		0	0	000 000 0 0	
110	6E		0	0	000 000 0 0	
111	6F		F	C	111 110 1 0	
112	70		0	0	000 000 0 0	
113	71	C	4	3	010 001 0 1	
114	72	o	6	F	011 111 0 1	
115	73	l	6	C	011 110 0 0	
116	74	o	6	F	011 111 0 1	
117	75	r	7	2	011 001 1 0	
118	76	SPACE	2	0	001 000 0 0	

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119	77	L	4	C	010 110 0 0	Monitor Name: Color LCD
120	78	C	4	3	010 001 0 1	
121	79	D	4	4	010 010 0 0	
122	7A	LF	0	A	000 101 0 0	
123	7B	SPACE	2	0	001 000 0 0	
124	7C	SPACE	2	0	001 000 0 0	
125	7D	SPACE	2	0	001 000 0 0	
126	7E	Extension flag = 00	0	0	000 000 0 0	Extension Flag
127	7F	Checksum	5	6	010 011 1 0	Checksum

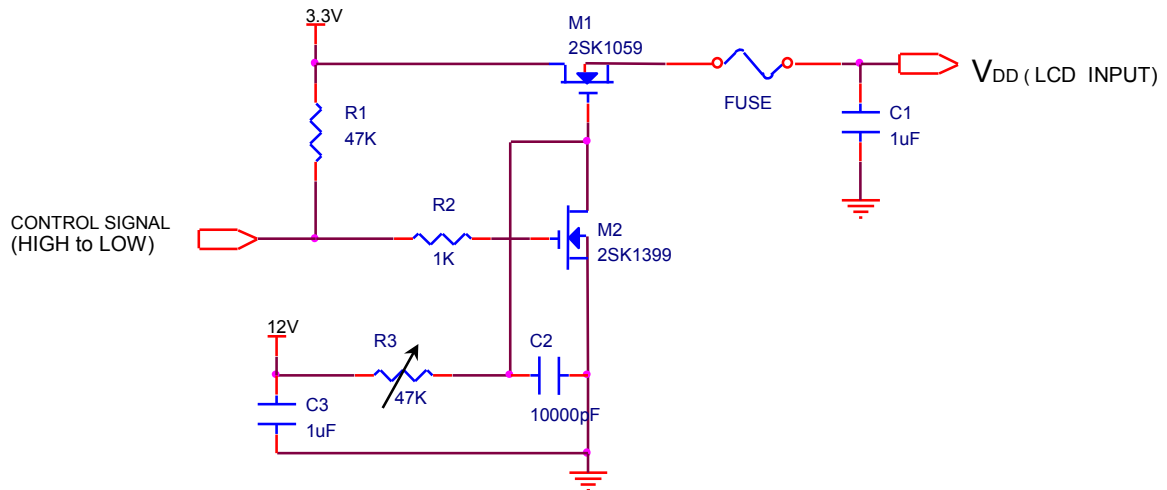
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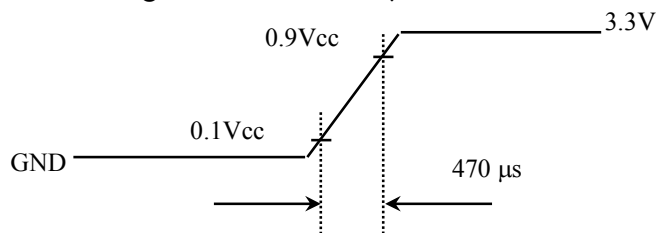
5.2.5 Electrical Ratings

PARAMETER	SYMBOL	VALUES			UNIT	NOTES
		Min.	Typ.	Max.		
Power Supply Input Voltage	V_{CC}	3.0	3.3	3.6	V (DC)	
Power Supply Ripple			50	100	mV _{p-p}	1
Power Supply Input Current	I_{CC}	-	540	620	mA	2
Power Consumption	P_c	-	1.75	-	W	2
Rush current	I_{RUSH}	-	-	1.5	A	4
Differential Impedance	Z_m	90	100	110	Ω	3
Differential Input Voltage Rx	V_{IH}			+100	mV	$V_{CM} =$
	V_{IL}	-100			mV	+1.25V

- Notes:
- (1) The power supply ripple is measured whereas a black pattern is displayed;
 - (2) The specified current and power consumption are under the conditions at $V_{cc} = 3.3$ V, $T = 25^\circ\text{C}$, and $f_v = 60$ Hz, whereas a vertical stripe pattern (the worst case) is displayed;
 - (3) This impedance value is needed to a proper display and is measured form LVDS T_x to its mating connector;
 - (4) The duration of the rush current is about 20 ms, which should have the following typical condition.



V_{cc} rising time is about 470 μ s



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Title: Spec., Elec., Dspl., LG 17"W TFT-LCD, Q41/Q41a Project

DWG Number: 062-9499 Rev. A

5.2.6 Signal Timing

5.2.5.1 Signal Impedance

Defined in VESA standard for LVDS FPDI 2

5.2.5.2 Timing Data

This is the signal timing required at the input of the control ASIC concerned with LVDS as a FlatLink or equivalent. All of the interface signal timing should be satisfied with the following specifications based on the VESA timing guideline (1440x900 @ 60 Hz) for its proper operation. LP171W01 panels with LVDS transmitter are recommended to be connected with the Display Enable, Horizontal Sync, Vertical Sync, Clock Signal from the Video Signal Controller to the input of the Transmitter simultaneously.

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Title: **Spec, Elec., Dspl., LG 17" W TFT-LCD, O41/O41a Project**

DWG Number: **062-9499** Rev. **A**

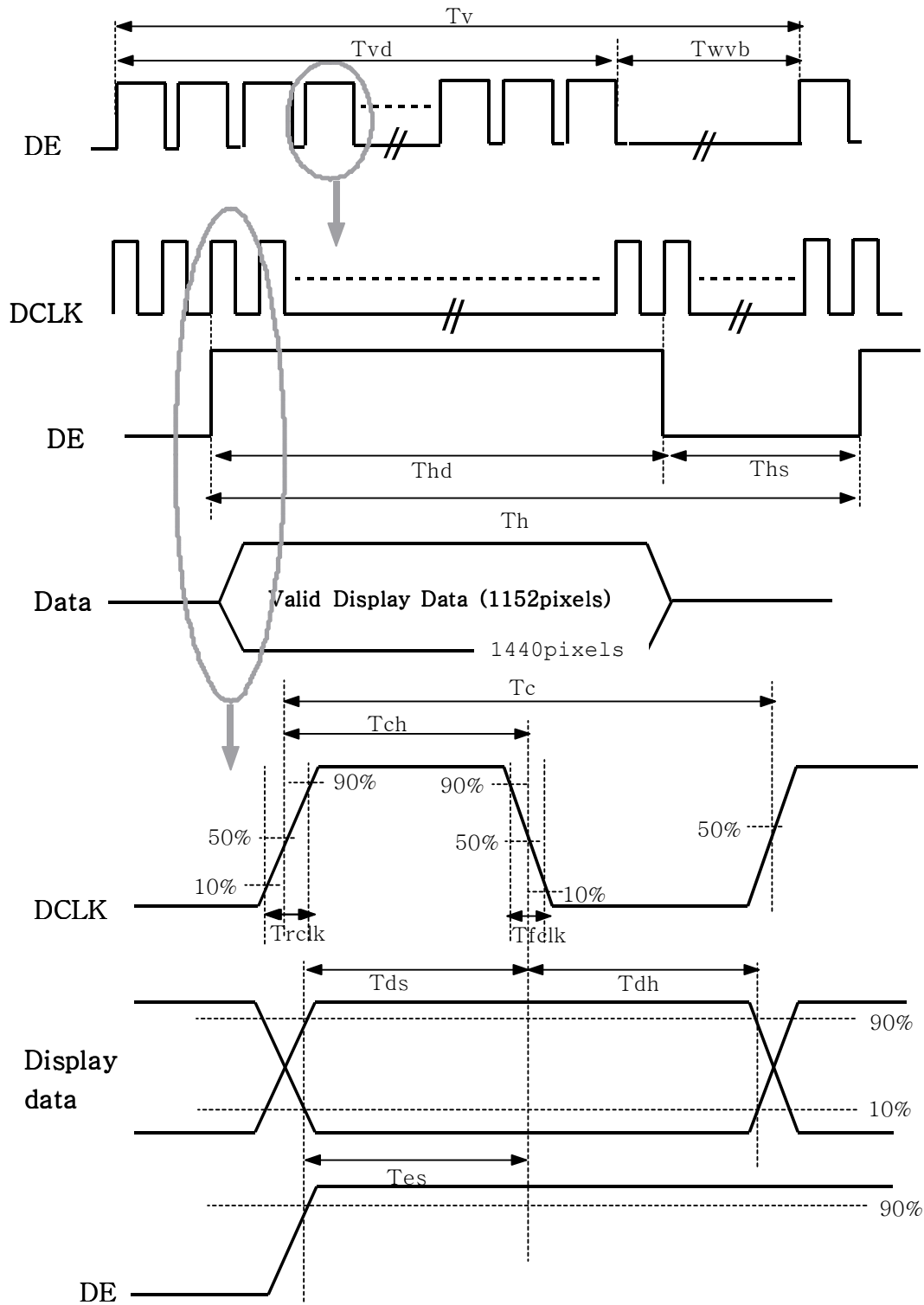
Video Timing Data

Signal	Parameter	Symbol	Min	Typ	Max	Unit	Note
D _{CLK}	Clock Period	T _C		10.39		ns	1
	Clock Frequency	f _C		96.21		MHz	1/T _C
	Duty Ratio (% High)	K _{dr}	40	50	60	%	T _{Ch} /T _C
	Rise Time	T _{R CLK}	-	4.42	-	ns	
	Fall Time	T _{F CLK}	-	4.42	-	ns	
DE (Data Enable Only) (DTMG) Data	DE Setup Time	T _{se}	4	-	-	ns	
	Data Setup Time	T _{sd}	4	-	-	ns	
	Data Hold Time	T _{hd}	2	-	-	ns	
	Horizontal Period	T _H	1648	1760		T _C	2
	Horizontal Blank Period	T _{ha}	208	320		T _C	
	Vertical Period	T _V	905	912		T _H	f _V =59.94 Hz, 3
H _{sync}	H _{sync} Back Porch	H _{bp}	176	224	-	T _C	
	H _{sync} Pulse Width	T _{WH}	16	32		T _C	
	H _{sync} Front Porch	H _{fp}	16	64	-	T _C	
	Horizontal Active Period	T _{HD}	1440	1440	1440	T _C	Display Period
V _{sync}	V _{sync} Back Porch	V _{bp}	3	6		T _H	
	V _{sync} Pulse Width	T _{WV}	1	3		T _H	
	V _{sync} Front Porch	V _{fp}	1	3		T _H	
	Vertical Active Period	T _{VD}	900	900	900	T _H	Display Period

- Note: (1) When the WXGA+ controller sets DE only Mode, H_{sync} and V_{sync} should be set low logic level or ground.
The duration of DE (DTMG) signal must be longer than 1 clock period (T_C) at every horizontal sync period;
- (2) Horizontal Period = One Line Scanning Time;
- (3) The vertical period T_V is related to the frame frequency f_V, i.e., 59.94 Hz.

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5.2.5.3 Video Timing Diagram

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5.3.1 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

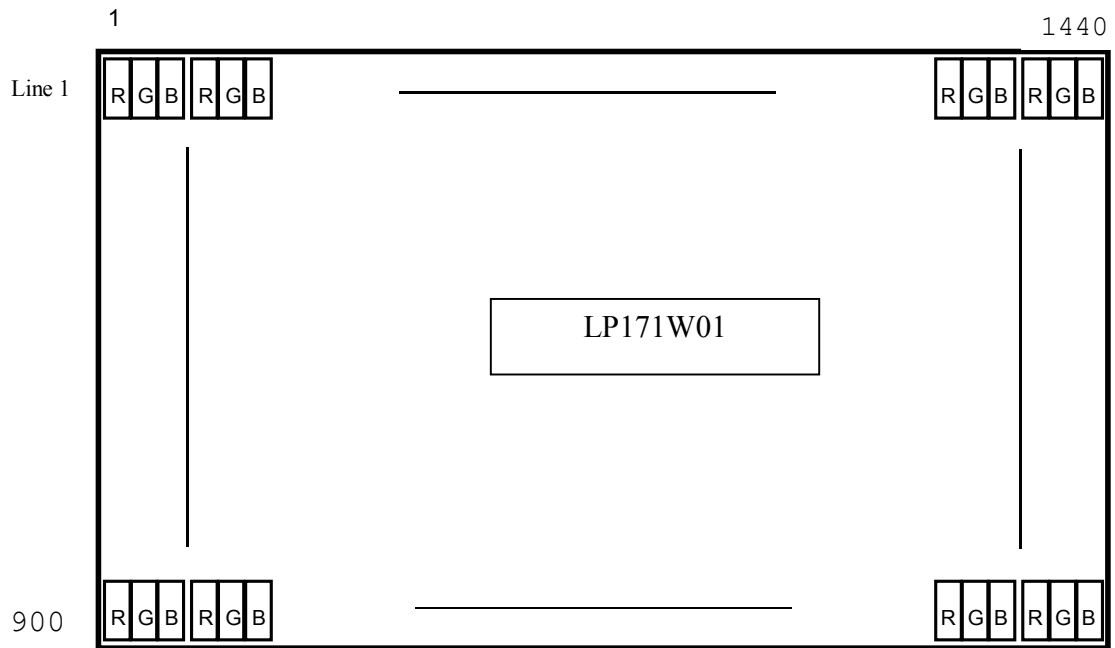
COLOR DATA REFERENCE

Color		Input Color Data																	
		Red						Green						Blue					
		MSB		LSB				MSB		LSB				MSB		LSB			
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(00) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63) Bright	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(00)Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)Bright	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue(00) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63) Bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

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Pixel Format on the Display



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Title: Spec, Elec., Dspl., LG 17"W TFT-LCD, O41/O41a Project

DWG Number: 062-9499 Rev. A

5.2.3 Power Measurements (W/O backlight)

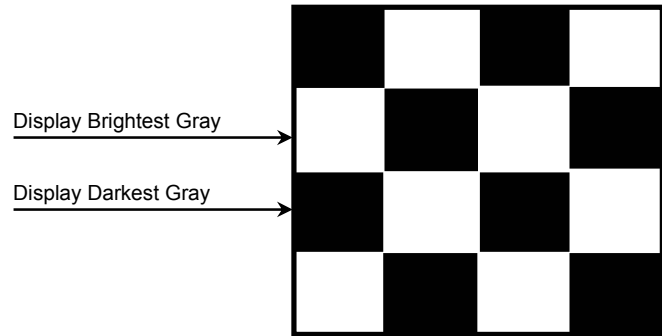
Pattern	Min	Typ	Max	Unit
White	-	380	-	mA
Mosaic	-	435	-	mA
V. Stripe	-	520	600	mA
Black	-	515	592	mA

- Note: (1) Display data pins and timing signal pins should be connected (GND = 0V);
 (2) Operation conditions: $f_v = 59.94$ Hz, $f_{CLK} = 96.21$ MHz, $V_{cc} = 3.3$ V;
 (3) Power dissipation patterns are as follows.

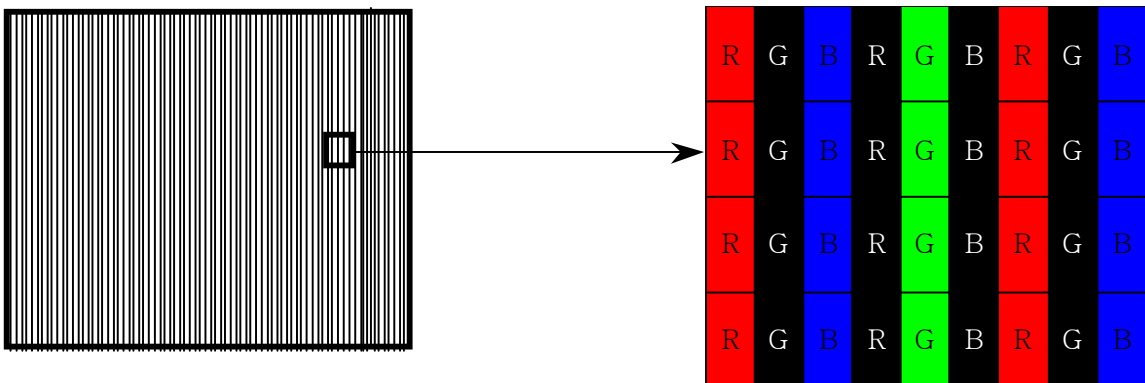
(a) White screen



(b) Mosaic (or checker) pattern



(c) Vertical Stripe Pattern

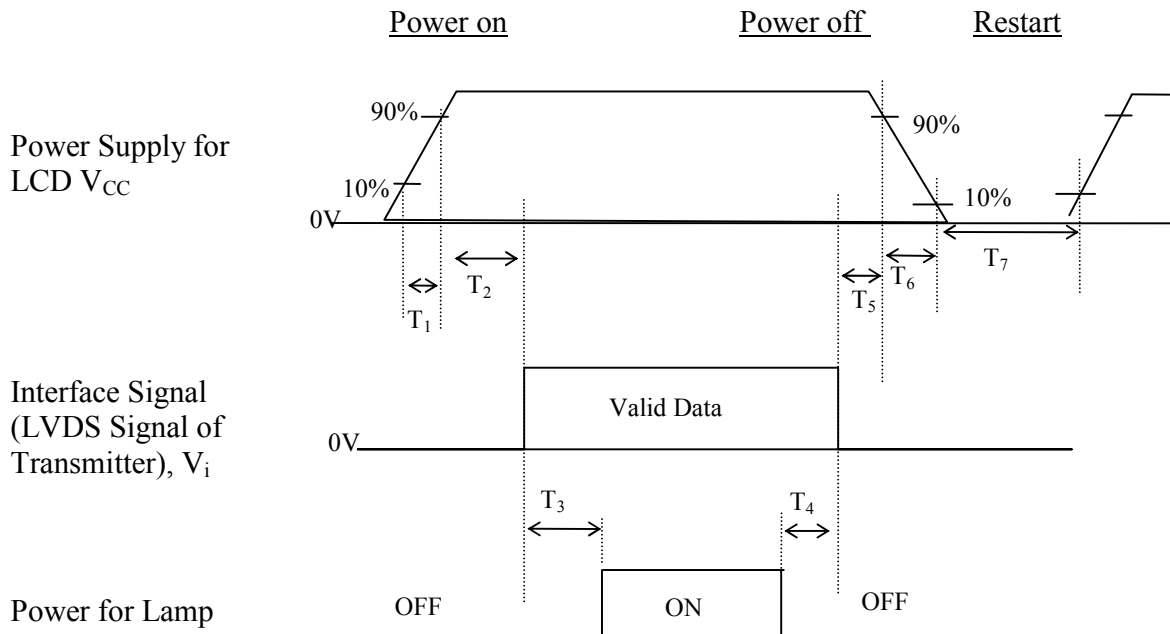


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5.2.4 Power on-off sequence

The LCD module must be powered up and down as indicated or the device may be damaged permanently. *The power-on includes both PowerBook system starting and the system from the sleep to wakeup; the power-off includes both PowerBook system shutdown and the one from on to sleep.*



Parameter	Values			Unit
	Min.	Typ.	Max.	
T_1	0.01	-	10	ms
T_2	0	20	50	ms
T_3	0	250	-	ms
T_4	0	250	-	ms
T_5	0	20	50	ms
T_6	0	-	100	ms
T_7	400	-	-	ms

- Notes:
- (1) Please avoid floating state of interface signal at invalid period;
 - (2) When the interface signal is invalid, be sure to pull down the V_{CC} to 0 V;
 - (3) The back light inverter power must be turned on after the power supply for the logic and the interface signal is valid. The back light inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

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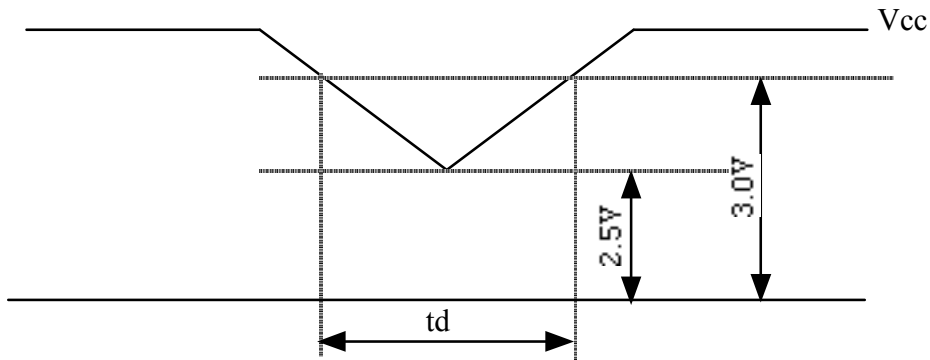
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5.2.9 V_{cc} Dip Condition

The V_{cc} dip condition is caused by the gate driver IC initialization.

(1) $2.5V \leq V_{cc} < 3.0V$, $T_d \leq 20$ ms;

(2) For $V_{cc} < 2.5V$, V_{cc} should follow the power on-off sequence defined in 5.2.7.



5.3 Backlight Subsystem

5.3.3 General Information

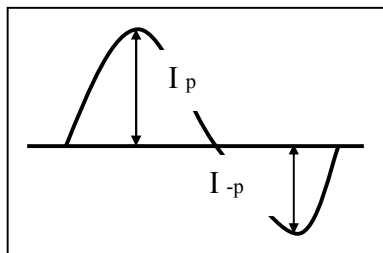
Bulb Manufacturer	NEC
Bulb Manufacturer Assembly P/N	CFL57E280285Y375F4U20
Length (mm)	374.6 ± 1.0
Outside Diameter (mm)	2.0
Inside Diameter (mm)	1.6
Ne:Ar	95:5
Gas Pressure (Torr)	80 ± 5
Hg Amount (mg)	1.5 min, 3.5 max

5.3.2 Backlight Electrical Characteristics

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PARAMETER	SYMBOL	VALUES			UNIT	NOTES
		Min.	Typ.	Max.		
Operating Voltage	V_{BL}	-	750 (6mA)	-	V_{RMS}	1
Operating Current	I_{BL}	2.0	6.0	6.5	mA	
Established Starting Voltage						2
at 25°C		-	-	1300	V_{RMS}	
at 0°C		-	-	1500	V_{RMS}	
Operating Frequency	f_{BL}	40	60	70	kHz	
Power Consumption	P_{BL}	-	4.3	-	W	3
Leakage Current	$I_{in} - I_{out}$			1.5	mA	4
Life Time		10,000	15,000		Hrs	5
				-		

- Notes: (1) The variance of the voltage is $\pm 10\%$;
- (2) The transformer output voltage in the inverter must be higher due to the loss of the ballast capacitor in the inverter;
- (3) The lamp power consumption shown above does not include loss of external inverter;
- (4) The lamp leakage current is measured by the current difference between in and out, whereas the output current is set at 6.0 mA;
- (5) The lifetime is determined by the time at which brightness of lamp is 50% compare to that of the initial value at the typical lamp current.
- (6) Requirements for the system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.
- The unbalance rate of the inverter waveform should be 10% below;
 - The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;
 - The ideal sine wave form shall be symmetric in positive and negative polarities.



* Unbalance rate:

$$|I_p - I_{-p}| / I_{rms} * 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$

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5.3.3 Lamp Connector

The backlight interface connector is BHSR-02VS-1, manufactured by JST. The mating connector part number is SM02B-BHSS-1 or equivalent. The pin configuration for the connector is shown in the table below.

Pin	Symbol	Description	Color
1	HV	High voltage input	Pink
2	LV	Low voltage input	White

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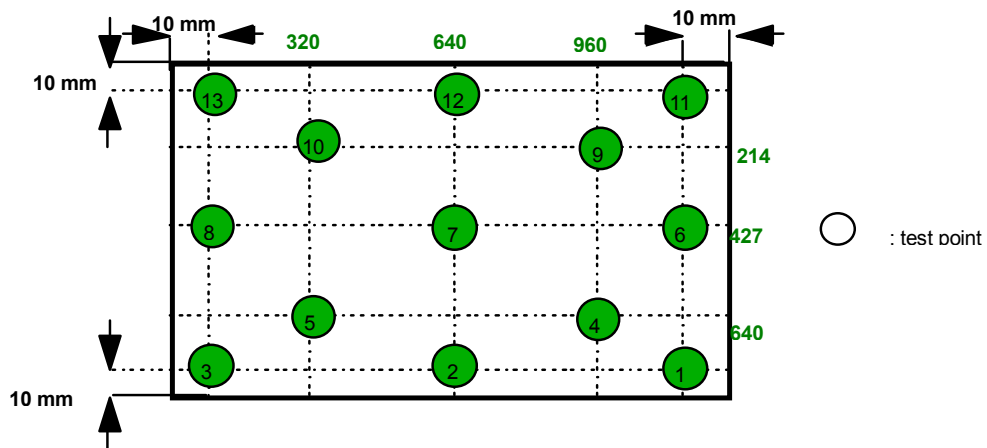
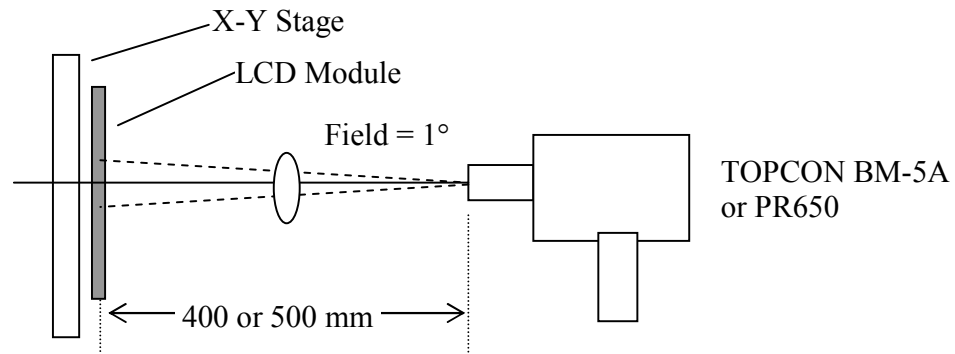
Title: **Spec, Elec., Dspl., LG 17" W TFT-LCD, Q41/Q41a Project**

DWG Number: **062-9499** Rev. **A**

6 OPTICAL REQUIREMENTS

6.1 Measuring Conditions

The optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes at the maximum brightness, in a dark environment at an ambient temperature at $25^{\circ}\text{C} \pm 2^{\circ}\text{C}$. The measuring distance is about 50 cm from the LCD surface at normal unless otherwise specified. The electrical conditions include $V_{cc} = 3.3\text{ V}$, $f_v = 59.94\text{ Hz}$, $f_{CLK} = 96.21\text{ MHz}$, $I_{BL} = 6.0\text{ mA}$ with 100% PWM duty cycle. The measurement spot at the center is approximately 12 mm in diameter from a distance of 400 mm by TOPCON BM-5A or 15 mm in diameter from a distance of 500 mm by PR 650. The CIE 1931 Standards will be used.



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Title: Spec, Elec., Dspl., LG 17"W TFT-LCD, O41/O41a Project

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6.2 Definition

6.2.1 Average Luminance

$$L_{Ave} = (L4 + L5 + L7 + L9 + L10) / 5,$$

where the luminance at 5 spots is measured at the front of screen on axis and at a backlight current I_{BL} of 5 mA.

6.2.2 Luminance Uniformity

$$\delta L/L = L_{max}/L_{min},$$

where, $L_{max} = \max \{\text{Luminance values at 13 points}\}$,

$L_{min} = \min \{\text{Luminance values at 13 points}\}$

L_{Ave} = Average Luminance as measured in Section 6.2.1.

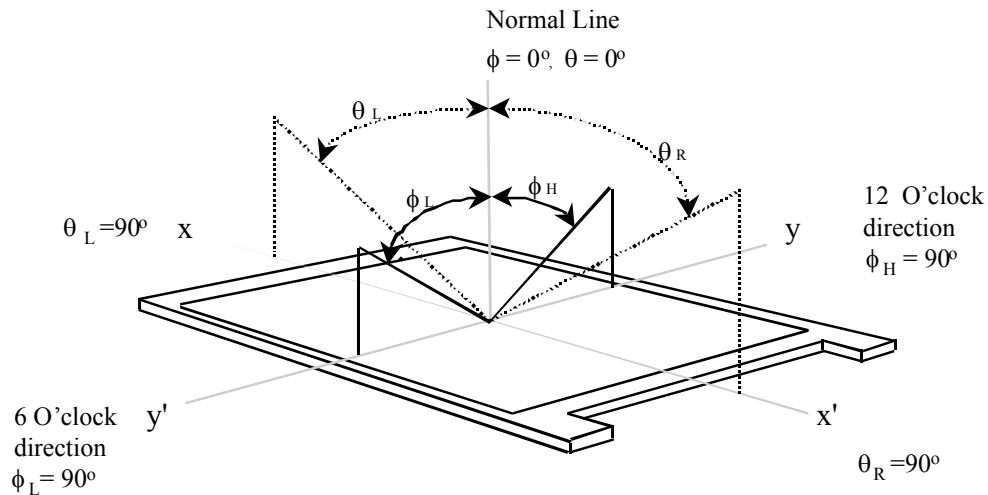
6.2.3 Contrast Ratio

$CR = \text{Luminance at } G_{max} / \text{Luminance at } G_{min}$

$$CR_{Ave} = [CR(4) + CR(5) + CR(7) + CR(9) + CR(10)] / 5$$

6.2.4 Viewing Angle

The viewing angle is defined as the viewing angle range under the condition at $CR \geq 10:1$.



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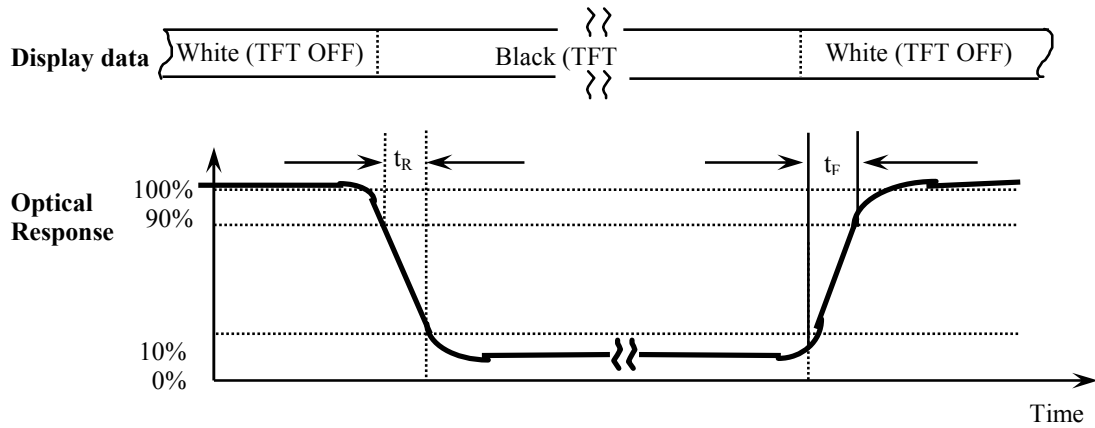
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Title: Spec, Elec., Dspl., LG 17"W TFT-LCD, O41/O41a Project

DWG Number: 062-9499 Rev. A

6.2.5 Response Time

The response time, $t_R + t_F$, is defined in the following figure and shall be measured by switching the input signal for “black” and “white”.



6.2.6 Chromaticity & White Balance

The color coordinates and white balance should be measured at G_{max} brightness level in CIE 1931 Standards. The tolerance should be within 0.030.

6.2.7 Gray Scale Linearity or Gamma Value

The display luminance, L_G , is measured at the different gray scales, G_{min}, \dots, G_{max} . The exponential fitting is used to determine the gamma (γ) value, which should be an intrinsic or uncorrected characteristic.

$$L_G \sim G^\gamma.$$

6.2.8 Flicker

No visual flicker will be allowed. The flicker level should be measured with either vertical stripes or a checker pattern, defined in Sec. 5.3.6. The output signal of a photometer is sent to an FFT analyzer. The flicker is essentially a ratio of the powers in the frequency spectrum at 30 Hz (P_x) and 0 Hz (P_0), *i.e.*,

$$F = 10 \text{ Log } (P_x / P_0).$$

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6.2.9 Cross-talk

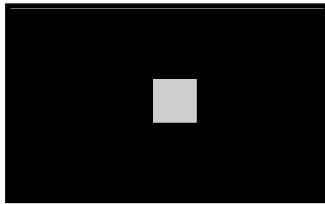
No visual cross-talk will be allowed. Two luminance values are measured at center spot with 50 x 50 pixels. The cross-talk, D_{SHA} , is defined as,

$$D_{SHA} = (L_B - L_A)/L_B \cdot 100\%,$$

Where, L_A = Luminance in Pattern A

L_B = Luminance in Pattern B.

Pattern A



Pattern A
Gray Scale = 31 in center
Black in surrounding area

Pattern B



Pattern B
Gray Scale = 31 full screen

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6.3 Optical Specifications

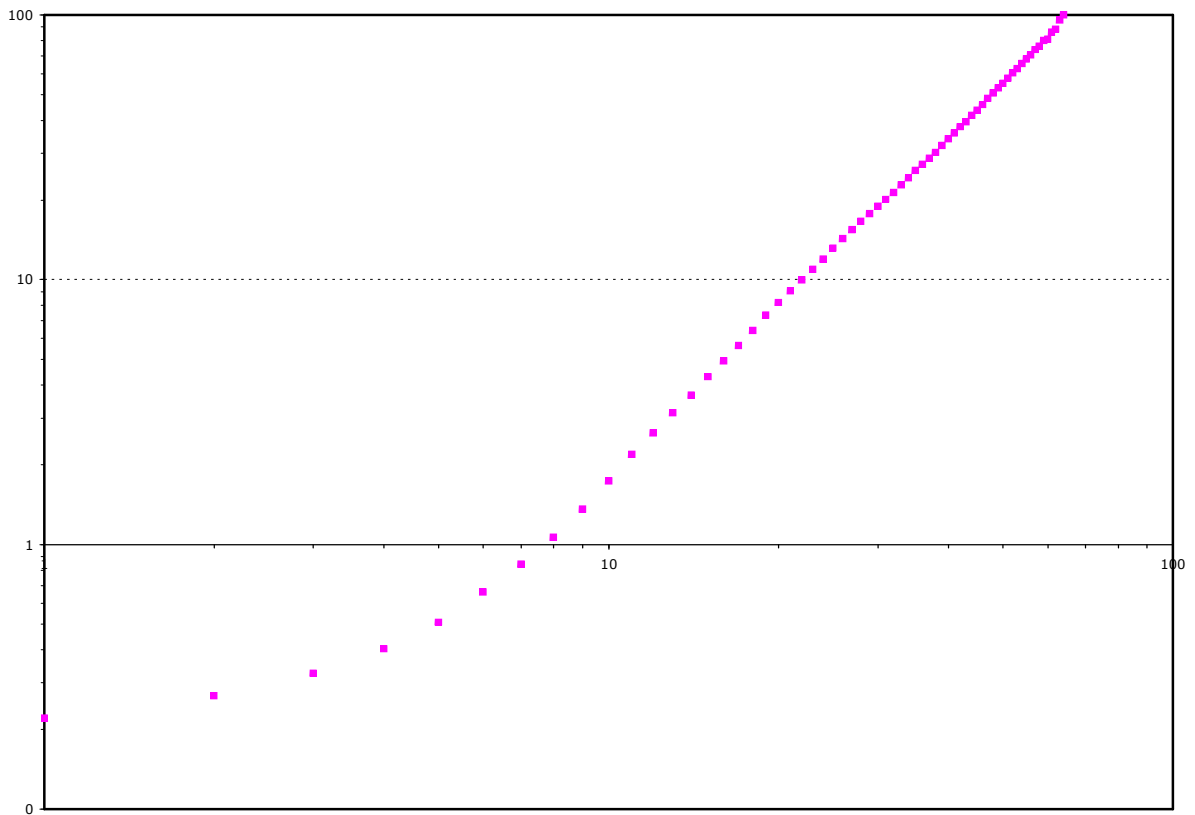
ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Average Luminance	L_{Ave}	140	160		nits	Cd/cm ²
Lum. Non-Unifomity	$\delta L/L$			1.7	%	
Contrast Ratio	CR	200	350		-	
Viewing Angle						
Horizontal	θ_L	60	65		¼	
	θ_R	60	65		¼	
Vertical	ϕ_H	45	50		¼	
	ϕ_L	55	60		¼	
Response Time						
Rising	t_R		8	10	m sec	
Falling	t_F		23	30	m sec	
Chromaticity						
Red	x	0.580	0.610	0.640	-	
	y	0.310	0.340	0.370	-	
Green	x	0.285	0.315	0.345	-	
	y	0.520	0.550	0.580	-	
Blue	x	0.115	0.145	0.175	-	
	y	0.085	0.115	0.145	-	
White	x	0.290	0.320	0.350	-	
	y	0.300	0.330	0.360	-	
Gray Scale	γ		2.2		-	1
Flicker	F			-30	dB	
Cross-talk	D_{SHA}			4.0	%	

Note: (1) Gray scale linearity should have the following typical curve.

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A Typical Gamma Curve



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7 ENVIRONMENTAL

The display modules shall meet all functional and cosmetic specifications after testing to the environmental quality standards listed in this section. Additionally, the LCD modules in Apple's products shall pass all the system testing requirements listed in the end of this document.

7.1 Shock and Vibration

7.1.1 There will be no functional or cosmetic defects following a shock to all 6 sides delivering at least 200 G in a half sine pulse no longer than 2 ms to the display module, secured by its designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.

7.1.1.1 There will be no functional defects following a shock delivering at least 260 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays. The displays are secured by designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.

7.1.2 There will be no functional or cosmetic defects following a shock delivering at least 60 G in a pulse 11 msec or longer to the display module, secured by its designated mounting details, in accordance with MIL-STD-202F Method 213B, test condition A.

7.1.3 There shall be no functional or cosmetic defects following a vibration test, conducted at 1.5 G from 5–150 Hz, 0.37 Oct/min with sine wave for 30 min./axis, with the display secured by its designated mounting details, and conducted in accordance with MIL-STD-202F, method 201A.

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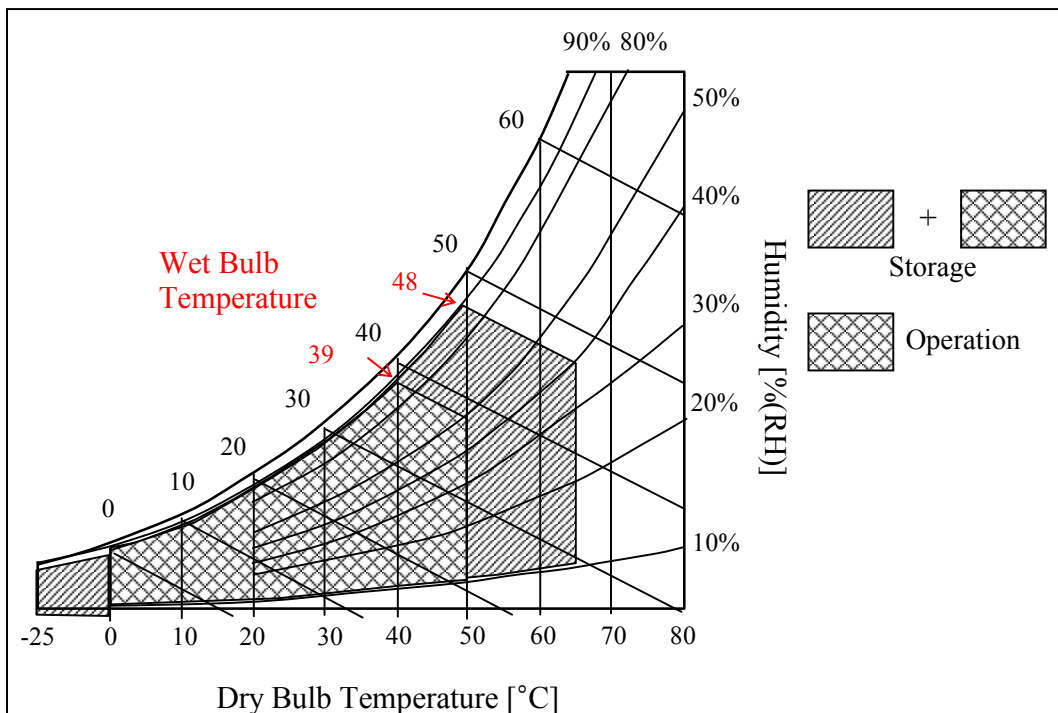
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7.2 Temperature and Humidity

Unless otherwise stated in this specification, the display module must meet functional and cosmetic requirements after testing in accordance with Apple Spec. # 080-0859, non-operating and operating conditions.

For these tests, the following limits set forth in Specification #080-0859 shall be altered to read.

7.2.1 General Performance Requirements



Note:

- 1) Maximum wet bulb temp operating temperature is 39°C.
- 2) Maximum wet bulb temp storage temperature is 48°C.

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7.2.2 Non-operational Testing

7.2.2.1 Low Temperature

-25°C @ 500 hrs

7.2.2.2 High Temperature

65°C @ 500 hrs

7.2.2.3 High Temperature and High Humidity

60°C @ 500 hrs, R.H. = 75% ± 10%

7.2.2.4 Thermal Shock

Cycle display from -25°C to 65°C with 5-minute transfer time,
100 cycles at -25°C/65°C/-25°C.

7.2.3 Operational Testing

7.2.3.1 Low Temperature

0°C for 500 hours

7.2.3.2 High Temperature

50°C for 500 hours

7.2.3.3 High Temperature and High Humidity

50°C and 90% R.H. for 240 hours (Functional Check)
Maximum wet-bulb temperature at 39°C or lower without
condensation.

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7.2.3.4 Four Corner Test (72 hrs – operating)

40°C @ 10% RH

40°C @ 90% RH

10°C @ 10% RH

10°C @ 90% RH

7.3 Special Process Temperature (Non-operational)

The display front metal shall be able to take a special process at 75°C up to 60 seconds and under a pressure up to 2 kg/cm². The panel shall have a flatness of 0.3 mm max.

7.4 Altitude

72 hour storage

Operational: 15,000 Ft.

Non-Operational: 40,000 Ft.

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8 RELIABILITY

8.1 Resistance to Normal Abuse

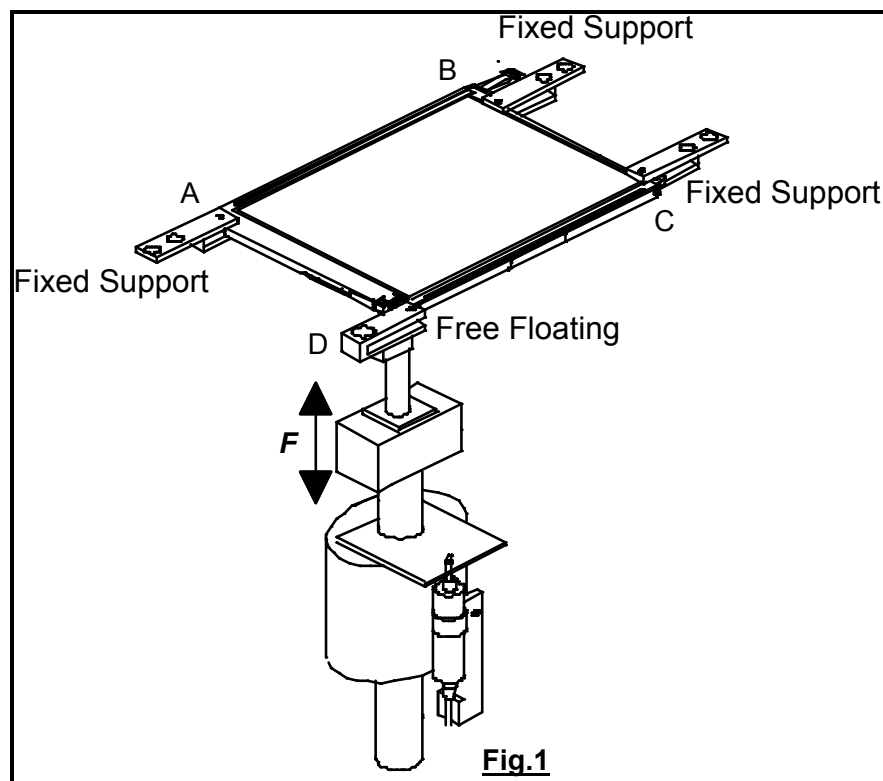
8.1.1 Torsion Test

Module is fixed by 3 mounting holes (A,B,C) on stable supports. Tester is connected to mounting hole on free floating module corner. Push/Pull test is conducted on all four corners.

8.1.1.1 Test Conditions:

Applied Force	20 N
Cycles	10 K
Frequency (F=push / pull)	1 Hz (1 cycle / sec.)

8.1.1.2 Test Set-up



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8.1.2 Static Load Deflection and Breakage

Supplier shall demonstrate compliance per Apple Specification 062-2208 Static Breakage Test

8.2 Electrostatic Discharge (ESD)

Display modules are to be tested for ESD susceptibility per Apple specification 062-0302. The display modules must meet the Level 1 for the bare module, and Level 1 through III test requirements stated in the above referenced specification, when assembled in a portable computer.

8.3 MTBF

Supplier to demonstrate display module meets minimum 50,000 Hrs.@90% Confidence Supplier to include any acceleration factors included in the calculations. Power cycling frequency during this test is to be approved by Apple.

8.4 Bulb Start Test

10000 cycles @ 0°C. (30 seconds on, 30 seconds off, the inspection shall be performed at room temperature.)

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9 COSMETIC REQUIREMENTS

The LCD module must meet Apple Cosmetic Specification over the entire viewing cone.

17" Wide XGA+ TFT-LCD Display Cosmetic Specification, 062-9511.

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10 REGULATORY

10.1 Product Safety (Environmental, Ergonomics, Safety and Health)

Materials: The vendor is to provide Apple, upon request, specific chemical composition information or certifications necessary for the product to enter countries, markets, and/or for component(s) material identification, or for Apple to respond to customer requests for information. The information may be in the form of, but is not limited to, Material Safety Data Sheets, material specification sheets, health hazard information, certifications, or other forms of documentation.

10.2 Material Content

This product's components, parts, and packaging shall be manufactured or assembled based upon the following requirements.

10.2.1 Chlorinated solvents, CFCs (chlorofluorocarbons), HCFCs (hydrochlorofluorocarbons), and ODCs (Ozone-depleting substances) shall not be used in the manufacture or assembly of the flat panel display. This includes compounds listed in annex A, B, and C of the "Montreal Protocol on Substances that Deplete the Ozone Layer."

The vendor shall provide a written statement that the flat panel display, supplied to Apple, does not contain or will not be manufactured with any chlorinated solvents, CFCs, HCFCs, and Ozone-depleting Chemicals

10.2.2 For the production of the flat panel display, substances may not be used which are listed in German TRGS 905 or 900 or in the German MAK list.

The vendor shall provide a written statement that the flat panel display, supplied to Apple, does not contain any substances listed in the German TRGS 905 and 900 as being carcinogenic category 3, or in the German MAK lists under MAK III A1, A2, or MAK IIIB.

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10.2.3 Plastics used in the flat panel display shall not contain PVC (poly vinyl chloride), PBBs (polybrominated biphenyls), PBDE (polybrominated diphenyl ethers), chlorinated paraffins, cadmium (Cd) additives, lead (Pb) additives, or flame-retardants classified by any country as carcinogenic, mutagenic, or teratogenic.

The vendor shall provide a written statement that the flat panel display, supplied to Apple, does not contain PVC (poly vinyl chloride), PBBs (polybrominated biphenyls), PBDEs (polybrominated diphenyl ethers), chlorinated paraffins, cadmium (Cd) additives, lead (Pb) additives, or flame-retardants classified by any country as carcinogenic, mutagenic, or teratogenic.

10.2.4 No Cadmium (Cd) may be found in the display.

The vendor shall provide a written statement that the flat panel display, supplied to Apple, does not contain any cadmium (Cd).

10.2.5 No Mercury (Hg) may be found in the display, with the exception of mercury used in the backlight. The backlight must be modular in design so that it may be easily separated from the rest of the flat panel without the use of any special tools.

The vendor shall provide a written statement that the flat panel display, supplied to Apple, does not contain any mercury (Hg), except for the mercury in the flat-panel display backlight. Also, that the backlight is modular in design so that it can be easily separated from the rest of the flat panel without the use of any special tools.

10.3 Recyclability

10.3.1 Flat panel display must be modular in design so that parts can be easily separated, without any special tools, for ease of proper recycling/disposal at the product's end-of-life.

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The vendor shall provide a written statement that the flat panel display, supplied to Apple is modular in design so that parts can be easily separated without any special tools, for ease of proper recycling/disposal at the product's end-of-life.

10.3.2 Flat panel display plastic parts >25 grams must be marked according to ISO 11469 (except for the LGP (light guide panel) and optical films in the backlight).

The vendor shall provide a written statement that the flat panel display, supplied to Apple, has all plastic parts >25 grams, marked according to ISO 11469 (except for the LGP (light guide panel) and optical films in the backlight).

10.4 Product Safety Certification For Flat Panel Display Assembly

10.4.1 Safety Agency Submittals:

10.4.2 The vendor shall submit their flat panel display to a Nationally Recognized Test Laboratory (NRTL, i.e. UL or CSA) at the earliest possible design stage for test and evaluation in accordance with United States standard UL 60950 (latest edition) and Canadian Standard CSA C22.2 No. 60950 (latest edition).

10.4.3 The US/Canadian Nationally Recognized Test Laboratory shall test the flat panel display sub-assembly and issue a US and Canadian safety report. The report shall clearly reference the model number for the flat panel display.

10.4.4 A copy of the US/Canadian Nationally Recognized Test Laboratory safety report shall be provided to Apple Product Safety at the earliest possible date prior to production. Delivery of these documents is expected at least one month before product ramp.

10.4.5 The vendor shall be responsible for resubmitting the flat panel display to the US/Canadian Nationally Recognized Test Laboratory if safety critical changes are made to the flat panel display materials or construction. All US/Canadian safety report revisions shall be delivered to the Apple Project coordinator and Apple Product Safety.

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10.4.6 The flat panel display shall be marked with an agency label with the following content:

10.4.6.1 Display Model number

10.4.6.2 Manufacturer's name or agency file number

10.4.6.3 UL or CSA US/Canadian Combination Mark

10.5 **Materials Construction for Flat Panel Display Assembly**

10.5.2 General: The flat panel display sub-assembly will be evaluated in the end product against the requirements of IEC 60950 (Safety of Information Technology Equipment) and all country deviations listed in the latest IECEE CB Bulletin. This sub-assembly is required to comply with the appropriate and applicable sub-clauses of this safety standard, and not impede the end product's compliance to this standard.

10.5.3 Plastic materials, films, structural plastics and foams: All flammable materials shall be UL Recognized or CSA certified component materials that comply with UL 94 "Tests for Flammability of Plastic Materials for Parts in Devices and Appliances" with a minimum flame rating at the specified wall thickness of V-2 or better; HF-2 or better.

10.5.4 Printed Circuit Boards: All printed circuit board shall be UL Recognized or CSA certified component materials that comply with UL 94 "Tests for Flammability of Plastic Materials for Parts in Devices and Appliances" with a minimum flame rating of V-1.

10.5.5 Connectors: All connectors shall be UL Recognized or CSA certified component materials that comply with UL 94 "Tests for Flammability of Plastic Materials for Parts in Devices and Appliances" with a minimum flame rating of V-2.

10.5.6 Low Voltage Wiring: All wiring shall be UL Recognized or CSA certified component Appliance Wiring Material (AWM) that complies with UL 758

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“Standard for Appliance Wiring Material” with a with a flame rating of VW-1. Wiring shall be protected from cutting, abrasion and crushing.

10.5.7 High Voltage Wiring: All high voltage wiring to the display lamps shall be UL Recognized or CSA certified component Appliance Wiring Material (AWM) that complies with UL 758 “Standard for Appliance Wiring Material” with a minimum voltage rating of 1.5 kV and a flame rating of VW-1. Wiring shall be protected from cutting, abrasion and crushing.

10.5.8 Rated Operating Temperature: Unless otherwise specified, the flat panel display sub-assembly and all components shall be rated for a 50°C ambient temperature.

10.5.9 Copies of applicable Material Safety Data Sheet (MSDS) per US OSHA requirements or other specific chemical information necessary to enter countries, markets, or for component material identification shall be supplied to Apple by the supplier before DVT.

10.6 Ergonomics

10.6.1 The flat panel display must comply with the ergonomic requirements of ISO 13406 parts 1 and 2.

The vendor shall provide a written statement that the flat panel display, supplied to Apple, is certified to comply with ISO 13406, parts 1 and 2.

10.7 Electromagnetic Compatibility (EMC)

10.7.1 Emissions

The final product must meet Apple Class B Emission Standards for home electronic device when configured within a system per Apple Spec. #062-0088. The display supplier must provide all necessary support as required to meet this requirement.

EMI measurements are taken at the worst-case contrast setting.

10.7.2 Susceptibility

Performance degradation due to external noise or RF will be considered as specified in #062-0088 for Class B products.

10.7.3 Spectrum Spreading Compatibility (SSC)

10.7.3.1 Emissions

The final product must be compatible with spectrum spreading conditions specified in 10.7.4 of this document. No failure or degradation in electronic functionality and optical performance is allowed with the spreading turned ON compared to that when it is turned OFF.

10.7.3.2 Conditions for Spectrum Spreading

Spreading %: 0 (min), 1.5 (typical), 2.0 (max)

Spreading type: down

Modulation Rate: 40 to 80 kHz.

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11 FACTORY/SERVICE REQUIREMENTS

11.1 SQBR

Factory requirements are outlined in Supplier Quality and Business Requirements, Apple specification 070-1191.

11.6 SERVICE REQUIREMENTS

Apple Service Requirements are outlined in Apple specification 070-0385.

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12 REFERENCE DOCUMENTS

NUMBER	TITLE
062-9511	17" Wide XGA+ TFT-LCD Cosmetic Specification
080-0855	Drop, Shock and Vibration
080-0854	Four-Corner Temperature and Humidity Test
062-0087	Packaging Finished Goods Shock and Vibration
062-0718	EMI Standards
062-0302	ESD Standards
062-2082	Vendor Packaging Procedure
062-0585	FG Labeling Specification
062-2111	Manufacturing Bar Code Specification
062-2208	Static Breakage Test
070-0371	Service: Packaging Standard
070-0385	Service: Product Quality Requirements
070-1191	Supplier Quality and Business Requirement
070-1193	Barcode Label Specification
074-0321	ESD Anti-static Label Specification
13406-2.3	ISO Specification
062-0093	Apple Corporate Specification, Mandatory Requirements for Product Safety
IEC60950	Safety of Information Technology Equipment (International Standard)
EN 60950	Safety of Information Technology Equipment (European Standard based on IEC 60950)
UL 1950	Safety of Information Technology Equipment. Third Edition (US Standard based on IEC 60950) C22.2 No. 950 Safety of Information Technology Equipment. Third Edition (Canadian Standard based on IEC 60950)
UL 94	Tests for Flammability of Plastic Materials for Parts in Devices and Appliances (UL standard for flame testing plastics. Includes test requirements for HB, V-2, V-1 and V-0 flame ratings)
JIS K 5401	Pencil Scratch Tester for Coated Film 13406-2.3

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