DATA SHEET

NEC

COLOR PDP MODULE

NP50C1MF01

127 cm (50 inches), Wide screen (1365 × 768 Pixels)
8-bit RGB signal

CosmoPlasma

DESCRIPTION

The NP50C1MF01 is a 50-inch wide color plasma display module with a resolution of 1365(H) × 768 (V) pixels. The display offers vibrant colors we reproduced in a thin and low profile package. This device uses AC plasma technology by NEC and includes an 8-bit digital video signal interface for each RGB color.

FEATURES

- Peak luminance of 450 cd/m^2 (typical value) and contrast ratio of 650:1 (typical value) are achieved through a new deriving method, which offers extremely vivid image with good contrast.
- CCF (Applied Capsulated Color Filter) technology, developed at NEC, which offers a high quality image match for CRT display. To offer remarkably pure colors, the color plasma display panel uses extremely clear, thin capsulated color filters to cut unnecessary light as the plasma discharges.
- Advanced-PLE (Applied Advanced Peak Luminance Enhancement) function that enables the display to operate with the ideal contrast. The PLE function makes it possible to automatically adjust the average luminance level of the PDP display in accordance with the average luminance level of an input video signal.

APPLICATIONS

- Wide Screen TV (aspect ratio 16:9)
- Public Information Displays
- Video Conference Systems
- Retail store decoration and displays
- Education and Training Systems

The information in this document is subject to change without notice.

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STRUCTURE AND PRINCIPLE OPERATION OF PLASMA DISPLAY

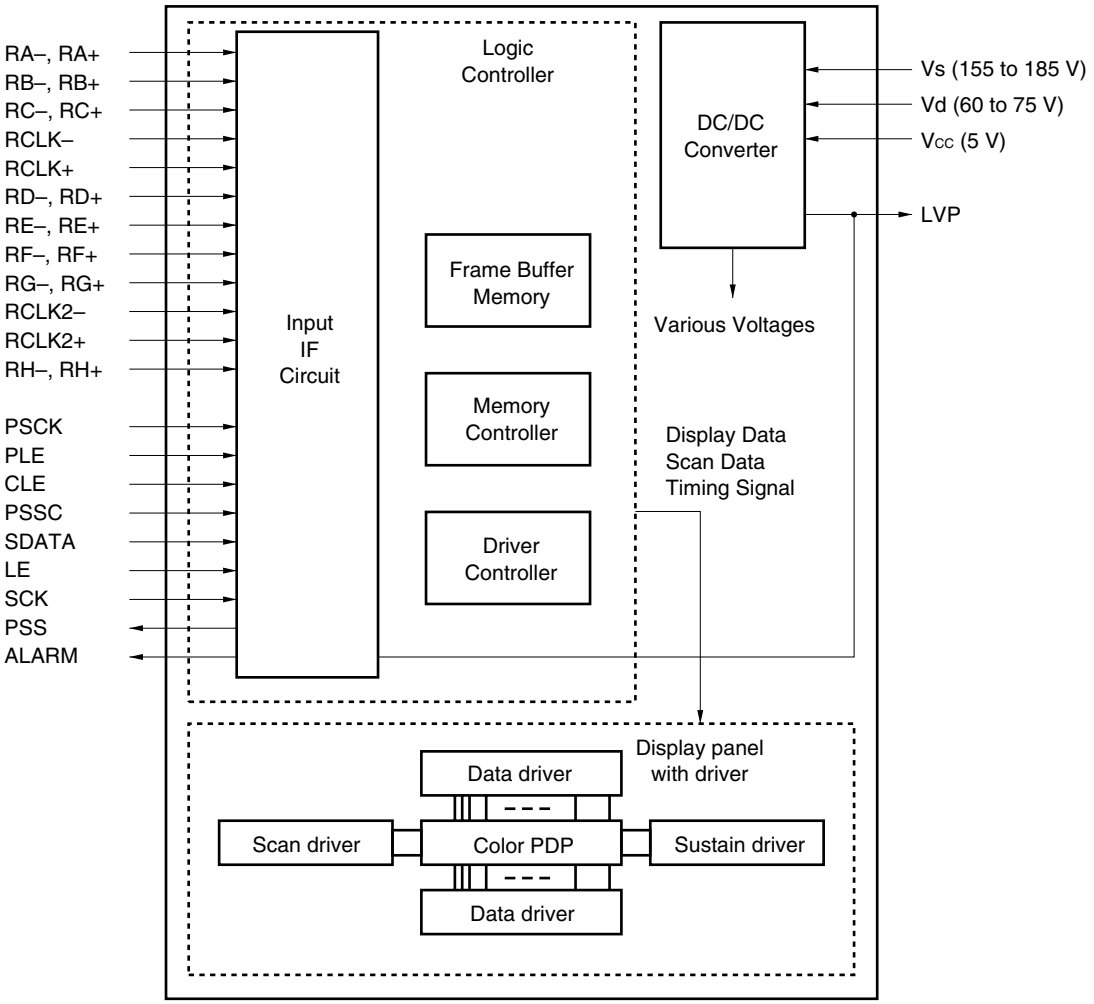
In a Plasma Display Panel, Row and Column electrodes are placed between two glass substrates. A rare gas is then filled between each substrate. When a high voltage is applied to these electrodes, the gas is activated resulting in the radiation of ultraviolet light, similar to the operation in fluorescent lamps. These ultraviolet rays then activate the phosphor that has been coated on the inside of the glass substrate, and visible light is emitted from the panel.

ELECTRICAL INTERFACE OF PLASMA DISPLAY

NP50C1MF01 requires 8-bits digital video signals for each RGB color. For the signal inputs, serial interface (LVDS video signal) is prepared in the module. In addition to the video signals, synchronous signals, mode control signals and 3 kinds of DC sources are required to operate the display.

This PDP module has a "Advanced-PLE" (Advanced Peak Luminance Enhancement) function that adjusts the luminance and contrast to the suitable value in accordance with the input video signal level variance, so that images can be displayed with the ideal luminance and contrast.

BASIC CONFIGURATION



GENERAL SPECIFICATION

Display area	1106(H) × 622(V) mm
Outline dimensions	1191(W) × 714(H) × 48(D) mm
Weight	24 kg
Aspect ratio	16:9
Number of pixels	1365(H) × 768(V) (1pixel = 3 RGB cells)
Pixel pitch	0.81 (H) × 0.81(V) mm
Color arrangement	RGB vertical stripes
Number of gradations	Video 60Hz mode: 8bits (256 steps) / 7bits (128 steps) Video 50Hz mode: 7bits (128 steps) PC mode: 8bits (256 steps)
Peak luminance	450cd/m^2 typical (Video signal*, 0.5% white window, PLE** mode set to the maximum)

* Signal of EDTV mode: fv = 59.94 Hz and fh = 31.47 kHz

** See PLE (Peak Luminance Enhancement) description.

OPERATION ENVIRONMENTAL CONDITIONS

Temperature	0 to 60°C (with forced-air cooling)
Humidity	20 to 80% R.H. (without condensation)
Atmospheric pressure	800 to 1100 hPa

STORAGE ENVIRONMENTAL CONDITIONS

Temperature	–20 to 60°C
Humidity	10 to 90% R.H. (without condensation)
Atmospheric pressure	700 to 1100 hPa

MECHANICAL TEST CONDITIONS

Vibration (operating)	4.9m/s^2 (0.5 G), 10 to 100 Hz, 3 directions, 10 minutes each
Vibration (non-operating)	4.9m/s^2 (0.5 G), 10 to 100 Hz, 3 directions, 2 hours each

LIFE EXPECTANCY

More than 10,000 hours of continuous operations

(Time when the luminance decreased to half to the initial at full white display and internal PLE operation)

POWER INPUT AND OUTPUT

1) Sustain Power Supply

Table 1. Sustain Power Supply

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	– – –	– – –	– – –	– – –	200	V
Voltage	Vs	Dependent on the characteristics of each PDP **(Note 1)**	155	– – –	185	V
Voltage Stability	– – –	– – –	– – –	– – –	±1.0	%
Average Current **(Note 2)**	Is-a	Under normal PLE operation	0.1	– – –	3.0	A
Peak Current	Is-peak	Duty:1/8, Cycle:60 to 75Hz	– – –	– – –	21	A
Voltage Regulation	– – –	At peak current	– – –	– – –	5	V
Ripple and Noise	– – –	– – –	– – –	– – –	500	mVp-p

Note 1: Voltage should be set to a specified value, which is located on a label attached to the module.

Note 2: Average current that include rippled current

2) Data Power Supply

Table 2. Data Power Supply

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	– – –	– – –	– – –	– – –	90	V
Voltage	Vd	Dependent on the characteristics of each PDP **(Note 1)**	60	– – –	75	V
Voltage Stability	– – –	– – –	– – –	– – –	±1.5	%
Average Current **(Note 2)**	Id-a	Varied correspondence to the Image	0.4	– – –	1.5	A
Peak Current	Id-peak	– – –	– – –	– – –	2.5	A
Ripple and Noise	– – –	– – –	– – –	– – –	300	mVp-p

Note 1: Voltage should be set to a specified value, which is located on a label attached to the module.

Note 2: Average current that include rippled current.

3) Logic Power Supply (Vcc)

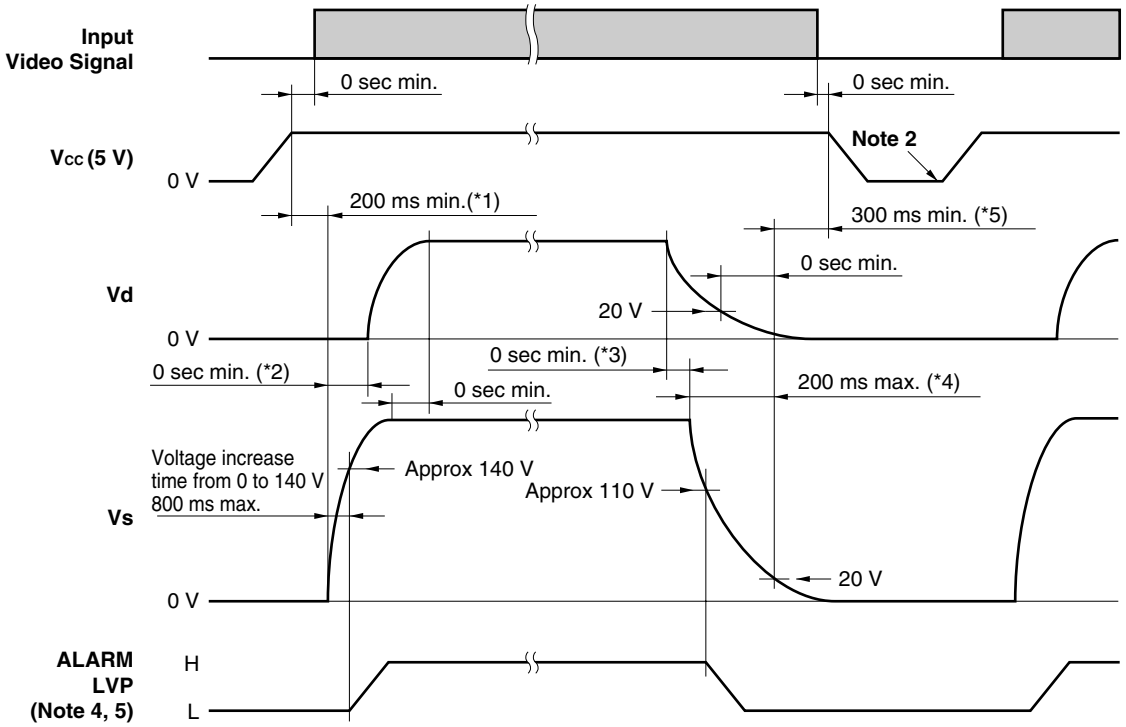
Table 3. Logic Power Supply (Vcc)

Item	Symbol	Condition and Remarks	Min.	Typ.	Max.	Unit
Absolute Maximum	– – –	– – –	4.5	– – –	6.0	V
Voltage Range	Vcc	– – –	4.75	5.0	5.25	V
Current **(Note 1)**	Icc	– – –	– – –	– – –	6.0	A
Peak Current	Icc-peak	– – –	– – –	– – –	7.0	A
Ripple	– – –	– – –	– – –	– – –	30	mVp-p
Noise	– – –	– – –	– – –	– – –	300	mVp-p

Note 1: Average of rippled current.

This module provides an automatic operation-stop function for internal malfunctions. When the module stops the operation, logic current may reduce to almost zero (0). Even if logic current becomes zero, applied voltage should be kept to less than 6.0 volts.

SUPPLY VOLTAGE AND SIGNAL SEQUENCE



Note 1: Power ON/OFF sequence is as follows (refer to the above sequence diagram):

Power ON sequence:

Vcc ON → 200ms min.(*1) → Vs ON → 0sec min. (*2) → Vd ON

Power OFF sequence:

Vd OFF → 0sec min. (*3) → Vs OFF → 200ms max.(*4) → 300ms min.(*5) → Vcc OFF

(Caution)

If power sequence does not meet to above sequence diagram, PDP drivers may have a permanent damage.

In order to decrease Vs and Vd voltages quickly to satisfy above sequence diagram, forced discharge circuits are essential in the power supply.

Note 2: Re-start (Power ON again) should be done after Vcc is reduced to 0.1 V or less.

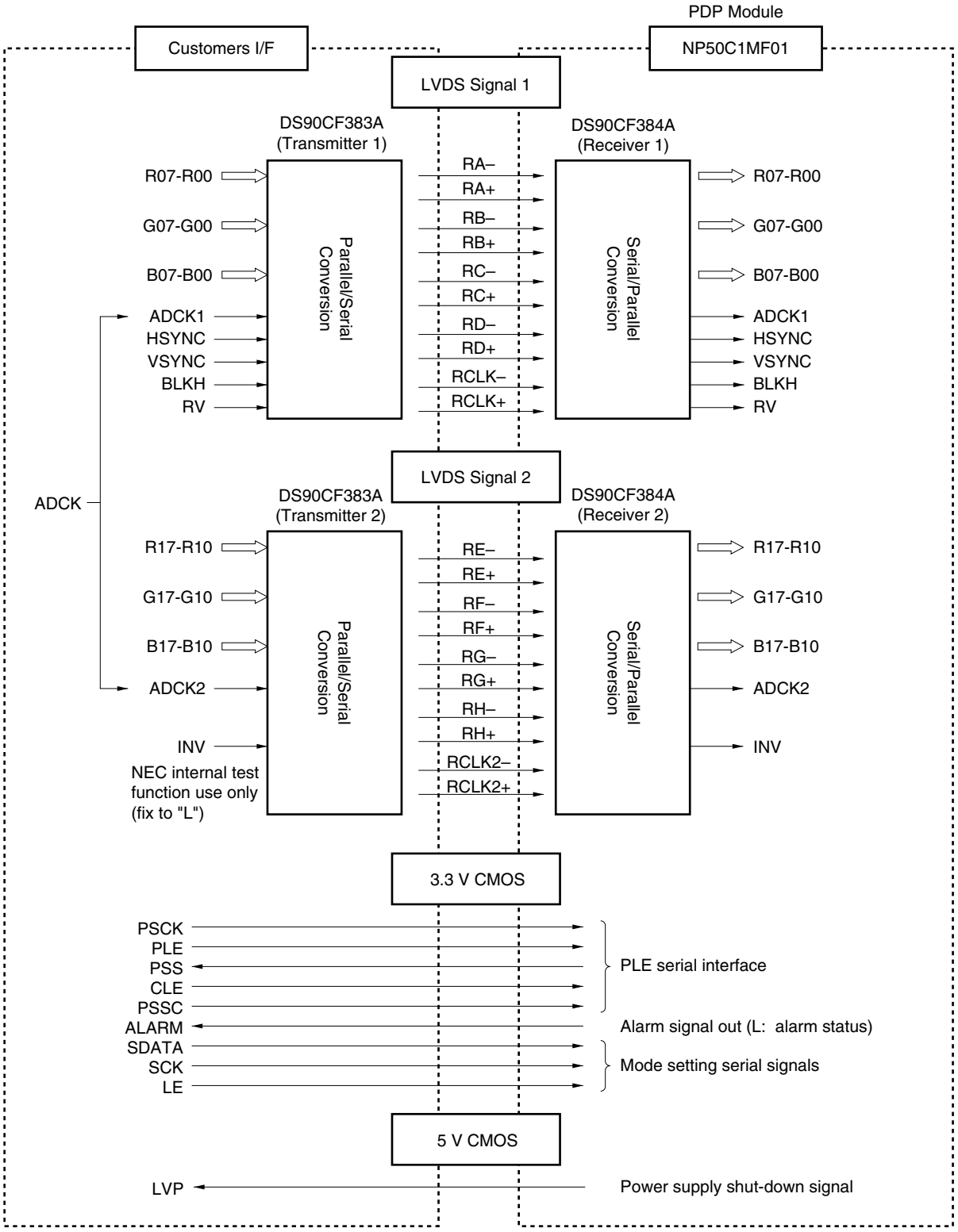
Note 3: The power source for the Input signal circuit and Vcc can be switched on and off at the same time.

Note 4: LVP is the power supply shutdown output signal when the panel is broken and/or failure of internal power source in the PDP module.

Note 5: When either ALARM or LVP signal is “L”, High voltage should be shut down. However, when Vcc is applied at first, ALARM and LVP signals are kept “L” until Vs is applied. In order to enable “high voltage power supply” operation, the initial ALARM and LVP signals’ status “L” should be disregarded.

INTERFACE SIGNAL

SERIAL INTERFACE CONFIGURATION



R07-R00, G07-G00, B07-B00: Odd pixel number data (D_1, D_3, -----,D_{n-1})
R17-R10, G17-G10, B17-B10: Even pixel number data (D_2, D_4, -----,D_n)

ELECTRICAL CHARACTERISTICS

1) Interface Signals; Absolute Ratings

Common conditions: Ta = 25°C, Vcc = 5 V

Table 4. Absolute Ratings

Item			Parameter	Symbol	Ratings	Unit
Input Signals	LVDS	RA-, RA+, RB-, RB+, RC-, RC+, RD-, RD+, RCLK-, RCLK+ RE-, RE+, RF-, RF+, RG-, RG+, RH-, RH+, RCLK2-, RCLK2+	Input Voltage	Vi	−0.3 to 3.6	V
			Input current	Ii	– – –	mA
	3.3V CMOS	PSCK, PLE, CLE, PSSC, SDATA, SCK, LE	Input Voltage	Vi	−0.5 to 4.6	V
			Input current	Ii	−15	mA
Output Signals	3.3V CMOS	PSS, ALARM,	Output Voltage	Vo	−0.5 to 3.5	V
			Output current	Io	±20	mA
	5V CMOS	LVP	Output Voltage	Vo	−0.5 to 5.5	V
			Output current	Io	±35	mA

2) Interface Signals; Electrical Characteristics

Common conditions: Ta = 25°C, Vcc = 5V

Table 5. Electrical Characteristics

Signal	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
LVDS	High Level Input Voltage	V_{TH}	V_{CM} = 1.2 V	– – –	– – –	100	mV
	Low Level Input Voltage	V_{TL}	V_{CM} = 1.2 V	−100	– – –	– – –	mV
	Input Current	I_{IN}	V_{IN} = +2.4/GND	– – –	– – –	±10	μA
3.3V CMOS	High Level Input Voltage	V_{IH}	– – –	2.0	– – –	– – –	V
	Low Level Input Voltage	V_{IL}	– – –	– – –	– – –	0.8	V
	Input Current	I_i	V_i = Vcc or GND	– – –	– – –	±5.0	μA
	High Level Output Voltage	V_{OH}	I_o = −1 mA	2.4	– – –	– – –	V
	Low Level Output Voltage	V_{OL}	I_o = 1 mA	– – –	– – –	0.4	V
5V CMOS	High Level Output Voltage	V_{OH}	I_o = −6 mA	4.18	– – –	– – –	V
	Low Level Output Voltage	V_{OL}	I_o = 6 mA	– – –	– – –	0.26	V

INPUT SIGNAL FUNCTION of LVDS TRANSMITTER (DS90CF383A)

Table 6. Interface Signal Function

Symbol	Function		(Remarks)
R07 to R00	8 bits red video signal	**(Note 1)**	(R07: MSB*,R00: LSB**)
R17 to R10	8 bits red video signal	**(Note 1)**	(R17: MSB*,R10: LSB**)
G07 to G00	8 bits green video signal	**(Note 1)**	(G07: MSB*,G00: LSB**)
G17 to G10	8 bits green video signal	**(Note 1)**	(G17: MSB*,G10: LSB**)
B07 to B00	8 bits blue video signal	**(Note 1)**	(B07: MSB*,B00: LSB**)
B17 to B10	8 bits blue video signal	**(Note 1)**	(B17: MSB*,B10: LSB**)
ADCK1,2	Clock for video signal		(latch the video signal at falling edge)
HSYNC	Horizontal synchronous signal	tw=4T_{ADCK} min.	(negative pulse)
VSYNC	Vertical synchronous signal	tw=200ns min.	(negative pulse)
BLKH	Video blanking and/or muting	**(Note 2)**	(“H” in blanking, muting)
RV	Reverse the RGB video data polarity		(Set to “L” level for normal use)
INV	NEC internal test function use only		(Fix to “L” level)

* MSB: Most Significant Bit

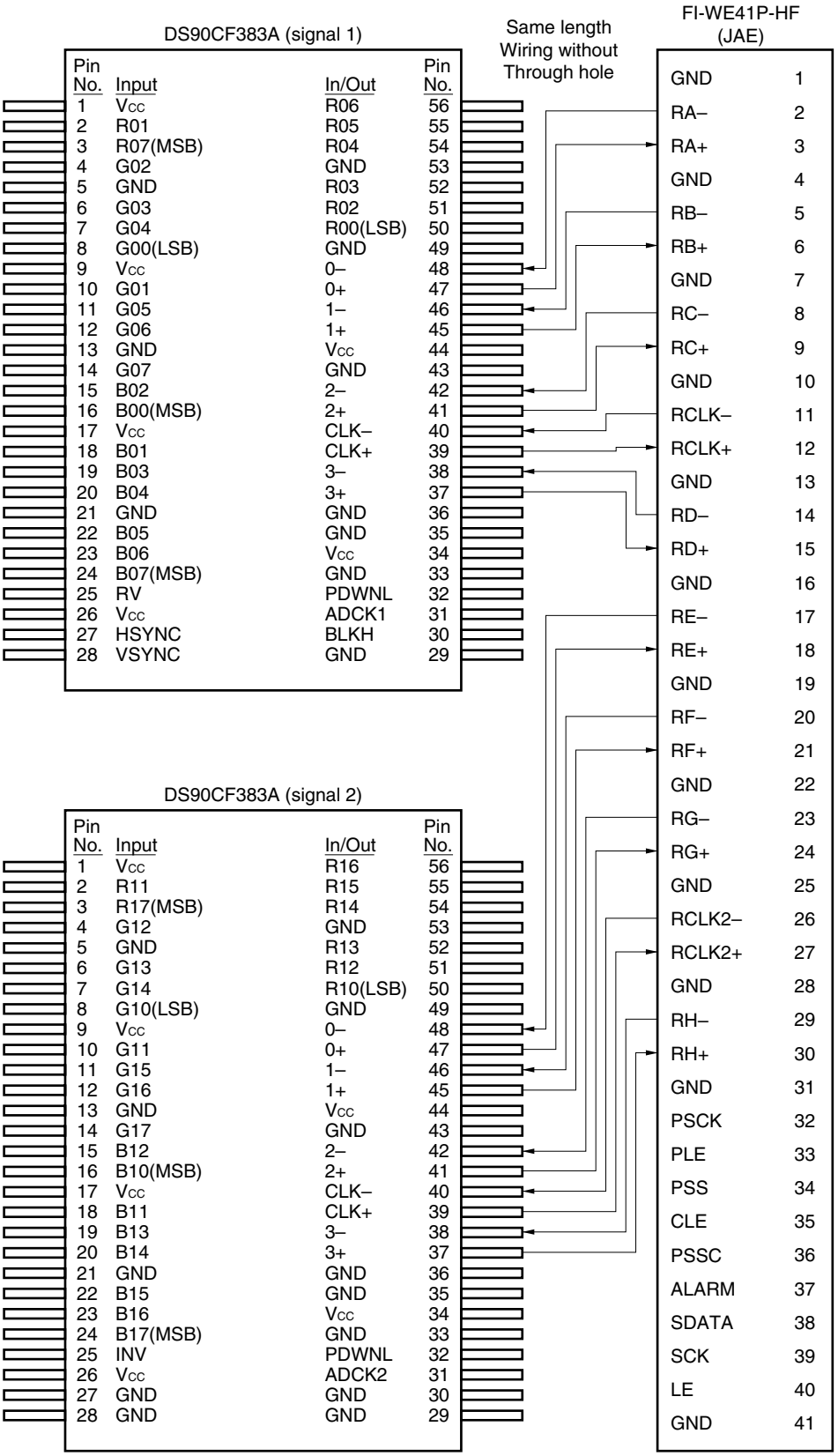
** LSB: Least Significant Bit

Note 1: The RGB video signal should be compensated with Inverse γ circuit before input to the color plasma display module.

When operate at 7bits (128steps) video data, upper 7bits (R7 to R1, G7 to G1, B7 to B1) are enable.

Note 2: While BLKH input is “H” level, all display area image turns to black color display.

PIN ASSIGNMENT OF LVDS TRANSMITTER



INPUT SIGNAL FUNCTION of PDP MODULE (NP50C1MF01)

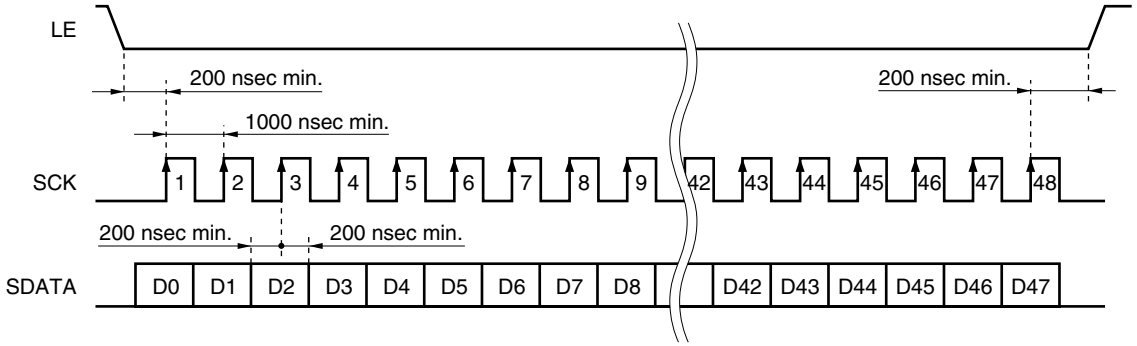
Table 7. Interface Signal Function

Symbol	I/O	Function		(Remarks)
RA–	I	Video signal input A–		LVDS signal 1
RA+	I	Video signal input A+		LVDS signal 1
RB–	I	Video signal input B–		LVDS signal 1
RB+	I	Video signal input B+		LVDS signal 1
RC–	I	Video signal input C–		LVDS signal 1
RC+	I	Video signal input C+		LVDS signal 1
RD–	I	Video signal input D–		LVDS signal 1
RD+	I	Video signal input D+		LVDS signal 1
RCLK–	I	Clock signal clock–		LVDS signal 1
RCLK+	I	Clock signal clock+		LVDS signal 1
RE–	I	Video signal input E–		LVDS signal 2
RE+	I	Video signal input E+		LVDS signal 2
RF–	I	Video signal input F–		LVDS signal 2
RF+	I	Video signal input F+		LVDS signal 2
RG–	I	Video signal input G–		LVDS signal 2
RG+	I	Video signal input G+		LVDS signal 2
RH–	I	Video signal input H–		LVDS signal 2
RH+	I	Video signal input H+		LVDS signal 2
RCLK2–	I	Clock signal clock–		LVDS signal 2
RCLK2+	I	Clock signal clock+		LVDS signal 2
SDATA	I	Mode setting serial data	(48-bit)	3.3V CMOS
SCK	I	Clock signal for SDATA		3.3V CMOS
LE	I	SDATA write enable	(“L” in SDATA write)	3.3V CMOS
PSCK **(Note 2)**	I	Clock signal for PSS, PSSC serial data		3.3V CMOS
PLE **(Note 2)**	I	PSS data read enable	(“L” in PSS data read)	3.3V CMOS
PSS **(Note 2)**	O	PLE average luminance signal	(10-bit serial)	3.3V CMOS
CLE **(Note 2)**	I	PSSC data write enable	(“L” in data write)	3.3V CMOS
PSSC **(Note 2)**	I	PLE luminance control data	(8-bit serial)	3.3V CMOS
ALARM	O	Alarm signal for panel broken and failure of internal power-source. **(Note 1)**	(“L” in alarmed status)	3.3V CMOS

Note 1: When ALARM output turns to “L” level, high voltage power input (Sustain power supply: Vs, and Data power supply: Vd) should be switched off immediately. When glass panel is broken, high voltage may occur at the electrode section and cause electric shock. Failure of internal power-source causes over-power status and gives damage to the display panel and driver-circuits.

Note 2: When use the internal PLE function, these signals become invalid. In this case, it is recommended to keep these terminals open.

SET-UP OF CONTROL MODE SIGNALS AND DISPLAY POSITION



Set-up Sequence:

1. Set LE to “L” level.
2. Enter the 48 bits of SDATA into the module synchronizing to the serial crock signal (SCK)
3. Set LE to “H” level.

Note 1: SCK clock rate: 1MHz max.

Note 2: Serial input data should be refreshed at least in every 5 or 6 seconds or less.

Note 3: Serial input data (SDATA) is latched into the module at the falling edge of the VSYNC signal after “LE” signal is returned back to “H” level. When VSYNC is overlapped with the “LE” signal’s “L” period, the serial data is latched with the next VSYNC timing.

Note 4: When only 48 SCK clocks are entered while LE is “L” level period, SDATA become enabled, If SCK clocks number is not 48, SDATA is not refreshed.

Note 5: When powers are supplied to the module, serial data in the module has vague status. Therefore serial data should be refreshed after powered on.

Mode setting signals

Table 8. Contents of SDATA (Mode setting serial input data)

SDATA	Signal name	Function	Remarks
D0	RESERVE	Spare bit	Fix to “L” level
D1	CODE 2	Selection of Video/PC mode	Refer to the Table 9
D2	CODE 1		
D3	CODE 0		
D4	RESERVE	NEC internal use	Fix to “L” level
D5	RESERVE	NEC internal use	Fix to “L” level
D6	SAFEL	NEC internal use	Fix to “L” level
D7	LIFEH	Switch for PLE luminance level	L: PLE normal operation H: Fix PLE to low luminance level for longer life operation
D8	RESERVE	Spare bit	Fix to “L” level
D9	SELFPLEH	Switch for “Internal PLE” and “External PLE”	H: Internal PLE control L: External PLE control
D10	TSELB	Switch for ADCK data latch timing	Fix to “H” level
D11	FV 2	Vertical frequency selection bits	Refer to the Table 9
D12	FV 1		
D13	FV 0		
D14	DISPLINE 2	Display line number Refer to the “DL” in the Table 10 Setting line numbers: 768	Fix to “H” level
D15	DISPLINE 1		Fix to “L” level
D16	DISPLINE 0		Fix to “H” level
D17	DISPDOT 2	Display pixel number/line Refer to the “DD” in the Table 10	Pixels 1024 1365 DD2 H H DD1 L H DD0 H H
D18	DISPDOT 1		
D19	DISPDOT 0		
D20	VDELAY 256	Display start vertical position Refer to the “Dv” in the table 10	Set the display start line numbers after the falling edge of the VSYNC. Range of setting line numbers: 0 to 511 This number should not exceed the total line numbers in one frame period (1V).
D21	VDELAY 128		
D22	VDELAY 64		
D23	VDELAY 32		
D24	VDELAY 16		
D25	VDELAY 8		
D26	VDELAY 4		
D27	VDELAY 2		
D28	VDELAY 1		
D29	HDELAY 512	Display start horizontal position Refer to the “Dh” in the table 10	Set the display start pixel numbers after the falling edge of the HSYNC. Range of setting pixels numbers: 0 to 1023 This number should not exceed the total pixel numbers in one line period (1H).
D30	HDELAY 256		
D31	HDELAY 128		
D32	HDELAY 64		
D33	HDELAY 32		
D34	HDELAY 16		
D35	HDELAY 8		
D36	HDELAY 4		
D37	HDELAY 2		
D38	HDELAY 1		
D39	HPOS 3	Setting of horizontal display position in normal mode. Display position is adjustable by 2 pixel steps.	Position Left - - - - - Center - - - - - Right POS3 L L L - - - - - H - - - - - H H H POS2 L L L - - - - - L - - - - - H H H POS1 L L H - - - - - L - - - - - L H H POS0 L H L - - - - - L - - - - - H L H
D40	HPOS 2		
D41	HPOS 1		
D42	HPOS 0		
D43	MASKLEVEL 3	Gray level in black area (Possible to set 0-24% of white level)	Level(%) Dark - Light ML2 L L L L L L L L H H H H H H H H ML1 L L L L H H H H L L L L H H H H ML0 L L H H L L H H L L H H L L H H MLL L H L H L H L H L H L H L H L H
D44	MASKLEVEL 2		
D45	MASKLEVEL 1		
D46	MASKLEVEL 0		
D47	RESERVE	Spare bit	Fix to “L” level

Table 9. Video Signal Mode setting Code								
Input Signal	Mode setting serial Data						Maximum Vertical Synchronous Freq. **(Note 1)**	Remarks
	D1	D2	D3	D11	D12	D13		
	CODE2	CODE1	CODE0	FV2	FV1	FV0		
Video 50Hz 7bits (128 steps)	H	L	H	L	L	L	54Hz	Vertical synchronous freq.: 46 to 54Hz LSB is deleted if the freq. ≥ 51Hz(approx.)
Video 50Hz 7bits (128 steps) Reduced False contour Mode	H	H	L	L	L	L	54Hz	Vertical synchronous freq.: 46 to 54Hz LSB is deleted if the freq. ≥ 51Hz(approx.) Low luminance mode with reduced false contour.
Video 60Hz 8bits (256 steps)	L	H	L	L	L	H	64Hz	Vertical synchronous freq.: 55 to 64Hz LSB is deleted if the freq. ≥ 61Hz(approx.)
Video 60Hz 7bits (128 steps)	L	H	H	L	L	H	64Hz	Vertical synchronous freq.: 55 to 64Hz LSB is deleted if the freq. ≥ 61Hz(approx.)
Video 60Hz 7bits (128 steps) Reduced False contour Mode	H	L	L	L	L	H	64Hz	Vertical synchronous freq.: 55 to 64Hz LSB is deleted if the freq. ≥ 61Hz(approx.) Low luminance mode with reduced false contour
PC 56-64Hz 8bits (256 steps)	L	L	L	L	L	H	64Hz	Low peak luminance mode for reducing Image-Sticking
PC 66Hz 8bits (256 steps)	L	L	L	L	H	L	68Hz	Low peak luminance mode for reducing Image-Sticking
PC 67-71Hz 8bits (256 steps)	L	L	L	L	H	H	71.5Hz	Low peak luminance mode for reducing Image-Sticking
PC 72-75Hz 8bits (256 steps)	L	L	L	H	L	L	76.5Hz	Low peak luminance mode for reducing Image-Sticking

Note 1: When Vertical synchronous freq is over than the above maximum freq., the module is set to low luminance mode.

EXAMPLE OF VIDEO SIGNAL INPUT AND SIGNAL TIMING

Table 10. Relation Between Input Signal and Module RGB Signal Input

		Standard Format of Video Signal					Mode Signal Data for PDP Module											
	No.	Signal Name	Display Resolution (Dot•Line)	Vertical synch-ronous Freq. (Hz)	Total number of Dot•Line	Horizontal Synchro-nous Freq. (KHz)	Display Resolution (Dot•Line)	Horizontal Synchro-nous Freq. (KHz)	Recommended dot-clock (dot-clock number in 1H period)		CODE	FV	DL	DD	VD Stand-ard (line)	HD Stand-ard (dot)	Read start timing after sync. signal	
																	Dv	Dh
Video Mode	1	EUTV	576 lines	50.00	625/2 lines	15.625	1365•768	41.67	69.3/2	(832)	5, 6	0	5	7	58	278	60	136
	2	EDTV	480 lines	59.94	525/2 lines	15.734	1365•768	50.35	83.8/2	(832)	2,3,4	1	5	7	52	252	54	123
	3	1035 I (HiVision)	1035 lines	60.00	2200•1125/2	33.75	1365•768	50.63	80.03/2	(791)	2,3,4	1	5	7	58	174	60	84
	4	1080 i	1920•1080	60.00/ 59.94	2200•1125/2	33.75 / 33.72	1365•768	50.61	83.51/2	(825)	2,3,4	1	5	7	28	182	30	88
PC Mode	5	VESA	1024•768	60.00	1344•806	48.36	1024•768	48.36	65.0/2	(672)	0	1	5	5	33	302	35	148
							1365•768	48.36	86.7/2	(896)	0	1	5	7	33	400	35	197
	6	EWS/L	1024•768	60.08	1344•806	48.36	1024•768	48.36	65.0/2	(672)	0	1	5	5	32	286	34	140
							1365•768	48.36	86.7/2	(896)	0	1	5	7	32	378	34	186
	7	VESA	1024•768	70.07	1328•806	56.48	1024•768	56.48	75.0/2	(664)	0	3	5	5	33	286	35	140
							1365•768	56.48	100.0/2	(886)	0	3	5	7	33	378	35	186
	8	VESA	1024•768	75.03	1312•800	60.02	1024•768	60.02	78.75/2	(656)	0	4	5	5	29	278	31	136
							1365•768	60.02	105.0/2	(875)	0	4	5	7	29	368	31	181
	9	MAC	1024•768	75.00	1328•803	60.24	1024•768	60.24	80.0/2	(664)	0	4	5	5	31	278	33	136
							1365•768	60.24	106.7/2	(886)	0	4	5	7	31	368	33	181

Note 1: Maximum data clock (ADCK) frequency is 57MHz.

Note 2: Maximum horizontal frequency in Video mode is 54 kHz

Note 3: Maximum horizontal frequency in PC mode is 65 kHz

Note 4: Digital picture data should be applied to the module correctly according to the display pixel number. This module reads every 2 pixels digital picture data simultaneously in parallel. Therefore, clock frequency is half of the sampling frequency in analog-digital video data conversion..

Note 5: Above mode signal (CODE, FV, DL, DD, VD, HD, Dh, Dv) described in decimal notation should be set in binary notation.

Note 6: In case of EUTV, EDTV, 1035i and 1080i signals, progressive signal should be applied to the module after scan conversion according to the display pixel numbers.

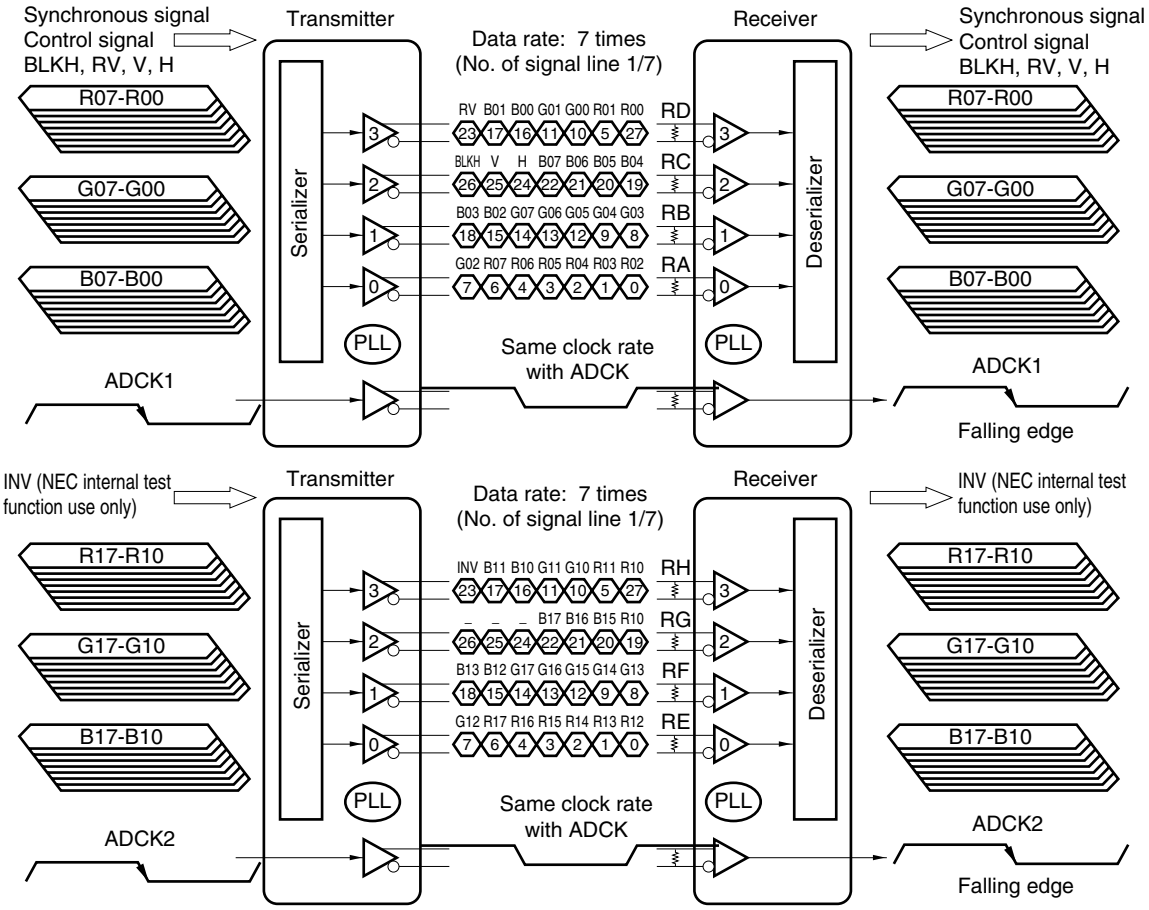
Note 7: In case PC-XGA mode (1024 X 768: DD set to “5”) is selected, horizontal display position is set to the center of the screen and both sides become blank.

Note 8: First video data on each horizontal line should correspond to LVDS signal 1.

Note 9: D11 to D19 (Vertical freq., Display lines number and Display pixel number/line) of serial input data should be set correctly according to the display data. If not done correctly, PLE function is not operated correctly.

Note10: In case input signal format is smaller than XGA / Wide-XGA format, input signal data should be applied to the module after converting to the XGA / Wide-XGA format.

LVDS DATA TRANSFER FORMAT



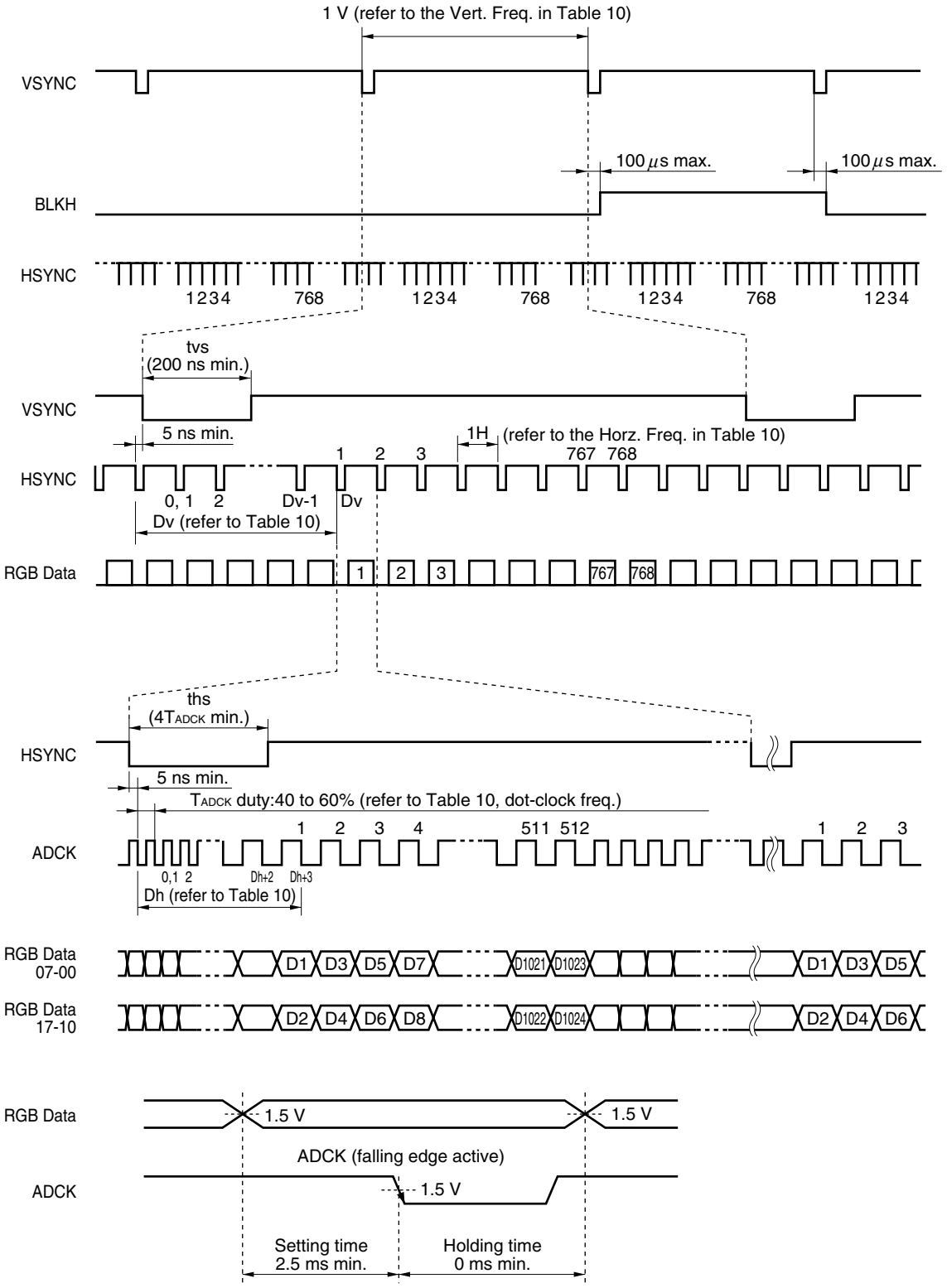
(As for detail of LVDS interface, please refer to www.national.com.)

SIGNAL TIMING

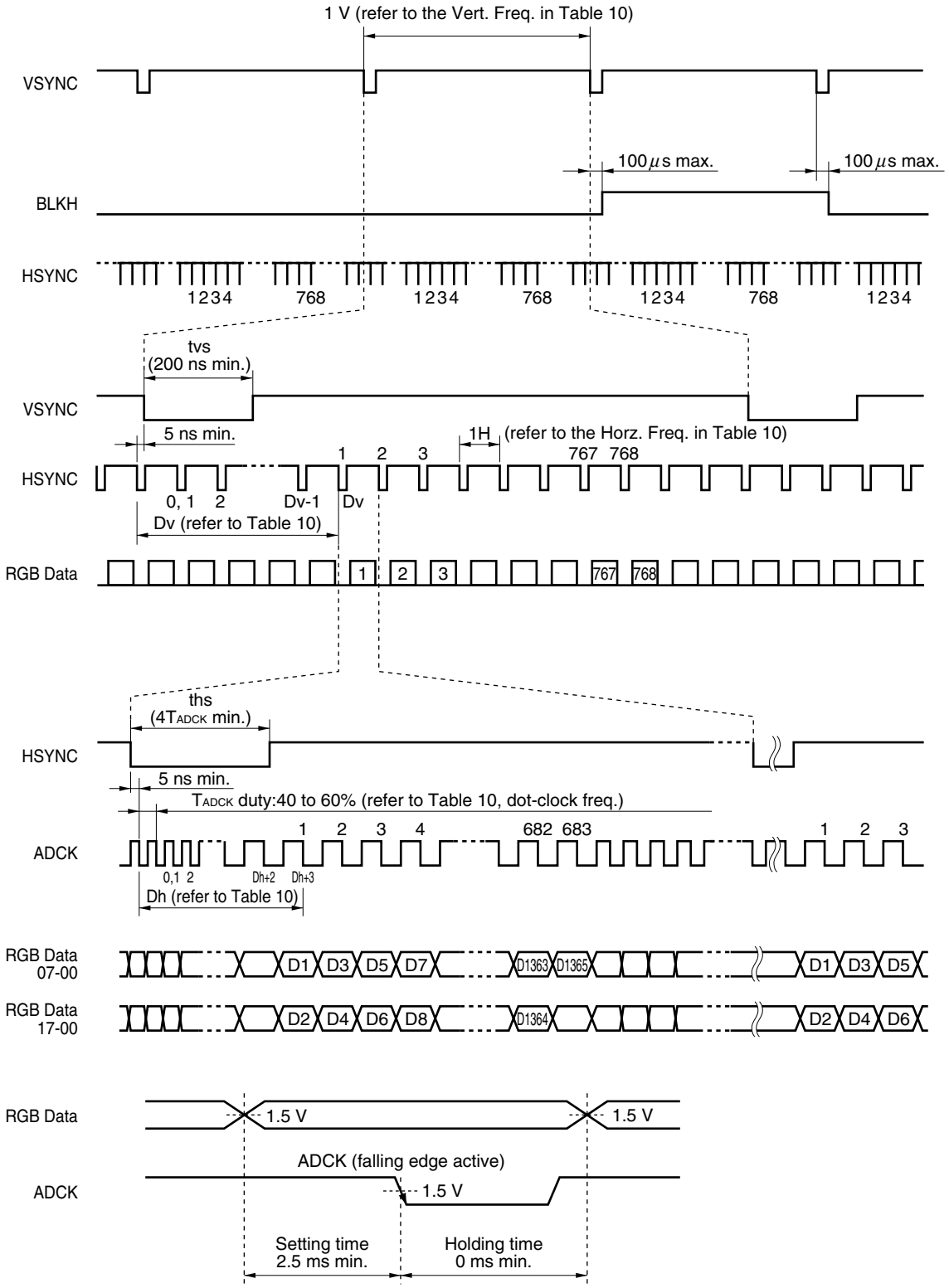
Refer to the timing diagram on the following pages.

- Input video signal format is determined by Mode signal (refer to Table 9)
- "T_{ADCK}" shows 1 cycle period of ADCK.
- "tvs" shows negative pulse width of VSYNC.
- "tvh" shows negative pulse width of HSYNC.
- "1H" shows 1 cycle period of HSYNC (Horizontal Synchronous Signal).
- "1V" shows 1 cycle period of VSYNC (Vertical Synchronous Signal).
- "Dv" is a period between "leading-edge of the vertical synchronous pulses" and " valid RGB lines data read start timing "
- "Dh" is a period between "leading-edge of the horizontal synchronous pulse" and " valid RGB dots data read start timing "
- In case of normal mode (1024 dot mode) is selected, both sides are masked with gray patterns.

TIMING DIAGRAM (XGA Mode)

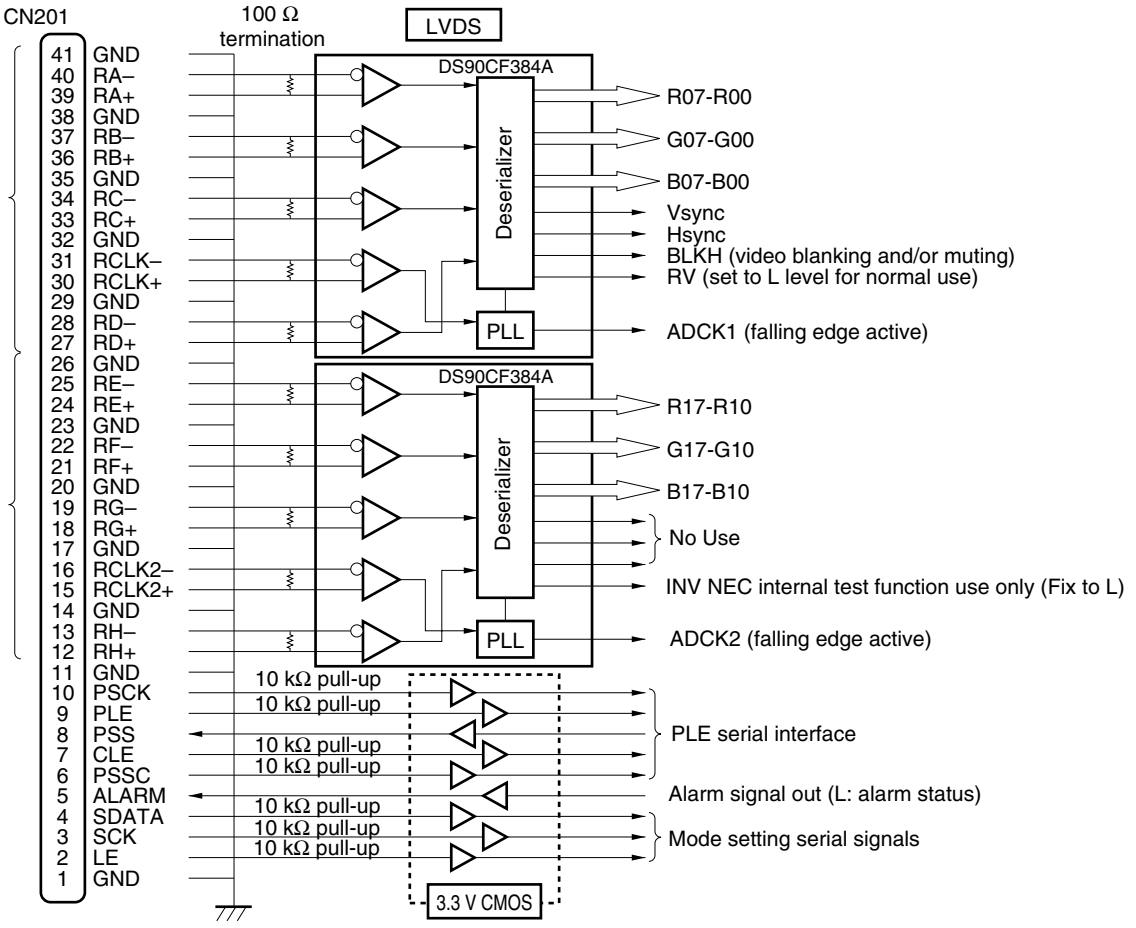


TIMING DIAGRAM (Wide XGA Mode)



INTERFACE CONNECTOR PIN ASSIGNMENT AND INPUT OUTPUT CIRCUITS

- Following shows the interface connector pin assingnment and input output circuits in the PDP module.

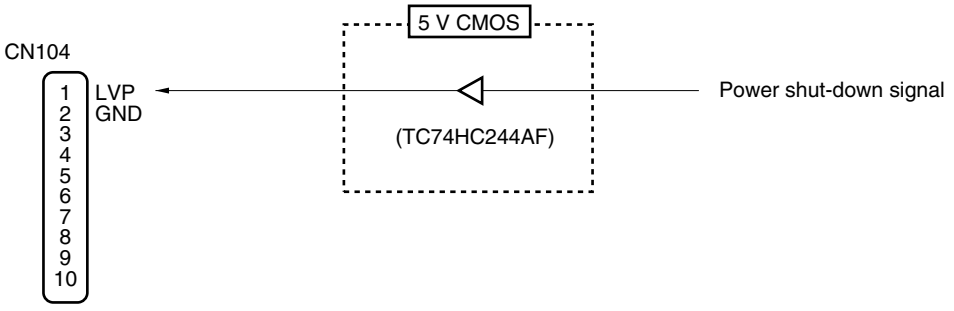


Type of serial interface connector

Module side connector:	FI-WE41P-HF
Mating connector:	FI-W41S (plug housing)
	FI-C3-A1-15000 (contact)
Connector supplier:	Japan Aviation Electronics Industry, Limited (JAE)
Fitting cable:	AWG#28 to 32 twist pair cable

(Total cable assembly is recommend to be shielded)

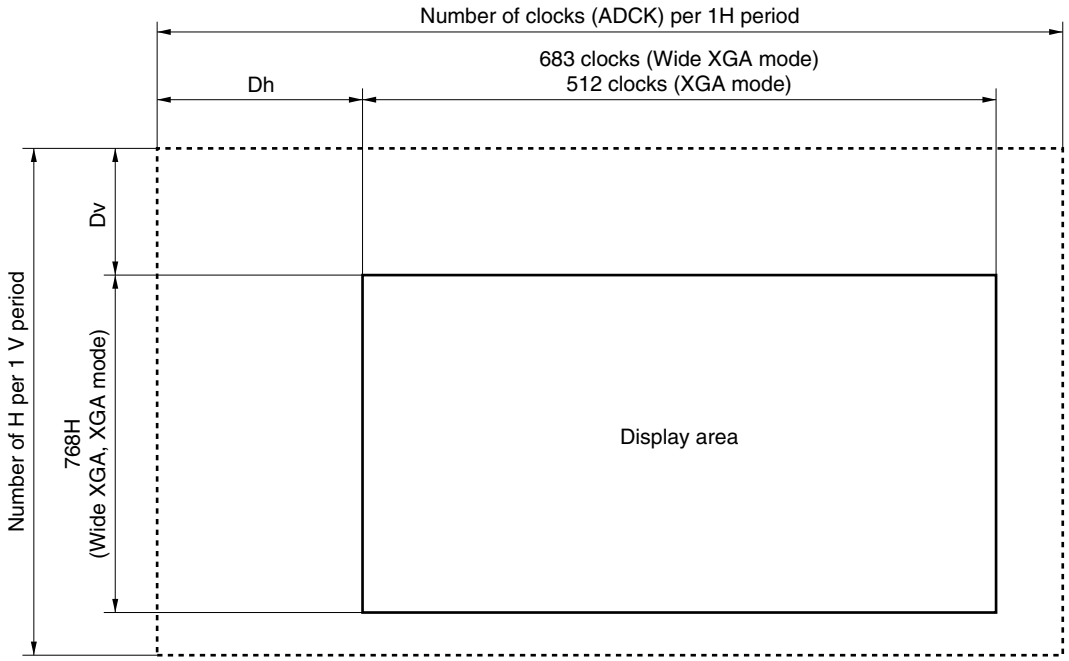
- Following shows the power input connector pin assignment and input output circuits in the PDP module.



Note: Regarding the connector specification, please refer to “CONNECTOR PIN ASSIGNMENT”.

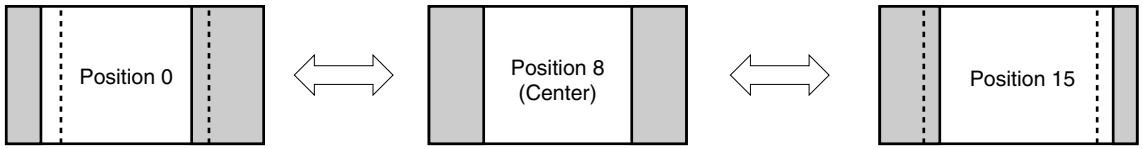
DISPLAY POSITION

The relation among Dv, Dh, and the display position is as shown below.



1) Setting range of Dv and Dh
   Dv: 9bit 0 to 511 line (HSYNC)
   Dh: 10bit 0-Number of clocks per 1H-period –1 (Max.1023) pixel (ADCK)
2) Limitation of number of clocks per 1H period
   normal mode: 2+512 ≤ Number of clocks per 1H period ≤ 3071
   full mode: 2+683 ≤ Number of clocks per 1H period ≤ 3071
3) Limitation of number of HSYNC pulses per 1V period
   2+768 ≤ Number of HSYNC pulses per 1V period ≤ 2047 (HSYNC)

Display horizontal position setting

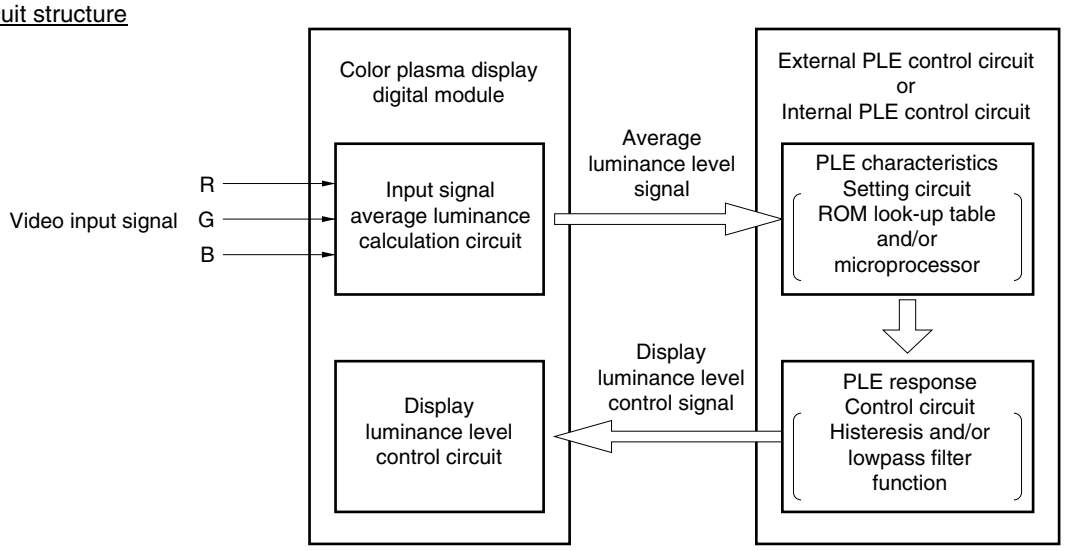


16 positions can be set by 2-poxel pitch through "Mode setting serial data".

PLE (Peak Luminance Enhancement) FUNCTION

The PLE function makes it possible to increase the luminance level of the PDP display when the average luminance level of the input video signal is low. This PLE function reduces the maximum power by absorbing the luminance when the high-power-load-image is displayed, and results in a higher contrast level.

PLE circuit structure



This plasma display module has following two modes. These two modes can be selected by the mode control signal.

1. “Internal PLE” mode – – – Built-in PLE function in the PDP module itself. This PLE mode realizes one of the best PLE characteristics without any additional circuit. Therefore this mode is very convenient, and it is recommend to utilized this function actively.

2. “External PLE” mode – – – Externally controlled PLE function from the customer’s interface circuit. External PLE mode enables to make customer’s original characteristics within the limitation range. The PLE characteristics is strongly related not only the luminance characteristics of plasma display module but also to the power consumption and the generated heat, therefore it is required to obtain the acknowledgement of NEC concerning the external PLE characteristics to be set at the customer.

(Caution)
When use the external PLE function, please use within the limitation range. If external PLE characteristic is set outside of the limitation range, plasma display module may have damage.
Any trouble caused by this incorrect operation is not included in the warranty

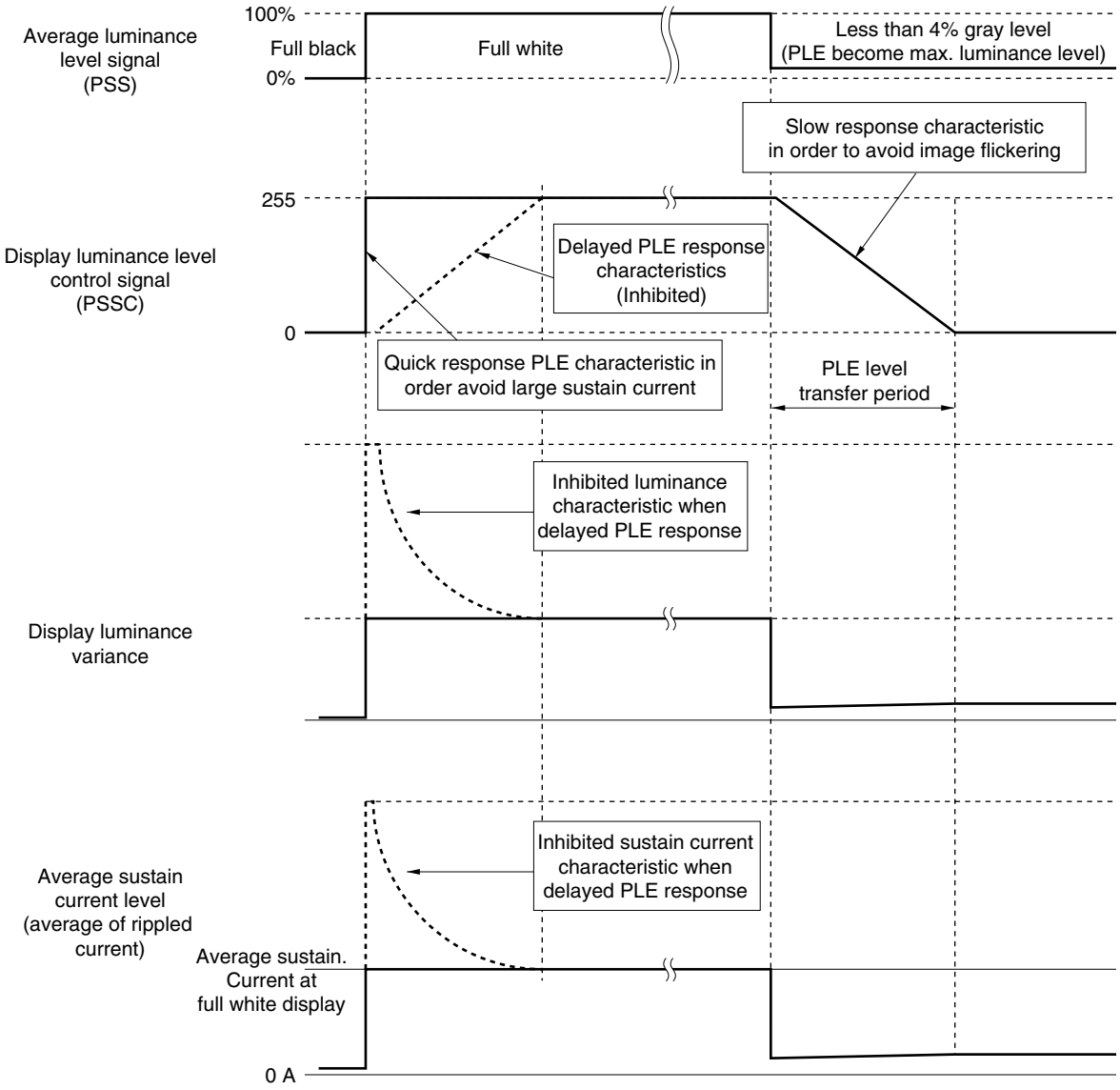
Power consumption and generated heat of plasma display module varies depending on the setting values of PLE characteristic. Therefore the temperature investigation and optimization of cooling design should be done in the state mounted in the plasma display set.

CHARACTERISTICS OF INTERNAL PLE

When PDP module displays full white with maximum luminance, or when PLE characteristic has some delayed response and display image is changed from full black to full white, large sustain current flows, and plasma display becomes over power status.

In the internal PLE function, when the ”Average luminance level” increases, in order to avoid large sustain current flow and over power status, the “Display luminance level” is immediately reduced to the setting level with quick response. And when display load decreases, in order to avoid image flickering caused by the short-term average luminance level’s fluctuations, the “Display luminance level” is gradually move to the setting level with a slow response characteristic.

(Refer to the following figures)



CONNECTORS PIN ASSIGNMENT

(For the connector position, please refer to the Rear View in the Outline Drawing)

1. POWER INPUT CONNECTORS

Table 11. Connector CN104 Pin Assignment

Pin No.	Symbol	Pin No.	Symbol
1	LVP	2	GND
3	GND	4	Vcc
5	GND	6	GND
7	Vd	8	N.C.
9	Vs	10	Vs

N.C. : non-connection pin.
Module side connector : B10PS-VH
Mating connector : VHR-10N (housing),
SVH-21T-P1.1(contact)
Connector supplier : J.S.T. TRADING COMPANY., LTD.
Fitting Cable : Equivalent to AWG#20

Table 12. Connector CN105 Pin Assignment

Pin No.	Symbol	Pin No.	Symbol
1	Vs	2	Vs
3	N.C.	4	Vd
5	GND	6	GND
7	Vcc	8	GND
9	GND	– – –	– – –

N.C. : non-connection pin.
Module side connector : B9PS-VH
Mating connector : VHR-9N (housing),
SVH-21T-P1.1 (contact)
Connector supplier : J.S.T. TRADING COMPANY, LTD.
Fitting Cable : Equivalent to AWG#20

(Note): If using a long cable, applied voltage may be dropped because of its resistance.
Specified voltage should be applied correctly at the input of the module side connector.

2. SIGNAL INTERFACE CONNECTOR

Serial mode inter-face connector (LVDS, 3.3V CMOS)

Table 13. Connector CN101 Pin Assignment

Pin No.	Symbol	Pin No.	Symbol
1	GND	2	LE
3	SCK	4	SDATA
5	ALARM	6	PSSC **(Note 1)**
7	CLE **(Note 1)**	8	PSS **(Note 1)**
9	PLE **(Note 1)**	10	PSCK **(Note 1)**
11	GND	12	RH+
13	RH–	14	GND
15	RCLK2+	16	RCLK2–
17	GND	18	RG+
19	RG–	20	GND
21	RF+	22	RF–
23	GND	24	RE+
25	RE–	26	GND
27	RD+	28	RD–
29	GND	30	RCLK+
31	RCLK–	32	GND
33	RC+	34	RC–
35	GND	36	RB+
37	RB–	38	GND
39	RA+	40	RA–
41	GND	– – –	– – –

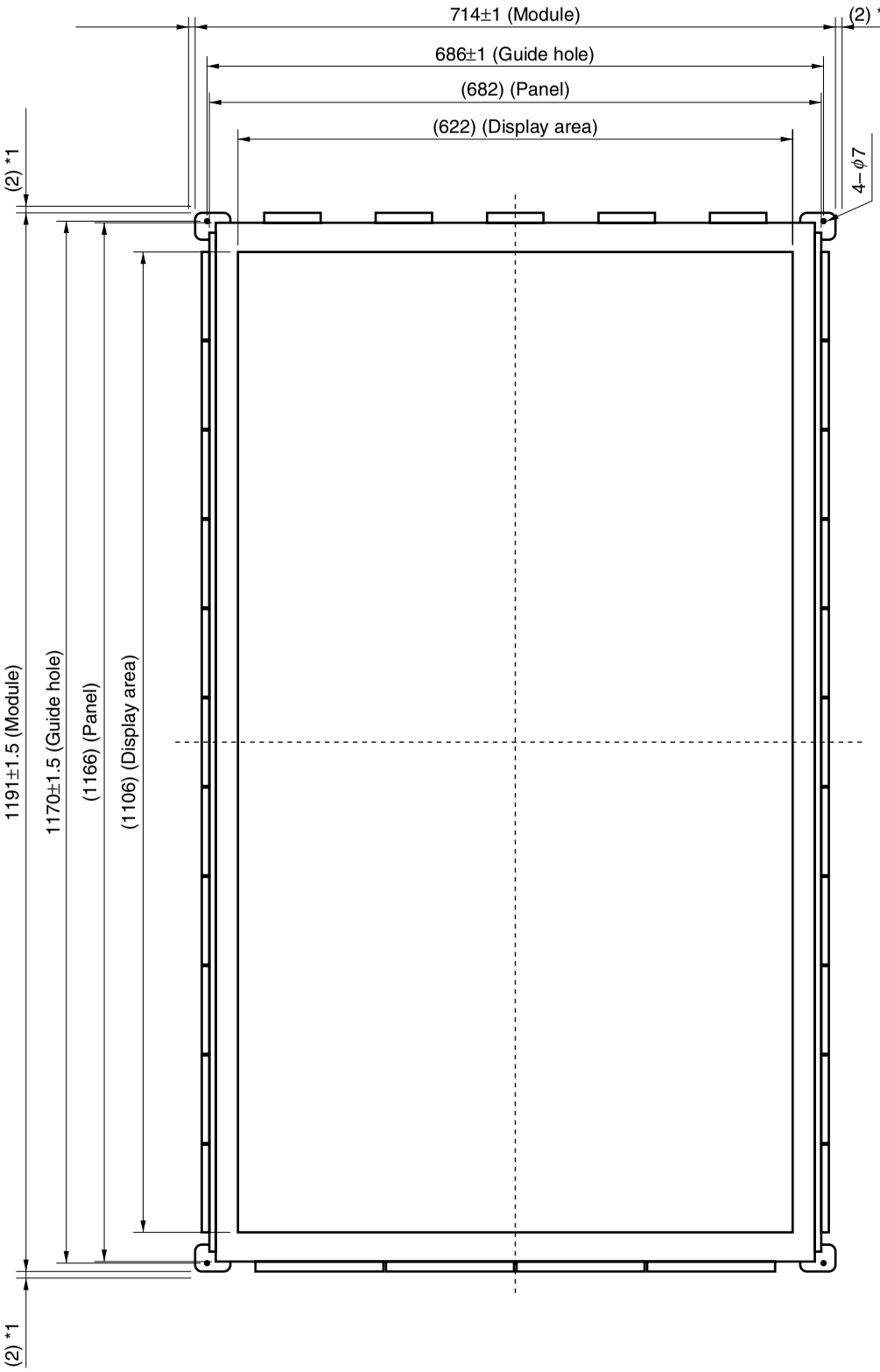
Module side connector:	FI-WE41P-HF
Mating connector:	FI-W41S (housing),
	FI-C3-A1-15000 (contact)
Connector supplier:	Japan Aviation Electronics Industry, Limited (JAE)
Fitting Cable:	AWG#28 to 32 twist pair cable
(Note 2)	(Total cable assembly is recommended to be shielded.)

Note 1: When use the internal PLE function, it is recommended to keep these terminals open.

Note 2: If using a long cable, applied voltage may be dropped because of its resistance.
Specified voltage should be applied correctly at the input of the module side connector.

MECHANICAL DRAWING (Unit: mm)

FRONT VIEW



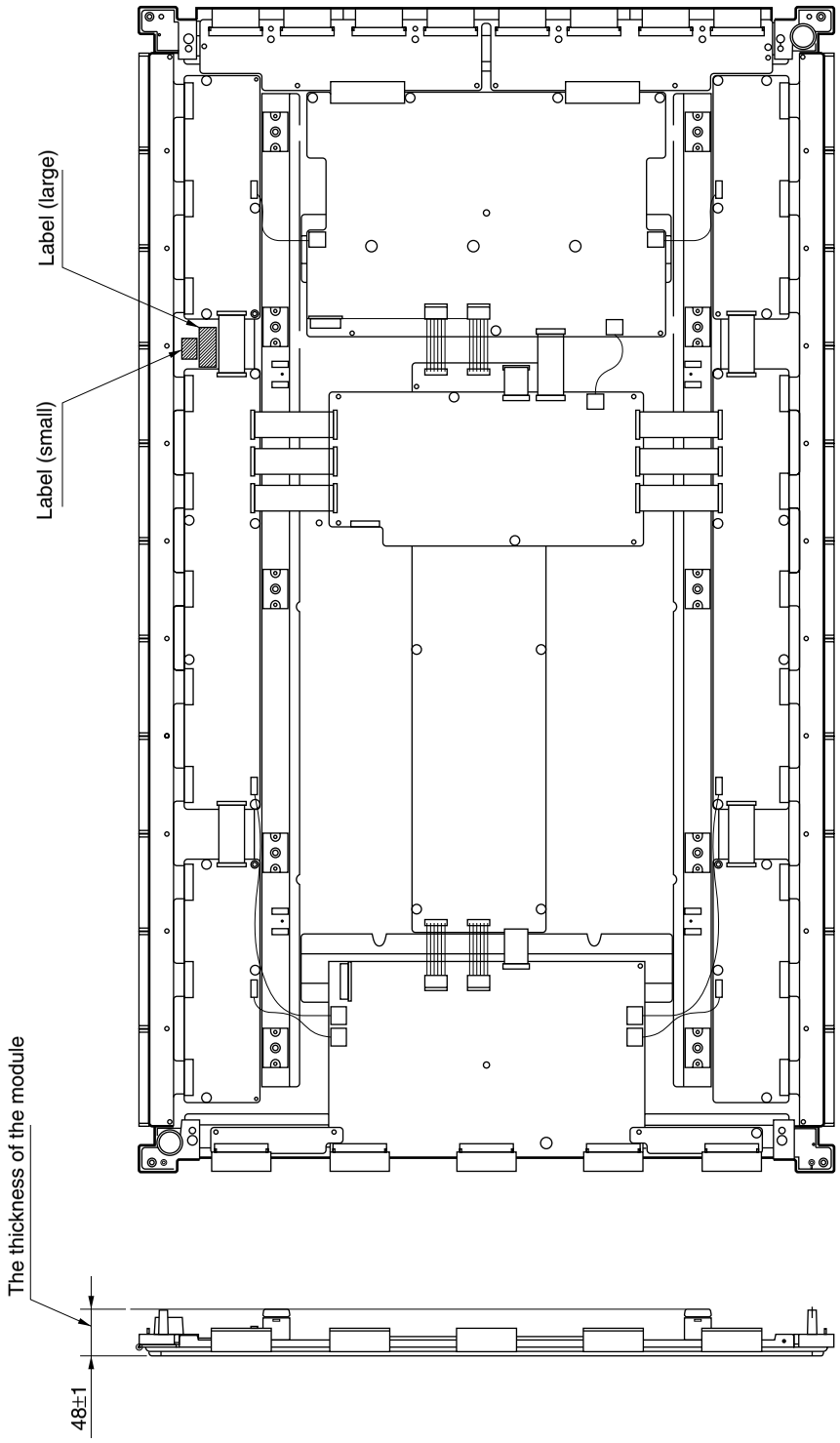
Note 1: The values parentheses are for reference.

Note 2: Do not use these guide holes for mounting the module to the cabinet.

***1:** The dimension of protruded FPC.

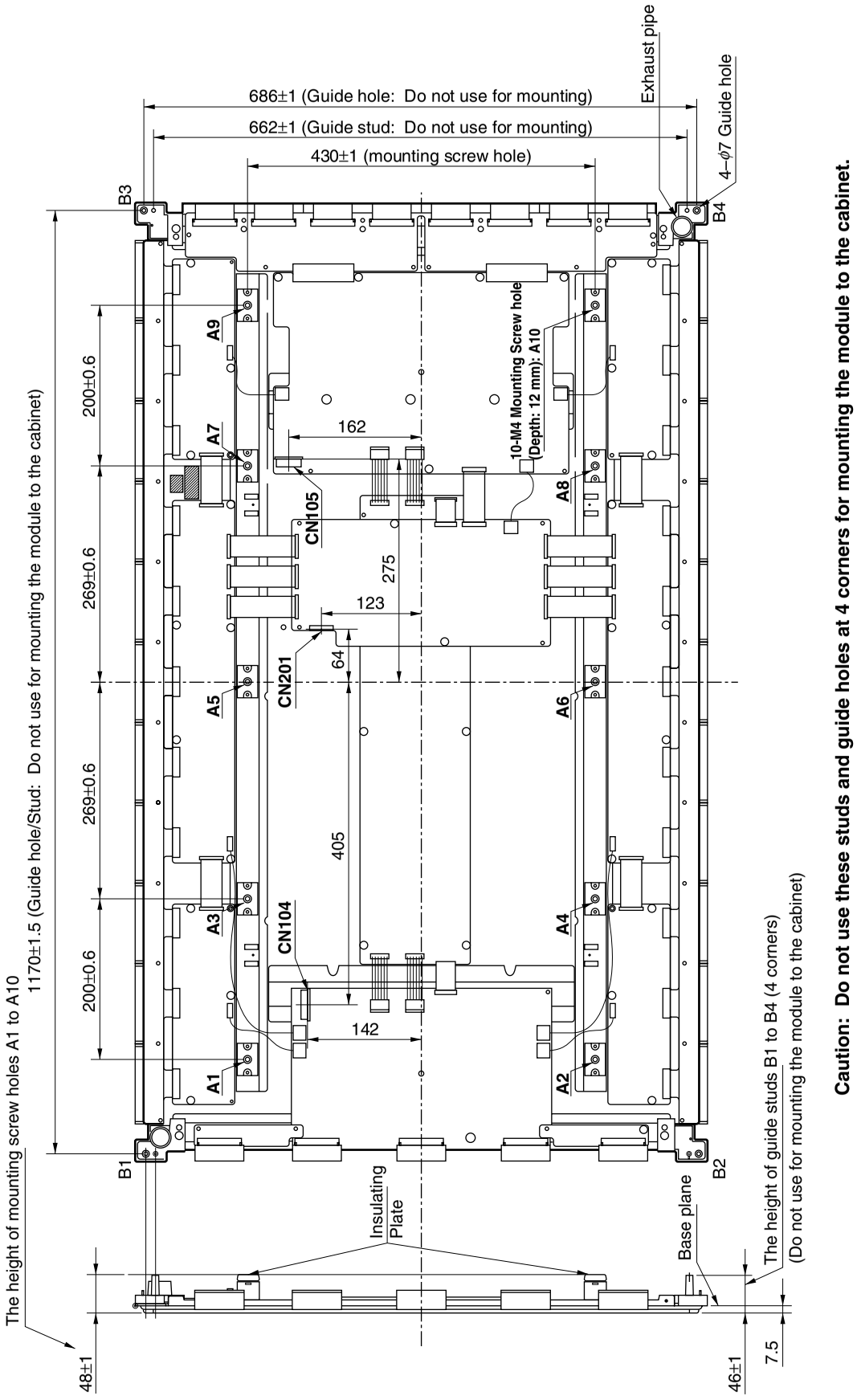
MECHANICAL DRAWING

REAR VIEW (Unit: mm)



MOUNTING POSITIONS AND CONNECTORS POSITION

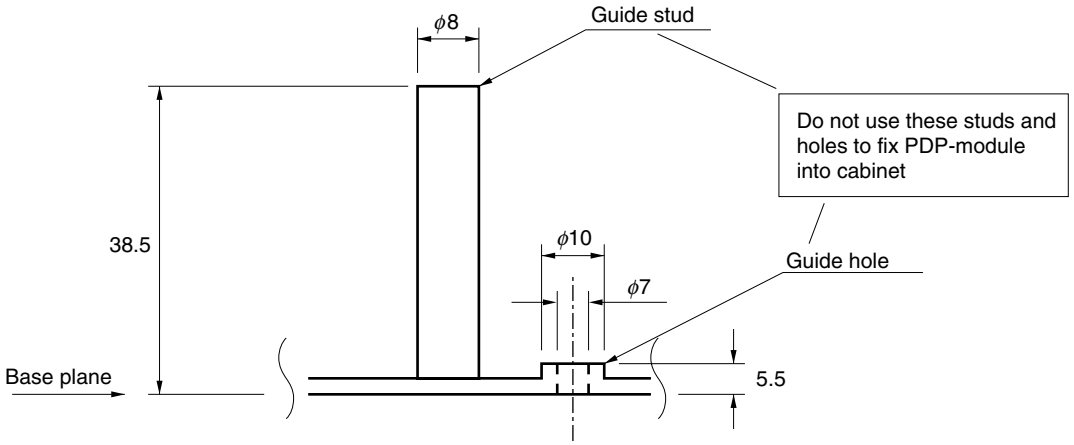
REAR VIEW (Unit: mm)



Caution: Do not use these studs and guide holes at 4 corners for mounting the module to the cabinet.

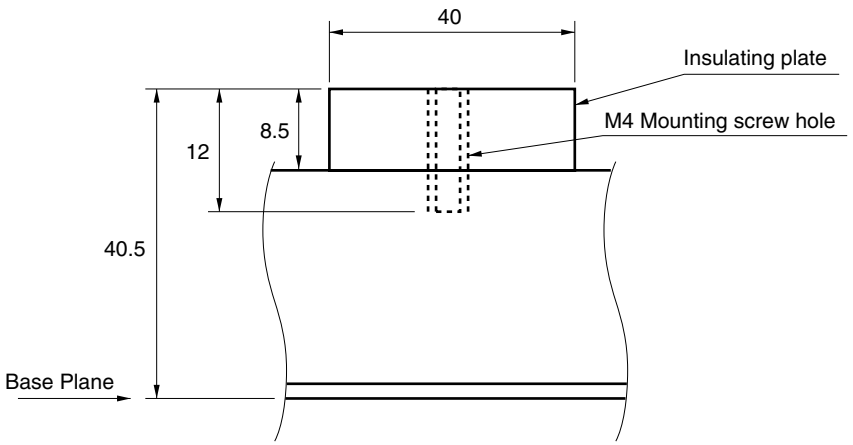
SHAPE OF GUIDE HOLE AND STUD **(Unit: mm)**

(Holes on the 4 corners of aluminum chassis, B1 to B4)



SHAPE OF MOUNTING SCREW HOLE **(Unit: mm)**

(Holes on the behind of PDP module, A1 to A10)



Locatable position of other parts or structures adjacent to the PDP module

Rear view (Unit: mm)

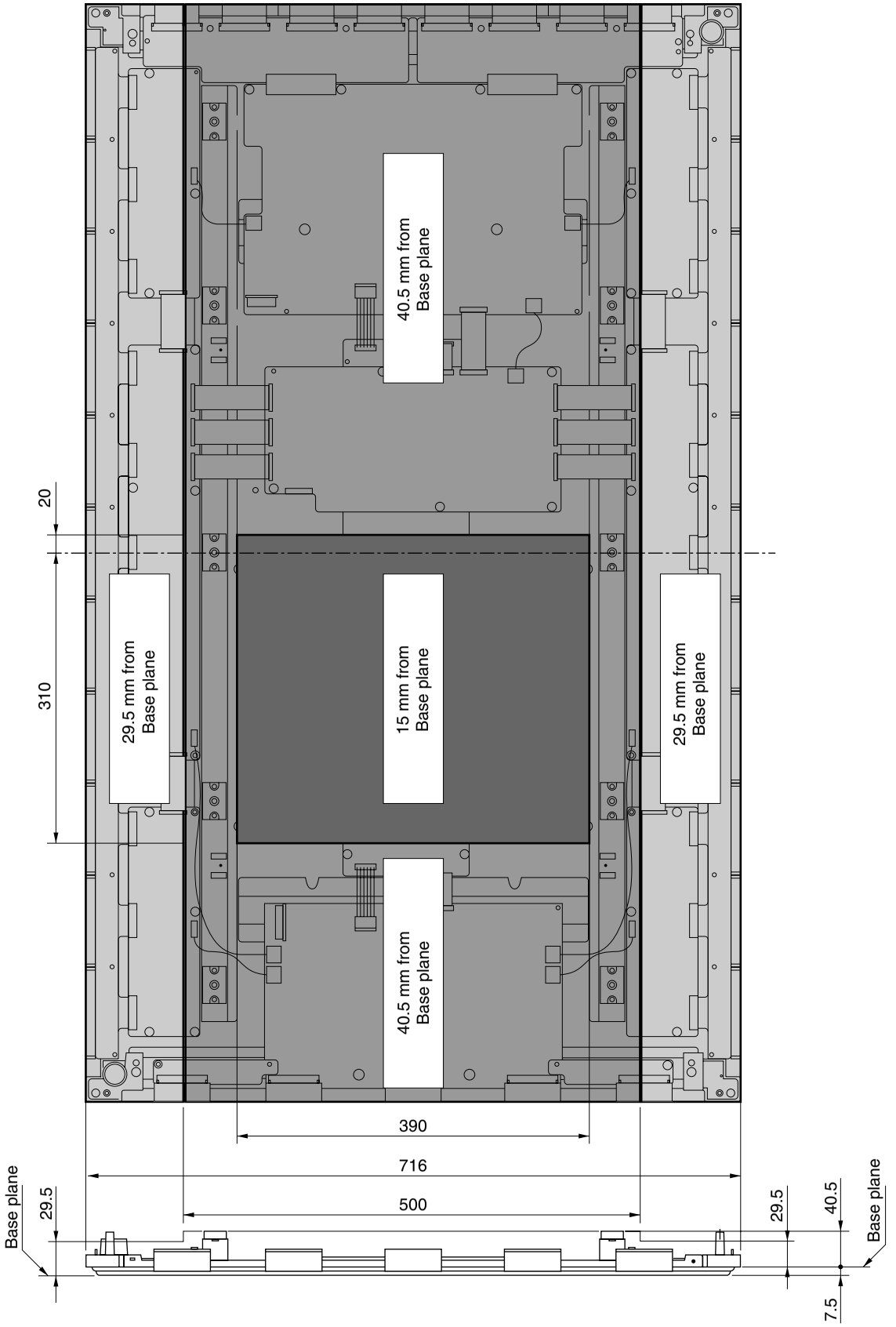


IMAGE STICKING CHARACTERISTICS

1) Image sticking

The fluorescent substance used in the plasma module loses its luminance with the lapse of lighting time.
This deterioration in luminance appears to be a difference in luminance in relation to the surroundings, and comes to be recognized as image sticking.

In other words, the image sticking is defined as follows: when the same pattern (of the fixed display) is displayed for a long time, a difference in luminance is caused around the lighting area and non-lighting area due to deterioration in the fluorescent substance.
When the present pattern is changed over to another one, the boundary comes to be seen between the lighting area and non-lighting area due to difference in luminance in the pattern shown shortly before changeover. If this condition is accumulated, the boundary or image sticking comes to be seen with the naked eyes.

2) Secular change in luminance

The life of luminance, defined as the reduction to half the initial level, is more than 10 thousand hours on average.
Conditions: All white (100% white) input at an ambient temperature of 25°C.
However, this life time is not a guarantee value for life and luminance. It should be recognized simply as the data for reference.

3) Warranty

Image sticking and faults in luminance and picture elements are excluded from the warranty objects.

4) Cause of deterioration in luminance

A major possible cause of deterioration in luminance is damage in the fluorescent substance due to impact caused by ions generated at the time of plasma discharges.

5) Practical value for Image sticking

The relationship between integrated lighting time and luminance in this plasma module is described in the attached material. In particular, the deterioration in luminance tends to be accelerated up to 100 hours in the initial period. In the initial period, the fixed display of patterns particularly tends to cause image sticking.
The practical value for image sticking is difficult to define in concrete numerals. As described below, you are advised to take proper measures to make the occurrence of image sticking as slow as possible.

6) Proposed measures taken to relieve image sticking

So long as there is the reduction of luminance in the fluorescent substance, it is impossible to avoid the occurrence of image sticking. Therefore, to relieve image sticking, we offer you a method of entering an image input that may ensure reluctance to the generation of the difference in luminance reduction among the displayed dots.

The images from TV broadcasting involve a high rate of motion picture displays.
Therefore,
there is less chance of being a cause of difference in luminance reduction among the cells. Even when the fixed patterns are displayed, they generally last for a few minutes.
Since the same pattern is less liable to be displayed, there is almost no influence toward image sticking.

If the fixed patterns tend to be displayed for a long time, however, there occurs a substantial imbalance between the lighting and non-lighting areas, thus causing a difference in luminance as a result. In this document, we offer you some proposals of installation, paying attentions to the two points: the reduction of difference in luminance achieved by integrated lighting time leveling and the method of edge smearing to make image sticking hard to be discerned.

The result from these proposals can, however, greatly depend on the contents of images and the operating environment. Therefore, we consider that it is essential to take the suitable measures in consideration of the customer's operating environment.

Example of Proposal 1: The display position is moved while the fixed display pattern is changed over, or it is scrolled during the display.

Example of Proposal 2: If possible, a pattern of complementary color is incorporated (for integrated time leveling).

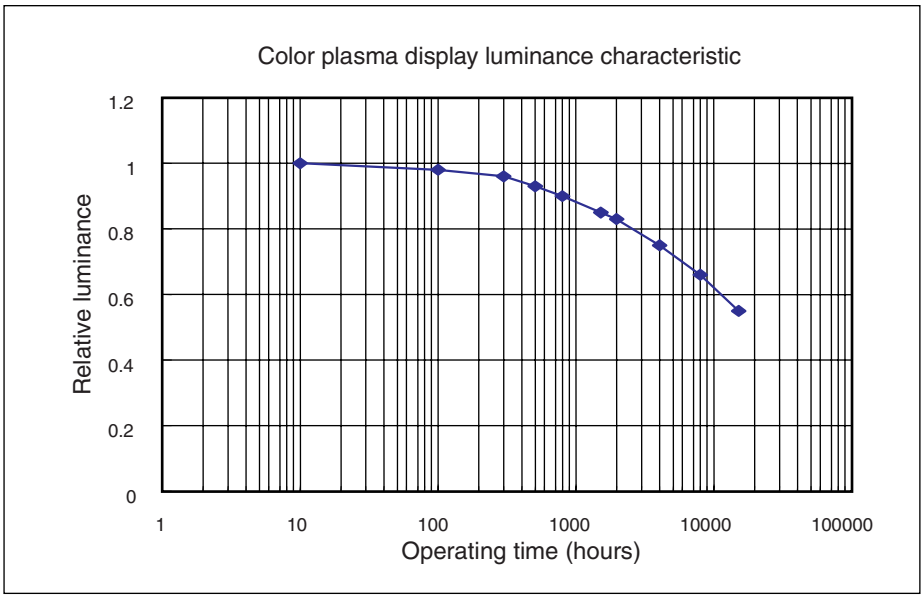
Example of Proposal 3: The fixed pattern and the motion picture display are reciprocally exchanged, in order to minimize the display period of the fixed pattern.

Example of Proposal 4: During operation, the luminance of screen is suppressed as low as possible. For the display patterns, characters are indicated not on the black ground (non-picture area) but on the colored ground (mixture of R, G, B recommended).

7) Proposed countermeasures for the plasma module

Since the PDP is a display that uses a fluorescent substance like the CRT, it is a fundamental phenomenon that image sticking occurs. Unlike the CRT, the PDP gives rise to deterioration in the fluorescent substance due to impact caused by ions generated during plasma display.

As a result of the above-mentioned improvements, it is possible to extend the PDP lifetime and relieve the effect of burning, but is impossible to realize the complete elimination of burning so far as a fixed pattern is displayed for a long time.



Usage Cautions

1. Cautions Regarding Handling of Module

(1) When taking the product out of its box, be careful to prevent shocks to the panel surface.

(2) The display panel used in this product is made of glass. Since shocks or vibrations may cause it to break, be very careful during handling. In case the panel breaks, be careful not to get injured with glass fragments.

(3) Since the panel surface gets easily scratched, be careful during handling not to press against the panel or scrape it with a hard object (anything harder than a 3H pencil lead).

(4) If the panel surface gets dirty, gently wipe it with a dry cloth. If a liquid gets on the panel, mop it up by gently applying a dry cloth without rubbing. In the case of a stubborn stain, wipe it with a cloth slightly wetted with a neutral detergent. Use only dry cloth for wiping, and avoid using the same cloth over and again. (Using an alcohol such as ethanol or chemicals such as those contained in a chemical cloth may cause discoloration of the panel surface or, depending on the type of stain, indelible fixing of the stain to the panel surface.)
Deleterious substances such as described above or water drops getting into the module or somewhere on the module surface other than the display panel may damage the product.

(5) Handle the product with care, avoiding pressing against or scraping the glass panel surface, as this may leave the panel surface scratched or blemished.

(6) Be careful not to touch the port for connecting the flexible cable exposed at the rear of the module because this may cause poor contact.

(7) When moving the product, be sure to turn off the power and disconnect all the cables. While moving the product, watch your step. The product may be dropped or fall, leading to injuries or electric shock. This product should be moved by two or more persons. If one person attempts to carry this product alone, he/she may be injured.

2. Cautions Regarding Design and Operation of Module

(1) Do not pull out or insert the power cable from/to an outlet with wet hands. Doing so may cause electric shock.

(2) This product emits near infrared rays (700 to 1100 nm) that may cause the remote controllers of other electric products to malfunction. To avoid this, use an infrared absorption filter and thoroughly evaluate the system and environment.

(3) This product uses a high voltage (approx. 400V). Do not touch the circuitry of this product with your hands when power is supplied to the product or immediately after turning off the power. Be sure to confirm that the voltage has dropped to a sufficiently low level.

(4) If you detect a strange smell or smoke coming out of the product, immediately turn off the power. Continuing to use the product under such conditions may cause electric shock or fire.

(5) Do not use this product with a voltage that exceeds the rated voltage as this may cause product failure or fire. The warranty does not cover problems that occur when the product is used under conditions other than those described in the specifications.

(6) When the product is used as a stationary text display device such as a text display board or for some similar display, it may get damaged by image sticking. Image sticking is a phenomenon whereby the luminance of parts of the screen where images are continuously displayed for a long time declines compared to parts of the screen where images are displayed for a shorter cumulative time, causing uneven screen luminance. The severity of image sticking is proportional to the cumulative display time and the luminance. Taking the following precautions reduce the possibility of image sticking.

<1> Lower the brightness as much as possible when displaying a stationary pattern.

<2> When displaying a stationary pattern, slightly vary the position of the pattern in the following sequence: Top → Right → Down → Left → Top and so on, or use scroll display.

<3> If possible, incorporate complementary color patterns to smooth the cumulative display time.

<4> Reduce the stationary pattern display time by alternating stationary pattern display and moving image display.

<5> When displaying stationary text, avoid display against a black background, and use a colored background instead.

Image sticking and faults in luminance and picture elements are excluded from the warranty objects.

(7) This product contains parts that generate heat during operation. During the set design stage, take into consideration the cooling method and design the frame based on careful evaluation of heating characteristics.

(8) The temperature of the glass surface of the display may rise to high temperature depending on the conditions of use. If you touch the glass inadvertently, you may be burned.

(9) This product uses a high-voltage drive pulse and emits electromagnetic noise. When this product is incorporated in a set, be sure to design the frame and fit an optical filter shield on the front side of the set so that the electromagnetic interference produced by the set falls within the allowed range.

(10) When installing this product in the frame of a set, use the indicated fixing screw holes and guide holes. Since the display panel of the product is made of glass, design the frame so as to prevent a large weight or shocks from being applied to the glass.

[MEMO]

[MEMO]

[MEMO]