PRELIMINARY

NLT Technologies, Ltd.

TFT COLOR LCD MODULE

NLB070WV01C-01

18cm (7.0 Type)
WVGA
CMOS interface

PRELIMINARY DATA SHEET

DOD-PP-1611(4th edition)

This PRELIMINARY DATA SHEET is updated document from DOD-PP-1532(3)

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INTRODUCTION

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The products are classified into three grades: **"Standard"**, **"Special"**, and **"Specific"**.
Each quality grade is designed for applications described below. Any customer who intends to use a product for application other than that of Standard is required to contact an NLT sales representative in advance.

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Examples: Office equipment, audio and visual equipment, communication equipment, test and measurement equipment, personal electronic equipment, home electronic appliances, car navigation system (with no vehicle control functions), seat entertainment monitor for vehicles and airplanes, fish finder (except marine radar integrated type), PDA, etc.

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Examples: Vehicle/train/ship control system, traffic signals system, traffic information control system, air traffic control system, surgery/operation equipment monitor, disaster/crime prevention system, etc.

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Examples: Aerospace system (except seat entertainment monitor), nuclear control system, life support system, etc.

The quality grade of this product is the **"Standard"** unless otherwise specified in this document.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NLB070WV01C-01 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing circuit, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION

- For industrial use

1.3 FEATURES

- High contrast
- 6-bit digital RGB signals
- Reversible-scan direction
- LED backlight type
- LED driver circuit Built-in
- Replaceable lamp for backlight

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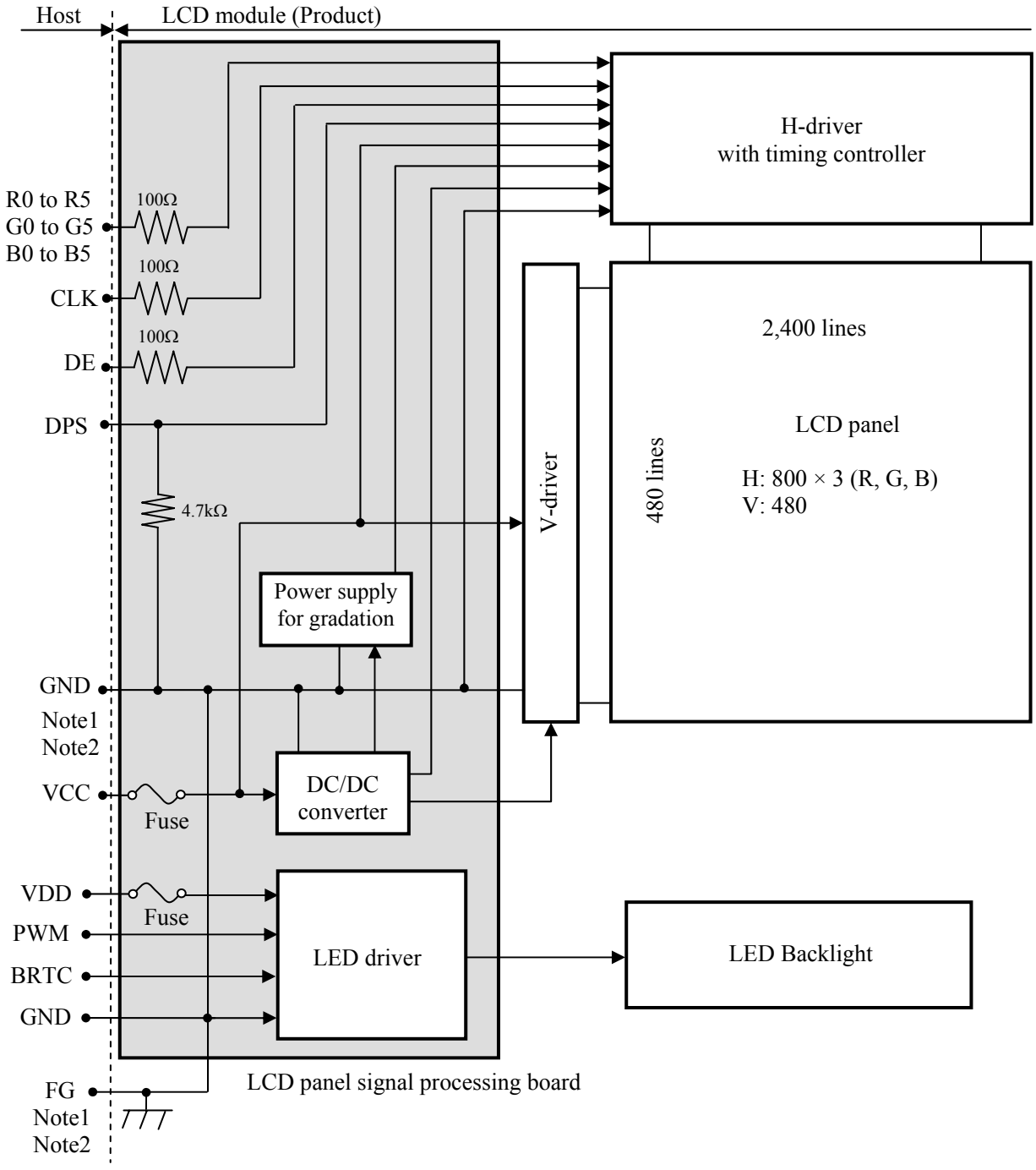
2. GENERAL SPECIFICATIONS

Display area	152.4 (H) × 91.44 (V) mm	
Diagonal size of display	18cm (7.0 inches)	
Drive system	a-Si TFT active matrix	
Display color	262,144 colors	
Pixel	800 (H) × 480 (V) pixels	
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe	
Dot pitch	0.0635 (H) × 0.1905 (V) mm	
Pixel pitch	0.1905 (H) × 0.1905 (V) mm	
Module size	170.0 (H) × 111.0 (V) × 8.25 (D) mm (typ.)	
Weight	(160) g (typ.)	
Contrast ratio	(800):1 (typ.)	
Viewing angle	*At the contrast ratio ≥10:1* • Horizontal: Right side (70°) (typ.), Left side (70°) (typ.) • Vertical: Up side (70°) (typ.), Down side (70°) (typ.)	4
Designed viewing direction	*At DPS= Low or Open: Normal scan* • Viewing direction without image reversal: Up side (12 o'clock) • Viewing direction with contrast peak: Down side (6 o'clock) • Viewing angle with optimum grayscale (γ≒ 2.2): Normal axis (perpendicular)	
Polarizer surface	Clear	
Polarizer pencil-hardness	3H (min.) [by JIS K5600]	
Color gamut	*At LCD panel center* (60) % (typ.) [against NTSC color space]	
Response time	*Ton+Toff (10%←→ 90%)* 18ms (typ.)	
Luminance	*At the maximum luminance control* 300 cd/m^2 (typ.)	
Signal system	6-bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE)	
Power supply voltage	LCD panel: 3.3V LED backlight: 5.0 to 12.0V	
Backlight	LED backlight type built in LED Driver Circuit (Replaceable part • Lamp holder set: Type No.70LHS201)	4
Power consumption	*At the maximum luminance control, VDD=5.0V, Checkered flag pattern* (1.7) W (typ.)	4

3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground and LED driver ground) and FG (Frame ground) in the LCD module are as follows.

GND- FG	Connected

Note2: GND and FG must be connected to customer equipment's ground, and it is recommended that these grounds be connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	170.0 ± 0.5 (W) × 111.0 ± 0.5 (H) × 8.25 ± 0.5 (D) Note1	mm
Display area	152.4 (H) × 91.44 (V) Note1	mm
Weight	(160) (typ.), (175) (max.)	g

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Note1: See "**8. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel	VCC	-0.3 to 3.96	V	Ta= 25°C
	LED driver	VDD	-0.3 to 17.5		
Input voltage for signals	Display signals Note1	VD	-0.5 to (VCC+0.5)	V	
	Function signal Note2	VF	-0.5 to 4.6		
	Function signal for LED driver	PWM	-0.3 to (11.2)	V	
		BRTC			
Storage temperature		Tst	-30 to +80	°C	-
Operating temperature	Front surface	TopF	-20 to +70	°C	Note3
	Rear surface	TopR	-20 to +70	°C	Note4
Relative humidity Note5		RH	≤ 90	%	Ta ≤ 40°C
			≤ 80	%	40 < Ta ≤ 50°C
Absolute humidity Note5		AH	≤ 70	g/m^3	Ta > 50°C

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Note1: CLK, DE, DATA (R0 to R5, G0 to G5, B0 to B5)
Note2: DPS
Note3: Measured at center of LCD panel surface (including self-heat)
Note4: Measured at center of LCD module's rear shield surface (including self-heat)
Note5: No condensation.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage		VCC	3.0	3.3	3.6	V	-	
Power supply current		ICC	-	(150) Note1	(250) Note2	mA	at VCC= 3.3V	4
Permissible ripple voltage		VRPC	-	-	100	mVp-p	for VCC	
Logic input voltage for display signals	High	VDH	0.7VCC	-	VCC	V	CMOS level	
	Low	VDL	0	-	0.3VCC	V		
Input voltage for DPS signal	High	VFH	0.7VCC	-	VCC	V		
	Low	VFL	0	-	(0.5)	V		4
Input current for DPS signal	High	IFH	-	-	TBD	μA	-	
	Low	IFL	TBD	-	-	μA		

Note1: Checkered flag pattern [by EIAJ ED-2522]
Note2: Pattern for maximum current

4.3.2 Backlight

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage		VDD	4.5	-	12.6	V	Note1	4
Power supply current		IDD	-	(240)	(260) Note2	mA	at VCC = 5.0V Note8	4
			-	(100)	(110) Note2	mA	at VCC = 12.0V Note8	
Permissible ripple voltage		VRPD	-	-	200	mVp-p	for VDD	
Input voltage for PWM signal	High	VDFH1	2.0	-	(5.5)	V	-	4
	Low	VDFL1	0	-	0.8	V		
Input voltage for BRTC signal	High	VDFH2	2.0	-	(5.5)	V	-	4
	Low	VDFL2	0	-	0.8	V		
PWM frequency		f_{PWM}	(100)	-	(1,000)	Hz	Note4, Note5	
PWM duty ratio		DR_{PWM}	1	-	100	%	Note6, Note7	
PWM pulse width		tPWH	10	-	-	μs		

Note1: When designing of the power supply, take the measures for the prevention of surge voltage.
Note2: This value excludes peak current such as overshoot current.
Note3: The power supply lines (VDD and GND) may have ripple voltage during luminance control of LED. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor between the power supply lines (VDD and GND) to reduce the noise if necessary.
Note4: A recommended f_{PWM} value is as follows.

$$f_{PWM} = \frac{2n-1}{4} \times fv$$

$$(n = \text{integer}, fv = \text{frame frequency of LCD module})$$

Note5: Depending on the frequency used, so noise may appear on the screen, please conduct a thorough evaluation.
Note6: While the BRTC signal is high, do not set the tPWH (PWM pulse width) is less than 10μs. It may cause abnormal working of the backlight. In this case, turn the backlight off and then on again by BRTC signal.
Note7: Regardless of the PWM frequency, both PWM duty ratio and PWM pulse width must be always more than the minimum values.
Note8: At the maximum luminance control.

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are over the permissible values as the following table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VCC	3.3V	≤ 100	mVp-p
VDD	5.0 to 12.0 V	≤ 200	mVp-p

Note1: The permissible ripple voltage includes spike noise.

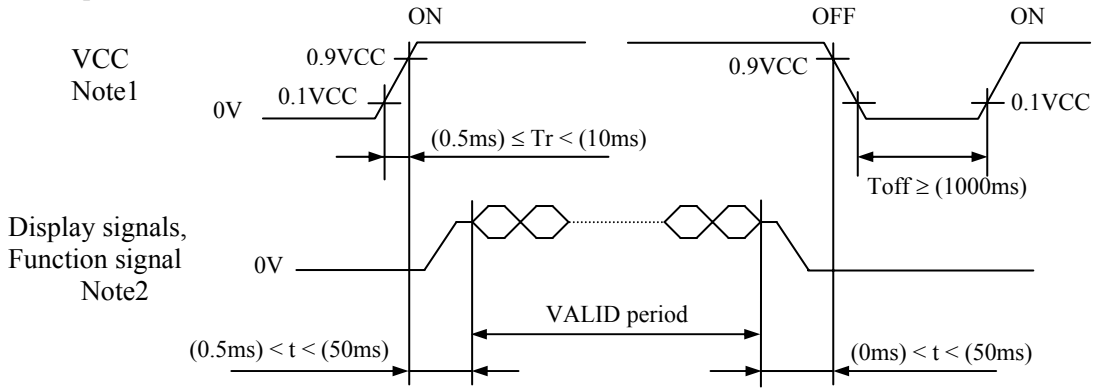
4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VCC	FCC16152AB	KAMAYA ELECTRIC CO.,LTD	1.5A 36V	3.0A	Note1
VDD	FCC16152AB	KAMAYA ELECTRIC CO.,LTD	1.5A 36V	3.0A	

Note1: The power supply's rated current must be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

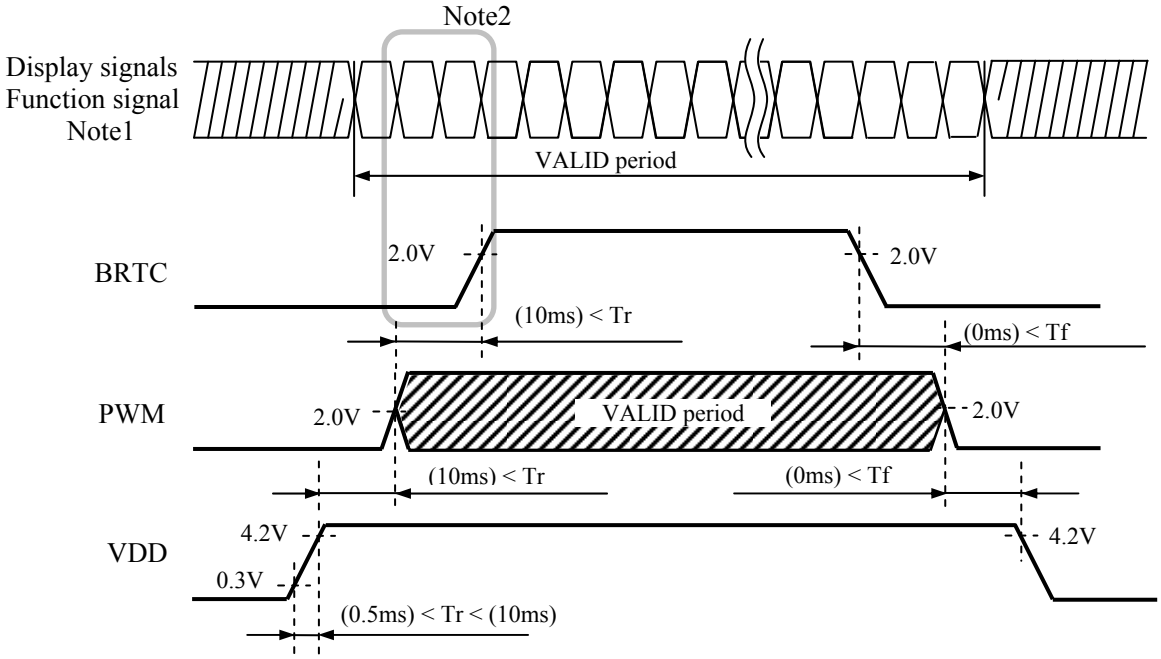
4.4.1 LCD panel



Note1: If there is a voltage variation (voltage drop) at the rising edge of VCC below 3.0V, there is a possibility that a product does not work due to a protection circuit.

Note2: Display signals (CLK, DE, DATA (R0 to R5, G0 to G5, B0 to B5)) and function signal (DPS) must be set to Low or High-impedance, except the VALID period (See above sequence diagram), in order to avoid the circuitry damage.
If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display and function signals, VCC also must be shut down.

4.4.2 LED driver board



Note1: These are the display and function signals for LCD panel signal processing board.

Note2: The backlight should be turned on within the valid period of display and function signals, in order to avoid unstable data display.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

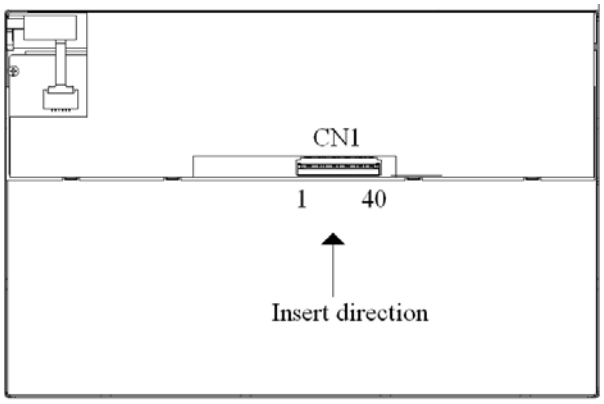
CN1 socket (LCD module side): FH52-40S-0.5SH (HIROSE ELECTRIC CO., LTD.)
Adaptable plug: [0.5mm pitch, Bottom Contact Type]

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	CLK	Dot clock	-
3	N. C.	-	Keep this pin Open.
4	N. C.	-	Keep this pin Open.
5	GND	Ground	Note1
6	R0	Red data (LSB)	Least significant bit
7	R1	Red data	-
8	R2	Red data	
9	R3	Red data	
10	R4	Red data	
11	R5	Red data (MSB)	Most significant bit
12	GND	Ground	Note1
13	G0	Green data (LSB)	Least significant bit
14	G1	Green data	-
15	G2	Green data	
16	G3	Green data	
17	G4	Green data	
18	G5	Green data (MSB)	Most significant bit
19	GND	Ground	Note1
20	B0	Blue data (LSB)	Least significant bit
21	B1	Blue data	-
22	B2	Blue data	
23	B3	Blue data	
24	B4	Blue data	
25	B5	Blue data (MSB)	Most significant bit
26	GND	Ground	Note1
27	DE	Data enable signal	-
28	VCC	Power supply	Note1
29	VCC	Power supply	
30	N. C.	-	Keep this pin Open.
31	DPS	Selection of scan direction	High: Reverse scan Low or Open: Normal scan Note2
32	N. C.	-	Keep this pin Open.
33	GND	Ground	Note1
34	VDD	Power supply	Note1
35	VDD	Power supply	
36	GND	Ground	Note1
37	GND	Ground	
38	BRTC	Back light ON/OFF control	High-ON / Low-OFF
39	PWM	Luminance control	PWM Dimming
40	GND	Ground	Note1

Note1: All GND, VCC and VDD terminals should be used without any non-connected lines.
Note2: See **"4.8 SCANNING DIRECTIONS"**.

4.5.2 Positions of plug and socket

Rear side



4.6 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 262,144 colors in 64 gray scales by combination between input data signals. See following table.

Display colors		Data signal (0: Low level, 1: High level)																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:						:						:		
	↓				:						:						:		
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	↑				:						:						:		
	↓				:						:						:		
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
		0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				:						:						:		
	↓				:						:						:		
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

4.7 DISPLAY POSITIONS

The following table is the coordinates per pixel (See **"4.8 SCANNING DIRECTIONS"**.).

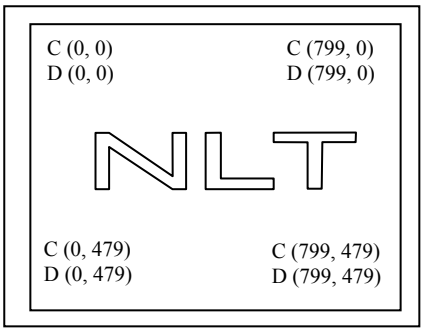
C (0, 0)

R	G	B

C(0, 0)	C(1, 0)	· · ·	C(X, 0)	· · ·	C(798, 0)	C(799, 0)
C(0, 1)	C(1, 1)	· · ·	C(X, 1)	· · ·	C(798, 1)	C(799, 1)
. . .	. . .	. . .	. . .	. . .	. . .	. . .
C(0, Y)	C(1, Y)	· · ·	C(X, Y)	· · ·	C(798, Y)	C(799, Y)
. . .	. . .	. . .	. . .	. . .	. . .	. . .
C(0, 478)	C(1, 478)	· · ·	C(X, 478)	· · ·	C(798, 478)	C(799, 478)
C(0, 479)	C(1, 479)	· · ·	C(X, 479)	· · ·	C(798, 479)	C(799, 479)

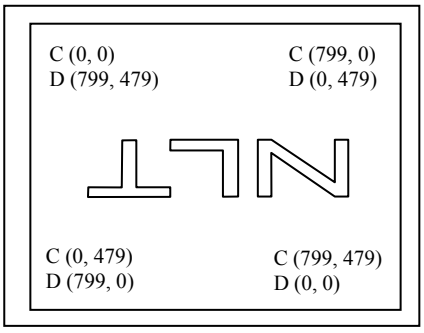
4.8 SCANNING DIRECTIONS

The following figures are seen from a front view.



Note1

Figure1. Normal scan (DPS: Low or Open)



Note1

Figure2. Reverse scan (DPS: High)

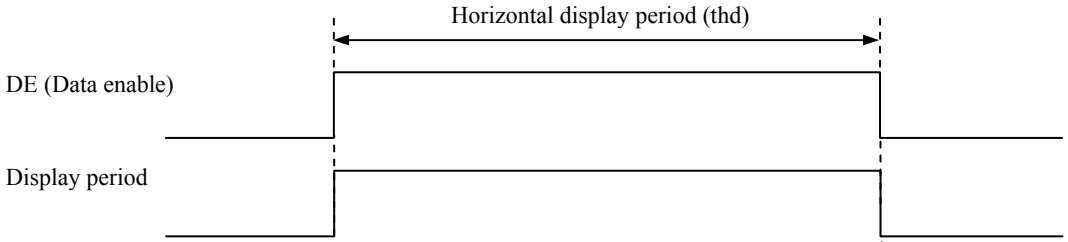
Note1: Meaning of C (X, Y) and D (X, Y)
C (X, Y): The coordinates of the display position (See "**4.7 DISPLAY POSITIONS**".)
D (X, Y): The data number of input signal for LCD panel signal processing board

4.9 INPUT SIGNAL TIMINGS

4.9.1 Outline of input signal timings

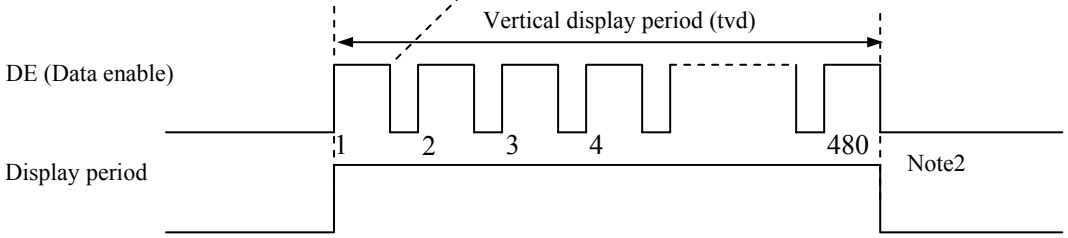
- Horizontal signal

Note1



- Vertical signal

Note1



Note1: This diagram indicates virtual signal for set up to timing.
Note2: See "**4.9.3 Input signal timing chart**" for the pulse number.

4.9.2 Timing characteristics

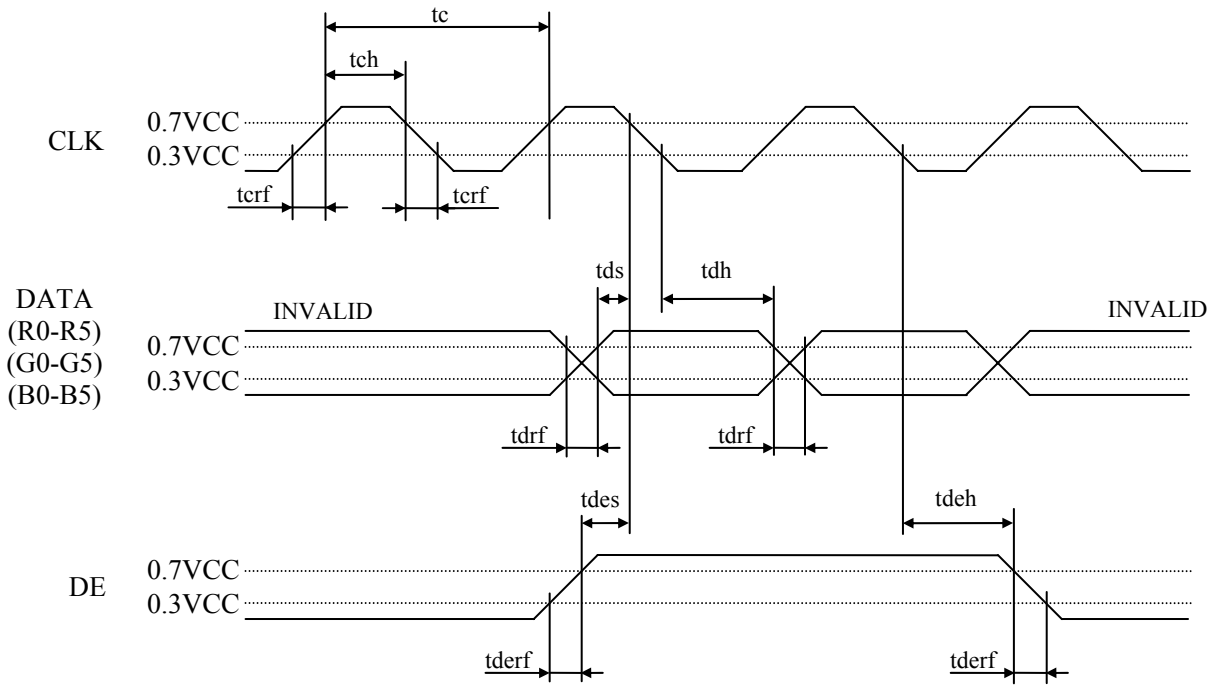
(Note1, Note2)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	28.0	32.256	36.0	MHz	31.002 ns (typ.)
	Duty		tcd	0.4	0.5	0.6	-	-
	Rise time, Fall time		tcrf	-	-	(10)	ns	
DATA (R0-R5) (G0-G5) (B0-B5)	CLK-DATA	Setup time	tds	8	-	-	ns	-
		Hold time	tdh	8	-	-	ns	
	Rise time, Fall time		tdrf	-	-	(10)	ns	
DE	Horizontal	Cycle	th	28.44	31.746	36.57	µs	31.5 kHz (typ.)
				889	1024	1143	CLK	
		Display period	thd	800			CLK	-
	Vertical (One frame)	Cycle	tv	14.931	16.667	19.19	ms	60.0 Hz (typ.)
				513	525	767	H	
		Display period	tvd	480			H	-
	CLK-DE	Setup time	tdes	8	-	-	ns	-
		Hold time	tdeh	8	-	-	ns	
	Rise time, Fall time		tderf	-	-	(10)	ns	

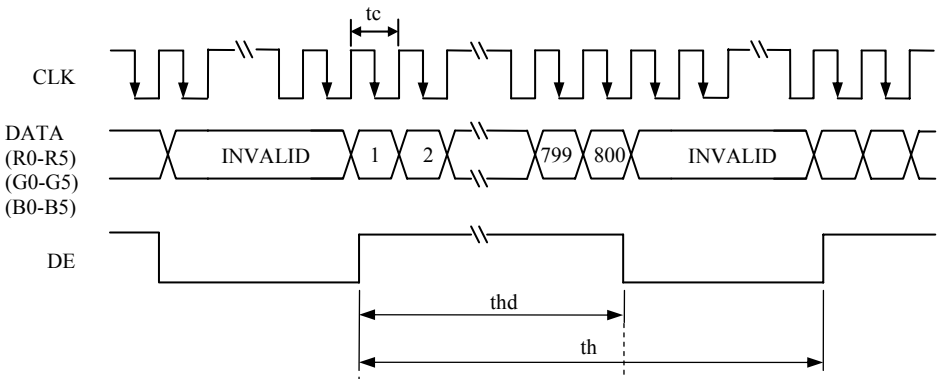
Note1: Definition of parameters is as follows.
tc= 1CLK, tcd= tch/tc, th= 1H

Note2: Vertical cycle (tv) should be specified in integral multiple of Horizontal cycle (th).

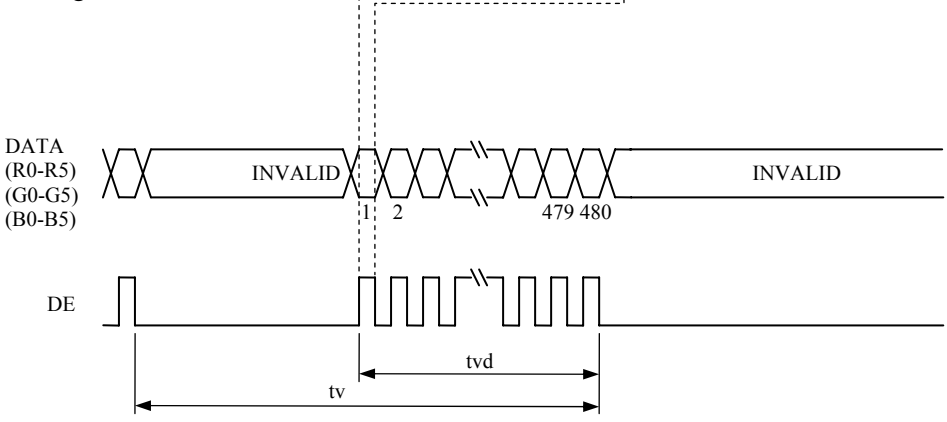
4.9.3 Input signal timing chart



Horizontal timing



Vertical timing



4.10 OPTICS

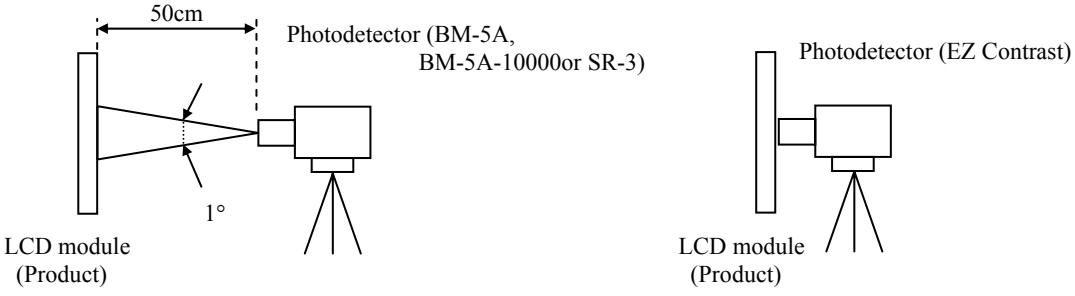
4.10.1 Optical characteristics

(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance		White at center θR= 0°, θL= 0°,θU= 0°,θD= 0°	L	(210)	300	-	cd/m^2	BM-5A	-	4
Contrast ratio		White/Black at center θR= 0°, θL= 0°,θU= 0°,θD= 0°	CR	(480)	(800)	-	-	BM-5A	Note3	4
Luminance uniformity		White θR= 0°, θL= 0°,θU= 0°,θD= 0°	LU	-	1.25	1.4	-	BM-5A	Note4	
Chromaticity	White	**x** coordinate	Wx	0.263	0.313	0.363	-	SR-3	Note5	
		y coordinate	Wy	0.279	0.329	0.379	-			
	Red	**x** coordinate	Rx	-	TBD	-	-			
		y coordinate	Ry	-	TBD	-	-			
	Green	**x** coordinate	Gx	-	TBD	-	-			
		y coordinate	Gy	-	TBD	-	-			
	Blue	**x** coordinate	Bx	-	TBD	-	-			
		y coordinate	By	-	TBD	-	-			
Color gamut		θR= 0°, θL= 0°,θU= 0°,θD= 0° at center, against NTSC color space	C	(55)	(60)	-	%			4
Response time		White to Black	Ton	-	3	(5)	ms	BM-5A -10000	Note6 Note7	
		Black to White	Toff	-	15	(21)	ms			4
		Ton + Toff	-	-	18	(26)	ms			
Viewing angle	Right	θU= 0°, θD= 0°, CR≥ 10	θR	(60)	(70)	-	°	EZ Contrast	Note8	
	Left	θU= 0°, θD= 0°, CR≥ 10	θL	(60)	(70)	-	°			4
	Up	θR= 0°, θL= 0°, CR≥ 10	θU	(60)	(70)	-	°			
	Down	θR= 0°, θL= 0°, CR≥ 10	θD	(60)	(70)	-	°			

Note1: These are initial characteristics.
Note2: Measurement conditions are as follows.
Ta= 25°C, VCC= 3.3V, VDD= 12.0V, PWM: Duty 100%,
Display mode: WVGA, Horizontal cycle= 1/31.5kHz, Vertical cycle= 1/60.0Hz,
DPS= Low or Open: Normal scan

Optical characteristics are measured at luminance saturation 20minutes after the product works, in the dark room. Also measurement methods are as follows.



Note3: See "**4.10.2 Definition of contrast ratio**".
Note4: See "**4.10.3 Definition of luminance uniformity**".
Note5: These coordinates are found on CIE 1931 chromaticity diagram.
Note6: Product surface temperature: TopF= 25°C 4
Note7: See "**4.10.4 Definition of response times**".
Note8: See "**4.10.5 Definition of viewing angles**".

4.10.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

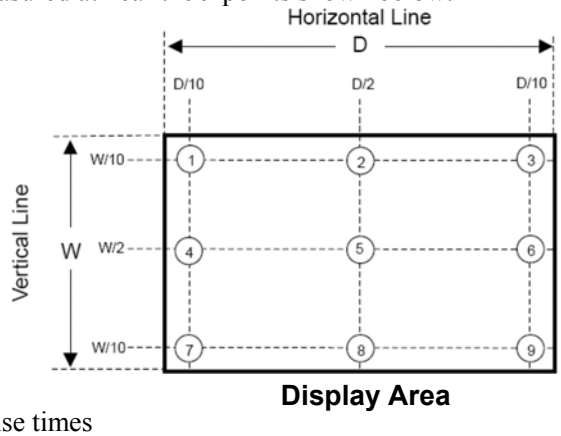
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.10.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

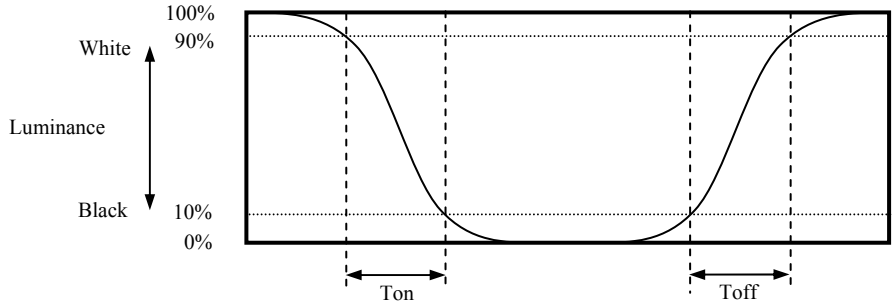
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑨}}{\text{Minimum luminance from ① to ⑨}}$$

The luminance is measured at near the 9 points shown below.

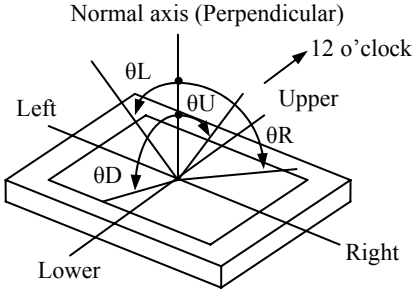


4.10.4 Definition of response times

Response time is measured at the time when the luminance changes from " white " to " black ", or " black " to " white " on the same screen point, by photo-detector. Ton is the time when the luminance changes from 90% down to 10%. Also Toff is the time when the luminance changes from 10% up to 90% (See the following diagram.).



4.10.5 Definition of viewing angles



5. ESTIMATED LUMINANCE LIFETIME

The luminance lifetime is the time from initial luminance to half-luminance.

This lifetime is the estimated value, and is not guarantee value.

Condition		Estimated luminance lifetime (Life time expectancy) Note1, Note2, Note3	Unit
LED elementary substance	25°C (Ambient temperature of the product) Continuous operation, PWM Duty: 100%	30,000	h

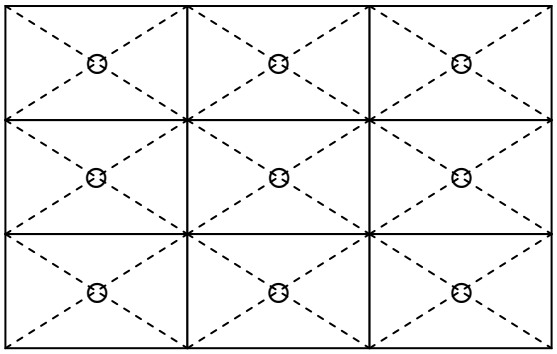
Note1: Life time expectancy is mean time to half-luminance.
Note2: Estimated luminance lifetime is not the value for an LCD module but the value for LED elementary substance.
Note3: By ambient temperature, the lifetime changes particularly. Especially, in case the product works under high temperature environment, the lifetime becomes short.

6. RELIABILITY TESTS

Test item	Condition	Judgment Note1
High temperature and humidity (Operation)	① 60 ± 2°C, RH= 90%, 240hours ② Display data is black.	No display malfunctions
High temperature (Operation)	① 70 ± 3°C, 240hours ② Display data is black.	
Thermal shock (Non operation)	① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
ESD (Operation)	Contact Discharge ① 150pF, 150Ω, ±15kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	
Vibration (Non operation)	① 5 to 100Hz, 19.6m/s^2 ② 1 minute/cycle ③ X, Y, Z directions ④ 120 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)	① 539m/s^2, 11ms ② X, Y, Z directions ③ 5 times each directions	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points.



7. PRECAUTIONS

7.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "7.2 CAUTIONS" and "7.3 ATTENTIONS"!**

This sign has the meaning that a customer will be injured or the product will sustain damage if the customer practices wrong operations.

This sign has the meaning that a customer will be injured if the customer practices wrong operations.

7.2 CAUTIONS

- **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: Equal to or no greater than 539m/s^2 and equal to or no greater than 11ms, Pressure: Equal to or no greater than 19.6 N (ϕ16mm jig))**

7.3 ATTENTIONS

7.3.1 Handling of the product

① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
② When the product is put on the table temporarily, display surface must be placed downward.
③ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
④ The torque for product mounting screws must never exceed 0.23 N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be ≤ 2.0 mm.
⑤ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
⑥ Do not press or rub on the sensitive product surface. When cleaning the panel surface, wipe it with a soft dry cloth.
⑦ Do not push or pull the interface connectors while the product is working.
⑧ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
⑨ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal by any chance, please wash it away with soap and water.

7.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
② In order to prevent dew condensation occurred by temperature difference, the product packing box must be opened after enough time being left under the environment of an unpacking room. Evaluate the storage time sufficiently because dew condensation is affected by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with the original packing state after a customer receives the package)
③ Do not operate in high magnetic field. If not, circuit boards may be broken.
④ This product is not designed as radiation hardened.

7.3.3 Characteristics

The following items are neither defects nor failures.

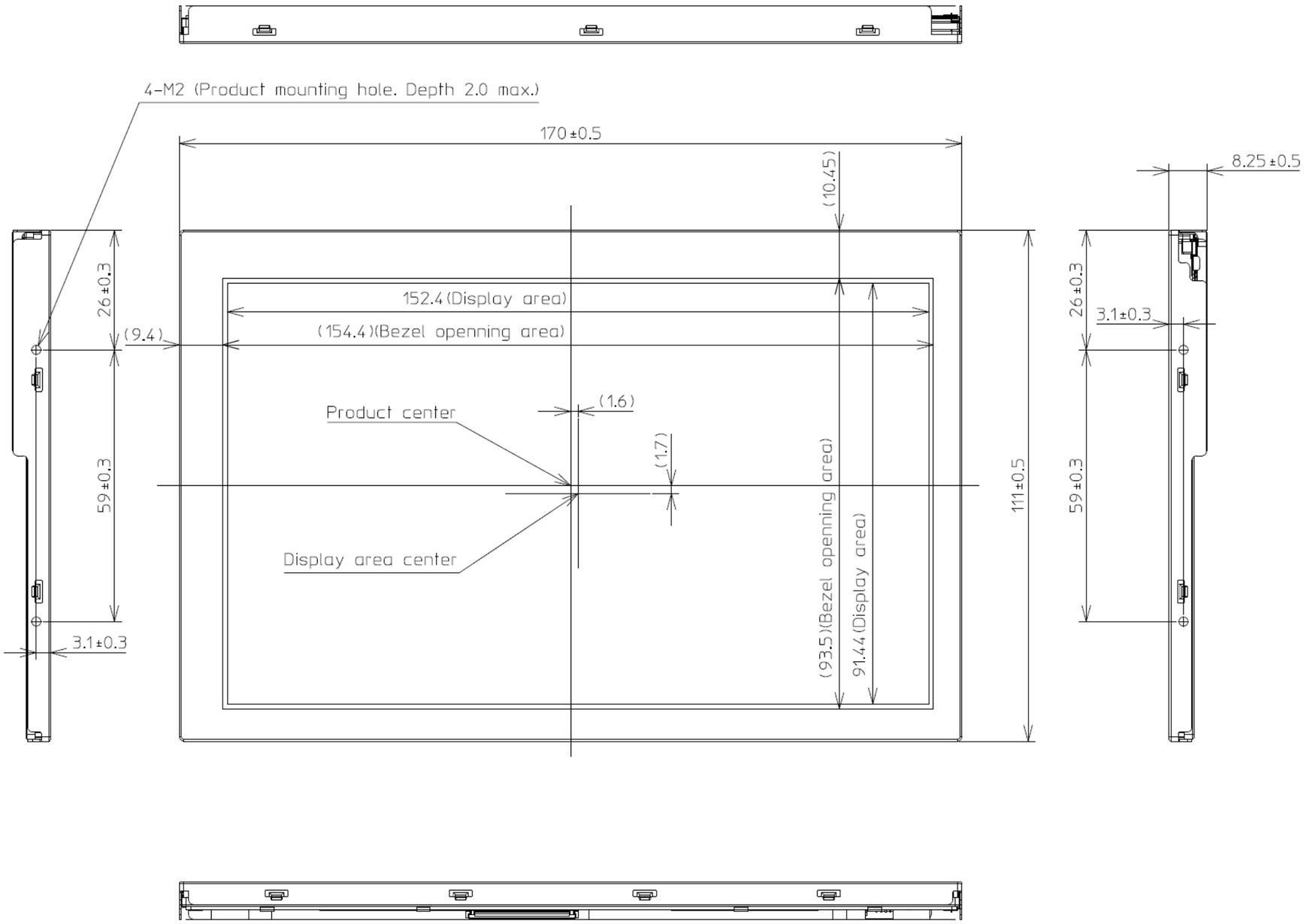
① Characteristics of the LCD (such as response time, luminance, color uniformity and so on) may be changed depending on ambient temperature. If the product is stored under condition of low temperature for a long time, it may cause display mura. In this case, the product should be operated after enough time being left under condition of operating temperature.
② Display mura, flickering, vertical streams or tiny spots may be observed depending on display patterns.
③ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
④ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
⑤ Optical characteristics may be changed depending on input signal timings.

7.3.4 Others

① All GND, VCC and VDD terminals should be used without any non-connected lines.
② Do not disassemble a product or adjust variable resistors.

8. OUTLINE DRAWINGS

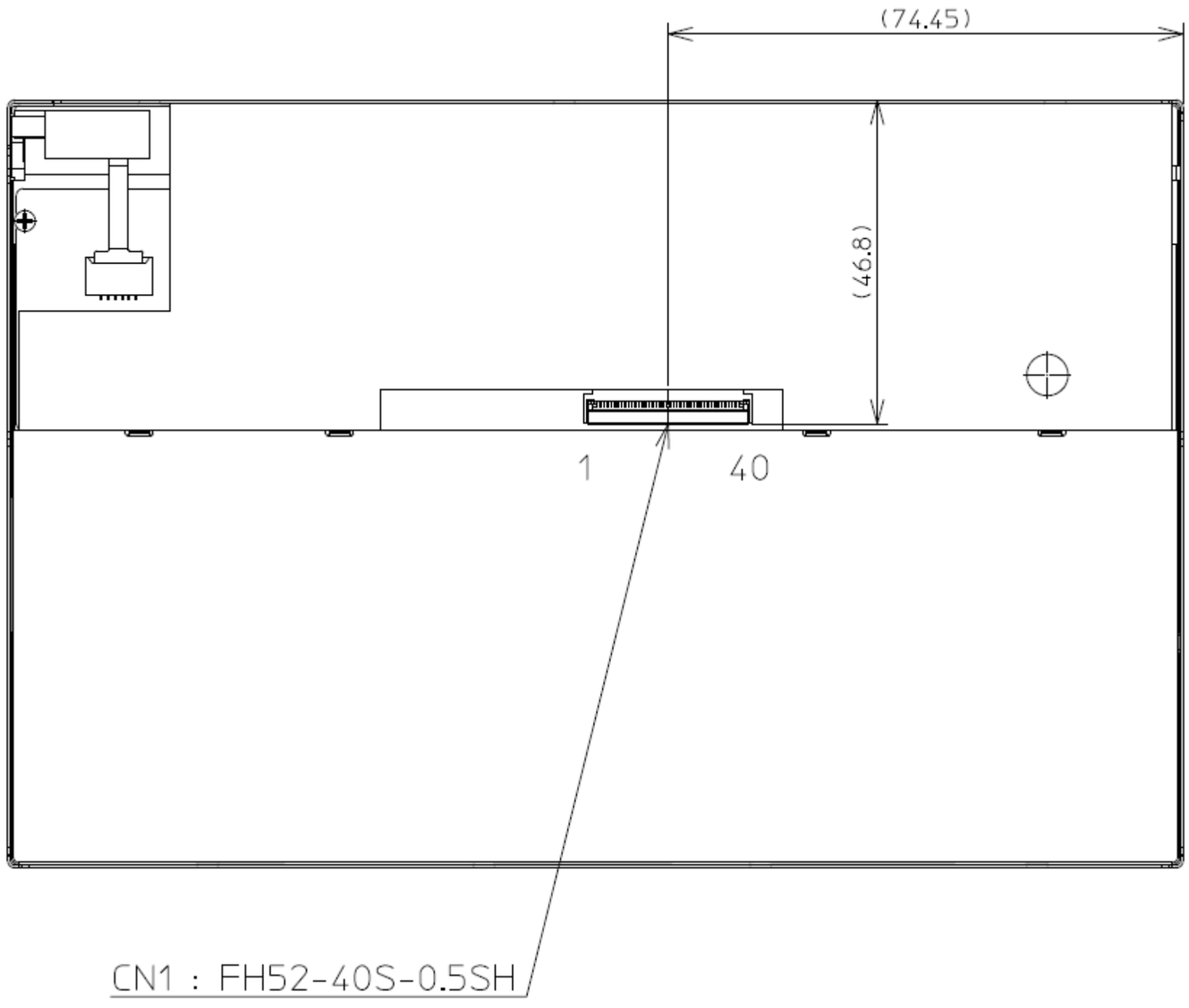
8.1 FRONT VIEW



Unit: mm

Note1: The values in parentheses are for reference.
Note2: The torque for product mounting screws must never exceed 0.23 N·m. And the length of product mounting screws must be ≤ 2.0 mm.

8.2 REAR VIEW



Note1: The values in parentheses are for reference.
Note2: The torque for product mounting screws must never exceed 0.23 N·m. And the length of product mounting screws must be ≤ 2.0 mm.

Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and signature
1st edition	DOD-PP-1476	Sep. 7, 2012	**Revision contents** New issue **Writer** *Approved by* H. USUI *Checked by* H. FUKUYOSHI *Prepared by* E. YOSHIMURA
2nd edition	DOD-PP-1496	Oct. 11, 2012	**Revision contents** P5 GENERAL SPECIFICATIONS • Color gamut: (72) % → (60) % • Power consumption: < 4 W (typ.) → (3.3) W (typ.) P7 ABSOLUTE MAXIMUM RATINGS • Note1: CLK, Hsync, Vsync, DE, DATA → CLK, Hsync, Vsync, DE, DATA (R0 to R5, G0 to G5, B0 to B5) (correction) P9 Backlight • PWM frequency: TBD (min.), TBD (max.) Hz → (100) (min.), (1,000) (max.) Hz P.10 POWER SUPPLY VOLTAGE SEQUENCE - LCD panel • Note2: Display signals (D0+/-, D1+/-, D2+/-, D3+/- and CLK+/-) → Display signals (CLK, Hsync, Vsync, DE, DATA (R0 to R5, G0 to G5, B0 to B5)) (correction) P11 LCD panel signal processing board • Pin No.27- Signal Selection of DE / Fixed mode → Data enable signal - Remarks High or Open: Fixed mode, Data enable signal: DE mode → - P14 SCANNING DIRECTIONS (Revised) P15 INPUT SIGNAL TIMINGS - Outline of input signal timings (Change of the figure) • Note2: Fixed mode cannot be used while working of DE mode. (elimination) P16 Timing characteristics • (a) Fixedmode (elimination) • Note2 Hsync signal …. (elimination) P17 Input signal timing chart • (a) Fixed mode (elimination) P18 OPTICS- Optical characteristics • Color gamut: (72) (typ.) % → (60) (typ.) % P21 RELIABILITY TESTS • Heat cycle (elimination) • Thermal shock: ① -30 ± 3°C → -20 ± 3°C, 80 ± 3°C → 60 ± 3°C • ESD: (Revised) • Vibration: ① 19.6 m/s^2 → 11.76 m/s^2, ④ 120 times → 50 times • Mechanical shock: ① 539 m/s^2 → 490 m/s^2, ③ 5 times → 3 times P22 CAUTIONS • … no great than 539 m/s^2 and … → no great than 490 m/s^2 and … **Writer** *Approved by* K. FUJIMOTO *Checked by* ——— *Prepared by* E. YOSHIMURA

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
3rd edition	DOD-PP-1532	Dec. 17, 2012	**Revision contents** P5 GENERAL SPECIFICATIONS • Module size: 8.5 (D) → 8.25 (D) • Designed viewing direction: At DPS= TBD or Open → At DPS= Low or Open • Signal system: Horizontal synchronous signal, Vertical synchronous signal (elimination) • Power supply voltage - LED backlight: 5.0V → 5.0 to 12.0 V • Power consumption: VDD= 12.0V (addition) (3.3) W (typ.) → (4.0) W (typ.) P6 BLOCK DIAGRAM (Revised) P7 MECHANICAL SPECIFICATIONS • Module size: (8.5) ±0.5 (D) → 8.25 ±0.5 (D) P7 ABSOLUTE MAXIMUM RATINGS • Power supply voltage - LCD panel: TBD V → -0.3 to 6.5 V - LED driver: TBD V → -0.3 to 26.5 V • Input voltage for signals - Display signals, Function signal: TBD V → -0.3 to VCC+0.3V - Function signal for LED driver: TBD V → -0.3 to 26.5 V • Relative humidity - Rating: ≤ 95 →≤ 90, ≤ 85 →≤ 80 : ≤ 55, ≤ 36 (elimination) • Absolute humidity - Remarks: Ta > 70°C → Ta > 50°C • Note1: Hsync, Vsync (elimination) P8 LCD panel signal processing board • Power supply voltage: TBD (min., max.) V → 3.0 (min.), 3.6 (max.) V P9 Backlight • Power supply voltage: TBD (min.), 5.0 (typ.), TBD (max.) V → 4.5 (min.), - (typ.), (12.6) (max.) V • Power supply current - Remarks: At the maximum luminance control → at VCC= 5.0 V, at VCC= 12.0 V • Input voltage for PWM signal - High: TBD (min.) V → 2.0 (min.) V - Low: TBD (max.) V → 0.8 (max.) V • Input voltage for BRTC signal - High: TBD (min.) V → 2.0 (min.) V - Low: TBD (max.) V → 0.8 (max.) V • PWM duty ratio (addition) • PWM pulse width: TBD (min.) μs →10 (min.) μs • Note6: 5 μs →10 μs (correction) • Note7 (addition) • Note8 (addition) P9 Power supply voltage ripple • Power supply voltage - VDD: 5.0 V → 5.0 to 12.0 V P9 Fuse (specified) P10 LCD panel • VCC: TBD → 0.1 VCC (2points), 0.9 VCC (2points) : TBD ≤ Tr < TBD → (0.5ms) ≤ Tr < (10ms), Toff ≥ TBD →Toff ≥ (1000ms) • TBD < t < TBD → (0.5ms) < t < (50ms), TBD < t < TBD → (0ms) < t < (50ms) • * These signals…. (elimination) • Note2: Hsync, Vsync (elimination) P10 LED driver board • BRTC: TBD → 2.0 V (2points) : TBD < Tr < TBD → (10ms) ≤ Tr, TBD < Tf < TBD → (0ms) < Tf • PWM: 2.0 V (2points) : TBD < Tr < TBD → (10ms) < Tr, TBD < Tf < TBD → (0ms) < Tf • VDD: 4.2 V (2points) , 0.3 V (1point) , TBD < Tr < TBD → (0.5ms) ≤ Tr < (10ms)

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
3rd edition	DOD-PP-1532	Dec. 17, 2012	**Revision contents** P11 LCD panel signal processing board • CN1 socket: TBD → FH52-40S-0.5SH (HIROSE ELECTRIC CO., LTD.) • Adaptable plug: → [0.5mm pitch, Bottom Contact Type] • Pin No.3 - Hsync, Horizontal synchronous signal , - →N.C., - , Keep this pin Open • Pin No.4 - Vsync, Vertical synchronous signal , - →N.C., - , Keep this pin Open • Pin No.31 - Remarks: TBD Reverse scan → High Reverse scan TBD or Open Normal scan → Low or Open Normal scan P12 Positions of plug and socket (specified) P14 SCANNING DIRECTIONS • Figure1: TBD → Low • Figure2: TBD → High P16 Timing characteristics • CLK - Frequency: TBD (min., max.) MHz → 28.0 (min.), 36.0(max.) MHz - Duty: TBD (min., max.) MHz → 0.4 (min.), 0.6 (max.) - Rise time, Fall time: TBD (max.) ns → (10) (max.) ns • DATA - CLK-DATA - Setup time: TBD (min.) ns → 8 (min.) ns - Hold time: TBD (min.) ns → 8 (min.) ns - Rise time, Fall time: TBD (max.) → (10) (max.) ns • DE - Horizontal - Cycle: TBD (min., max.) µs → 28.44 (min.), 36.57 (max.) µs : TBD (min., max.) CLK → 889 (min.), 1,143 (max.) CLK • DE - Vertical - Cycle: TBD (min., max.) ms → 14.931 (min.), 19.19 (max.) ms : TBD (min., max.) H → 513 (min.), 767 (max.) H • DE - CLK-DE - Setup time: TBD (min.) ns → 8 (min.)ns - Hold time: TBD (min.) ns → 8 (min.) ns - Rise time, Fall time: TBD (max.) → (10) (max.) ns P18 Optical characteristics • Note2: VDD=5.0V, DPS= TBD or Open Normal scan →VDD=12.0V, DPS= Low or Open Normal scan P21 RELIABILITY TESTS • ESD: Contact Discharge ① 330Ω, ±8kV →150Ω, ±15kV : Air Discharge (elimination) • Vibration: ① 11.76 m/s^2 → 19.6m/s^2 ④ 50 times → 120 times • Mechanical shock: ① 490 m/s^2 → 539 m/s^2 ③ 3 times → 5 times P23 CAUTIONS • 490 m/s^2 → 539 m/s^2 P23 Handling of the product • ④ TBD N·m. → 0.23 N·m., TBD mm → 2.0 mm P25,26 OUTLINE DRAWINGS (specified) • Note2: TBD N·m. → 0.23 N·m., TBD mm → 2.0 mm **Writer** *Approved by* K. FUJIMOTO *Checked by* *Prepared by* E. YOSHIMURA

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and signature
4th edition	DOD-PP-1611	Apr. 5, 2013	**Revision contents** P4 FEATURES • Replaceable lamp for backlight (addition) P5 GENERAL SPECIFICATIONS • Viewing angle - Vertical: (60°) → (70°) • Backlight: Replaceable part (addition) • Power consumption: VDD=12.0V, (4.0) W (typ.) → VDD=5.0V, (1.7) W (typ.) P7 MECHANICAL SPECIFICATIONS • Weight: TBD (max.) g → (175) (max.) g P7 ABSOLUTE MAXIMUM RATINGS • Power supply voltage - LCD panel: -0.3 to 6.5 V → -0.3 to 3.96 V - LED driver: -0.3 to 26.5 V → -0.3 to 17.5 V • Input voltage for signals - Display signals: -0.3 to VCC+0.3 V → -0.5 to (VCC+0.5) V - Function signals: -0.3 to VCC+0.3 V → -0.5 to 4.6 V - Function signal for LED driver: -0.3 to 26.5 V → -0.3 to (11.2) V P8 LCD panel signal processing board • Power supply current: TBD (typ., max.) mA → (150) (typ.), (250) (max.) mA • Input voltage for DPS signal - Low: 0.3VCC (max.) V → (0.5) (max.) V P9 Backlight • Power supply voltage: (12.6) (max.) V → 12.6 (max.) V • Power supply current - VCC=5.0: TBD (typ., max.) mA → (240) (typ.), (260) (max.) mA - VCC=12.0: TBD (typ., max.) mA → (100) (typ.), (110) (max.) mA • Input voltage for PWM signal - High: - (max.) V → (5.5) (max.) V - Low: - (min.) V → 0 (min.) V • Input voltage for BRTC signal - High: - (max.) V → (5.5) (max.) V - Low: - (min.) V → 0 (min.) V P17 Input signal timing chart • CLK - tcrf (change) P18 Optical characteristics • Luminance: TBD (min.) cd/m^2 → (210) (min.) cd/m^2 • Contrast ratio: TBD (min.) → (480) (min.) • Color gamut: TBD (min.) % → (55) (min.) % • Response time: TBD (max.) ms → (5), (21), (26) (max.) ms • Viewing angle - (θR, θL, θU, θD): TBD (min.) ° → ((60), (60), (60), (60)) (min.) ° - θD: (60) (typ.) ° → (70) (typ.) ° • Note6: TopF= TBD°C → TopF= 25°C **Signature of writer** *Approved by* K. Fujimoto — K. FUJIMOTO *Checked by* — *Prepared by* E. Yoshimura — E. YOSHIMURA