LCD MODULE SPECIFICATION

Model : BI0500DAT

This module uses RoHS material

For Customer's Acceptance:

Customer	
Approved	
Comment	

REVISION RECORD

REV NO.	REV DATE	CONTENTS	REVISED PAGE NO.
1.0	2015-05-25	First Release	

CONTENTS

■ GENERAL INFORMATION

■ EXTERNAL DIMENSIONS

■ ABSOLUTE MAXIMUM RATINGS

■ ELECTRICAL CHARACTERISTICS

■ BACKLIGHT CHARACTERISTICS

■ ELECTRO-OPTICAL CHARACTERISTICS

■ INTERFACE DESCRIPTION

■ APPLICATION NOTES

■ RELIABILITY TEST

■ INSPECTION CRITERION

■ PRECAUTIONS FOR USING LCD MODULES

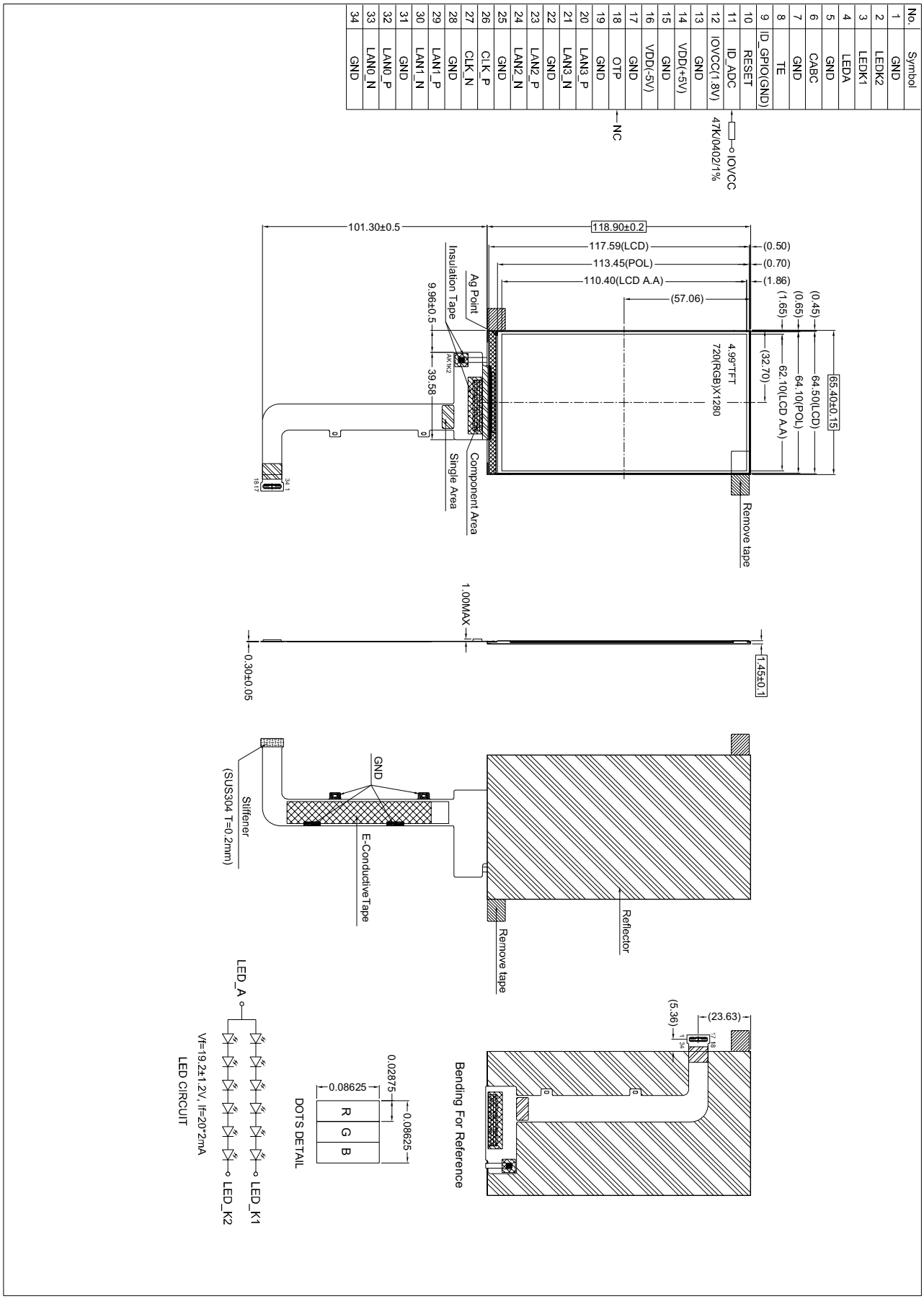
■ PRIOR CONSULT MATTER

■ GENERAL INFORMATION

Item	Contents	Unit
LCD type	A-SI SFT	/
Size	5.0	Inch
Viewing direction	Full viewing angle	O' Clock
LCM (W × H × D)	65.40×118.90×1.45	mm^3
Active area (W×H)	62.10×110.40	mm^2
Pixel pitch (W×H)	0.08625×0.08625	mm^2
Number of dots	720 (RGB) × 1280	/
Driver IC	ILI9881C	/
Backlight type	12 LEDs	/
Interface type	MIPI	/
Color depth	16.7M	/
Pixel configuration	R.G.B vertical stripe	/
Top polarizer surface treatment	Hard coating	/
Input voltage	TBD	V
With/Without TSP	Without TSP	/
TP surface treatment	TBD	/
Weight	TBD	g

Note 1: RoHS compliant;
Note 2: LCM weight tolerance: ± 5% .

■ EXTERNAL DIMENSIONS



■ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Logic supply voltage	VDDI	-0.3	3.3	V
Power supply voltage	VDD+	-0.3	6.5	V
	VDD-	-0.3	-6.5	V
Logic low level input voltage	VIL	-0.3	IOVCC*0.3	V
Logic high level input voltage	VIH	IOVCC*0.3	IOVCC	V
Backlight forward current	I_{LED}	-	25	mA
Operating temperature	T_{OP}	-20	70	°C
Storage temperature	T_{ST}	-30	80	°C

■ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Logic supply voltage	IOVCC	1.75	1.8	3.3	V
Power supply voltage	VDD+(VSP)	4.5	5.0	6.0	V
	VDD-(VSN)	-6.0	-5.0	-4.5	V
Input voltage ' H ' level	V_{IH}	0.7VDDI	-	VDDI	V
Input voltage ' L ' level	V_{IL}	GND	-	0.3VDDI	V
Output voltage ' H ' level	V_{OH}	0.8VDDI	-	VDDI	V
Output voltage ' L ' level	V_{OL}	GND	-	0.2VDDI	V

■ BACKLIGHT CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward voltage	Vf	-	19.2	-	V	Ta=25±2°C, 60%RH±5%
Forward current	If	-	40	-	mA	
Power consumption	W_{BL}	-	768	-	mW	
Operating life time	-	20,000	30,000	-	Hrs	

Note :

Operating life time means brightness goes down to 50% initial brightness;

The life time of LED will be reduced if LED is driven by high current,high ambient temperature and humidity conditions;

Typical operating life time is an estimated data.

■ELECTRO-OPTICAL CHARACTERISTICS

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark	Note
Response time		Tr+Tf	θ=0° ∅=0° Ta=25℃	25	35	-	ms	FIG 1.	4
Contrast ratio		Cr		600	800	-	---	FIG 2.	1
Luminance uniformity		δ WHITE		70	80	-	%	FIG 2.	3
Surface Luminance		Lv		400	430	-	cd/m^2	FIG 2.	2
Viewing angle range		θ	∅ = 90°	70	80	-	deg	FIG 3.	6
			∅ = 270°	70	80	-	deg	FIG 3.	
			∅ = 0°	70	80	-	deg	FIG 3.	
			∅ = 180°	70	80	-	deg	FIG 3.	
CIE (x, y) chromaticity	Red	x	θ=0° ∅=0° Ta=25℃	0.571	0.621	0.671		FIG 2.	5
		y		0.271	0.321	0.371			
	Green	x		0.261	0.311	0.361			
		y		0.579	0.629	0.679			
	Blue	x		0.105	0.155	0.205			
		y		0.002	0.052	0.102			
	White	x		0.260	0.290	0.320			
		y		0.280	0.300	0.340			
NTSC	-	-	-	60	70	-	%	-	-

Note 1. Contrast Ratio(CR) is defined mathematically as For more information see FIG 2.

$$\text{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P 3,P4, P5)}}$$

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see FIG 2.

Lv = Average Surface Luminance with all white pixels (P1, P2, P 3, P4, P5)

Note 3. The uniformity in surface luminance ， δ WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the maximum luminance of 5 points luminance by minimum luminance of 5 points luminance. For more information see FIG 2.

$$\delta\ \text{WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P 3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P 3, P4, P5)}}$$

Note 4. Response time is the time required for the display to transition from White to black(Rise Time, Tr) and from black to white(Decay Time, Tf). For additional information see FIG 1. The test equipment is Autronic-Melchers's ConoScope. Series.

Note 5. CIE (x, y) chromaticity，The x, y value is determined by measuring luminance at each test position 1 through 5,and then make average value.

Note 6. Viewing angle is the angle at which the contrast ratio is greater than 2. For TFT module the conrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 3.

Note 7. For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope. Series Instruments For contrast ratio, Surface Luminance, Luminance uniformity, CIE The test data is base on TOPCON's BM-5 photo detector.

FIG. 1 The definition of Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".

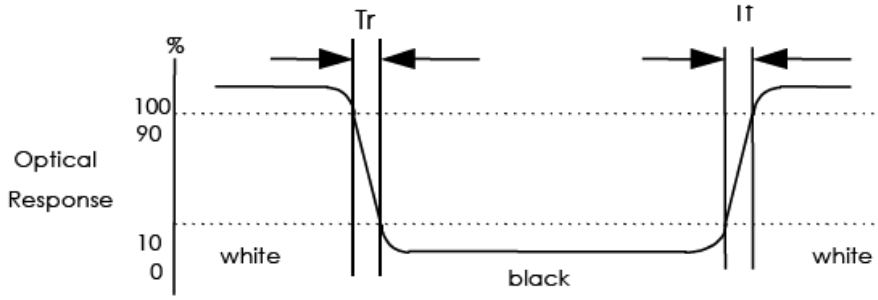
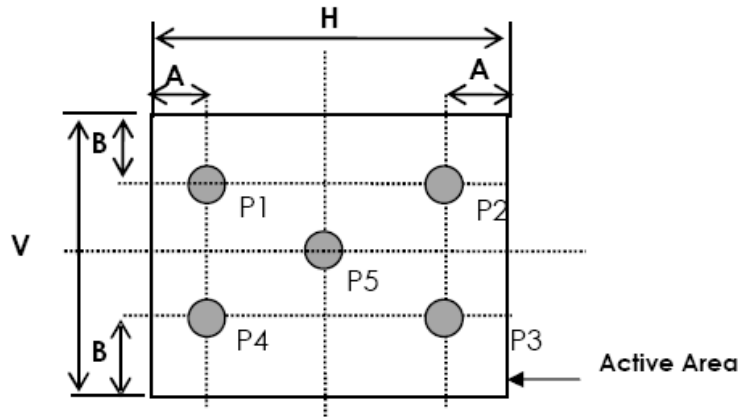
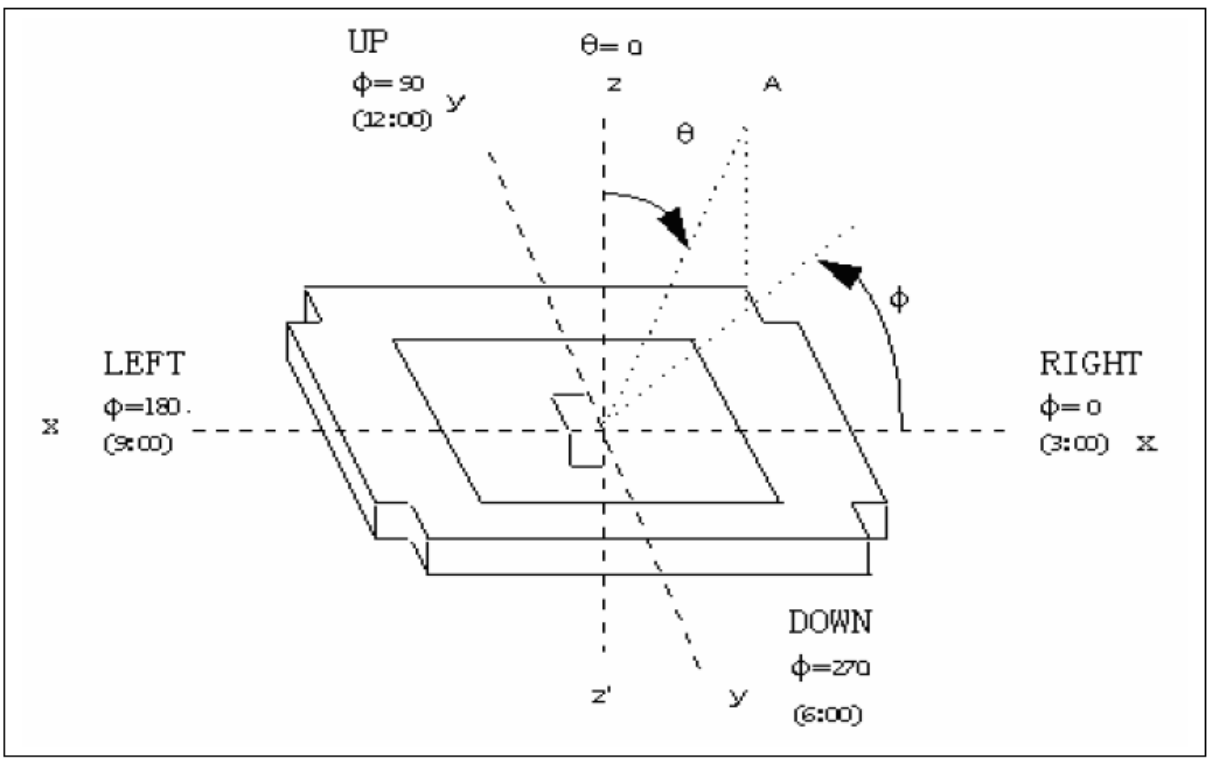


FIG. 2 Measuring method for Contrast ratio, surface luminance, Luminance uniformity , CIE (x, y) chromaticity



A : 5 mm
B : 5 mm
H,V : Active Area
Light spot size ∅=7mm, 500mm distance from the LCD surface to detector lens
measurement instrument is TOPCON's luminance meter BM-5

FIG. 3 The definition of viewing angle



■INTERFACE DESCRIPTION

Pin No.	Symbol	I/O	Function
1	GND	p	Power ground
2	LEDK2	P	Cathode for LED backlighting
3	LEDK1	p	Cathode for LED backlighting
4	LEDA	P	Anode for LED backlighting
5	GND	p	Power ground
6	CABC	P	CABC function enable
7	GND	P	Power ground
8	TE	I/O	
9	ID_GPIO(GND)	I	ID
10	RESET	I	Reset pin
11	ID_ADC	I	ID
12	IOVCC(1.8V)	P	1.8V
13	GND	P	Power ground
14	VDD(+5V)	P	+5V
15	GND	P	Power ground
16	VDD(-5V)	P	-5V
17	GND	P	Power ground
18	OTP	I/O	NC
19	GND	P	Power ground
20	LAN3_P	I	MIPI data input
21	LAN3_N	I	MIPI data input
22	GND	P	Power ground

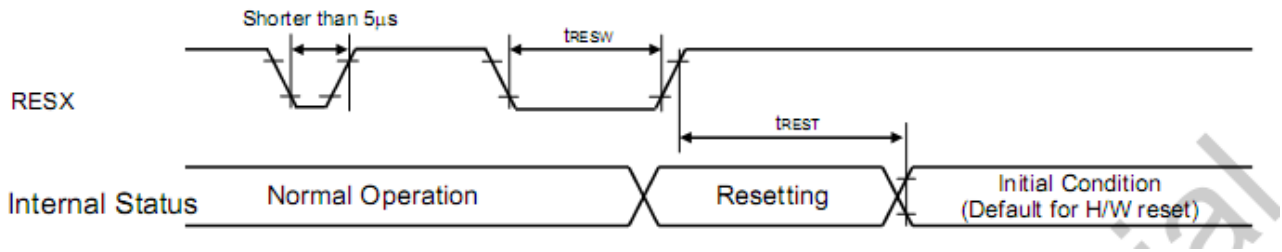
23	LAN2_P	I	MIPI data input
24	LAN2_N	I	MIPI data input
25	GND	P	Power ground
26	CLK_P	I	MIPI CLK input
27	CLK_N	I	MIPI CLK input
28	GND	P	Power ground
29	LAN1_P	I	MIPI data input
30	LAN1_N	I	MIPI data input
31	GND	P	Power ground
32	LAN0_P	I	MIPI data input
33	LAN0_N	I	MIPI data input
34	GND	P	Power ground

Note1：Please add the FPC connector type and matched one if necessary .

■ APPLICATION NOTES

1 Timing chart

1.1 Reset Timing Characteristics



Reset input timing

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

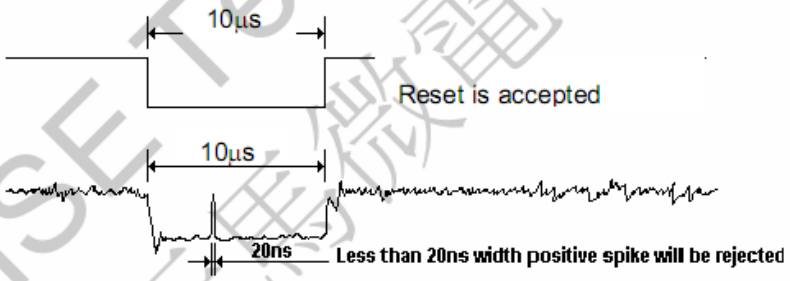
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, ID1/ID2/ID3/ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

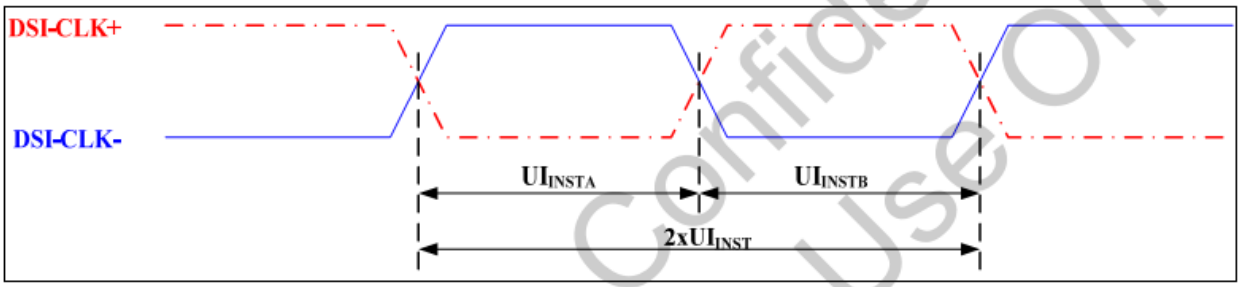
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

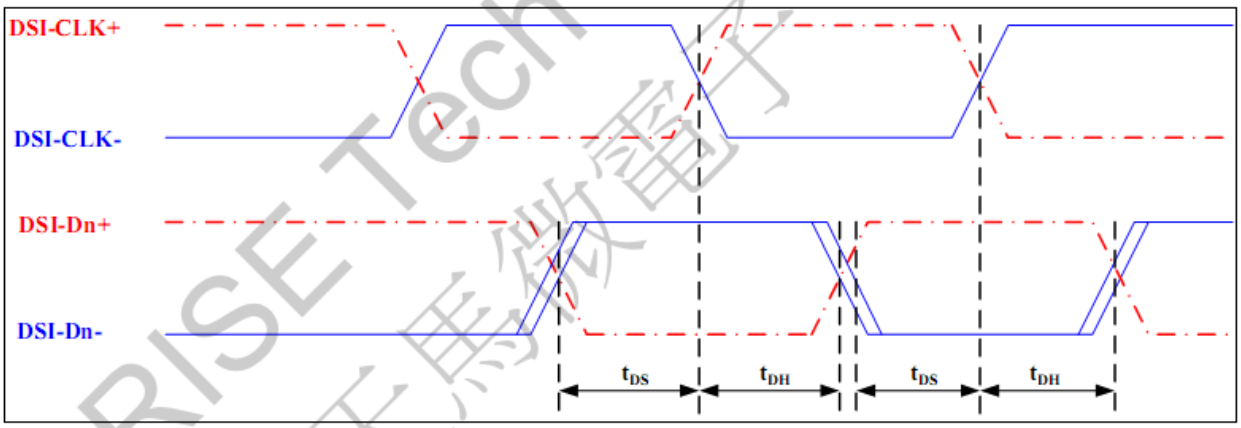


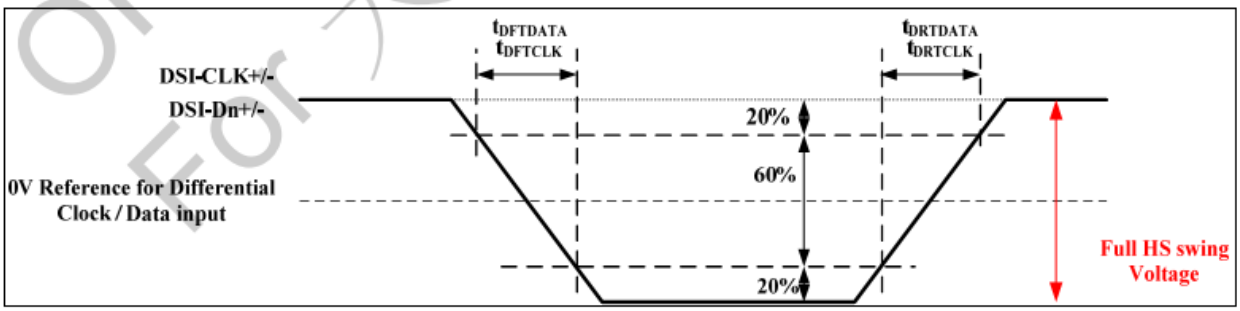
Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

1.2 High Speed Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	2	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps



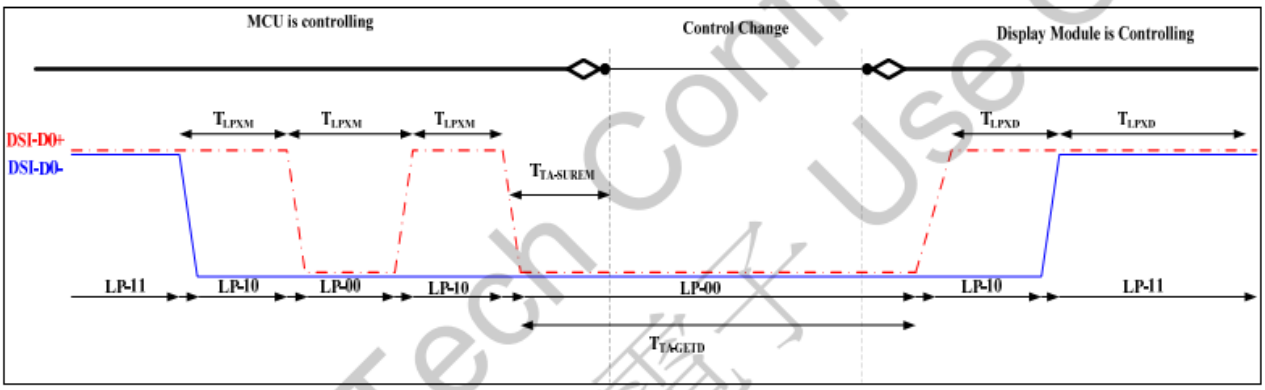




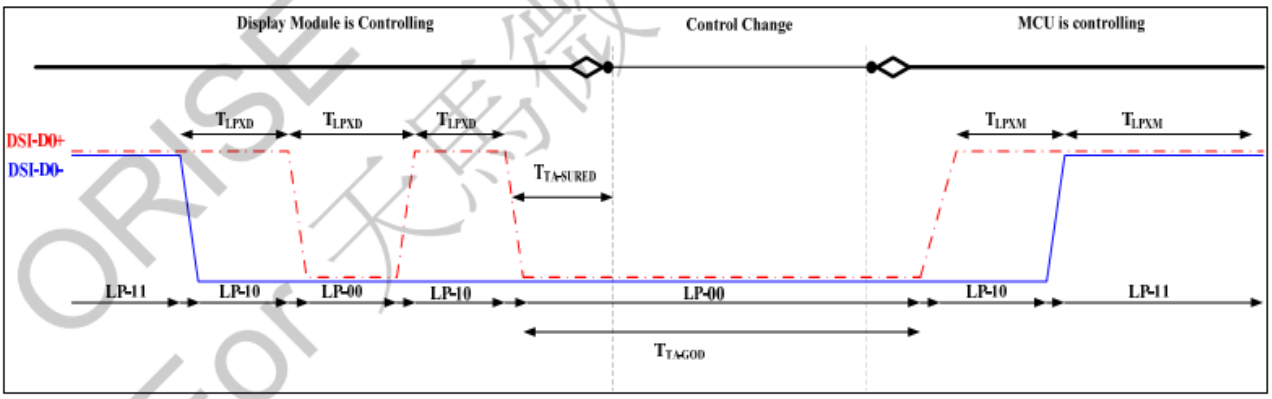
AC characteristics for MIPI-DSI High speed mode

1.3 Low Speed Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	58	-	-	ns
DSI-D0+/-	$T_{TA\text{-}SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA\text{-}GETD}$	Time to drive LP-00 by display module	$5XT_{LPXD}$	-	-	ns
DSI-D0+/-	$T_{TA\text{-}GOD}$	Time to drive LP-00 after turnaround request - MPU	$4XT_{LPXD}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	



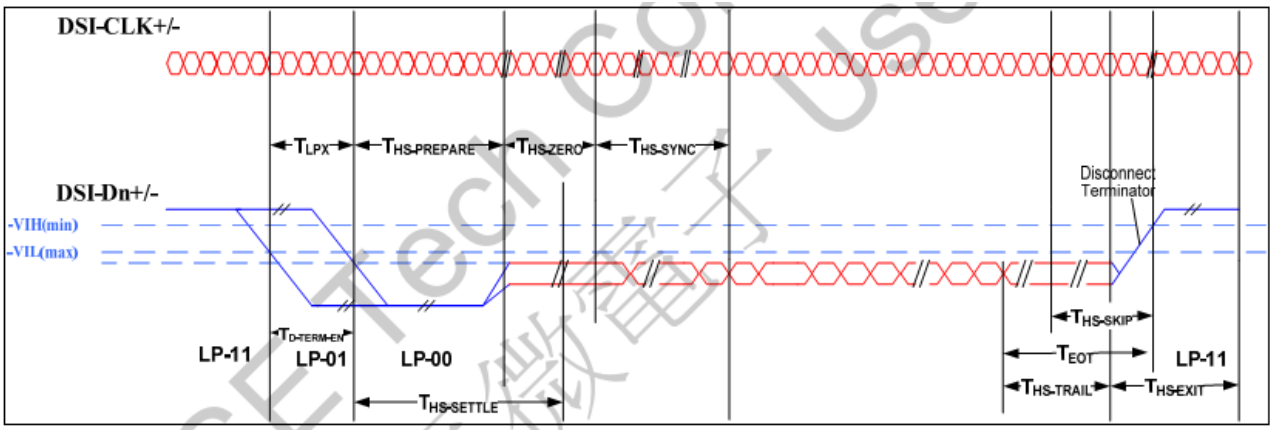
BTA from the MCU to the Display Module



BTA from the the Display Module to the MCU

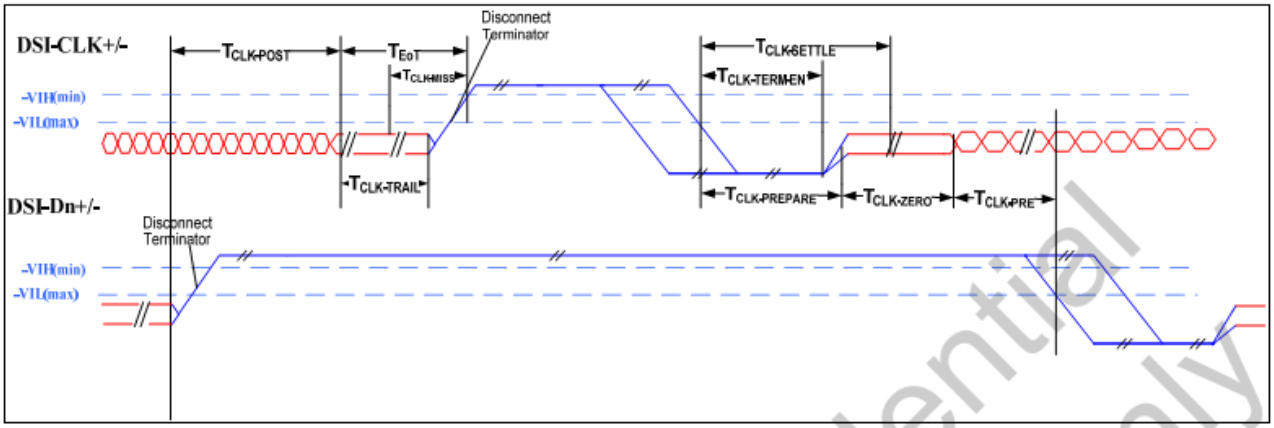
1.4 Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS\text{-}PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS\text{-}PREPARE}$ +$T_{HS\text{-}ZERO}$	$T_{HS\text{-}PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D\text{-}TERM\text{-}EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM\text{-}EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS\text{-}SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS\text{-}TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS\text{-}EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS\text{-}TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns



High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK\text{-}POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK\text{-}PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK\text{-}PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK\text{-}TERM\text{-}EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM\text{-}EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK\text{-}PREPARE}$ +$T_{CLK\text{-}ZERO}$	$T_{CLK\text{-}PREPARE}$ + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK\text{-}TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK\text{-}TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns



Switching the clock Lane between clock Transmission and Low Power Mode

1.5 LP-11 Between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when 4 different combinations, what are listed below, are possible:

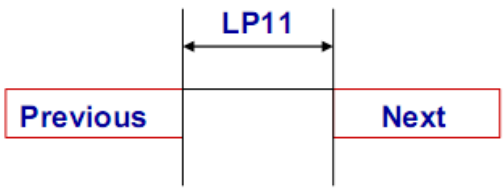
1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100 ns	-	100 ns	-	100 ns	-
HSDT	60ns + 52UI	-	60ns + 52UI	-	60ns + 52UI	-
BTA	100 ns	-	100 ns	-	100 ns	-

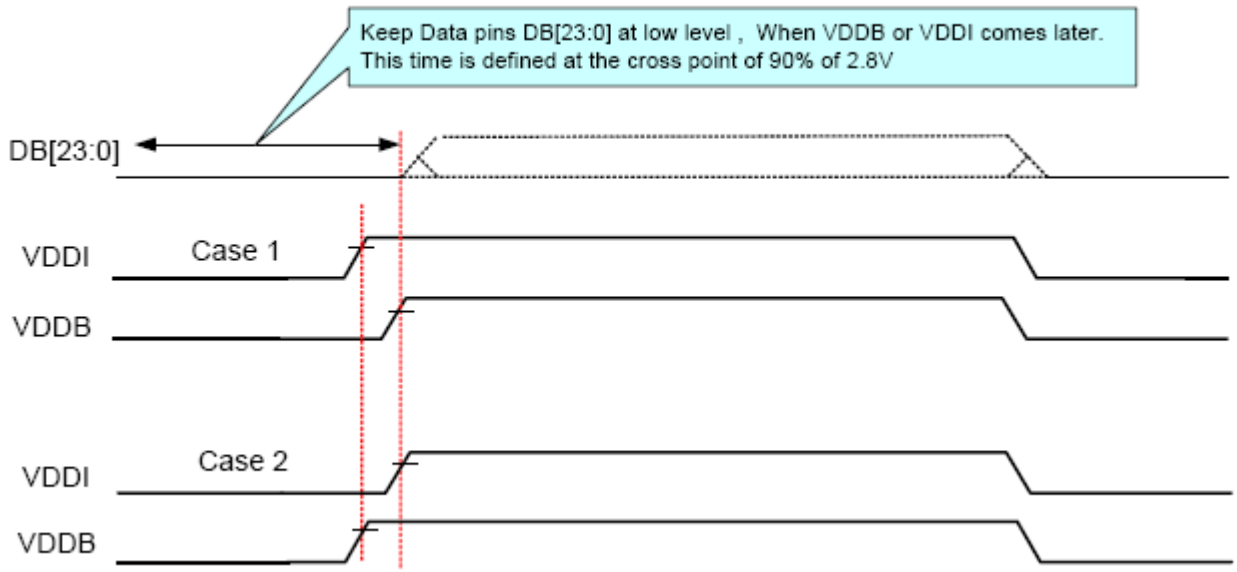


1.6 Power On/Off Sequence

VDDI and VDDA can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note:

1. There will be no damage to ILI9806C if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 13.1 and 13.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. Keep data pins DB[23:0] at low level, when VDDB or VDDI comes later



■ RELIABILITY TEST

No	Test Item	Test condition	Remark
1	High Temperature Storage	80℃±2℃96Hrs	
2	Low Temperature Storage	-30℃±2℃ 96Hrs	
3	High Temperature Operation	70℃±2℃96Hrs	
4	Low Temperature Operation	-20℃±2℃ 96Hrs	
5	High Temperature & Humidity Storage	60℃±2℃ 90%RH 96Hrs	
6	Temperature Cycle	−30℃← →80℃ 30min 30min after 32cycle, change time 30s Restore 2H at 25℃ Power off	
7	Vibration Test	Frequency:10Hz~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz, 120min ±x,±Y,±Z for each direction	1Carton-box
8	Shock Test	Half-sine wave,600m/s2,6ms ±x,±Y,±Z 3 times,for each direction	-
9	Drop Test(package state)	800mm, concrete floor,1corner, 3edges, 6 sides each time	1Carton-box
10	ESD Sensitivity test	5points/panel Contact ±4KV，150PF/330，5times Air ±8KV,150PF/330，5times	-

Note:

1.Sample size for each test item is 5~10pcs.

2.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

3.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part. Using ionizer(an antistatic blower)