PART NO : EE150XGA02

CUSTOMER :_____

Accepted by :_____

Proposed by :_____

Date : 06,04,2004

RECORD OF REVISION

DATE	PAGE	SUMMARY

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1.0 GENERAL DESCRIPTIONS

1.1 Introduction

Model EE150XGA02 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, the voltage reference, common voltage , DC-DC converter, column, and row driver circuit. This TFT LCD has a 15-inch diagonally measured active display area with XGA resolution (768 vertical by 1024 horizontal pixel array).

1.2 Features

15” XGA TFT LCD panel
4 CCFLs Backlight system
Supported XGA (V : 768 lines, H : 1024 pixels) resolution
Supported to 75HZ refresh rate
Without LCD Timing Controller

1.3 General information

Item	Specification	Unit
Outline dimension	331.5 × 254.6 × 12	mm
Display area	304.1(H) × 228.1(V) (15.0” diagonal)	mm
Number of Pixel	1024(H) × 768(V)	pixels
Pixel pitch	0.297(H) × 0.297(V)	mm
Pixel arrangement	RGB Vertical stripe	
Display color	6-bits driver	
Display mode	Normally white	
Surface treatment	Antiglare	
Weight	950 (Typ.)	g
Back-light	4-CCFLs,Top & bottom edge side	
Power consumption	9.2 Watt (Typ)	
Input signal	Source and Gate Driver control signals	
Optimum viewing direction	6 o’ clock	

1.4 Applications

Desktop monitors
Display terminals for AV applications
Monitors for industrial applications

1.5 Mechanical information

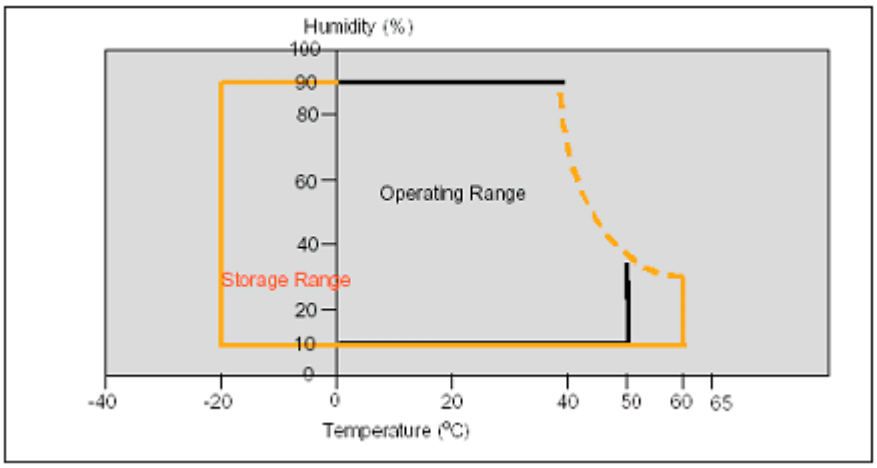
Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal(H)	-----	331.5	-----	mm
	Vertical(V)	-----	254.6	-----	mm
	Depth(D)	-----	12	-----	mm
Weight (without inverter)		-----	950	-----	g

2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Absolute Rating of Environment

Item	Symbol	Min.	Max.	Unit	Note
Storage temperature	T_{STG}	-20	60	°C	
Operating temperature	T_{OPR}	0	50	°C	
Vibration(non-operating)	V_{NOP}	---	1.5	G	(1)
Shock(non-operating)	S_{NOP}	---	70	G	(2)
Storage humidity	H_{STG}	10	90	%RH	(3)
Operating humidity	H_{DP}	10	80	%RH	(3)
Low pressure(operating)	P_{LOP}	697	---	HPa	(4)
Low pressure(non-operating)	P_{LNOP}	116	---	HPa	(5)

Note (1) 5-500Hz sine wave,X,Y,Z each directions, 30 min/cycle.
(2) 11ms, ±X , ±Y , ±Z direction, one time each. For this shock test, it is necessary to fill the silicon rubber between the shock jig as buffer.
(3) Max wet bulb temp.=39°C
(4) 2hrs.(10000 feet)
(5) 24hrs.(50000 feet)



2.2 Electrical Absolute Rating :

2.2.1 TFT LCD Module :

Item	Symbol	Condition	Value		Unit
			min.	max.	
Input Power Voltage	V_{DD}	Normal	+3.0	+3.6	V(DC)
Logic Signal input voltage	V_{SIG}	Normal	-0.3	VDD +0.3	V

2.2.2 Back Light Unit :

Item	Symbol	Min.	Max.	Unit	Note
Lamp voltage	V_L	0	2000	V(rms)	(1)
Lamp current	I_L	---	7.0	mA	(1)
Lamp frequency	f_L	0	100	KHz	(1)

Note : (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

3.0 OPTICAL CHARACTERISTICS

3.1 Measuring Condition

Measuring surrounding : dark room

Lamp current I_{BL} : (6.0)±0.1mA , lamp freq. F_L=50KHz

V_{DD1}=3.3V,fv=60Hz,F_{DCLK}=32.5MHz

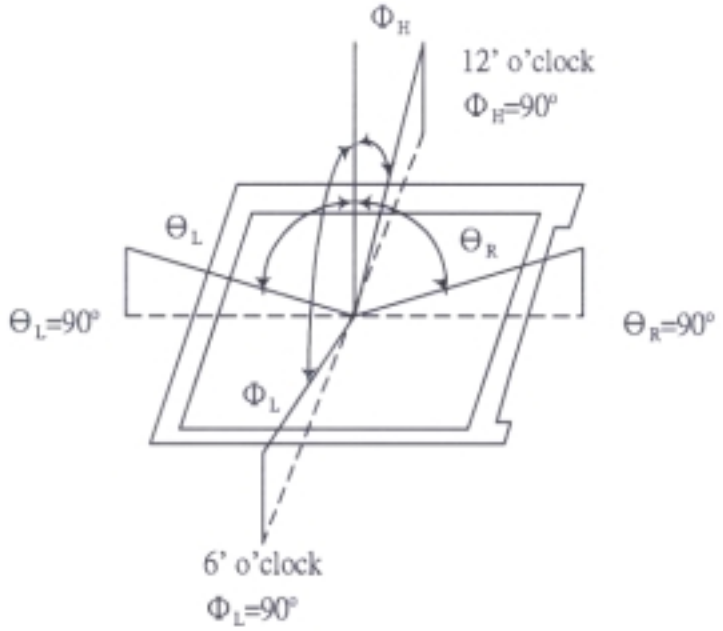
Surrounding temperature : 25±2°C

30min. Warm-up time.

3.2 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast		CR	θ = 0° φ = 0° Normal viewing angle	400	500	---		(1),(2),(5)
White luminance (center of screen)		Y_L		---	300		cd/m^2	
Response time	Rising	T_R		---	T_R+T_F =(35)	---	msec	(1),(3),(5)
	Falling	T_F		---		---		
Color chromaticity (CIE 1931)	Red	Rx		---	(0.623)	---		(1),(4),(5)
		Ry		---	(0.335)	---		
	Green	Gx		---	(0.293)	---		
		Gy		---	(0.599)	---		
	Blue	Bx		---	(0.144)	---		
		By		---	(0.113)	---		
	White	Wx		---	(0.310)	---		
		Wy		---	(0.330)	---		
Viewing angle	Hor.	θ_L	CR>10	---	60	---		
		θ_R		---	60	---		
	Ver.	θ_H		---	40	---		
		θ_L		---	50	---		

Note (1) Definition of Viewing Angle :

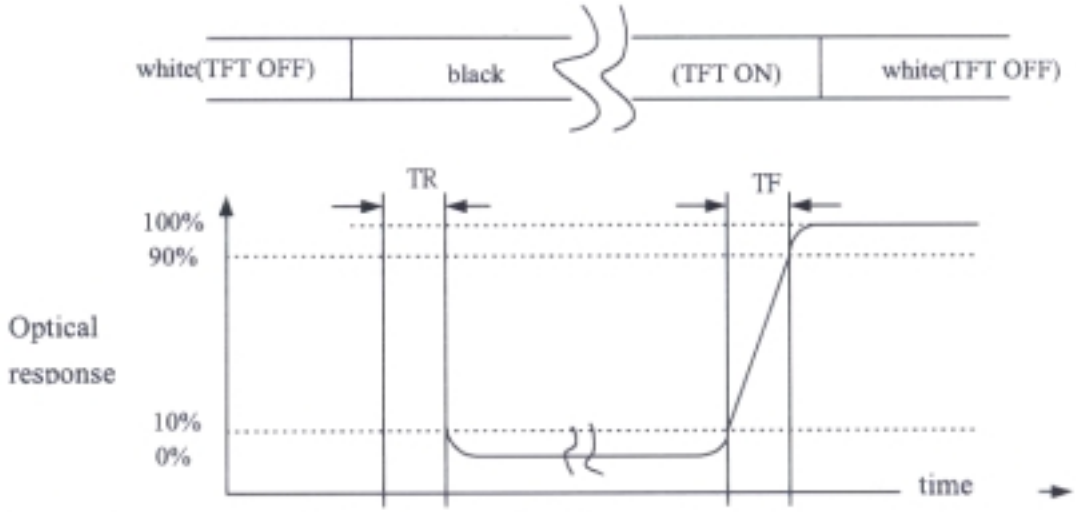


Note (2) Definition of Contrast Ratio (CR) :

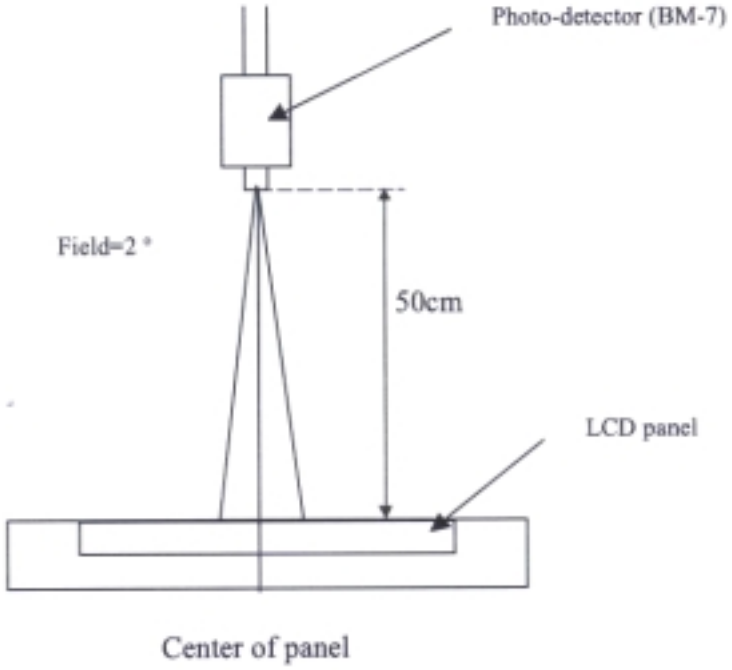
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white (L63)}}{\text{Luminance with all pixels black (L0)}}$$

Note (3) Definition of Response Time : Sum of T_R and T_F

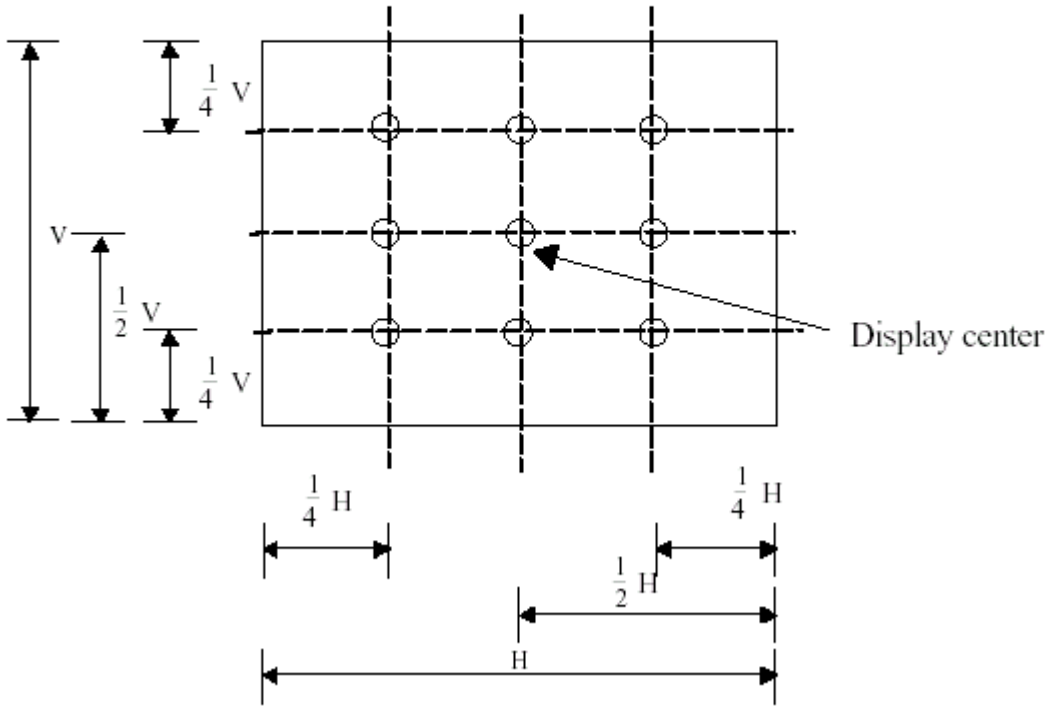


Note (4) Optical characteristics measurement setup



Note (5) Definition of brightness uniformity

Luminance uniformity =(Min Luminance)/(Max Luminance) x 100%



Note (6) Definition of crosstalk CT(1) ~ CT(4)

$$CT(n) = \frac{\left| L(n) - LB(n) \right|}{L(n)} \times 100\% \text{ , } n = 1 \sim 4$$

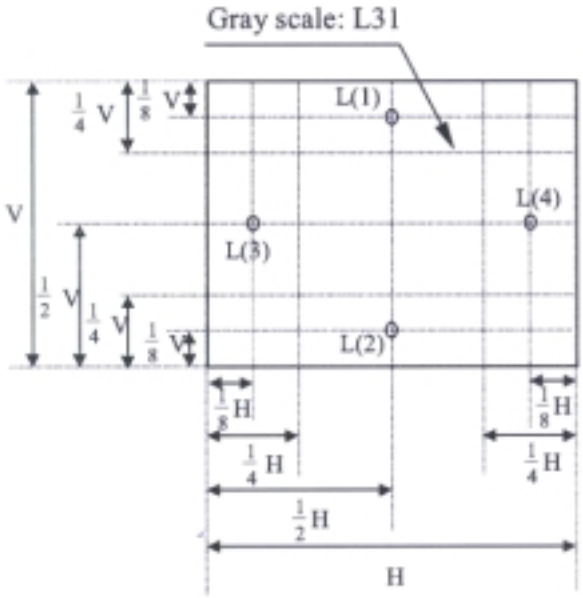
Where L(n) = Luminance of point "n" at pattern A (cd/m^2) , n=1～4

LB(n) = Luminance of point "n" at pattern B (cd/m^2) , n=1～4

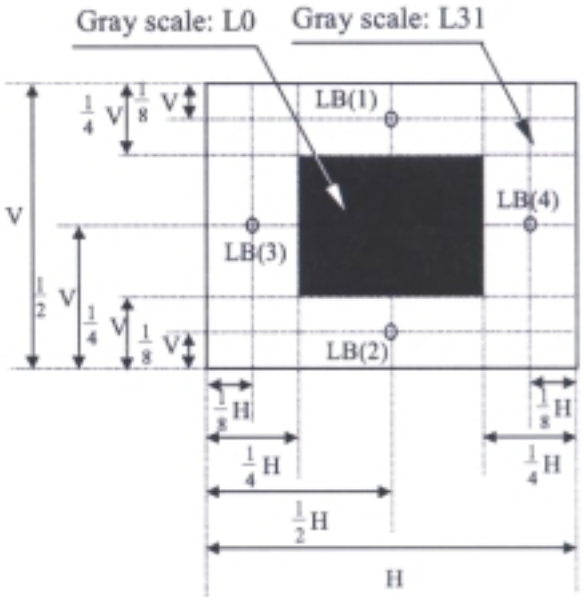
The location measured will be exactly the same in both patterns.

L0 : Luminance with all pixels black

L63 : Luminance with all pixels white



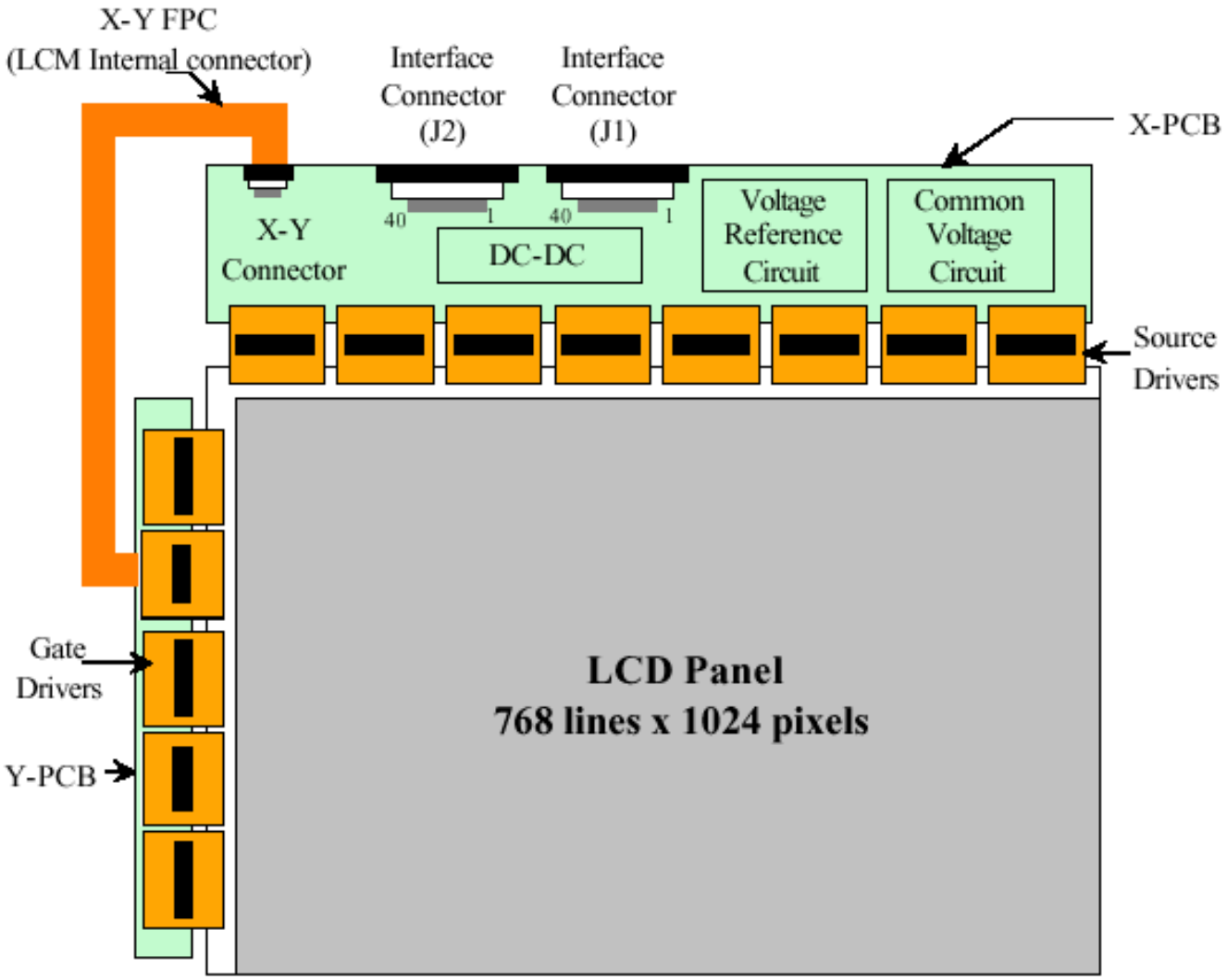
Pattern A



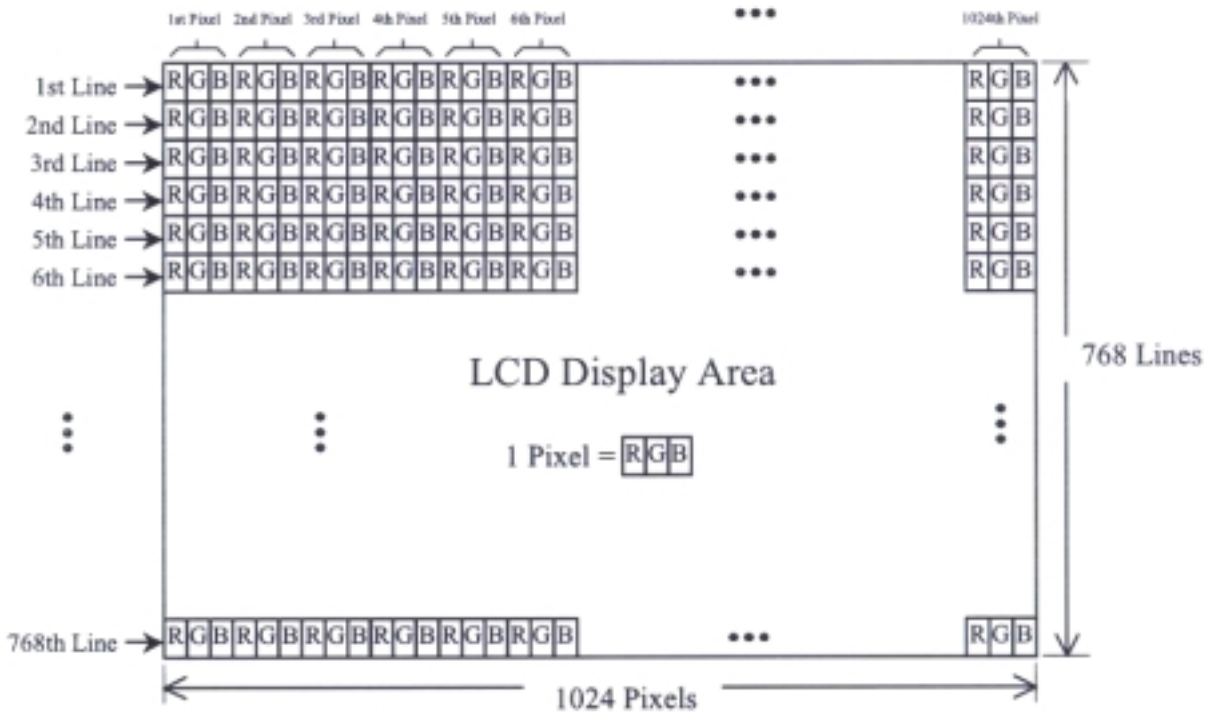
Pattern B

4.0 BLOCK DIAGRAM

4.1 LCD Module Block Diagram:



4.2 Pixel Format



4.3 Relationship between Displayed Color and Input Data

	Display	MSB R5	R4	R3	R2	R1	LSB R0	MSB G5	G4	G3	G2	G1	LSB G0	MSB B5	B4	B3	B2	B1	LSB B0	Gray scale level
Basic color	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	-
	Blue	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	-
	Green	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	-
	Light Blue	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	-
	Red	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	-
	Purple	H	H	H	H	H	H	L	L	L	L	L	L	H	H	H	H	H	H	-
	Yellow	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	-
	White	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	-
Gray scale of Red	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L1
		L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L2
				:						:						:				L3..L60
	Light	H	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L61
		H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L62
	Red	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	Red L63
Gray scale of Green	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L1
		L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L2
				:						:						:				L3..L60
	Light	L	L	L	L	L	L	H	H	H	H	L	H	L	L	L	L	L	L	L61
		L	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	L62
	Green	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	Green L63
Gray scale of Blue	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L1
		L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L2
				:						:						:				L3..L60
	Light	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H	L61
		L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L	L62
	Blue	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	Blue L63
Gray scale of White and Black	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	H	L1
		L	L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	H	L	L2
				:						:						:				L3..L60
	Light	H	H	H	H	L	H	H	H	H	H	L	H	H	H	H	H	L	H	L61
		H	H	H	H	H	L	H	H	H	H	H	L	H	H	H	H	H	L	L62
	White	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	White L63

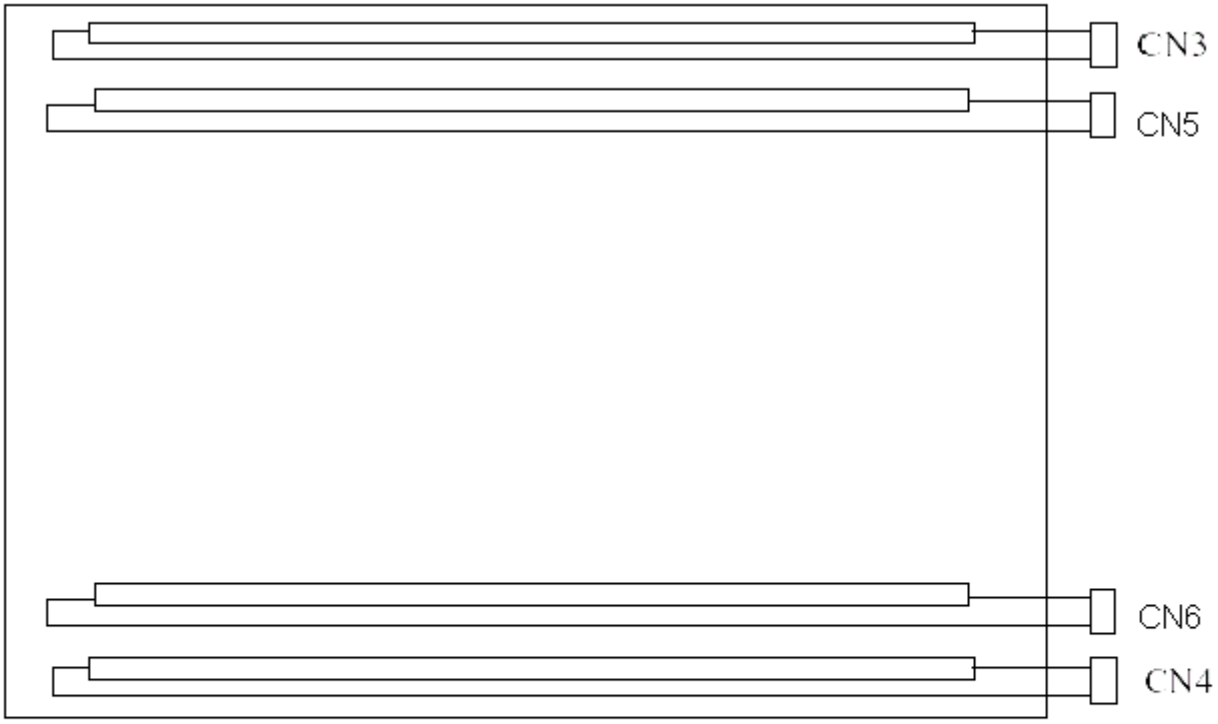
5.0 I/O CONNECTION PIN ASSIGNMENT

5.1 Interface FPC Connector (40-pins x 2)

I/F FRC Connector (J1)			I/F FRC Connector (J2)		
Pin NO.	Symbol	Description	Pin NO.	Symbol	Description
1	NC	No Connecting	1	VDD	Digital Power Input (DC +3.3V)
2	NC	No Connecting	2	VDD	Digital Power Input (DC +3.3V)
3	GND	Ground	3	GND	Ground
4	GND	Ground	4	GND	Ground
5	EB5	Even-dot Blue Data bit 5 (MSB)	5	OB5	Odd-dot Blue Data bit 5 (MSB)
6	EB4	Even-dot Blue Data bit 4	6	OB4	Odd-dot Blue Data bit 4
7	EB3	Even-dot Blue Data bit 3	7	OB3	Odd-dot Blue Data bit 3
8	EB2	Even-dot Blue Data bit 2	8	OB2	Odd-dot Blue Data bit 2
9	EB1	Even-dot Blue Data bit 1	9	OB1	Odd-dot Blue Data bit 1
10	EB0	Even-dot Blue Data bit 0 (LSB)	10	OB0	Odd-dot Blue Data bit 0 (LSB)
11	GND	Ground	11	GND	Ground
12	EG5	Even-dot Green Data bit 5 (MSB)	12	OG5	Odd-dot Green Data bit 5 (MSB)
13	EG4	Even-dot Green Data bit 4	13	OG4	Odd-dot Green Data bit 4
14	ER3	Even-dot Green Data bit 3	14	OG3	Odd-dot Green Data bit 3
15	EG2	Even-dot Green Data bit 2	15	OG2	Odd-dot Green Data bit 2
16	EG1	Even-dot Green Data bit 1	16	OG1	Odd-dot Green Data bit 1
17	EG0	Even-dot Green Data bit 0 (LSB)	17	OG0	Odd-dot Green Data bit 0 (LSB)
18	GND	Ground	18	GND	Ground
19	ER5	Even-dot Red Data bit 5 (MSB)	19	OR5	Odd-dot Red Data bit 5 (MSB)
20	ER4	Even-dot Red Data bit 4	20	OR4	Odd-dot Red Data bit 4
21	ER3	Even-dot Red Data bit 3	21	OR3	Odd-dot Red Data bit 3
22	ER2	Even-dot Red Data bit 2	22	OR2	Odd-dot Red Data bit 2
23	ER1	Even-dot Red Data bit 1	23	OR1	Odd-dot Red Data bit 1
24	ER0	Even-dot Red Data bit 0 (LSB)	24	OR0	Odd-dot Red Data bit 0 (LSB)
25	GND	Ground	25	GND	Ground
26	CPH1	Pixel Clock Input	26	CPH2	Pixel Clock Input
27	GND	Ground	27	GND	Ground
28	GND	Ground	28	GND	Ground
29	STH	Horizontal Start Pulse	29	NC	No Connecting
30	LOAD	Source Driver Latch Pulse	30	NC	No Connecting
31	POL	Source Driver Output Polarity control	31	NC	No Connecting
32	REV	Data Reverse Control Signal	32	NC	No Connecting
33	GND	Ground	33	NC	No Connecting
34	GND	Ground	34	NC	No Connecting
35	STV1	Vertical Start Pulse 1	35	NC	No Connecting
36	STV2	Vertical Start Pulse 2	36	NC	No Connecting
37	CPV	Vertical Clock Input	37	NC	No Connecting
38	OE	Gate Driver Output Enable Signal	38	NC	No Connecting
39	GND	Ground	39	GND	Ground
40	GND	Ground	40	GND	Ground

FH 12-40S-0.5SH (Hirose) or equivalent

5.2 Back Light Unit (CCFL) Connectors :



The backlight interface connector is a modol BHSR-02VS-1, manufactured by JST, The mating Connector part number is SM02B-BHSS-1-TB or equivalent.

Terminal No.	Symbol	Function
1	VL	CCFL power supply (high voltage)
2	GL	CCFL power supply (low voltage)

6.0 ELECTRICAL CHARACTERISTICS

6.1 Electrical System of LCD Module :

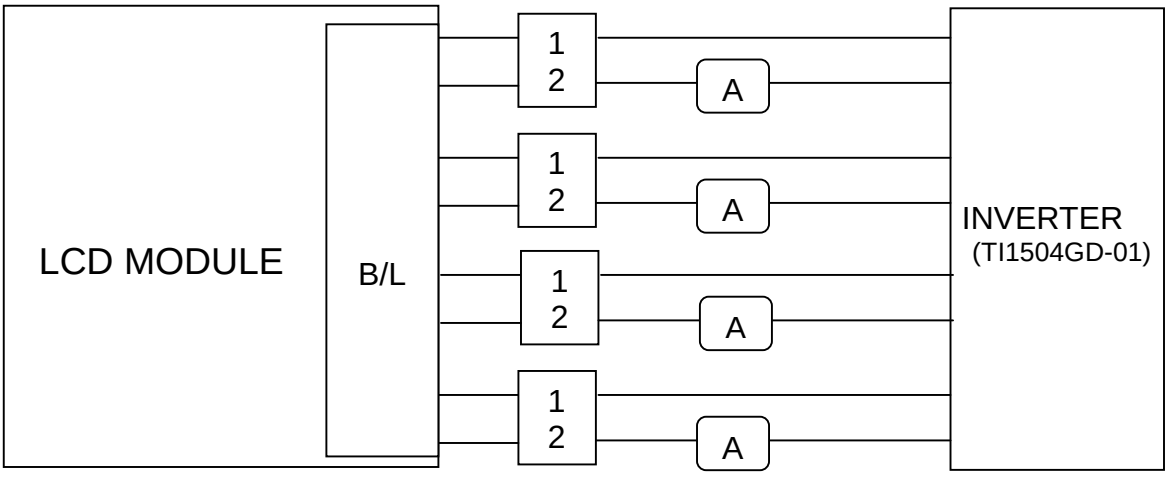
Item	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input Voltage	V_{DD}		+3.0	+3.3	+3.6	V(DC)
Input Signal voltage	V_{IH}	High Level	0.7* VDD2	-----	VDD+0.2	V
	V_{IL}	Low Level	0	-----	0.3*VDD2	V

6.2 Back-Light Unit :

The back-light system is an edge-lighting type with CCFL (Cold Cathode Fluorescent Lamp). The characteristics of four lamps are shown in the following tables.

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Lamp current	I_L	4.68	4.70	4.76	mA(rms)	(1)
Lamp voltage	V_L	565	----	580	V(ms)	I_L=6.0mA
Frequency	f_L	----	33	----	KHz	(2)
Operating life time	Hr	25000	----	35000	Hour	(3)
Startup voltage	V_S	710	----	728	V(rms)	at 25°C
		----	1350	----	V(rms)	at 25°C

Note: (1) Lamp current is measured with current meter for high frequency as shown below.Specified Values are for a lamp.



(2) Lamp frequency may produce interference with horizontal synchronous frequency and this may cause line flow on the display. Therefore lamp frequency shall be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.

(3) Life time (Hr) can be defined as the time in which it continues to operate under the condition: Temp. =25±3°C,I_L=6.0mA(rms.) and f_L=50 KHz until one of the following event occurs:

1. When the brightness becomes 50%.
2. When the startup voltage (Vs) at 0°C becomes higher than the maximal value of Vs specified above.

6.3 AC Electrical Characteristics:

6.3.1 AC Timing: (VDD=3.0V~3.6V, T_{OPR}=25°C) [5)]

Item		Symbol	Min.	Typ.	Max.	Unit	Signals	Note
Reference Signal (Pixel Clock)	Periodic	F1 T1=CLK T2=T1*2	50 12.5 25	65 15.384 30.769	80 20 40	MHz n-Sec n-Sec		
Reference Signal (DENB)	Line Periodic	T3=Line	526	672	900	T2		1), 2), 4)
	Line Active	T4	512	512	512	T2		
	Line Blank	T5	14	160	388	T2		
	Frame Periodic	T6	773	806	950	Lines		
	Frame Active	T7	768	768	768	Lines		
	Frame Blank	T8	5	---	---	Lines		
Vertical Periodic	Periodic	T6	773	806	950	Lines	STV1 STV2	2)
	Pulse Width	T9 T10	1 2	1 2	--- ---	Lines		
	Rising Time	T11	---	40	60	n-Sec		
	Falling Time	T12	---	40	60	n-Sec		
	Set-up Time	T13	700	800	---	n-Sec		
	Hold Time	T14	700	800	---	n-Sec		
Horizontal Periodic	Period	T15	---	1	---	Lines	OE CPV LOAD STH	
	Pulse Width	T16A T16B T16C T16D	1 1 2 25	--- --- 64 30.769	--- --- 100 40	u-Sec u-Sec T2 n-Sec		
	Rising Time	T17A T17B T17C T17D	--- --- 2 2	40 40 4 4	60 60 --- ---	n-Sec		
	Falling Time	T18A T18B T18C T18D	--- --- 2 2	40 40 4 4	60 60 --- ---	n-Sec		
	Set-up Time	T19A T19B	7 7	10 10	---	n-Sec	LOAD STH	
	Hold Time	T20A T20B	7 7	10 10	---	n-Sec		

Item		Symbol	Min.	Typ.	Max.	Unit	Signals	Note
Horizontal Periodic	Period	T21	---	2	---	Lines	POL	
	Pulse Width	T22	---	1	---	Lines		
	Rising Time	T23	7	10	---	n-Sec		
	Falling Time	T24	7	10	---	n-Sec		
	Set-up Time	T25	-5	---	---	n-Sec		
	Hold Time	T26	6	---	---	n-Sec		
Clock	Period	T2	25.00	30.769	40	n-Sec	CPH1 CPH2	3)
	Rising Time	T27	2	4	---	n-Sec		
	Falling Time	T28	2	4	---	n-Sec		
Image Data And Data Reverse Control Pin	Setup time	T29	2	---	---	n-Sec	ER(5:0) EG(5:0) EB(5:0) OR(5:0) OG(5:0) OB(5:0) REV	
	Hold time	T30	2	---	---	n-Sec		
Relative Signals	LOAD rising-STH rising	T31	2	---	---	n-Sec		
	CPV rising-LOAD rising	T32	2	4	---	u-Sec		

Note 1) Refer to VESA standard.

Note 2) In case of using the long frame period, the deterioration of display quality, noise etc. may be occurred.

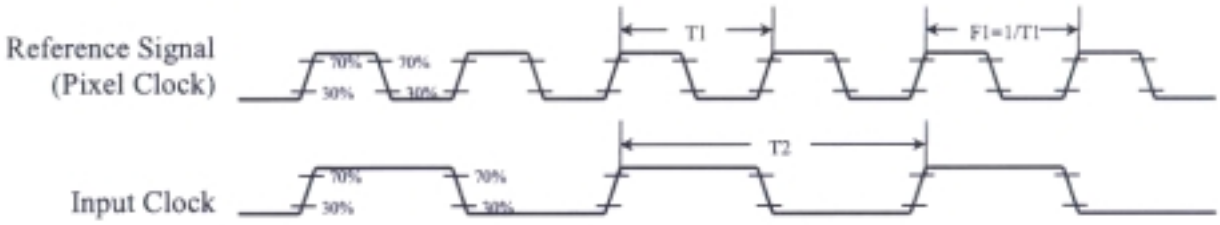
Note 3) Do not fix CPH1 and CPH2 to "H" or "L" level while the V_{DD} (+3.3V) is supplied. If CPH1 and CPH2 is fixed to "H" level or "L" level for certain period while the V_{DD} (+3.3V) is suppliéd, the panel may be damaged.

Note 4) Do not change t3 and t6 values in the operation. When t1 or t4 is changed, the panel is displayed as black.

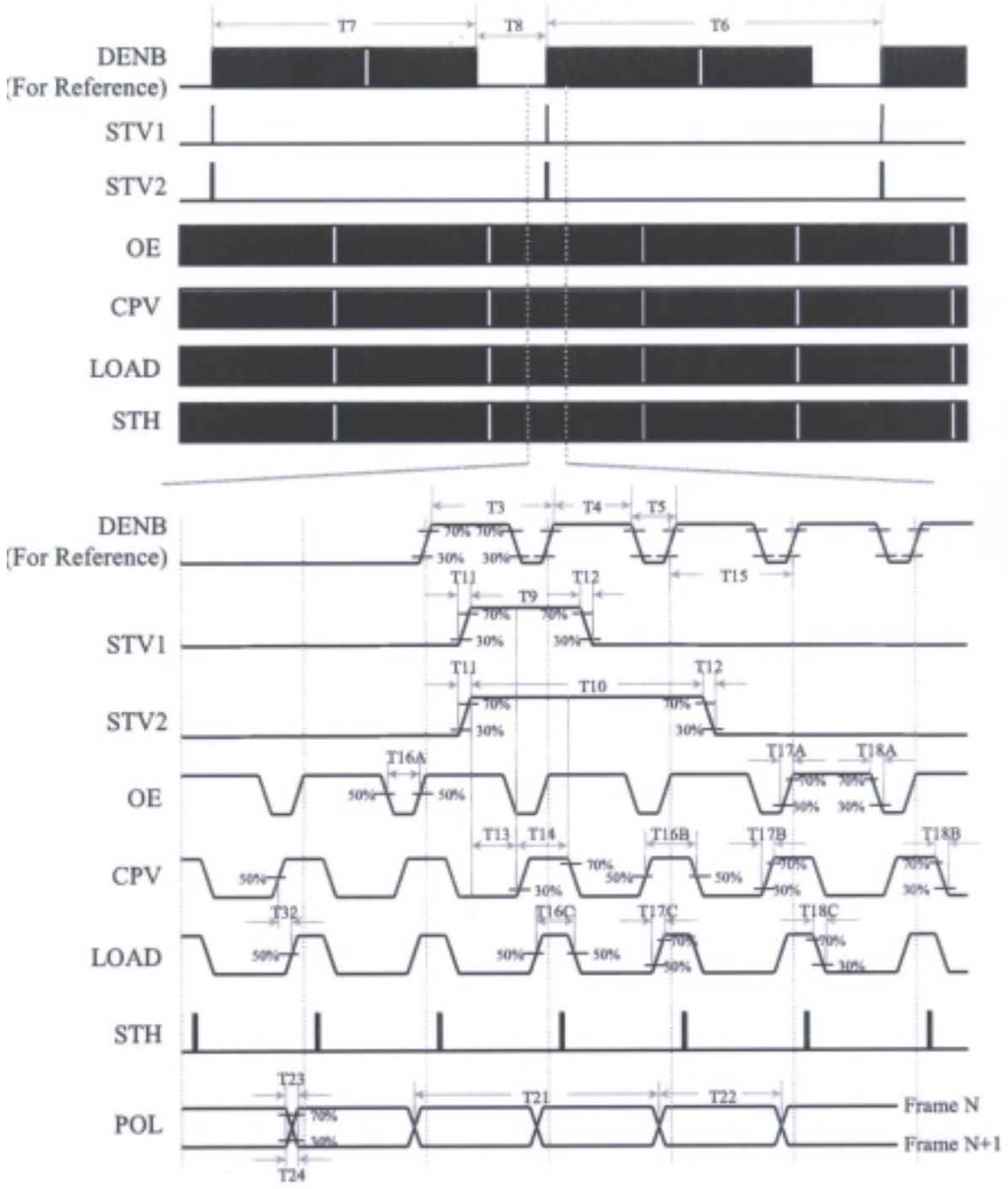
Note 5) Please adjust LCD operating signal timing and FL driving frequency, to optimize the display quality. There is a possibility that flicker is observed by the interference of LCD operating signal timing and FL driving condition (especially driving frequency).

6.3.2 AC Timing Charts:

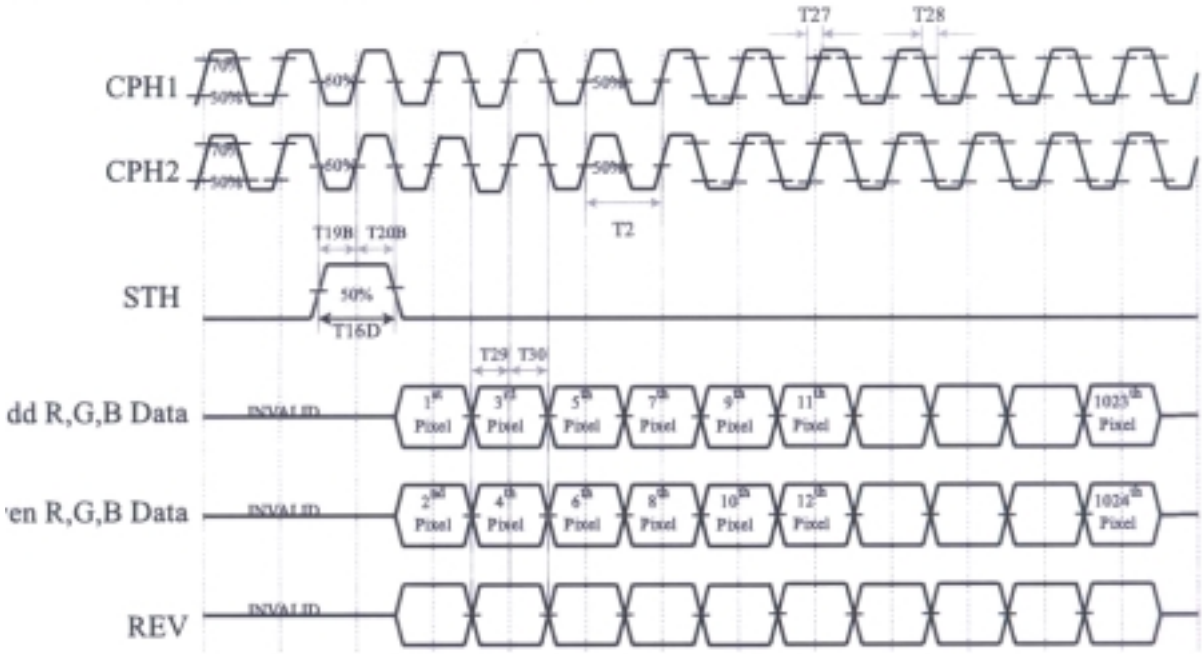
(1). Reference Signal (pixel clock):



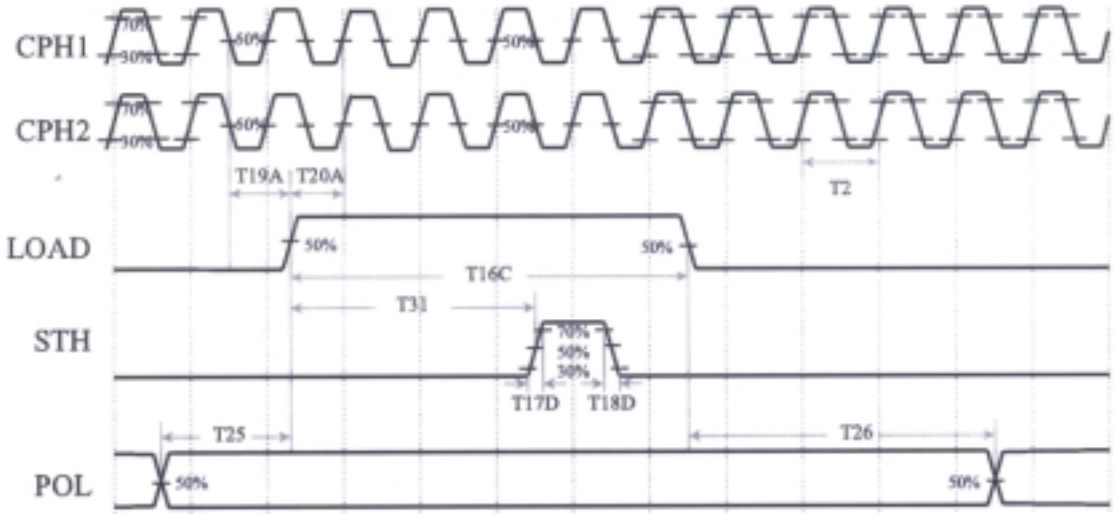
(2). Vertical Periodic (STV1, STV2, OE, CPV):



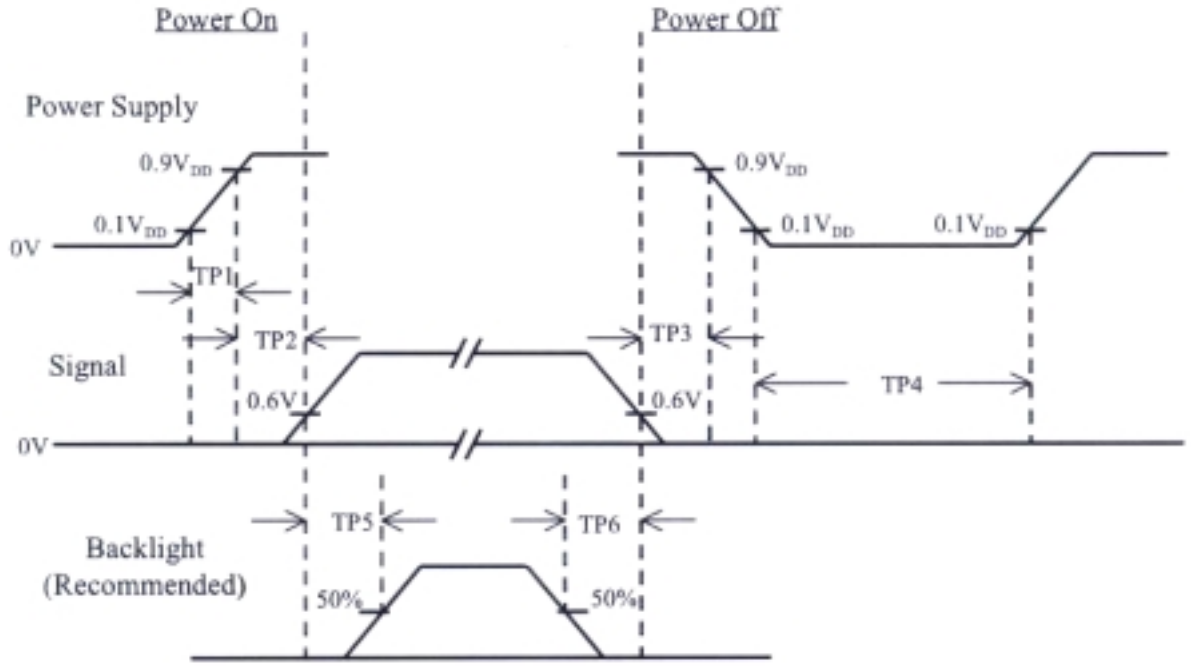
(3). Horizontal Periodic 1 (STH, CPH, DATA):



(4). Horizontal Periodic 2 (CPH, LOAD, STH, POL):



6.4 Power On / Off Sequence :



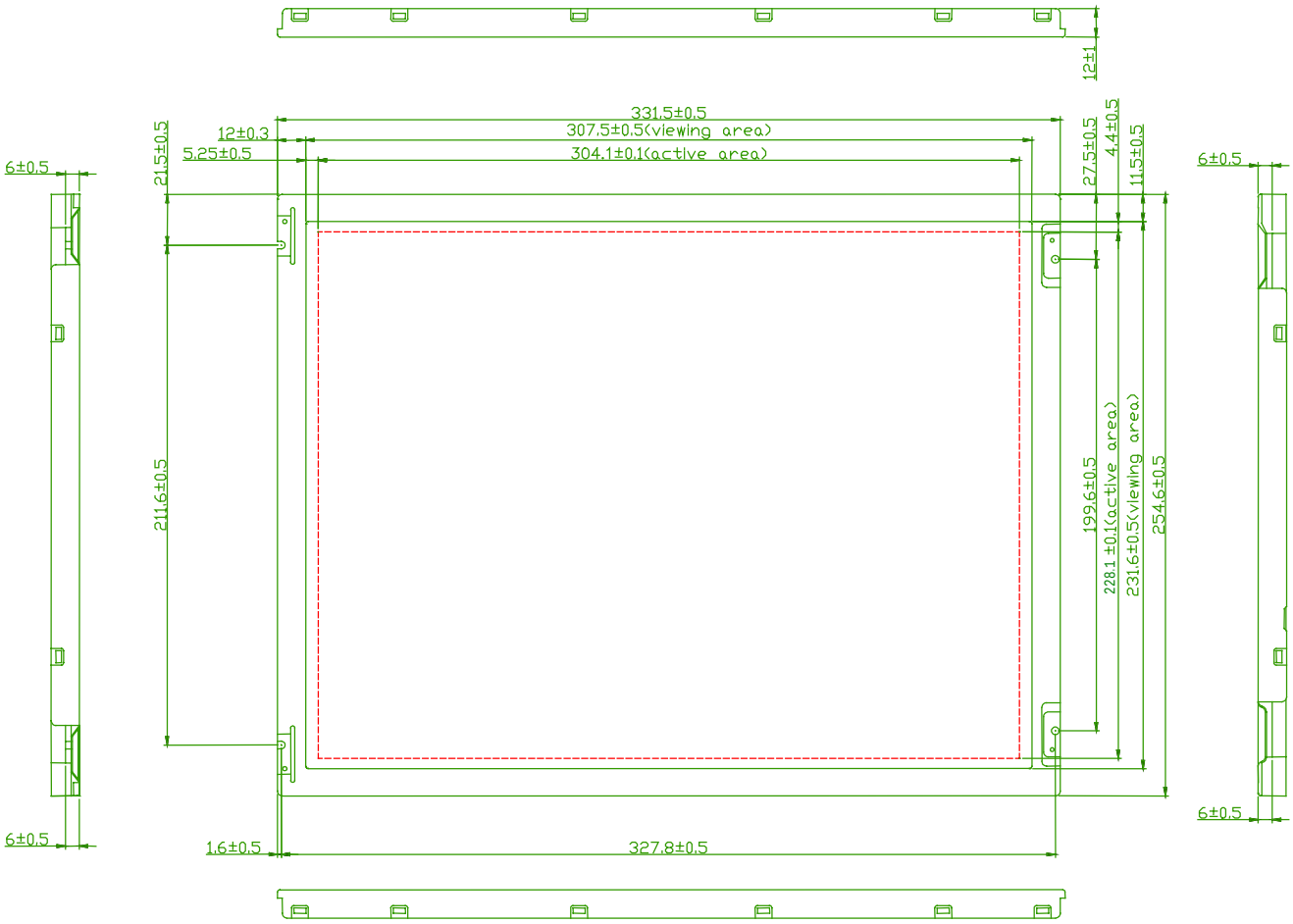
Item	Min.	Typ.	Max.	Unit	Remark
TP1	0	–	10	msec	
TP2	0	–	50	msec	
TP3	0	–	50	msec	
TP4	1	–	–	sec	
TP5	200	–	–	msec	
TP6	200	–	–	msec	

Note : (1) The supply voltage of the external system for the module input should be the same as the definition of V_{DD}.

(2) Apply the lamp volatge within the LCD operation range. When the back-light turns on before the LCD operation or the LCD truns off before the back-light turns off, the display may momentarily become white.

(3) In case of VDD = off level, please keep the level of input signal on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. 0 Outline dimension