MODEL NAME:	PAGE:	DOC. NO.:	VERSION:
LTM022A120	1 OF 24	TA-LTM022A-1200	A.0

2.2” 262K TFT LCD PANEL
PRELIMINARY SPECIFICATION

MODEL NAME: LTM022A120

Record of Revision

Ver.	Revise Date	Page	Content	Modified By
A.0	2003/09/08	-	Preliminary specification was first issued.	Sammi Chen

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1. GENERAL DESCRIPTION

1.1 Description

LTM022A120 is a transmissive type color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that used amorphous silicon TFT as a switching device. This model is composed of a TFT-LCD panel and a driver circuit. The resolution of 2.2” contains 176 x 220 pixels and can display up to 262K colors.

1.2 Features

LCD Type	:	Transmissive color active matrix LCD panel TN (Twisted Nematic) mode
Drive IC	:	Gate IC: Himax 8609A; Source IC: Himax 8301A
Built-in Drive Power		Low power consumption
MPU Interface	:	80-systems 18-bit/9-bit bus Serial data transfer bus
Internal RAM Capacity	:	95,040 bytes max.
Color Mode	:	262,144 colors
Outline Dimensions	:	39.8500 (W) ×53.9.000 (H) ×1.4 (D) mm
Effective Viewing Area	:	34.848 (W) ×43.560 (H) mm
Dot Size	:	0.045 (W) ×0.173 (H) mm
Dot Pitch	:	0.066 (W) ×0.198 (H) mm
Pixel Pitch	:	0.198 (W) ×0.198 (H) mm
Viewing Direction	:	12 O’ Clock
Weight	:	TBD
Applications	:	Display terminals for cellular phone

2. ELECTRICAL CHARACTERISTICS

2.1.Absolute Maximum Ratings

(Ta = 25 +/- 2°C, Vss = GND = 0)

Item	Symbol	Value	unit	Note
Power Supply Voltage (1)	Vcc	T.B.D.	V	-
Power Supply Voltage (1)	DDVDH	T.B.D.	V	
Input Voltage	Vi	T.B.D.	V	

Note: (1) If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

(2) Vcc ≧ GND must be maintained.

(3) DDVDH ≧ GND must be maintained.

2.2. Absolute Environment Ratings

Item	Symbol	Min.	Max.	unit	Note
Storage temperature	Tstg	(-30)	(70)	℃	(1)
Operating temperature (Ambient temperature)	Topr	(-20)	(60)	℃	(1),(2)

Note: (1) 95 % RH Max. (40°C ≧ Ta)

(2) In Case of below 0℃, the response time of liquid crystal (LC) becomes slower and the color of panel becomes darker than normal one.

3. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (1).

Measuring equipment: BM-5A, BM-7

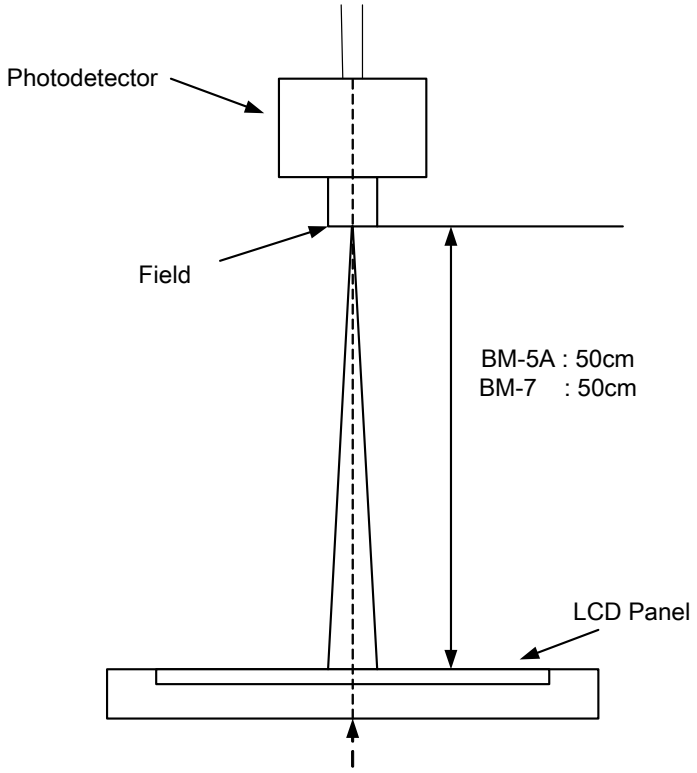
(Ta = 25 +/- 2°C, Vcc = Vci = 2.8V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio (Center Point)		C/R	Note (1) Θ= 0 Φ= 0 Normal Viewing Angle B/L On		(150)		-	(1)(2) BM-5A
Transmittance		T			(7.0)	-	%	(1)(3) BM-5A
Response Time	Rising: Tr	Tr + Tf			(45)		msec	(1)(4) BM-7
	Falling: Tf							
Color Chromaticity (CIE 1931)	White	Wx		-	(0.32)	-	-	(1)(5) BM-5A
		Wy		-	(0.34)	-		
	Red	Rx		-	(0.56)	-		
		Ry		-	(0.34)	-		
	Green	Gx		-	(0.32)	-		
		Gy		-	(0.54)	-		
	Blue	Bx		-	(0.14)	-		
		By		-	(0.17)	-		
Viewing Angle	Hor.	ΘL	C/R≧10 B/L On	-	(40)	-	Degree	(1)(6) BM-5A
		ΘR		-	(40)	-		
	Ver.	ΦH		-	(40)	-		
		ΦL		-	(15)	-		

Note: (1) Test Equipment Setup

After stabilizing and leaving the panel alone at a given temperature for 30 min, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. 30 min after lighting the lighting the back-light. This

should be measured in the center of screen with a viewing cone of 1^{o} by photodetector.



(2) Definition of Contrast Ratio (C/R): Ratio of gray max (Gmax) & gray min (Gmin) at the center point:

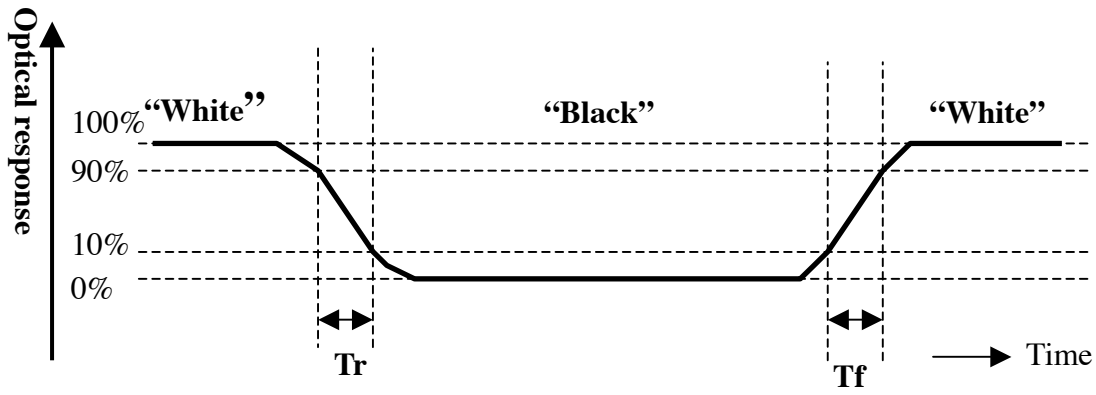
$$CR = \frac{Gmax}{Gmin}$$

* Gmax: Luminance with all pixels white

Gmin: Luminance with all pixels black

(3) Definite of Luminance of White: Luminance of white at the center point

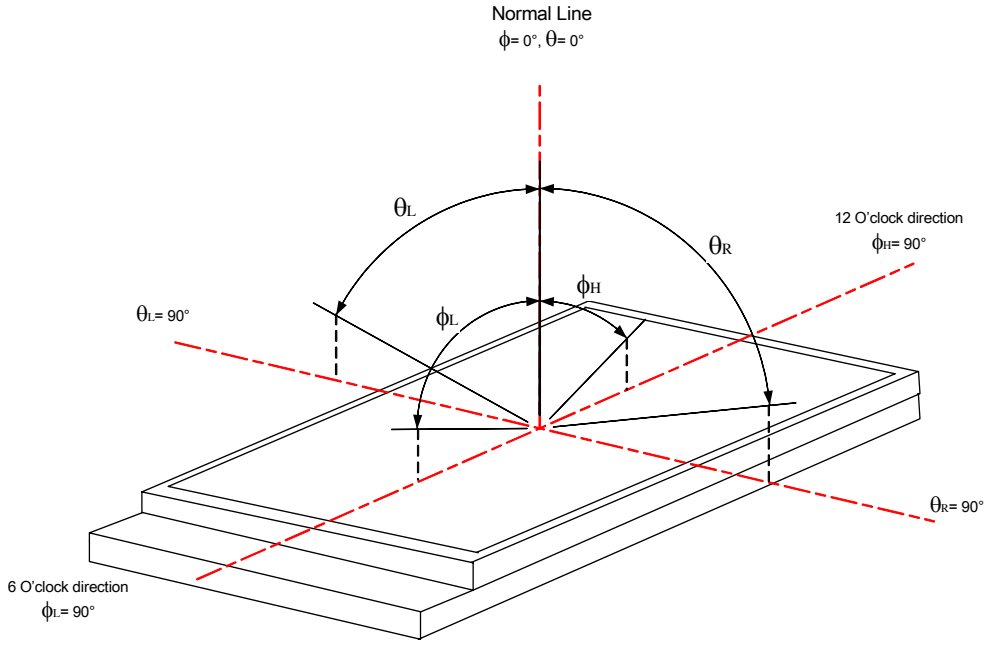
(4) Definition of Response time: Sum of Tr, Tf



(5) Definition of Color Chromaticity (CIE 1931)

Color coordinate of white & red, green, blue at center point.

(6) Definition of Viewing Angle: Viewing angle range (CR ≧ 10)



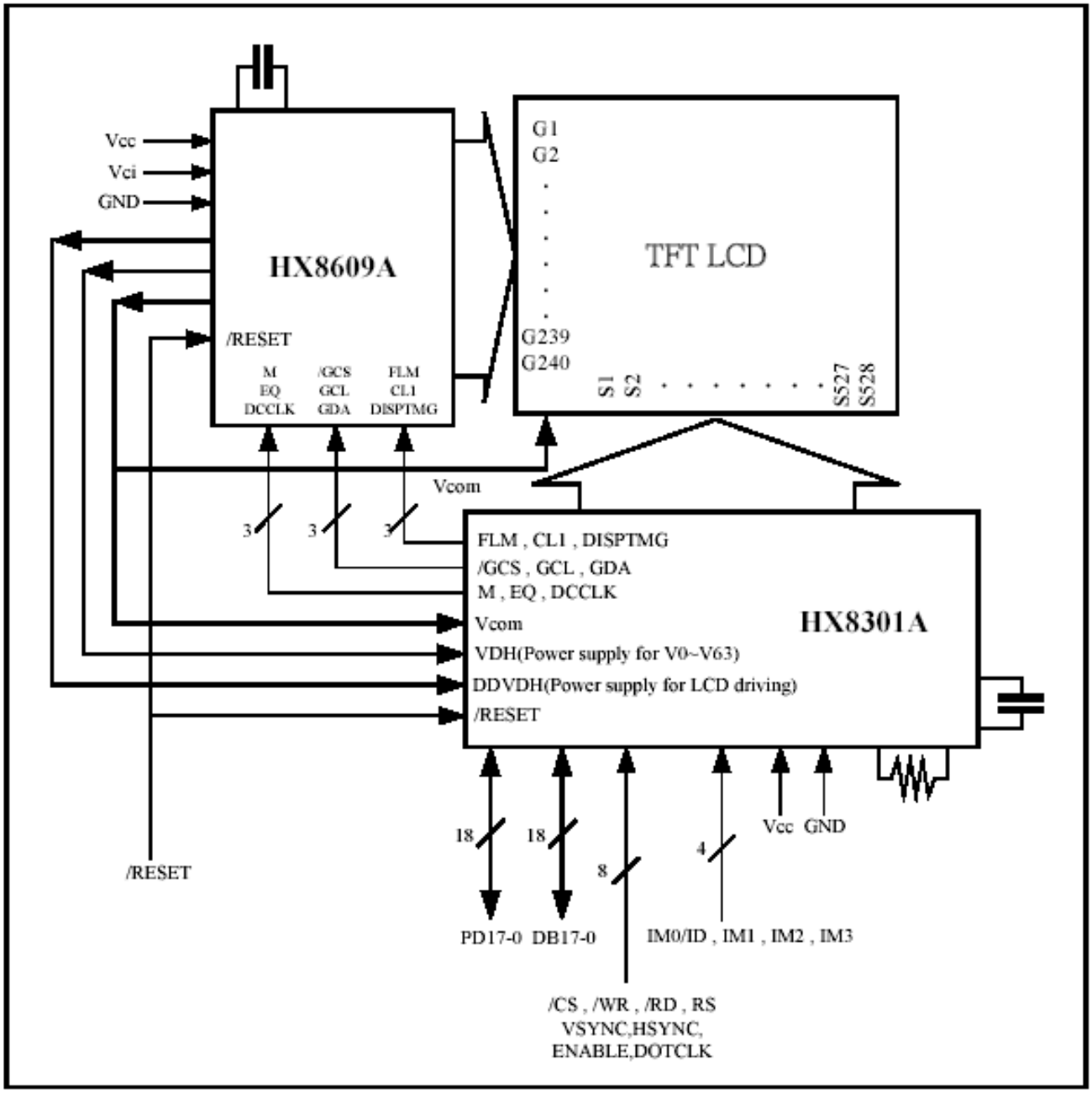
4. DC CHARACTERISTICS

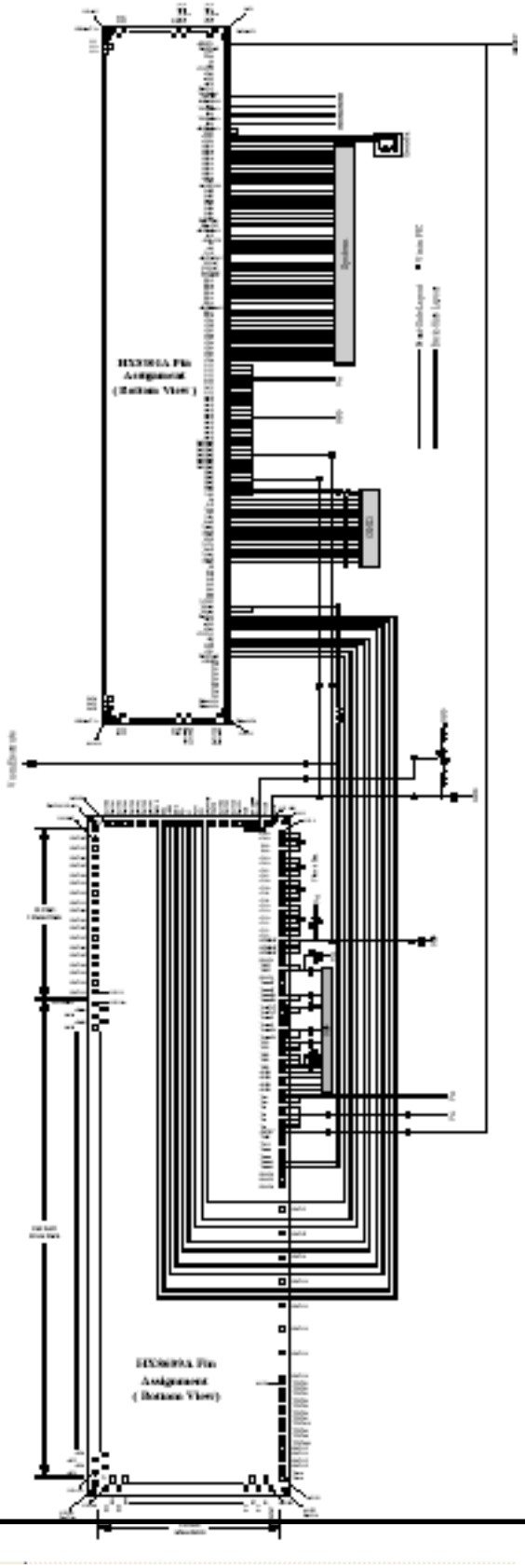
(Ta = -40~85°C, Vcc=1.8~3.7V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input High Voltage (1) (OSC1 Pin)	V_{IH}	Vcc=1.8~3.7V		T.B.D.		V	
Input Low Voltage (1) (OSC1 Pin)	V_{IL} (1)	Vcc=1.8~3.7V		T.B.D.		V	
Input Low Voltage (1) (Except OSC1 Pin)	V_{IL} (2)	Vcc=1.8~2.4V		T.B.D.		V	
		Vcc=2.4~3.7V		T.B.D.		V	
Output High Voltage (DB15~0 Pin)	V_{OH}	I_{OH} = -0.1 mA		T.B.D.		V	
Output Low Voltage (DB15~0 Pin)	V_{OL}	Vcc=1.8~2.4V I_{OL} = 0.1 mA		T.B.D.		V	
		Vcc=2.4~3.7V I_{OL} = 0.1 mA		T.B.D.		V	
I/O Leakage Current	I_{Li}	Vin = 0~Vcc		T.B.D.		μA	
Current Consumption During Normal Operation (Vcc - GND)	I_{OP}	f_{OSC} = 250KHz (240 line), Vcc=3.0V, Ta=25℃ GRAM data=0000h		T.B.D.		μA	
Current Consumption During Standby Mode (Vcc - GND)	I_{ST}	Vcc=3V, Ta≦50℃		T.B.D.		μA	
		Vcc=3V, Ta＞50℃		T.B.D.		μA	

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
LCD Power Current (DDVDH-GND)	I_{LCD}	Vcc=3V, VDH=5.0V DDVDH=5.5V, f_{OSC} = 250KHz (240 line),Ta=25℃, GRAM data=0000h, REV=0, SAP=001, VRN4-0=VRP4-0=0, PKP52-00=000, PRP12-00=000		T.B.D.		μA	
LCD Driving Voltage	V_{LCD}	--		T.B.D.		V	
Output Voltage Deviation		--		T.B.D.		mV	
Variation of Average Output Voltage		--		T.B.D.		mV	

5. BLOCK DIAGRAM





6. INTERFACE PIN CONNECTION

6.1.Pin Description

Pin No.	Symbol	I/O	Connected to	Description
1~2	NC			Dummy
3	DCCLK	I	DCCLK Pin of Source Driver	A clock for the step-up circuits supply from source driver.
4	GCL	I	GCL Pin of Source Driver	Operates as a clock in the serial transfer for register settings. Latches data on the rising edge of GCL signal.
5	/GCS	I	/GCS Pin of Source Driver	Operates as a chip-select signal in the serial transfer for register settings, Low: selected (serial transfer enabled), high: no selected (serial transfer disabled)
6	GDA	I	GDA Pin of Source Driver	Operates as the serial data in the serial transfer for register settings
7	EQ	I	EQ Pin of Source Driver and GND	Input signal supplied from source driver for controlling Vcom and Vcom2 output. The following levels are output according to the status of EQ: (1) EQ = LOW .Vcom = VcomH / VcomL .Vcom2 = VcomH2 / VcomL2 (2) EQ=HIGH .Vcom = Hi-Z .Vcom2 = Hi-Z Connect to GND pin when EQ is not used.
8	M	I	M Pin of Source Driver	Alternating input signal supplied from source driver for controlling Vcom and Vcom2 alternation. The following levels are output according to the status of M: (1) M = LOW .Vcom = VcomL .Vcom2 = VcomL2 (2) M = HIGH .Vcom = VcomH .Vcom2 = VcomH2
9	FLM	I	FLM Pin of Source Driver	Performs frame synchronization with the source driver. This signal is supplied from source driver.
10	CL1	I	CL1 Pin of Source Driver	Clock input pin and supplied from source driver. Gate line output changes at the falling edge of the signal.

11	DISPTMG	I	DISPTMG Pin of Source Driver	Control signal for G1~G240 scan-line output. This signal operates asynchronously with the FLM and CL1. G1~G240 output level is decided by DISPTMG and internal register (GON) as follow list.
12,13	NC			
14	Vcom2	O	TFT-display Common Electrode or Open	A power supply for the TFT-display common electrode. The alternating voltage between VcomH2 and VcomL2 level is output. The alternating cycle is according to the M signal received in M input pin.
15	RESET	I	External Reset Circuit	The reset pin. When a low level is input, the LSI is reinitialized. Be sure to apply a reset signal to the pin during the system's power-on.
16,17	Vci	I	Power Supply	An analog-circuit power supply. Vci = 2.5~3.3V
18,19	Vcc	I	Power Supply	A logic-circuit power supply, which is the same as voltage supply for source driver. Vcc = 1.7~3.3V
20,21	GND	I	Power Supply	Ground of all power sources. GND = 0 (V)
22	VGL	O	Capacitor for Stabilization	A power supply for gate driver output driving / Vcom driving (TFT-gate off level). Outputs a step-up voltage from step-up circuit 2 with VciOUT and DDVDH input. The step-up factor is set by internal register (BT). VGL = -4.0~-14.0 (V)
23,24	VCL	O	Capacitor for Stabilization	A power supply for VcomL driving. Outputs a –1-time voltage from step-up circuit 2 with VciOUT input. VCL = 0~ -3.3 (V)
25	VcomL2	O	Capacitor for Stabilization or Open	The low level of Vcom2 voltage generated for Vcom2 voltage alternating driving. VcomL2 is adjusted by internal register (VDV). When the register (VCOMG) is set to low, the VcomL2 output is fixed to GND level and a capacitor for stabilization is not necessary. VcomL2 = (VCL + 0.5) ~1 (V)
26	VciOUT	O	Capacitor for Stabilization	Outputs the internal reference voltage generated by Vci with the generated factor set by internal register (VC). The output voltage DDVDH, VGH, VGL, VCL must be set not over the their limitation as listed above.
27	VcomH2	O	Capacitor for Stabilization or Open	The high level of Vcom2 voltage generated for Vcom2 voltage alternating driving, VcomH2 can be adjusted by internal register (VCM) or VcomR or VcomR2. Connect this pin to a capacitor for stabilization.

				VcomH2 = 3.0 ~ (DDVDH-0.5) (V)
28	VGH	O	Capacitor for Stabilization	A power supply for gate driver output driving (TFT-gate on level). Outputs a step-up voltage from step-up circuit 2 with DDVDH input. The step-up factor is set by internal register (BT). VGH = 9.0~16.5 (V)
29,30	DDVDH	O	Source Driver & Capacitor for Stabilization	A power supply for source driver output driving / Vcom driving. Outputs a step-up voltage from step-up circuit 1 with VciOUT input. The step-up factor is set by internal register (BT). DDVDH = 4.0~5.5 (V)
31	C11-	I/O	Step-up Capacitor	Connect a step-up capacitor to step-up capacitor pin of internal step-up circuit 1.
32	C11+	I/O		
33	C12-	I/O	Step-up Capacitor	Connect a step-up capacitor to step-up capacitor pin of internal step-up circuit 2.
34	C12+	I/O		
35	C21-	I/O		
36	C21+	I/O		
37	C22-	I/O		
38	C22+	I/O		
39	NC			Dummy
40	VDH	O	VDH pin of Source Driver & Capacitor for Stabilization	Outputs a step-up voltage generated by VciOUT that is generated by Vci internally. The step-up factor is set by internal register (VRH). It is used for (1) source driver gray-level reference voltage VDH. (2) VcomH level. (3) Vcom/Vcom2 amplitude reference. Connect this pin to a stabilized capacitor. When this pin is not used, leave it open. VDH = 3.0 ~ (DDVDH-0.5) (V)
41	NC			Dummy
42	VcomR2	I	Variable Resistor or GND	A reference voltage for generating VcomH2. When VcomH2 is externally adjusted, halt the internal register (VCM) operation and connect a variable resistor between VDH and GND. When VcomH2 is not externally adjusted, connect this pin to GND pin and adjust VcomH2 by internal register (VCM).
43~55	NC			Dummy

56~58	Vcom	I	HX8609A	Connect this pin to Vcom output of gate driver for equalizer functions. All LCD outputs (S1~S528) are shorted to this pin input when EQ=1. When VcomL(2) is lower than 0V, this signal should not be connected.
59	VGL	O	Capacitor for Stabilization	A power supply for gate driver output driving / Vcom driving (TFT-gate off level). Outputs a step-up voltage from step-up circuit 2 with VciOUT and DDVDH input. The step-up factor is set by internal register (BT). VGL = -4.0~-14.0 (V)
60	NC			Dummy
61,62	Vcom	I	HX8609A	Connect this pin to Vcom output of gate driver for equalizer functions. All LCD outputs (S1~S528) are shorted to this pin input when EQ=1. When VcomL(2) is lower than 0V, this signal should not be connected.
63	DISPTMG	O	HX8609A	Gate off signal used in partial display. Low : The gate driver output is always in Voff output. High : The gate driver output is normal output *Connect DISPTMG output in either right or left terminal of a chip to gate driver. Set unused pins open.
64	CL1	O	HX8609A	The one-line-cycle pulse is output. *Connect CL1 output in either right or left terminal of a chip to gate driver. Set unused pins open.
65	FLM	O	HX8609A	Output for the frame-start pulse. *Connect FLM output in either right or left terminal of a chip to gate driver. Set unused pins open.
66	M	O	HX8609A	Output for the AC-cycle driving signal. *Connect either right or left terminal of a chip. Set unused pins open.
67	EQ	O	HX8609A	When EQ=1, the Vcom output of gate driver (HX8609A) is high-impedance state. Low:Vcom(2) voltage is output from Vcom(2) pin of HX8609A. High : Vcom output of HX8609A is in high-impedance state. *Connect EQ output in either right or left terminal of a chip to gate driver. Set unused pins open.
68	NC			Dummy
69	GDA	O	HX8609A	Data signal of serial transfer for HX8609A register setting. *Connect GDA output in either right or left terminal of a chip to gate driver. Set unused pins open.

70	/GCS	O	HX8609A	Chip-select signal of serial transfer for HX8609A register setting. Low: Gate driver is selected and can receive a serial transfer；High: Gate Driver is not selected and cannot receive a serial transfer. *Connect /GCS output in either right or left terminal of a chip to gate driver. Set unused pins open.
71	GCL	O	HX8609A	Clock signal of a serial transfer for HX8609A register setting. Data is output on the falling edge of this clock. *Connect GCL output in either right or left terminal of a chip to gate driver. Set unused pins open.
72	DCCLK	O	HX8609A	Outputs clocks for the step-up circuit driving of gate driver IC (HX8609A). *Connect DCCLK output in either right or left terminal of a chip to gate driver. Set unused pins open.
73	Vcom	I	HX8609A	Connect this pin to Vcom output of gate driver for equalizer functions. All LCD outputs (S1~S528) are shorted to this pin input when EQ=1. When VcomL(2) is lower than 0V, this signal should not be connected.
74	V63N	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, “011”,”100”,”101”), it is used for outputs of negative-polarity op amp. Connect these pins to stabilized capacitors.
75	V63P	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, 011”,”100”,”101”), it is used for outputs of positive-polarity op amp. Connect these pins to stabilized capacitors
76	V62N	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, “011”,”100”,”101”), it is used for outputs of negative-polarity op amp. Connect these pins to stabilized capacitors.
77	V62P	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, 011”,”100”,”101”), it is used for outputs of positive-polarity op amp. Connect these pins to stabilized capacitors
78	V55N	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, “011”,”100”,”101”), it is used for outputs of negative-polarity op amp. Connect these pins to stabilized capacitors.
79	V55P	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, 011”,”100”,”101”), it is used for outputs of positive-polarity op amp. Connect these pins to stabilized capacitors

80	V43N	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, “011”,”100”,”101”), it is used for outputs of negative-polarity op amp. Connect these pins to stabilized capacitors.
81	V43P	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, 011”,”100”,”101”), it is used for outputs of positive-polarity op amp. Connect these pins to stabilized capacitors
82	V20N	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, “011”,”100”,”101”), it is used for outputs of negative-polarity op amp. Connect these pins to stabilized capacitors.
83	V20P	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, 011”,”100”,”101”), it is used for outputs of positive-polarity op amp. Connect these pins to stabilized capacitors
84	V8N	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, “011”,”100”,”101”), it is used for outputs of negative-polarity op amp. Connect these pins to stabilized capacitors.
85	V8P	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, 011”,”100”,”101”), it is used for outputs of positive-polarity op amp. Connect these pins to stabilized capacitors
86	V1N	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, “011”,”100”,”101”), it is used for outputs of negative-polarity op amp. Connect these pins to stabilized capacitors.
87	V1P	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, 011”,”100”,”101”), it is used for outputs of positive-polarity op amp. Connect these pins to stabilized capacitors
88	V0	O	Stabilized Capacitor	When built-in op amp is on (SAP2-0 = ”001”, ”010”, 011”,”100”,”101”), it is used for outputs of positive-polarity op amp. Connect these pins to stabilized capacitors
89	VGS	I	GND or External Resistor	Reference level for the grayscale-voltage generation circuit. For connection to a variable resistor that adjusts the source-driver level for a panel.
90	VDH	I	HX8609A	The reference level for gray level voltage generation circuit, which can be provided by HX8609A. VDH(max.)：DDVDH-0.5V.
91,92	DDVDH	I	HX8609A	Input for the LCD-drive voltage for the source driver,. DDVDH：4.5 V ~ 5.5V.

93,94	GND	-	GND	GND (logic): 0.
95,96	Vcc	-	Power Supply	Vcc: + 1.8 V to + 3.3 V
97~114	PD0~PD17	I	MPU	Serves as a 18-bit bus for RGB data.
115	ENABLE	I	MPU	Indicates whether data is written to GRAM or not when the RGB interface is in use via RGB interface PD17~0.
116	DOTCLK	I	MPU	Dot-clock signal.
117	HSYNC	I	MPU	Line synchronization signal.
118	VSYNC	I	MPU	Frame synchronization signal.
119	VLD	I	MPU	Indicates whether or not the data is valid when writing to GRAM
120	/CS	I	MPU	Chip select signal. Low: chip is selected (can be accessed); High: chip is not selected (cannot be accessed).
121	RS	I	MPU	Register select signal. Low: Index/status; High: Control register
122	/WR	I	MPU	For an 80-system bus interface, serves as a write strobe signal and writes data at the low level. For a synchronous clock interface, serves as the synchronous clock signal.
123	/RD	I	MPU	(Low: Write；High: Read) For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.
124	DB0/SD1	I/O	MPU	Serves as a 18-bit bi-directional data bus. For an 9-bit bus interface, data transfer uses DB17-DB9； fix unused DB8-DB0 to the Vcc or GND level. For a clock-synchronous serial interface, serves as the serial data input pin (SDI). The input level is read on the rising edge of the SCL signal.
125	DB1/SD0	I/O	MPU	Serves as a 18-bit bi-directional data bus. For an 9-bit bus interface, data transfer uses DB17-DB9； fix unused DB8-DB0 to the Vcc or GND level. or a clock-synchronous serial interface, serves as a erial data output pin (SDO). Successive bit values are utput on the falling edge of the SCL signal.
126~141	DB2~DB17	I/O	MPU	Serves as a 18-bit bi-directional data bus.

				For an 9-bit bus interface, data transfer uses DB17-DB9； fix unused DB8-DB0 to the Vcc or GND level.
142	OSC2	I/O	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal be supplied through OSC1 with OSC2 open-circuit or high level.
143	OSC1	I/O		
144~147	IM3-1, IM0(ID)	I	GND or Vcc	Refer to 5.2 MPU Interface Mode Selection
148	RESET1	I	MPU or External RC Circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied. Input data through /RESET1 or /RESET2. Unused pins should not be connected.
149~151	Vcom			Connect this pin to Vcom output of gate driver for equalizer functions. All LCD outputs (S1~S528) are shorted to this pin input when EQ=1. When VcomL(2) is lower than 0V, this signal should not be connected.
152, 153	NC			Dummy

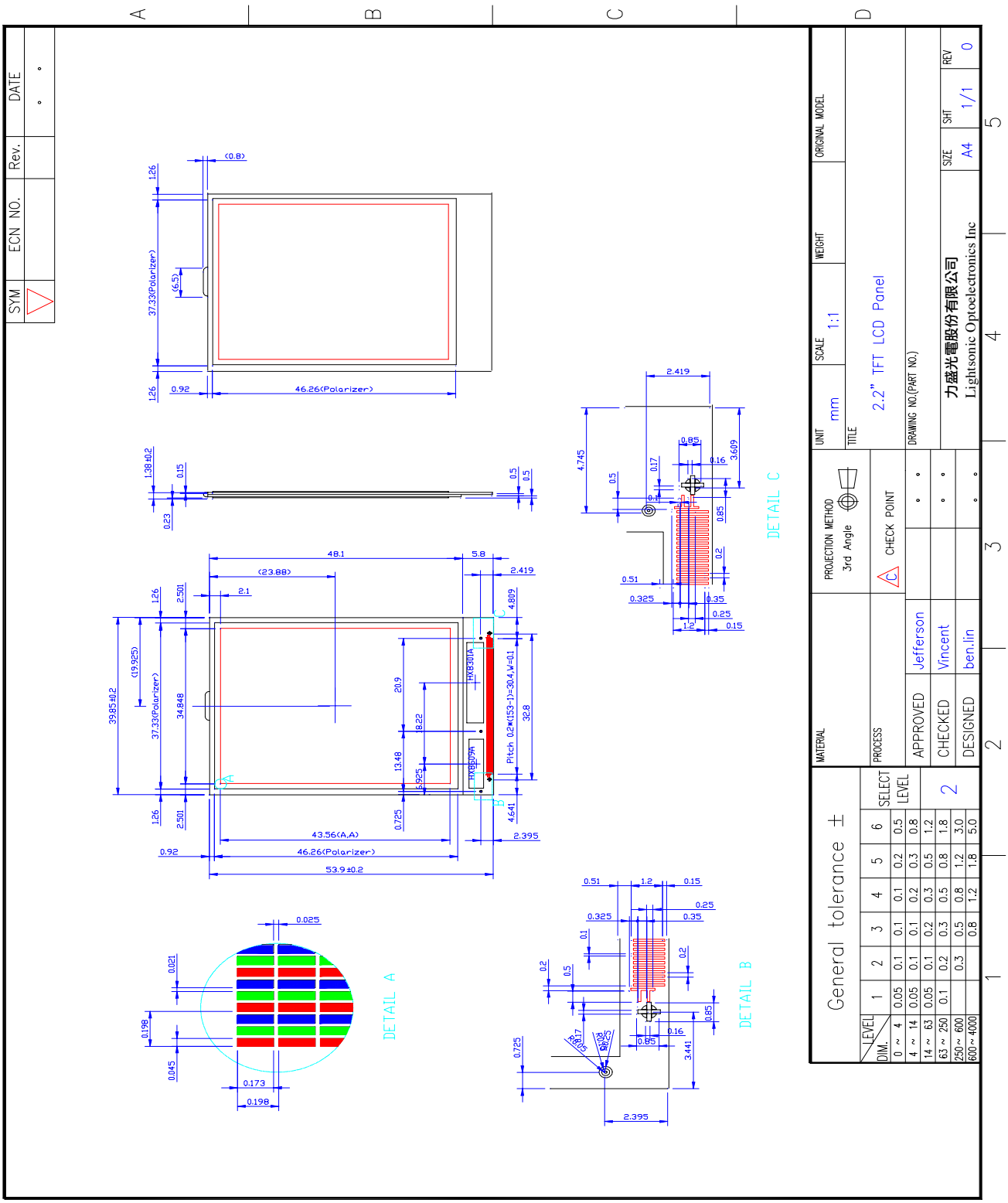
6.2.Select the MPU interface mode

Select the MPU interface mode as listed below IM3, IM2, IM1, IM0/ID MPU interface mode.

IM3	IM2	IM1	IM0/ID	MPU-interface mode	DB Pin
GND	GND	GND	*	Setting disable	
GND	GND	Vcc	GND	80-system, 16-bit bus interface	DB17~10 and 8~1
GND	GND	Vcc	Vcc	80-system, 8-bit bus interface	DB17~10
GND	Vcc	GND	ID	Clocked serial peripheral interface	DB1~0
GND	Vcc	Vcc	*	Setting disable	
Vcc	GND	GND	*	Setting disable	
Vcc	GND	Vcc	GND	80-system, 18-bit bus interface	DB17~0
Vcc	GND	Vcc	Vcc	80-system, 9-bit bus interface	DB17~9
Vcc	Vcc	*	*	Setting disable	

When a serial interface is selected, IM0 pin is used as the ID setting for a device code.

7. OUTLINE DRAWING



8. PACKING

TBD

9. RELIABILITY

No.	Test Items	Test Conditions
1	High Temperature Storage Test	Ta=80℃, 120 Hrs
2	Low Temperature Storage Test	Ta=-30℃, 120Hrs
3	High Temperature and High Humidity Operating Test	Ta=40℃, 90%RH, 120Hrs (No condensation of dew)
4	High Temperature Operating Test	Ta=70℃, 120Hrs
5	Low Temperature Operating Test	Ta=-20℃, 120Hrs
6	Heat Shock Test	Ta=-30℃ (0.5H) ~ 80℃ (05H) / 32 cycles
7	Electro Static Discharge Test	+200V, 200pF (0Ω), 1 time for each terminal

Note: (1) Evaluation should be tested after storage at room temperature for one hour.

(2) There should be no change that might affect the practical display function when the display quality test is conducted under normal operating conditions.

(3) Judgment:

2. In the standard condition, there shall be no practical problems that may affect the display function.
3. No serious image quality degradation.

10. PRECAUTIONS

10.1.Handling

(1) Refrain from strong mechanical shock and / or any force to the panel. In addition to damage, this may cause improper operation or damage to the panel.

(2) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a B pencil lead.

(3) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, staining and discoloration may occur.

(4) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(5) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Don't use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(6) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(7) Protect the panel from static, it may cause damage to the CMOS Gate Array IC.

(8) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(9) Pins of I/F connector shall not be touched directly with bare hands.

10.2. Storage

(1) Do not leave the panel in high temperature, and high humidity for a long time. It is

highly recommended to store the panel with temperature from 0 to 35℃ and relative humidity of less than 70%.

(2) The panel shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

10.3. Operation

(1) The LCD shall be operated within the limits specified. Operation at values outside of these limits may shorten life, and/or harm display images.

(2) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation in part contents and environmental temperature and so on).. Otherwise the panel may be damaged.

(3) If the panel displays the same pattern continuously for a long period of time, it can be the situation when the image” Sticks” to the screen.