ITEM	SPECIFICATION
Screen Diagonal	12.0 inch
Active Area	254.016 (H) x 169.344 (V) mm
Pixels H x V	2160 x 1440
Pixel Pitch	0.0392mm (H) x 0.1176mm (V) TYP.
Pixel Arrangement	R.G.B Vertical Stripe
Display Mode	Normally Black (PLS mode)
Input Voltage	3.3 V
Power Consumption (max.)	Cell: 0.89 W BLU: 2.88 W
Outline Dimension	286.4 x 197.55 mm (Typ.)
Weight	265 g (Max.)
Display Colors	16 million colors
Surface Treatment	Haze 0, Hard-Coating 2H - Contact angle (DI water) <70 degree

2 ABSOLUTE MAXIMUM RATINGS

The following are maximum value, which if exceeded, may cause faulty operation or damage to the unit.

ITEM	SYMBOL	MIN	MAX	UNIT	NOTE
LCD Power Voltage	VCC	-0.3	4.0	V	
Operating Temperature	TOP	0	50	℃	Note
Operating Humidity	HOP	8	95	%RH	Note
Storage Temperature	TST	-20	60	℃	Note
Storage Humidity	HST	10	95	%RH	Note

【Note】

*1) The range of temperature and relative humidity are shown in the graph below 90% RH Max. (39℃ ≥ Ta) If the temperature is higher than 40 ℃, the maximum temperature of wet–bulb shall be less than 39℃. No condensation.

*2) The maximum wet bulb temperature ≦39℃(Ta＞40℃) and without dewing.

*3) If product in environment which over the definition of the relative temperature and humidity out of range too long, it will affect visual of LCD.

*4) If you operate LCD in normal temperature range, the center surface of panel should be 0℃ min 60℃ max.

3 ELECTRICAL CHARACTERISTICS

3.1 TFT LCD

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	NOTE
LCD Power Voltage		VCC	3	3.3	3.6	V	*1)
LCD Current	Mosaic		-	-	(303)	mA	*1) *2) *3)
	V.Stripe			-	(363)	mA	*1) *2) *3)
LCD Power consumption	Mosaic	P_{LCD}			(1)	W	*1) *2) *3)
Rush Current		I_{RUSH}	-	-	1.5	A	*1),*2)
HPD		V_{HPD}	2.25	-	2.75	V	
Differential Signal Common Mode Voltage (Main Link and AUX)		VCM	0	-	2	V	*4)
LED Input Voltage		V_{LED}	5.5	12	18	V	
LED Input Current		I_{LED}		198		mA	
LED Input Power		P_{LED}		2.38	-	W	
High Level input voltage(PWM)		PWM_{high}	1.26		3.6	V	
Low Level input voltage(PWM)		PWM_{low}			0.54	V	
LED PWM		PWMI	200		20K	Hz	
PWM Duty Cycle Range		PWMR	1		100	%	
High Level input voltage of PWM voltage		PWMV	1.26		3.6V	V	
Low Level input voltage of PWM voltage		PWMV	-		0.54	V	

【Note】

*1) The ambient temperature is Ta = 25 ± 2°C.

*2) I_{RUSH} : the maximum current when VCCS is rising
Measurement Conditions : Shown as the following figure. Test pattern : Black

*4) eDP Signal Definite :

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{RX-DIFFpp}$	Differential peak-to peak input voltage for 2.7GHz	120	-	-	mV
$V_{RX-DIFFpp}$	Differential peak-to peak input voltage for 1.6GHz	40	-	-	mV
VRX-DC-CM	RX. Input DC common mode voltage	-	0.85		V
R_{RX_SE}	Single-ended termination resistance	40	50	60	Ohm
R_{RX_DIFF}	Differential termination resistance	80	100	120	Ohm
L_{RX_SKEW}	Rx intra-pair skew tolerance at HBR for 2.7GHz			300	Ps
L_{RX_SKEW}	Rx intra-pair skew tolerance at HBR for 1.62GHz			100	Ps
$V_{AUX-DIFF-PP}$	AUX differential peak-to-peak Voltage swing at transmitting device	0.39		1.38	V
$V_{AUX-DIFF-PP}$	AUX differential peak-to-peak Voltage swing at receiving device	0.32		1.36	V
$V_{AUX\_TERM\_R}$	AUX CH termination DC resistance		100		Ohm
$V_{AUX-DC-CM}$	AUX DC common mode voltage	0		2.0	V
$V_{AUX-Turn-CM}$	AUX DC turn around common mode voltage	-		0.4	V
$I_{AUX-SHORT}$	AUX short circuit current limit			90	mA

(a) Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version 1. Revision 1a and VESA Embedded DisplayPort Standard Version 1.1
(b) The AUX AC Coupling Capacitor should be placed on Source Devices.
(c) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS)1.1

Timing (ms)	Remarks	Note
$0.5 < T_1 \leq 10$	Power rail rise time, 10% to 90%	
$0 < T_2 \leq 200$	Delay from LCDVCC to automatic Black Video generation	(1)(2)
$0 < T_3 \leq 200$	Delay from LCDVCC to HPD high	(3)
$0 \leq T_4$	Delay from HPD high to link training initialization	
$0 \leq T_5$	Link training duration	
$0 \leq T_6$	Link idle	
$0 < T_7 \leq 50$	Delay from valid video data from Source to video on display	
$50 < T_8$	Delay from valid video data from Source to backlight enable	
$0 < T_9$	Delay from backlight disable to end of valid video data	(1)(2)

Note (1) Please don't plug or unplug the interface cable when system is turned on.
Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:
- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)
- When no Main Link data, or invalid video data, is received from Source. Black video must be display within 50ms(max) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.
Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

4.1 CN1 (Interface signal) Outlet connector: Molex B2B 40pin (Receptacle)

Pin	Symbol	Description	Remark
1	PWR	LCD logic and driver power	
2	PWR	LCD logic and driver power	
3	PWR	LCD logic and driver power	
4	PWR	LCD logic and driver power	
5	NC	BIST for PLD Panel	LCD Panel Self Test Enable
6	NC	NC	
7	NC	NC	
8	GND	GND(0V)	
9	GND	GND(0V)	
10	DAUXP	True Signal Auxiliary Channel	
11	DRX0N	Complement Signal Link Lane 0	
12	DAUXN	Complement Signal Auxiliary Channel	
13	DRX0P	True Signal Link Lane 0	
14	GND	GND(0V)	
15	GND	GND(0V)	
16	BRD_REV[0]	Shows BRD version	
17	DRX1N	Complement Signal Link Lane 1	
18	BRD_REV[1]	Shows BRD version	
19	DRX1P	True Signal Link Lane 1	
20	GND	GND(0V)	
21	GND	GND(0V)	
22	PL_PWM	System PWM signal input	
23	DRX2N	Complement Signal Link Lane 2	
24	NC	BIST for Samsung Panel	LCD Panel Self Test Enable
25	DRX2P	True Signal Link Lane 2	
26	GND	GND(0V)	
27	GND	GND(0V)	
28	BL_EN	Backlight enable	
29	DRX3N	Complement Signal Link Lane 3	
30	HPD	HPD signal pin	
31	DRX3P	True Signal Link Lane 3	
32	GND	GND(0V)	
33	GND	GND(0V)	
34	NC	NC	
35	NC	NC	
36	NC	NC	
37	VLED	LED Anode Power Supply	
38	VLED	LED Anode Power Supply	
39	VLED	LED Anode Power Supply	
40	VLED	LED Anode Power Supply	

5 INTERFACE TIMING CHART

5.1 Timing Chart

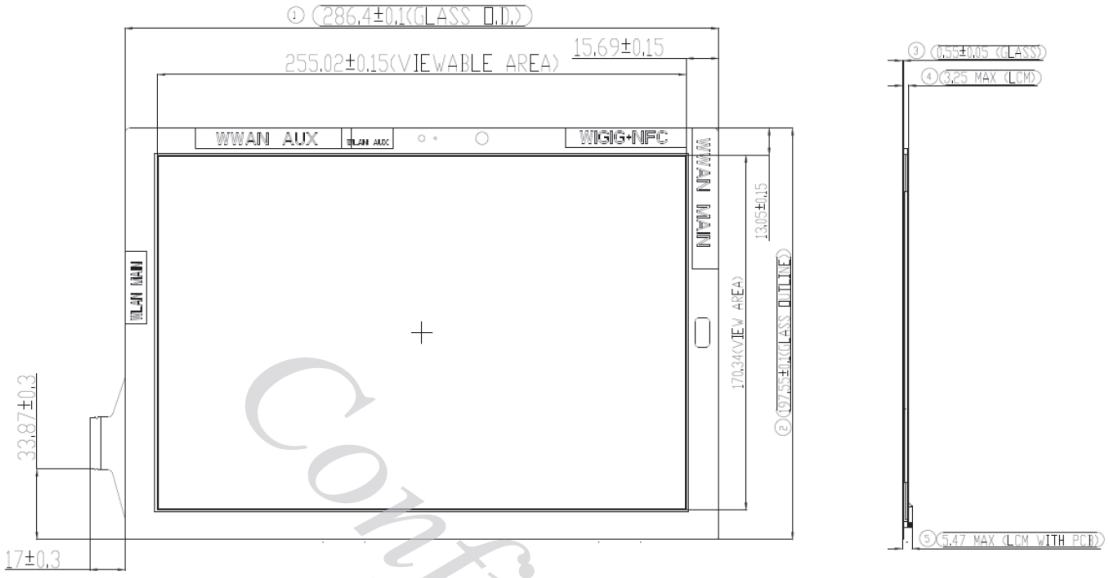
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frame Frequency	Cycle	T_V	1812	1816	1850	Lines	
Vertical active in the display term	Display Period	T_{VD}	-	1800	-	Lines	
Scanning time in one line	Cycle	T_H	3300	3316	3600	Clocks	
Horizontal active in the display term	Display Period	T_{HD}	-	3200	-	Clocks	

6 EDID Description

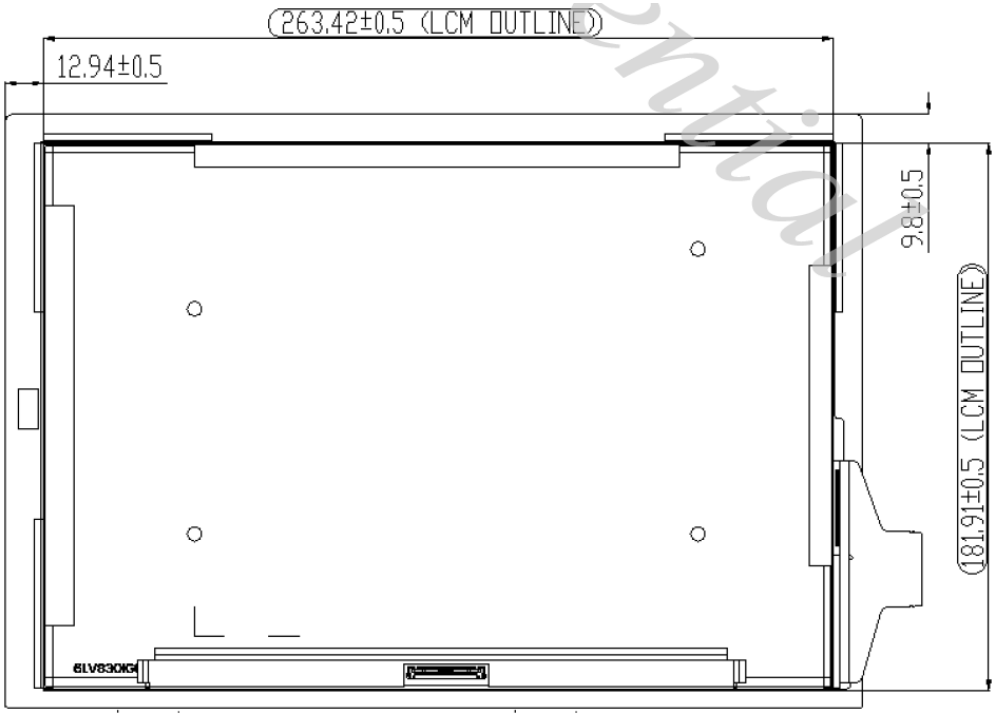
SPWG V2.1			
Byte#	Byte#		Value
(dec)	(hex)	Field Name and Comments	(hex)
0	0		00
1	1		FF
2	2		FF
3	3		FF
4	4		FF
5	5		FF
6	6		FF
7	7		00
8	8	EISA manufacture code= SEC (1st byte)	4C
9	9	(2nd byte)	83
10	0A	Product code LSB =	44
11	0B	Product code MSB	42
12	0C	ID(32-bit) serial number *(preferred, but optional, zero if not used)*	00
13	0D		00
14	0E		00
15	0F		00
16	10	Week of manufacture	00
17	11	Year of manufacture	19
18	12	EDID Structure version # = 1	01
19	13	EDID Revision # = 4	04
20	14	Video input definition *(Digital I/P, non TMDS CRGB)*	80
21	15	Max H image size = (25) *(rounded to cm)*	19
22	16	Max V image size = (17) *(rounded to cm)*	11
23	17	Display gamma = 2.2 *(=(gamma*100)-100)*	78
24	18	Features *(no DPMS, Active off, RGB, timing BKL1)*	0A
25	19	Red/Green low Bits	EE
26	1A	Blue/White low Bits	95
27	1B	Red X Rx=0.640	A3
28	1C	Red Y Ry=0.330	54
29	1D	Green X Gx=0.300	4C
30	1E	Green Y Gy=0.600	99
31	1F	Blue X Bx=0.150	26
32	20	Blue Y By=0.060	0F
33	21	White X Wx=0.313	50
34	22	White Y Wy=0.329	54
35	23	Established Timing I not used	00
36	24	Established Timing II not used	00
37	25	Manufacturer's Timing not used	00
38	26	Standard Timing Identification 1 not used	01
39	27	Standard Timing Identification 1 not used	01
40	28	Standard Timing Identification 2 not used	01
41	29	Standard Timing Identification 2 not used	01
42	2A	Standard Timing Identification 3 not used	01
43	2B	Standard Timing Identification 3 not used	01
44	2C	Standard Timing Identification 4 not used	01
45	2D	Standard Timing Identification 4 not used	01
46	2E	Standard Timing Identification 5 not used	01
47	2F	Standard Timing Identification 5 not used	01
48	30	Standard Timing Identification 6 not used	01
49	31	Standard Timing Identification 6 not used	01

50	32	Standard Timing Identification 7 not used	01
51	33	Standard Timing Identification 7 not used	01
52	34	Standard Timing Identification 8 not used	01
53	35	Standard Timing Identification 8 not used	01
54	36	Detailed timing description # 1 (LSB)	78
55	37	Pixel Clock =206MHz 21600x1440@60Hz (MSB)	50
56	38	Horizontal Active = 2160 pixels Notes2 (lower 8 bits)	70
57	39	Horizontal Blanking = 160 pixels (lower 8 bits)	A0
58	3A	Horizontal Active : Horizontal Blanking (upper 4:4 bits)	80
59	3B	Vertical Active = 1440 lines	A0
60	3C	Vertical Blanking = 32 lines (DE Blanking min for DE-only panels)	29
61	3D	Vertical Active : Vertical Blanking (upper 4:4 bits)	50
62	3E	Horizontal Sync. Offset = 48 pixels	30
63	3F	Horizontal Sync Pulse Width = 32 pixels(WHL)	20
64	40	Vertical Sync Offset = 3 lines, Sync Width(tWVL) = 10 lines	3A
65	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00
66	42	Horizontal Image size = 254mm (lower 8 bits)	FE
67	43	Vertical Image size = 169mm (lower 8 bits)	A9
68	44	Horizontal & Vertical Image size (upper 4:4 bits)	00
69	45	Horizontal Border = 0 (Zero for internal LCD)	00
70	46	Vertical Border = 0 (Zero for internal LCD)	00
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	19
72	48	Detailed timing description # 2	00
73	49	# 2 Flag	00
74	4A	# 2 Reserved	00
75	4B	# 2 ASCII string Model name	0F
76	4C	# 2 Flag	00
77	4D	# 2 1st character of name	00
78	4E	# 2 2nd character of name	00
79	4F	# 2 3rd character of name	00
80	50	# 2 4th character of name	00
81	51	# 2 5th character of name	00
82	52	# 2 6th character of name	00
83	53	# 2 7th character of name	00
84	54	# 2 8th character of name	00
85	55	# 2 9th character of name	44
86	56	# 2 10th character of name	DC
87	57	# 2 11th character of name	03
88	58	# 2 New line character indicates end of ASCII string	74
89	59	# 2 Padding with "Blank" character	00
90	5A	Detailed timing description # 3	00
91	5B	# 3 Flag	00
92	5C	# 3 Reserved	00
93	5D	# 3 FE (hex) defines ASCII string (Vendor "CMN", ASCII)	FE
94	5E	# 3 Flag	00
95	5F	# 3 1st character of string S	53
96	60	# 3 2nd character of string A	41
97	61	# 3 3rd character of string M	4D
98	62	# 3 4th character of name S	53
99	63	# 3 5th character of name U	55
100	64	# 3 5th character of name N	4E
101	65	# 3 6th character of name G	47
102	66	# 3 Padding with "Blank" character	0A
103	67		20
104	68		4C

105	69		83
106	6A		51
107	6B		4C
108	6C	Detailed timing description # 4	00
109	6D	# 4 Flag	00
110	6E	I# 4 Reserved	00
111	6F	# 4 FE (hex) defines ASCII string (Model Name"N116HSE-EA2", ASCII)	FE
112	70	# 4 Flag	00
113	71	# 4 1st character of name L	4C
114	72	# 4 2nd character of name S	53
115	73	# 4 3rd character of name N	4E
116	74	# 4 4th character of name 1	31
117	75	# 4 5th character of name 2	32
118	76	# 4 6th character of name 0	30
119	77	# 4 7th character of name Q	51
120	78	# 4 8th character of name L	4C
121	79	# 4 9th character of name 0	30
122	7A	# 4 10th character of name 1	31
123	7B	# 4 11th character of name L	4C
124	7C	# 4 12th character of name 0	30
125	7D	# 4 13th character of name 1	31
126	7E	Extension Flag *(# of optional 128-byte EDID extension block to follow, typ=0)*	00
127	7F	Checksum *(the 1-byte sum of all 128 bytes in this EDID block shall equal zero)*	E3



Front view



Back view

9 OPTICAL CHARACTERISTICS

Ta=25℃ , VDD=3.3V

ITEM		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Average Luminance		L_{AVE}	5 Points	288	360	-	cd / m²	*1) 3)
Luminance uniformity		$\delta_{WHITE-5P}$	5 Points	78	80	-	%	*1) 3)
Luminance uniformity		$\delta_{WHITE-13P}$	13Points	65	-	-	%	*1) 3)
Color Gamut		CG		-	60		-	-
Response Time		R + F	θ=ψ= 0°	-	16	25	ms	*5)
Contrast Ratio (CEN)		CR	θ=ψ= 0°	-	800	-	-	*1) 2)
View Angle	Horizontal	Left(θ_L)	CR≧10	80	85	-	-	*4)
		Right(θ_R)		80	85	-		
	Vertical	Up(Ψ_H)		80	85	-		
		Down(ψ_L)		80	85	-		
Color Coordinate	W	Wx	θ=ψ= 0°	-0.03	0.313	+0.03	-	*1) 3)
		Wy			0.329			
	R	Rx			0.6399			
		Ry			0.3356			
	G	Gx			0.3166			
		Gy			0.6033			
	B	Bx			0.1526			
		By			0.0582			

Color coordinate and color gamut are measured by BM5A or equal equipment, and all the other items are measured by BM-5A(TOPCON). All these items are measured under the dark room condition (no ambient light). Measurement Condition: IL=17.5mA