



Type No. **F-51405GNY-LA-AA**

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Revision History

Rev.	Date	Page	Comment

1. General Specifications

Operating Temp.	:	min. 0°C ~max. 50°C
Storage Temp.	:	min. -20°C ~max. 70°C
Dot Pixels	:	240 (W) × 64 (H) dots
Dot Size	:	0.51 (W) × 0.51 (H) mm
Dot Pitch	:	0.53 (W) × 0.53 (H) mm
Viewing Area	:	130.2 (W) × 36.7 (H) mm
Outline Dimensions	:	135.2** (W) × 51.7* (H) × 9.8max.* (D) mm * Without Cable and CFL Cable **Without Hook
Weight	:	88.8g max.
LCD Type	:	NTD-21409 (STN / Yellow-mode / Transmissive)
Viewing Angle	:	6:00
Data Transfer	:	8-bit parallel data transfer
Backlight	:	LED Backlight / Amber
Drawings	:	Dimensional Outline UE-310631B

2. Electrical Specifications

2.1. Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage (Logic)	V _{DD} -V _{SS}	-	-0.3	7.0	V
Supply Voltage (Booster Circuit)	V _{SS2}	With Double *1	-7.0	+0.3	V
		With Triple *1	-6.0	+0.3	
		With Quad *1	-4.5	+0.3	
Supply Voltage 1 (LCD Drive)	V ₅ , V _{OUT}	*1	-18.0	+0.3	V
Supply Voltage 2 (LCD Drive)	V ₁ , V ₂ , V ₃ , V ₄	*1	V ₅	+0.3	V
Input Voltage	V _{IN}	-	-0.3	V _{DD} +0.3	V
Output Voltage	V _{OUT}	-	-0.3	V _{DD} +0.3	V

*1 Relative to V_{DD}.

2.2. DC Characteristics

T_a=25°C, V_{SS}=0V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage (Logic)	V _{DD} -V _{SS}	-	1.8	-	5.5	V
Supply Voltage (LCD Drive)	V ₅	*1	-16.0	-	-4.5	V
	V ₁ , V ₂		0.4×V ₅	-	V _{DD}	
	V ₃ , V ₄		V ₅	-	0.6×V ₅	
Supply Voltage (Booster Circuit)	V _{SS2}	With Triple *1	-6.0	-	-1.8	V
		With Quad *1	-4.5	-	-1.8	
Booster Output Voltage	V _{OUT}	*1	-18.0	-	-	V
Voltage Regulator Operating Voltage	V _{OUT}	*1	-18.0	-	-6.0	V
Voltage Follower Operating Voltage	V ₅	*1	-16.0	-	-4.5	V
Base Voltage	V _{REG0}	-0.05%/°C *1	-2.04	-2.10	-2.16	V
	V _{REG1}	-0.20%/°C *1	-4.65	-4.90	-5.15	V
"High" Level Input Voltage	V _{IH}	-	0.8×V _{DD}	-	V _{DD}	V
"Low" Level Input Voltage	V _{IL}	-	V _{SS}	-	0.2×V _{DD}	V
"High" Level Output Voltage	V _{OH}	I _{OH} =-0.1mA	0.8×V _{DD}	-	V _{DD}	V
"Low" Level Output Voltage	V _{OL}	I _{OL} =0.1mA	V _{SS}	-	0.2×V _{DD}	V
Supply Current	I _{DD}	V _{DD} -V _{SS} =-5.0V	-	2.6	3.9	mA
	I ₅	V _{DD} -V ₅ =12.4V	-	0.2	0.3	mA

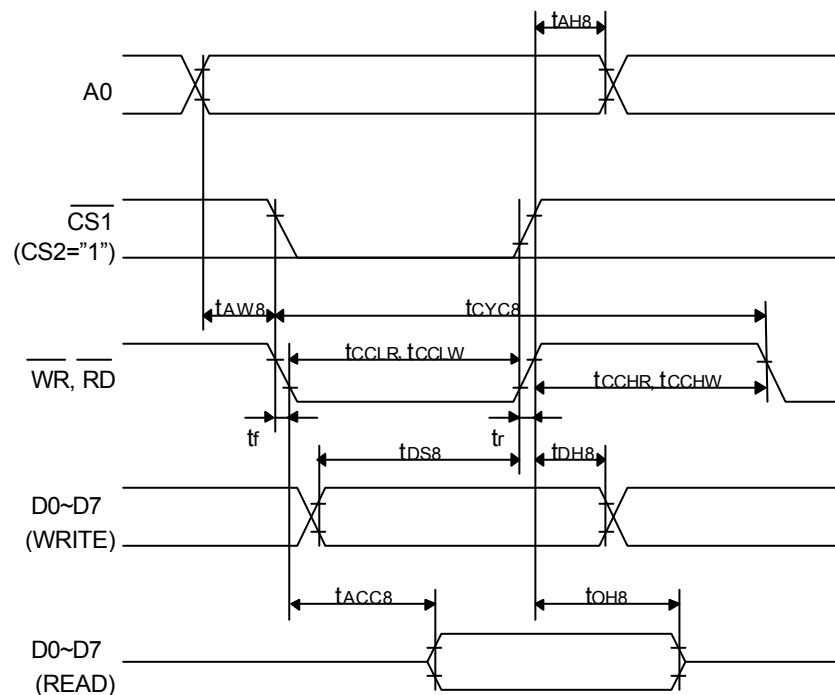
*1 Relative to V_{DD}.

2.3.AC Characteristics

2.3.1.Read/Write Operation Sequence (80 series CPU)

$V_{DD}=5.0V\pm 10\%$

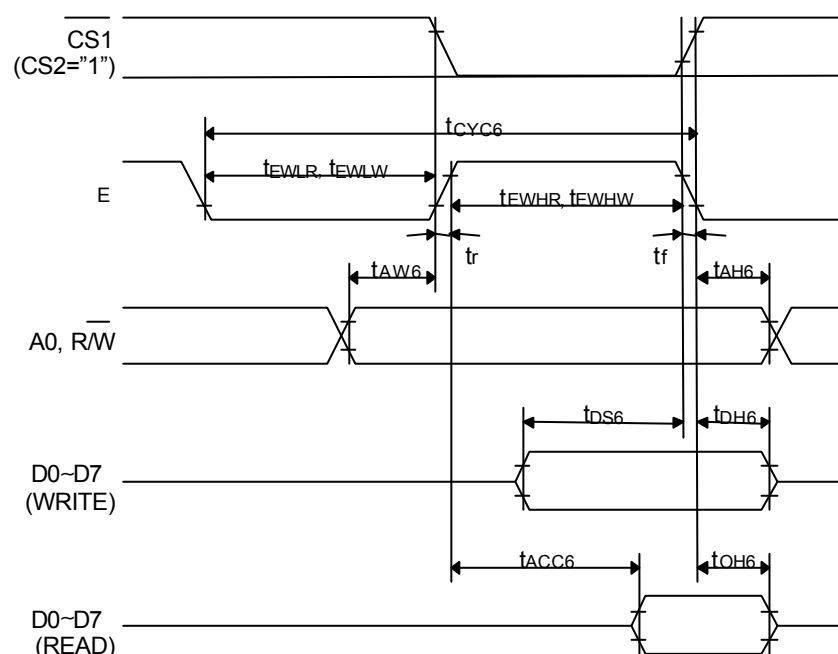
Parameter		Symbol	Min.	Max.	Units
Address Setup Time		t_{AW8}	0	-	ns
Address Hold Time		t_{AH8}	0	-	ns
System Cycle Time		t_{CYC8}	166	-	ns
Control Low Pulse Width	WRITE	t_{CCLW}	30	-	ns
	READ	t_{CCLR}	70	-	ns
Control High Pulse Width	WRITE	t_{CCHW}	30	-	ns
	READ	t_{CCHR}	30	-	ns
Data Setup Time		t_{DS8}	30	-	ns
Data Hold Time		t_{DH8}	10	-	ns
RD Access Time		t_{ACC8}	-	70	ns
Output Disable Time		t_{OH8}	5	50	ns



2.3.2. Read/Write Operation Sequence (68 series CPU)

$V_{DD}=5.0V \pm 10\%$

Parameter		Symbol	Min.	Max.	Units
Address Setup Time		t_{AH6}	0	-	ns
Address Hold Time		t_{AW6}	0	-	ns
System Cycle Time		t_{CYC6}	166	-	ns
Data Setup Time		t_{DS6}	30	-	ns
Data Hold Time		t_{DH6}	10	-	ns
Access Time (CL=100pF)		t_{ACC6}	-	70	ns
Output Disable Time		t_{OH6}	10	50	ns
Enable High Pulse Width	READ	t_{EWHR}	70	-	ns
	WRITE	t_{EWHW}	30	-	ns
Enable Low Pulse Width	READ	t_{EWLR}	30	-	ns
	WRITE	t_{EWLW}	30	-	ns



2.3.3. Display Control Timing Characteristics

Reset Input Timing

$V_{DD}=5.0\pm10\%$

Parameter	Symbol	Min.	Typ.	Max.	Units
Reset time	t_R	-	-	0.5	μs
Reset "L" Pulse Width	t_{RW}	0.5	-	-	

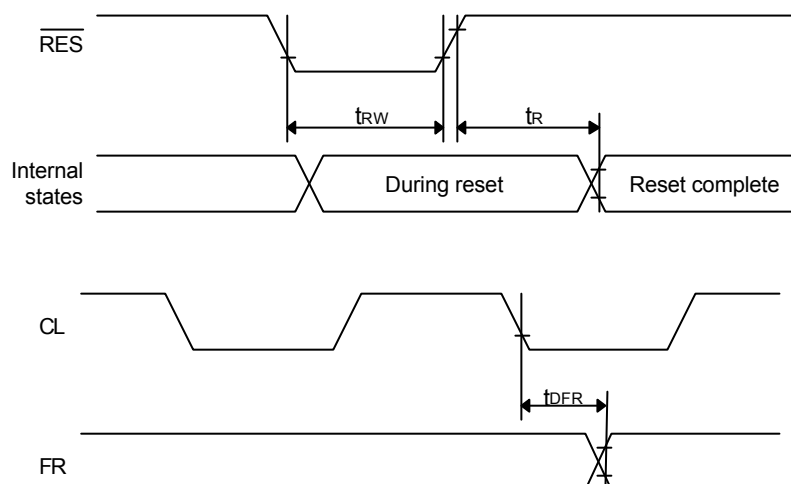
Output Timing

$V_{DD}=5.0\pm10\%$

Parameter	Symbol	Min.	Typ.	Max.	Units
FR Delay Time	t_{DFR}	-	10	40	ns

Note 1 :Valid only when the master mode is selected.

Note 2:All timing is based on 20% and 80% of V_{SS} .

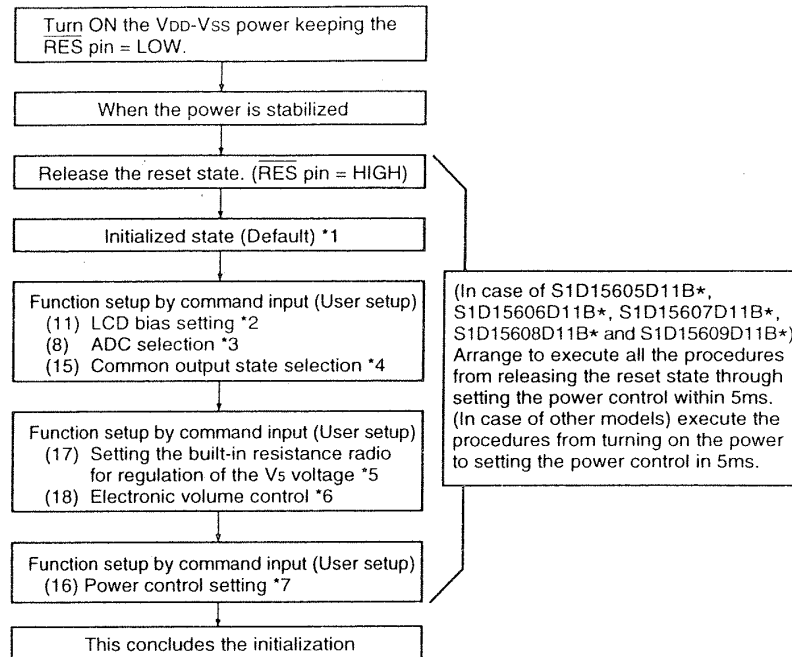


Instruction Setup: Reference (reference)

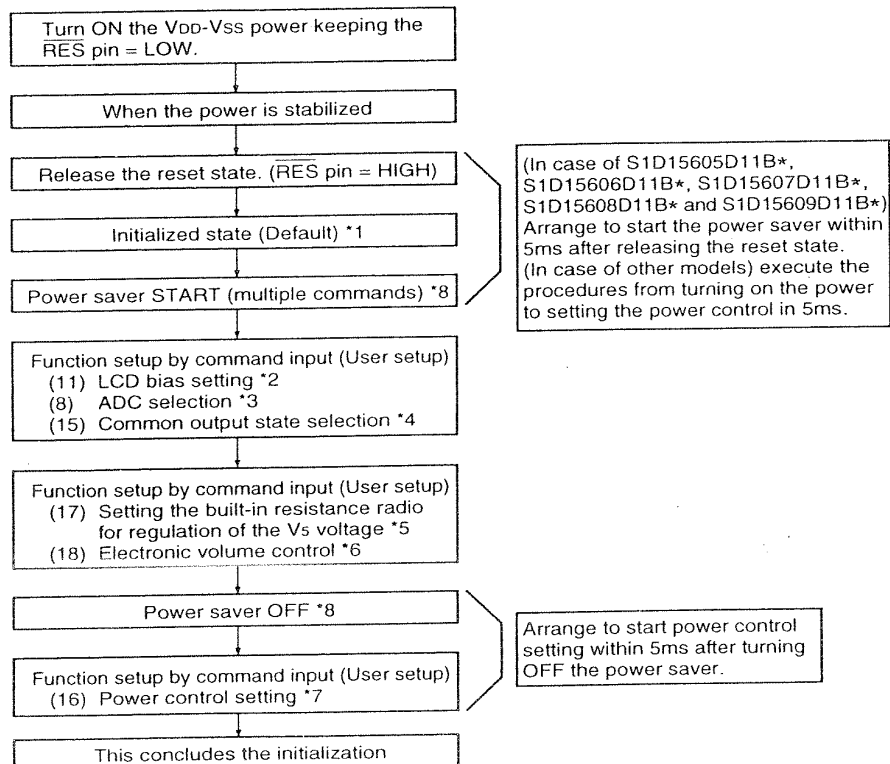
(1) Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V₂ and V₃ (SEG pin) and V₁ and V₄ (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V₁ ~ V₅) and the V_{DD} pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

① When the built-in power is being used immediately after turning on the power:



② When the built-in power is not being used immediately after turning on the power:

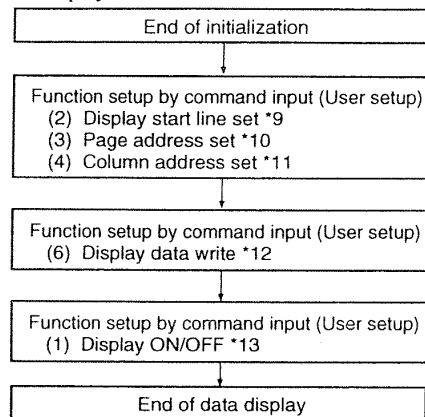


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

- *1: 6. Description of functions; "Resetting circuit" (The contents of DDRAM can be variable even in the initial setting (Default) at the reset state.)
- *2: 7. Command description; "(11) LCD bias setting"
- *3: 7. Command description; "(8) ADC selection"
- *4: 7. Command description; "(15) Common output state selection"
- *5: 6. Description of functions; "Power circuit" & "(17) Command description; Setting the built-in resistance ratio for regulation of the V₅ voltage"
- *6: 6. Description of functions; "Power circuit" & "(18) Command description; Electronic volume control"
- *7: 6. Description of functions; "Power circuit" & "(16) Command description; Power control setting"
- *8: 7. The power saver ON state can either be in sleep state or stand-by state.
Command description; "Power saver START (multiple commands)"

(2) Data Display

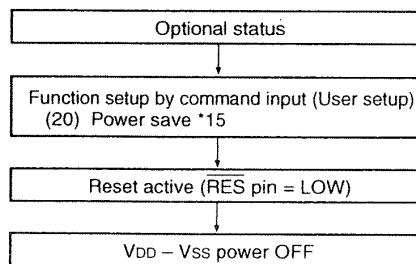


Notes: Reference items

- *9: Command Description; Display start line set
- *10: Command Description; Page address set
- *11: Command Description; Column address set
- *12: Command Description; Display data write
- *13: Command Description; Display ON/OFF
Avoid displaying all the data at the data display start (when the display is ON) in white.

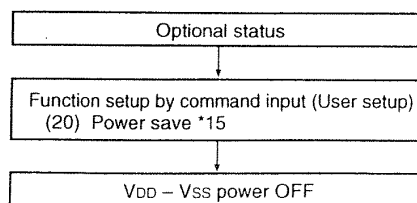
(3) Power OFF *14

- In case of S1D15605D11B*, S1D15606D11B*, S1D15607D11B*, S1D15608D11B* and S1D15609D11B*,



Set the time (t_L) from reset active to turning off the V_{DD} - V_{SS} power (V_{DD} - V_{SS} = 1.8 V) longer than the time (t_H) when the potential of V₅ ~ V₁ becomes below the threshold voltage (approximately 1 V) of the LCD panel. For t_H , refer to the <Reference Data> of this event. When t_H is too long, insert a resistor between V₅ and V_{DD} to reduce it.

- In case of other models,



Set the time (t_L) from power save to turning off the V_{DD} - V_{SS} power (V_{DD} - V_{SS} = 1.8 V) longer than the time (t_H) when the potential of V₅ ~ V₁ becomes below the threshold voltage (approximately 1V) of the LCD panel.

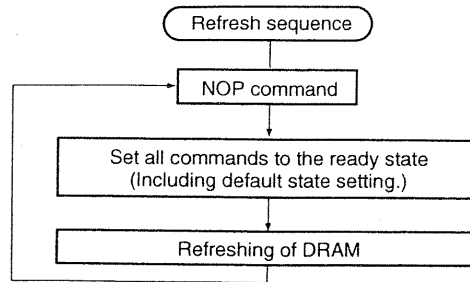
- t_H is determined depending on the voltage regulator external resistors R_a and R_b and the time constant of V₅ ~ V₁ smoothing capacity C₂.
- When an internal resistor is used, it is recommended to insert a resistor R between V_{DD} and V₅ to reduce t_H .

Notes: Reference items

- *14: The logic circuit of this IC's power supply V_{DD} - V_{SS} controls the driver of the LCD power supply V_{DD} - V₅. So, if the power supply V_{DD} - V_{SS} is cut off when the LCD power supply V_{DD} - V₅ has still any residual voltage, the driver (COM, SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:
 - After turning off the internal power supply, make sure that the potential V₅ ~ V₁ has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (V_{DD} - V_{SS}).
6. Description of Function, 6.7 Power Circuit
- *15: After inputting the power save command, be sure to reset the function using the $\overline{\text{RES}}$ terminal until the power supply V_{DD} - V_{SS} is turned off. 7. Command Description (20) Power Save
- *16: After inputting the power save command, do not reset the function using the RES terminal until the power supply V_{DD} - V_{SS} is turned off. 7. Command Description (20) Power Save

(4) Refresh

It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.



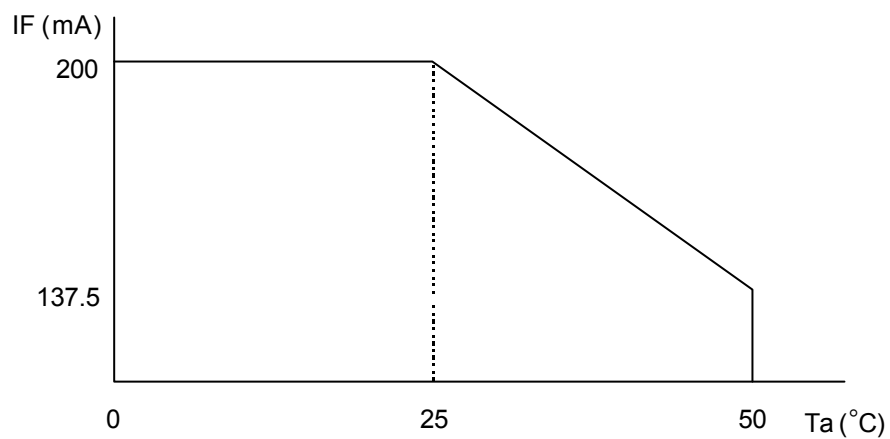
2.4. Lighting Specifications

2.4.1. Absolute Maximum Ratings

Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Foward Current	I _F	Note 1	-	-	200	mA
Reverse Voltage	V _R	-	-	-	8	V
LED Power Dissipation	P _D	-	-	-	920	mW

Note 1 : Refer to the foward current derating curve.



2.4.2. Operating Characteristics

Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Foward Voltage	V _F	I _F =80mA	-	4.4	4.6	V
Luminance of Backlight Surface	L	I _F =80mA	45	60	-	cd/m ²

3.Optical Specifications

3.1.LCD Driving Voltage

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Recommended LCD Driving Voltage Note 1	V _{DD} -V ₅	Ta= 0°C	-	-	13.7	V
		Ta=25°C	11.5	12.4	13.3	V
		Ta=50°C	10.9	-	-	V

Note 1 : Voltage (Applied actual waveform to LCD Module) for the best contrast. The range of minimum and maximum shows tolerance of the operating voltage. The specified contrast ratio and response time are not guaranteed over the entire range.

3.2.Optical Characteristics

Ta=25°C, 1/65 Duty, 1/9 Bias, V_{OD}=12.4V (Note 4), $\theta = 0^\circ$, $\phi = -^\circ$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Contrast Ratio Note 1	CR	$\theta = 0^\circ, \phi = -^\circ$	-	3.5	-	
Viewing Angle		Shown in 3.3				
Response Time	Rise Note 2	T _{ON}	-	130	200	ms
	Decay Note 3	T _{OFF}	-	60	120	ms

Note 1 : Contrast ratio is defined as follows.

$$CR = L_{OFF} / L_{ON}$$

L_{ON} : Luminance of the ON segments

L_{OFF} : Luminance of the OFF segments

Measuring Spot : 0.9mm ϕ

Note 2 : The time that the luminance level reaches 90% of the saturation level from 0% when ON signal is applied.

Note 3 : The time that the luminance level reaches 10% of the saturation level from 100% when OFF signal is applied.

Note 4 : Definition of Driving Voltage V_{OD}

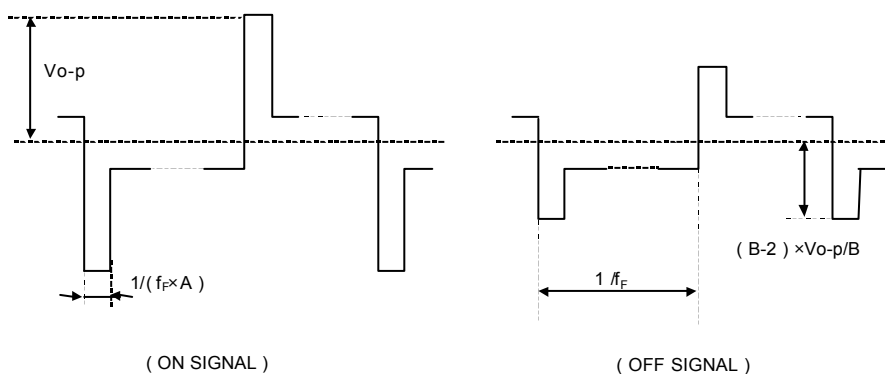
$$V_{OD} = V_{CC} - V_{ADJ} - V_{BE}$$

Assuming that the typical driving waveforms shown below are applied to the LCD Panel at 1/A Duty - 1/B Bias (A: Duty Number, B: Bias Number). Driving voltage V_{OD} is defined as follows.

$$V_{OD} = (V_{th1} + V_{th2}) / 2$$

V_{th1}: The voltage V_{O-P} that should provide 70% of the saturation level in the luminance at the segment which the ON signal is applied to.

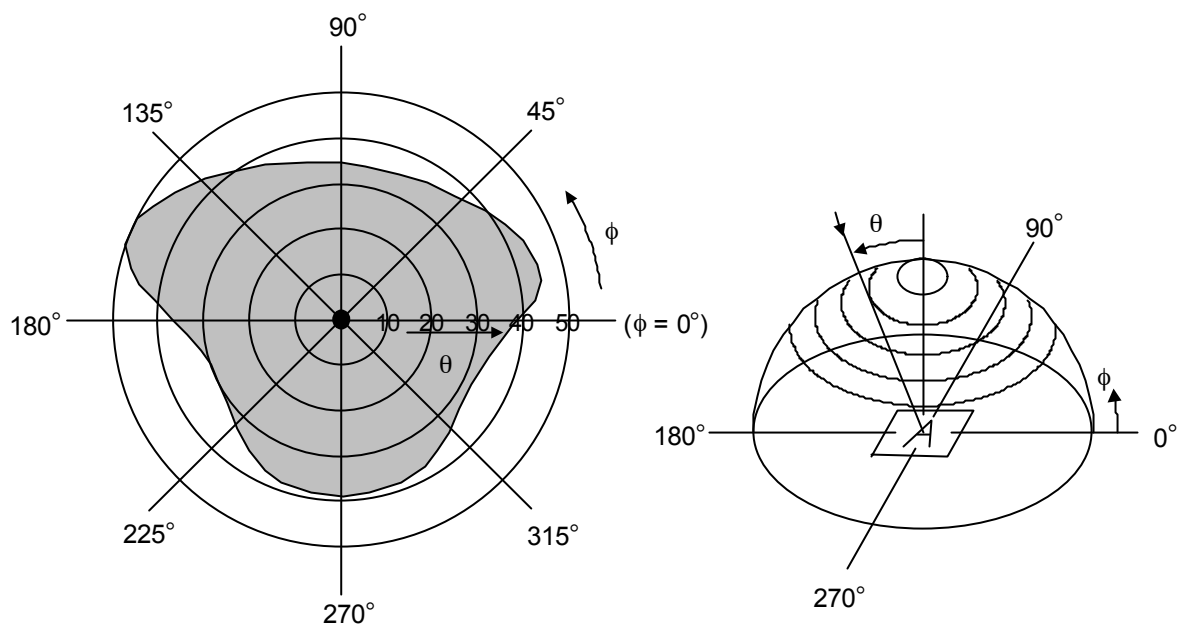
V_{th2}: The voltage V_{O-P} that should provide 20% of the saturation level in the luminance at the segment which the OFF signal is applied to.




3.3. Definition of Viewing Angle and Optimum Viewing Area

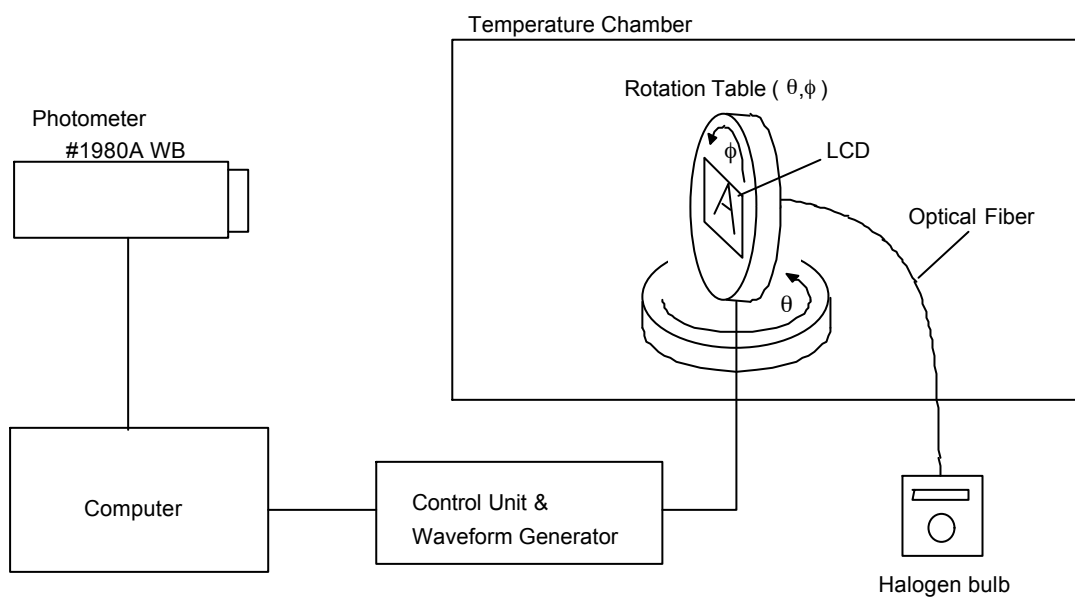
*Point • shows the point where contrast ratio is measured. : $\theta = 0^\circ$, $\phi = 0^\circ$

*Driving condition: 1/65 Duty, 1/9 Bias, $V_{OD}=12.4V$, $f_F=84.6Hz$



*Area  shows typ. $CR \geq 1.5$ (Measuring Spot : $0.9mm\phi$)

3.4. System Block Diagram



4.I/O Terminal

4.1.Pin Assignment

CN1,2

No.	Symbol	Function
1	NC	Non-connection
2	FR	Input/Output for LCD AC Drive
3	CL	Input for Display Clock
4	DOF	LCD Blanking Control Terminal
5	CS1	Chip Select Signal L : Active
6	CS2	Chip Select Signal H : Active
7	RES	Reset Signal L : Reset
8	A0	H : D0~D7 are Display Data L : D0~D7 are Instructions
9	WR (R/W)	68 family CPU : Read/Write Select Signal H : Read 80 family CPU : Write Signal L : Active
10	RD (E)	68 family CPU : Enable Signal H : Active 80 family CPU : Read Signal L : Active
11	D0	Data Bus Line
12	D1	Data Bus Line
13	D2	Data Bus Line
14	D3	Data Bus Line
15	D4	Data Bus Line
16	D5	Data Bus Line
17	D6	Data Bus Line
18	D7	Data Bus Line
19	V _{DD}	Power Supply for Logic
20	V _{SS}	Power Supply (0V, GND)
21	V _{OUT}	DC/DC Voltage Converter Output
22	CAP3-	DC/DC Voltage Converter Capacitor 3 Negative Connection
23	CAP1+	DC/DC Voltage Converter Capacitor 1 Positive Connection
24	CAP1-	DC/DC Voltage Converter Capacitor 1 Negative Connection
25	CAP2-	DC/DC Voltage Converter Capacitor 2 Negative Connection
26	CAP2+	DC/DC Voltage Converter Capacitor 2 Positive Connection
27	V ₁	Power Supply for LCD Drive V ₁ = 1/5,V ₅
28	V ₂	Power Supply for LCD Drive V ₂ = 2/5,V ₅
29	V ₃	Power Supply for LCD Drive V ₃ = 3/5,V ₅
30	V ₄	Power Supply for LCD Drive V ₄ = 4/5,V ₅
31	V ₅	Power Supply for LCD Drive V ₅ ,V _{OUT}
32	VR	Voltage Adjustment Pin Applies voltage between V _{CC} and V ₅ using a resistive divider.

33	C86	Interface Mode Select Signal H : 68 series L : 80 series
34	P/S	Parallel/Serial Data Select Signal H : Parallel L : Serial
35	IRS	This terminal selects the resistors for the V5 voltage level adjustment. IRS="H" :Use the internal resistors IRS="H" :Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.
36	NC	Non-connection

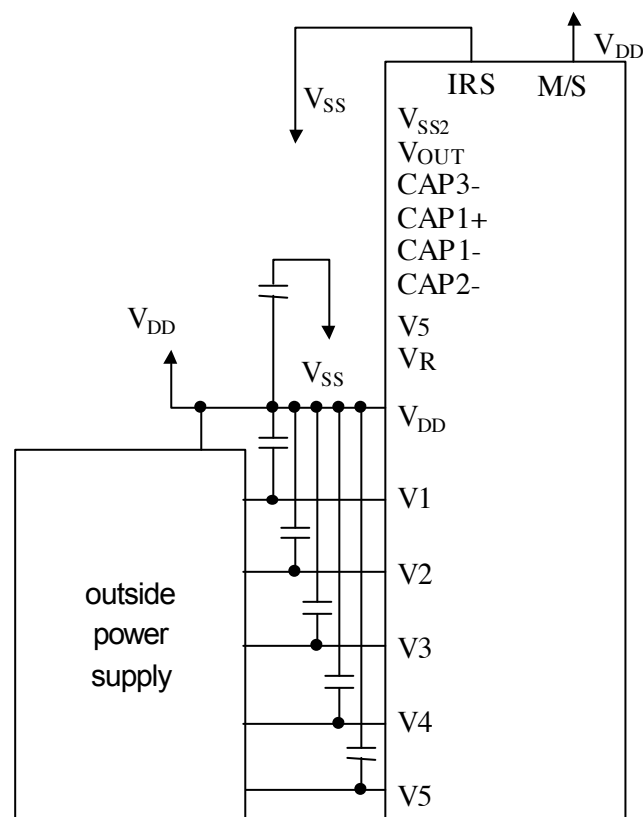
CN3

No.	Symbol	Function
1	ANODE	LED Anode Terminal
2	CATHODE	LED Cathode Terminal

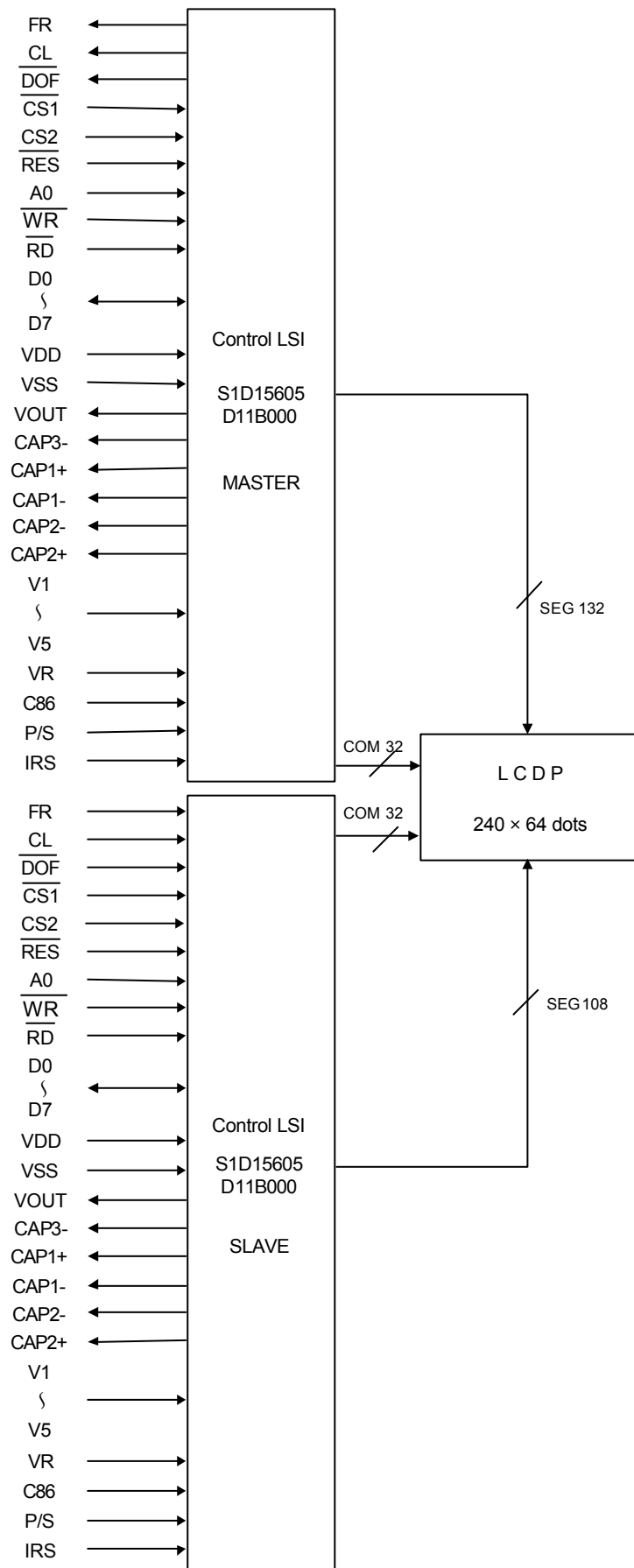
4.2.Recommendation Example of the circuit

When installing the COG,it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors).By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.

Please use circuit by outside power supply.



4.3. Block Diagram



5.Test

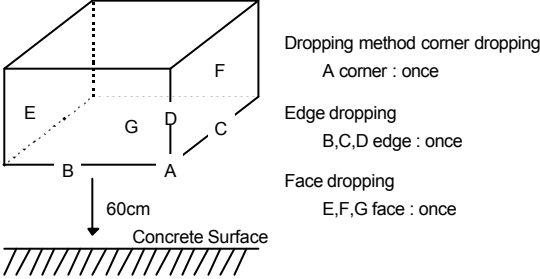
No change on display and in operation under the following test condition.

Conditions: Unless otherwise specified, tests will be conducted under the following condition.

Temperature: $20\pm5^{\circ}\text{C}$

Humidity : $65\pm5\%\text{RH}$

tests will be not conducted under functioning state.

No.	Parameter	Conditions	Notes
1	High Temperature Operating	$50^{\circ}\text{C}\pm2^{\circ}\text{C}$, 96hrs (operation state)	
2	Low Temperature Operating	$0^{\circ}\text{C}\pm2^{\circ}\text{C}$, 96hrs (operation state)	1
3	High Temperature Storage	$70^{\circ}\text{C}\pm2^{\circ}\text{C}$, 96hrs	2
4	Low Temperature Storage	$-20^{\circ}\text{C}\pm2^{\circ}\text{C}$, 96hrs	1,2
5	Damp Proof Test	$40^{\circ}\text{C}\pm2^{\circ}\text{C}$, 90~95%RH, 96hrs	1,2
6	Vibration Test	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X, Y, Z for each 15 minutes	3
7	Shock Test	To be measured after dropping from 60cm high on the concrete surface in packing state. 	

Note 1 :No dew condensation to be observed.

Note 2 :The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after removed from the test chamber.

Note 3 :Vibration test will be conducted to the product itself without putting it in a container.

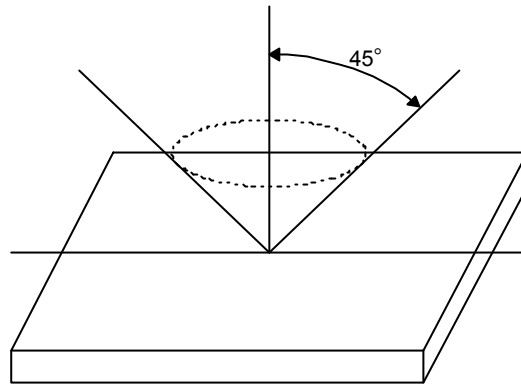
6.Appearance Standards

6.1.Inspection conditions

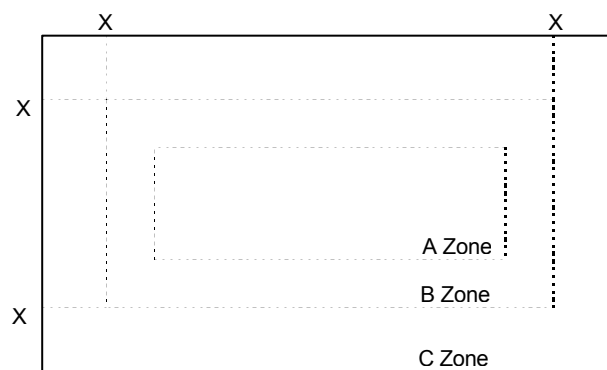
The LCD shall be inspected under 40W white fluorescent light.

The distance between the eyes and the sample shall be more than 30cm.

All directions for inspecting the sample should be within 45°against perpendicular line.



6.2.Definition of applicable Zones



X : Maximum Seal Line

A Zone : Active display area

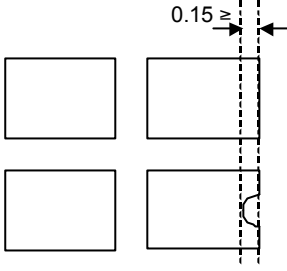
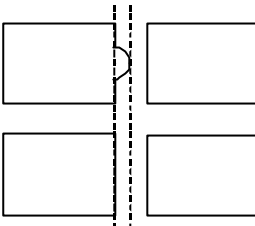
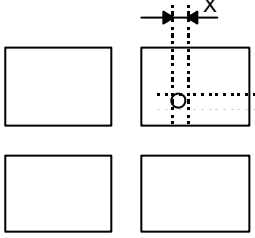
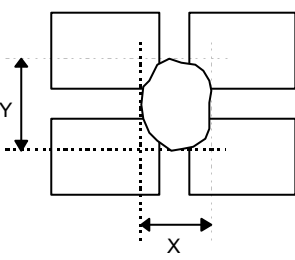
B Zone : Out of active display area ~ Maximum seal line

C Zone : Rest parts

A Zone + B Zone = Validity viewing area

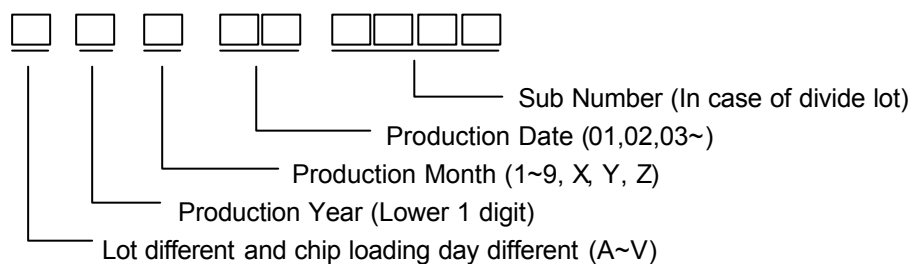
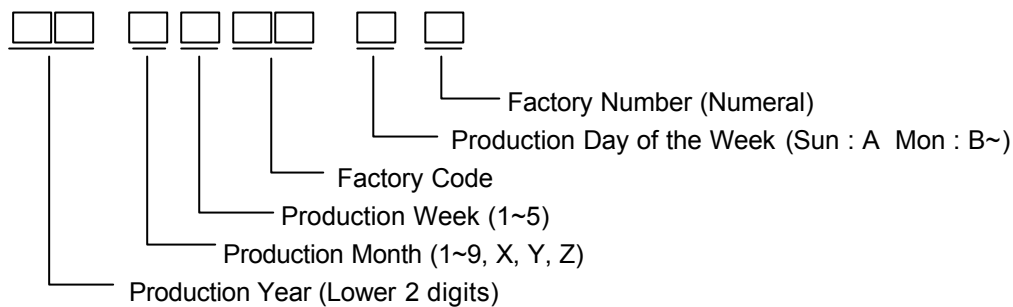
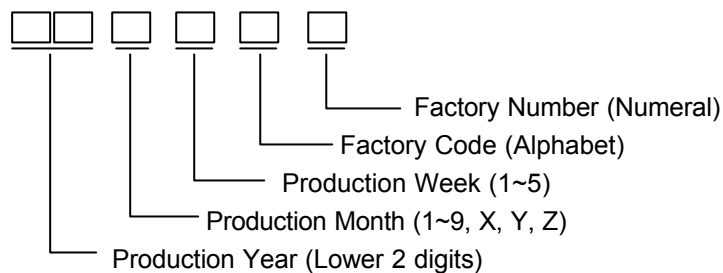
6.3. Standards

No.	Parameter	Criteria																												
1	Black and White Spots, Foreign Substances	(1) Round Shape																												
		<table><tr><th rowspan="2">Zone Dimension (mm)</th><th colspan="3">Acceptable Number</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$D \leq 0.1$</td><td>*</td><td>*</td><td>*</td></tr><tr><td>$0.1 < D \leq 0.2$</td><td>3</td><td>5</td><td>*</td></tr><tr><td>$0.2 < D \leq 0.25$</td><td>2</td><td>3</td><td>*</td></tr><tr><td>$0.25 < D \leq 0.3$</td><td>0</td><td>1</td><td>*</td></tr><tr><td>$0.3 < D$</td><td>0</td><td>0</td><td>*</td></tr></table>	Zone Dimension (mm)	Acceptable Number			A	B	C	$D \leq 0.1$	*	*	*	$0.1 < D \leq 0.2$	3	5	*	$0.2 < D \leq 0.25$	2	3	*	$0.25 < D \leq 0.3$	0	1	*	$0.3 < D$	0	0	*	
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		$D = (\text{Long} + \text{Short}) / 2$ * : Disregard																												
(2) Line Shape																														
<table><tr><th colspan="2">Zone X (mm) Y (mm)</th><th colspan="3">Acceptable Number</th></tr><tr><th colspan="2"></th><th>A</th><th>B</th><th>C</th></tr><tr><td>-</td><td>$0.03 \geq W$</td><td>*</td><td>*</td><td>*</td></tr><tr><td>$2.0 \geq L$</td><td>$0.05 \geq W$</td><td>3</td><td>3</td><td>*</td></tr><tr><td>$1.0 \geq L$</td><td>$0.1 \geq W$</td><td>3</td><td>3</td><td>*</td></tr><tr><td>-</td><td>$0.1 < W$</td><td colspan="3">In the same way (1)</td></tr></table>	Zone X (mm) Y (mm)		Acceptable Number					A	B	C	-	$0.03 \geq W$	*	*	*	$2.0 \geq L$	$0.05 \geq W$	3	3	*	$1.0 \geq L$	$0.1 \geq W$	3	3	*	-	$0.1 < W$	In the same way (1)		
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X : Length Y : Width * : Disregard																														
Total defects shall not exceed 5.																														
2	Air Bubbles (between glass & polarizer)	<table><tr><th rowspan="2">Zone Dimension (mm)</th><th colspan="3">Acceptable Number</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$D \leq 0.3$</td><td>*</td><td>*</td><td>*</td></tr><tr><td>$0.3 < D \leq 0.4$</td><td>3</td><td>*</td><td>*</td></tr><tr><td>$0.4 < D \leq 0.6$</td><td>2</td><td>3</td><td>*</td></tr><tr><td>$0.6 < D$</td><td>0</td><td>0</td><td>*</td></tr></table>	Zone Dimension (mm)	Acceptable Number			A	B	C	$D \leq 0.3$	*	*	*	$0.3 < D \leq 0.4$	3	*	*	$0.4 < D \leq 0.6$	2	3	*	$0.6 < D$	0	0	*					
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No.	Parameter	Criteria
3	The Shape of Dot	<p>(1) Dot Shape (with Dent)</p>  <p>As per the sketch of left hand.</p>
		<p>(2) Dot Shape (with Projection)</p>  <p>Should not be connected to next dot.</p>
		<p>(3) Pin Hole</p>  <p> $(X+Y) / 2 \leq 0.2\text{mm}$ (Less than 0.1mm is no counted.) </p>
		<p>(4) Deformation</p>  <p> $(X+Y) / 2 \leq 0.2\text{mm}$ </p>
		<p>Total acceptable number : 1/dot, 5/cell (Defect number of (4) : 1pc.)</p>
4	Polarizer Scratches	Not to be conspicuous defects.
5	Polarizer Dirts	If the stains are removed easily from LCDP surface, the module is not defective.
6	Complex Foreign Substance Defects	Black spots, line shaped foreign substances or air bubbles between glass & polarizer should be 5pcs maximum in total.
7	Distance between Different Foreign Substance Defects	$D \leq 0.2$: 20mm or more $0.2 < D$: 40mm or more

7.Code System of Production Lot

The production lot of module is specified some of the following.



8.Type Number

The type number of module is specified as follows.

F-51405GNY-LA-AA

9.Applying Precautions

Please contact us when questions and/or new problems not specified in this Specifications arise.

10.Precautions Relating Product Handling

The Following precautions will guide you in handling our product correctly.

1) Liquid crystal display devices

1. The liquid crystal display device panel used in the liquid crystal display module is made of plate glass. Avoid any strong mechanical shock. Should the glass break handle it with care.
2. The polarizer adhering to the surface of the LCD is made of a soft material. Guard against scratching it.

2) Care of the liquid crystal display module against static electricity discharge.

1. When working with the module, be sure to ground your body and any electrical equipment you may be using. We strongly recommend the use of anti static mats (made of rubber), to protect work tables against the hazards of electrical shock.
2. Avoid the use of work clothing made of synthetic fibers. We recommend cotton clothing or other conductivity-treated fibers.
3. Slowly and carefully remove the protective film from the LCD module, since this operation can generate static electricity.

3) When the LCD module alone must be stored for long periods of time:

1. Protect the modules from high temperature and humidity.
2. Keep the modules out of direct sunlight or direct exposure to ultraviolet rays.
3. Protect the modules from excessive external forces.

4) Use the module with a power supply that is equipped with an overcurrent protector circuit,since the module is not provided with this protective feature.

5) Do not ingest the LCD fluid itself should it leak out of a damaged LCD module. Should hands or clothing come in contact with LCD fluid, wash immediately with soap.

6) Conductivity is not guaranteed for models that use metal holders where solder connections between the metal holder and the PCB are not used. Please contact us to discuss appropriate ways to assure conductivity.

7) For models which use CFL:

1. High voltage of 1000V or greater is applied to the CFL cable connector area. Care should be taken not to touch connection areas to avoid burns.
2. Protect CFL cables from rubbing against the unit and thus causing the wire jacket to become worn.
3. The use of CFLs for extended periods of time at low temperatures will significantly shorten their service life.

8) For models which use touch panels:

1. Do not stack up modules since they can be damaged by components on neighboring modules.
2. Do not place heavy objects on top of the product. This could cause glass breakage.

9) For models which use COG,TAB,or COF:

1. The mechanical strength of the product is low since the IC chip faces out unprotected from the rear. Be sure to protect the rear of the IC chip from external forces.
2. Given the fact that the rear of the IC chip is left exposed, in order to protect the unit from electrical damage, avoid installation configurations in which the rear of the IC chip runs the risk of making any electrical contact.

- 10) Models which use flexible cable, heat seal, or TAB:
 1. In order to maintain reliability, do not touch or hold by the connector area.
 2. Avoid any bending, pulling, or other excessive force, which can result in broken connections.
- 11) have an adverse effect on connecting parts (LCD panel-TCP / HEAT SEAL / FPC / etc., PCB-TCP / HEAT SEAL / FPC etc., TCP-HEAT SEAL, TCP-FPC, HEAT SEAL-FPC, etc.,) depending on its materials.
Please check and evaluate these materials carefully before use.
- 12) In case of acrylic plate is attached to front side of LCD panel, cloudiness (very small cracks) can occur on acrylic plate, being influenced by some components generated from polarizer film..
Please check and evaluate those acrylic materials carefully before use.

11.Warranty

This product has been manufactured to your company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect, which may arise from additional manufacturing of the product (including disassembly and reassembly), after product delivery.
2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.
4. When the product is in CFL models, CFL service life and brightness will vary According to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.
5. We cannot accept responsibility for intellectual property of a third party, which may arise through the application of our product to your assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.
6. Optrex will not be held responsible for any quality guarantee issue for defect products judged as Optrex-origin longer than 2 (two) years from Optrex production or 1(one) year from Optrex, Optrex America, Optrex Europe, Display LC delivery which ever comes later.