SPECIFICATIONS FOR
LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
PART NO.	**240320M6TNQW-00H**
APPROVED BY	
DATE	

☑Approved For Specifications

☐**Approved For Specifications & Sample**

APPROVED BY	CHECKED BY	ORGANIZED BY

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2007/06/08	-	New Release	Emil

1 Features

This single-display module is suitable for cell phone application. The Main-LCD adopts one backlight with High brightness 4-lamps white LED.

(1) Construction: 2.8” a-Si color TFT-LCD, White LED Backlight, and FPCB.

(2) Main LCD : 2.1 Amorphous-TFT 2.8 inch display, transmissive, Normally white type, 12 o’clock.
2.2 240(RGB)X320 dots Matrix,1/320 Duty.
2.3 Narrow-contact ledge technique.
2.4 Main LCD Driver IC: ILI9320
2.5 Real 262K colors display:
262K: Red-6bit, Green-6bit, Blue-6bit (9/18-bit interface)
Dithering 262K: Red-5bit, Green-6bit, Blue-5bit (8/16-bit interface)

(3) Low cross talk by frame rate modulation
(4) Direct data display with display RAM
(5) Partial display function: You can save power by limiting the display space.
(6) MPU interface: 8/16-bit 80-Series, parallel interface.
(7) Abundant command functions:
Area scroll function
Display direction switching function
Power saving function
Electric volume control function: you are able to program the temperature compensation function.

2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*1 50.0 (W)×98.5 (H)×2.8	mm
Main LCD	Pixel size	0.18 (W)×0.18 (H)	mm
	Active area	43.2 (W)×57.6 (H)	mm
	Number of Pixels	240(H)×320(V) pixels	mm
Weight		TBD	g

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+3.3	V	
Power voltage	LED A – LED K	-0.5	+4.0	V	Parallel
Input voltage	VIN	-0.5	VDD	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +70°C Min. -20°C	Note 1: Non-condensing
Operating temperature	Max. +60°C Min. -10°C	Note 1: Non-condensing

Note 1：Ta≦+40°C・・・・Max.85%RH

Ta＞+40°C・・・・The max. humidity should not exceed the humidity with 40°C 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCM

(V_{DD}=3.0V, Ta=25 ^{o}C)

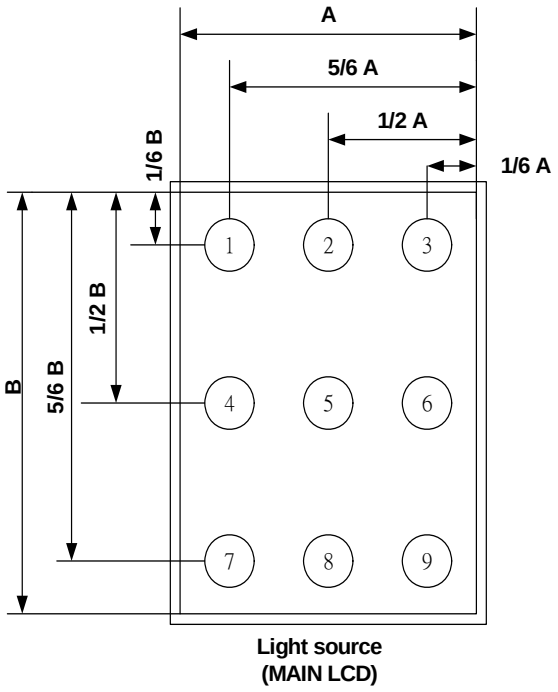
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{DD}		2.6	2.8	3.3	V
High-level input voltage	V_{IHC}		0.8V_{DD}		V_{DD}	V
Low-level input voltage	V_{ILC}		0		0.2V_{DD}	V
Consumption current of VDD	I_{DD}	LED OFF	-	8	-	mA
Consumption current of LED	I_{LED_ON}	V_{LED_ON}=3.6V	-	80	-	mA

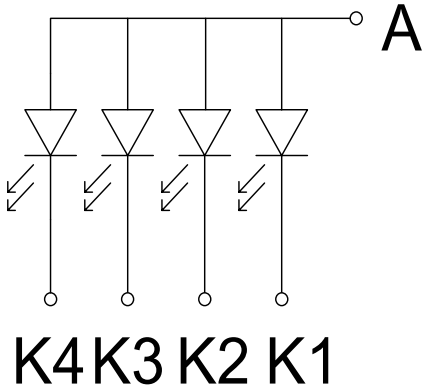
※ 1. 1/320 duty.

4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =80mA	3.4	3.6	3.8	V
Reverse voltage	V_r		-	-	12	V
Forward current	I_f	4-chip Parallel	75	80	85	mA
Power Consumption	P_{BL}	I_f =80mA	-	288	-	mW
Uniformity (with L/G)	-	I_f=80mA	80%*1	-	-	
Bare LED Luminous intensity	V_f I_f	3.6V 80mA	3000	-	-	cd/m^2
Luminous color	White					
Chip connection	4 chip parallel connection					

Bare LED measure position:





*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 80\%$

5 Optical characteristics

Main LCD

5.1 Optical characteristics

(1/320 Duty in case except as specified elsewhere Ta = 25°C)

LED backlight transmissive module:

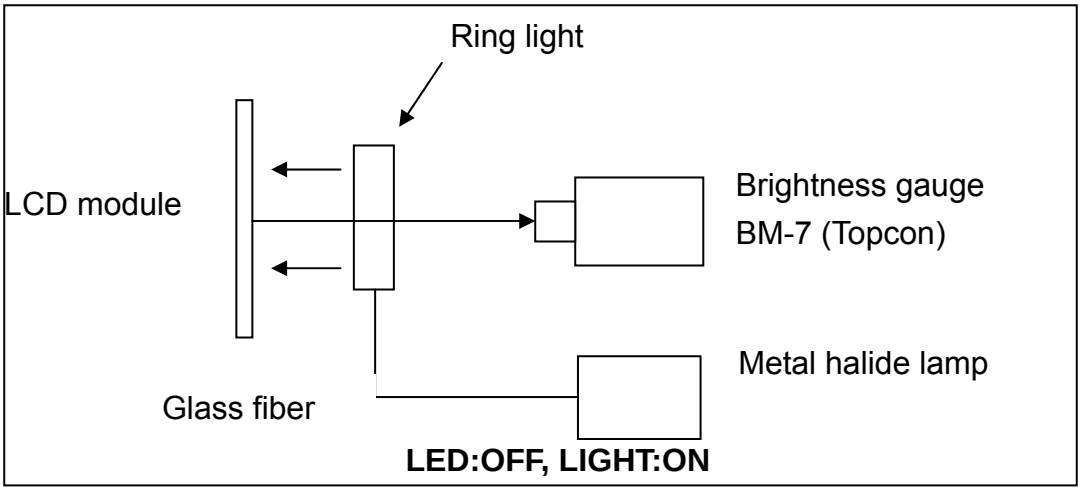
Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25°C	--	10	--	ms	θ=0°, φ=0° (Note 2)
	Tf	25°C	--	15	--		
Contrast ratio	CR	25°C	-	T.B.D.	-	-	θ=0°, φ=0° LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25°C	-	T.B.D.	-	%	
Visual angle range front and rear	θ	25°C	(θf) 35 (θb) 15			De-gree	φ = 0°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25°C	(θl) 45 (θr) 45			De-gree	φ=90°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			-	T.B.D.	--	Cd/m2	V_{LED}=3.6V, 80mA Full White pattern

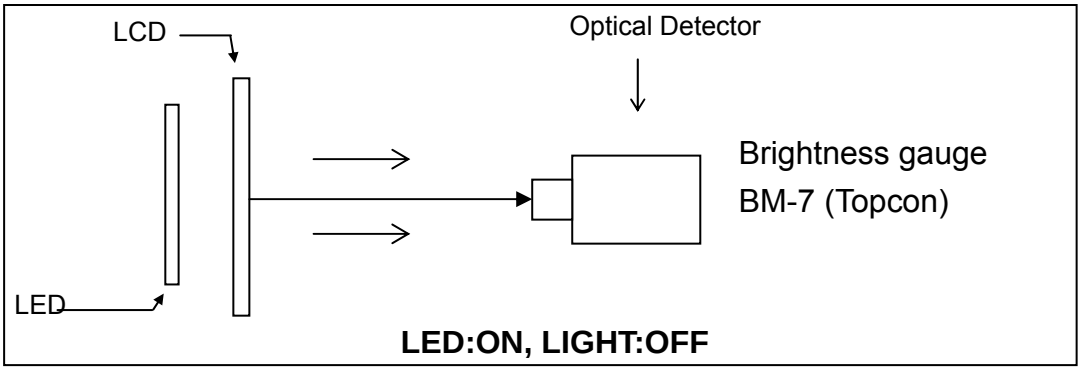
( ) is a default

5.2 CIE (x, y) chromaticity (1/320 Duty Ta = 25°C)

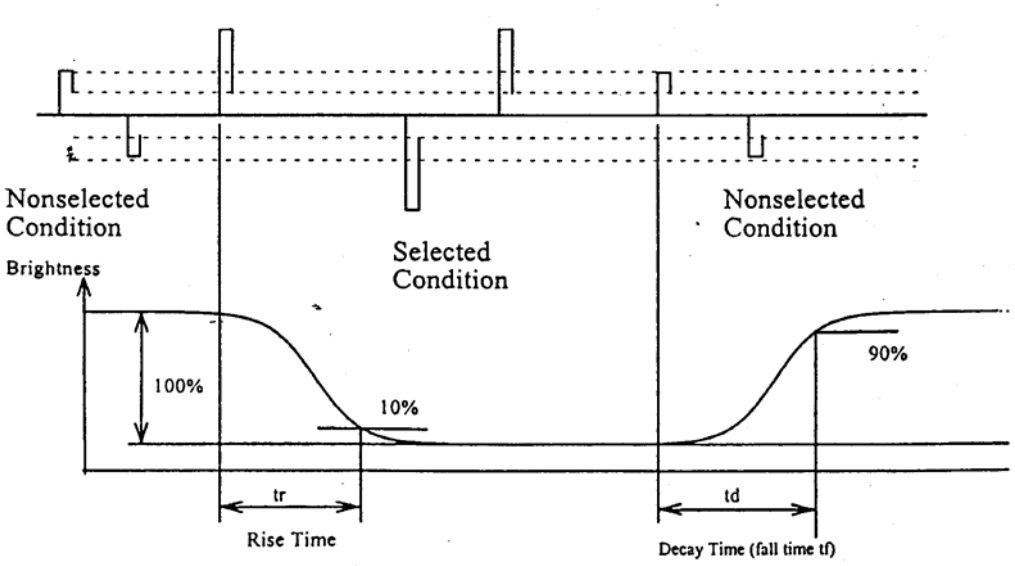
Item	Symbol	Transmissive			Conditions
		Min.	Typ.	Max.	
Red	X	T.B.D.	T.B.D.	T.B.D.	θ=0°, φ=0°
	Y	T.B.D.	T.B.D.	T.B.D.	
Green	X	T.B.D.	T.B.D.	T.B.D.	θ=0°, φ=0°
	Y	T.B.D.	T.B.D.	T.B.D.	
Blue	X	T.B.D.	T.B.D.	T.B.D.	θ=0°, φ=0°
	Y	T.B.D.	T.B.D.	T.B.D.	
White	X	T.B.D.	T.B.D.	T.B.D.	θ=0°, φ=0°
	Y	T.B.D.	T.B.D.	T.B.D.	

NOTE 1: Optical characteristic measurement system

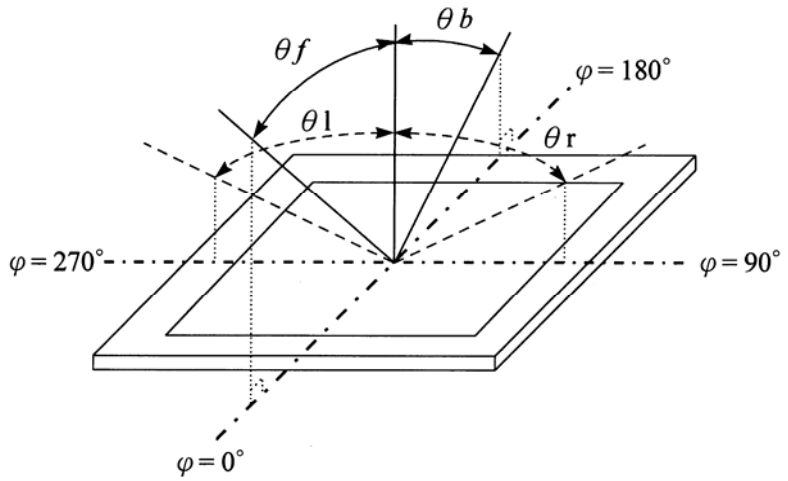




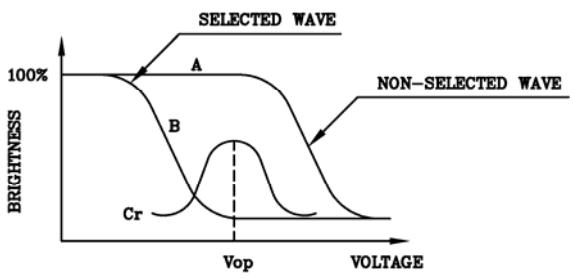
NOTE 2: Response tome definition



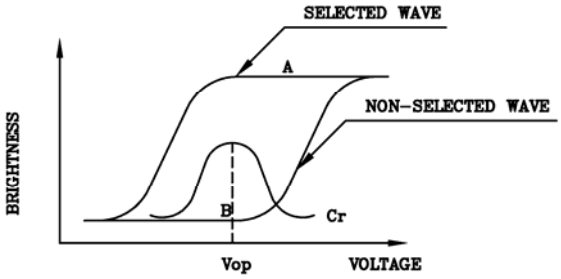
NOTE 3: φ 、θ definition



NOTE 4: Contrast definition



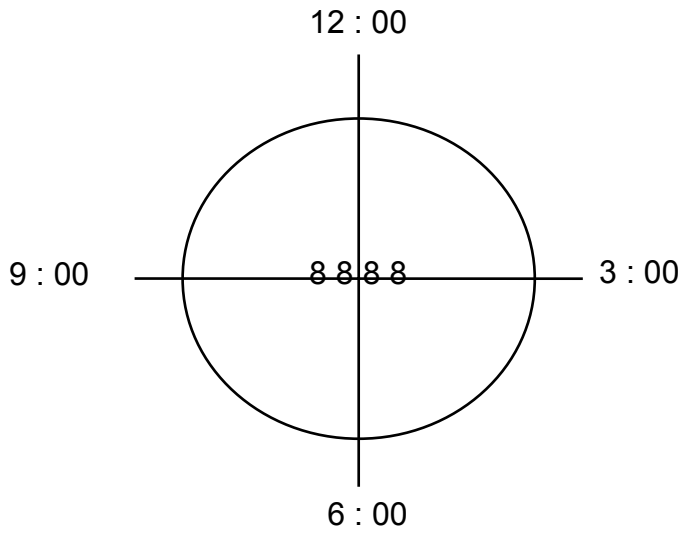
(positive type)



(negative type)

Contrast Ratio : Cr=A/B

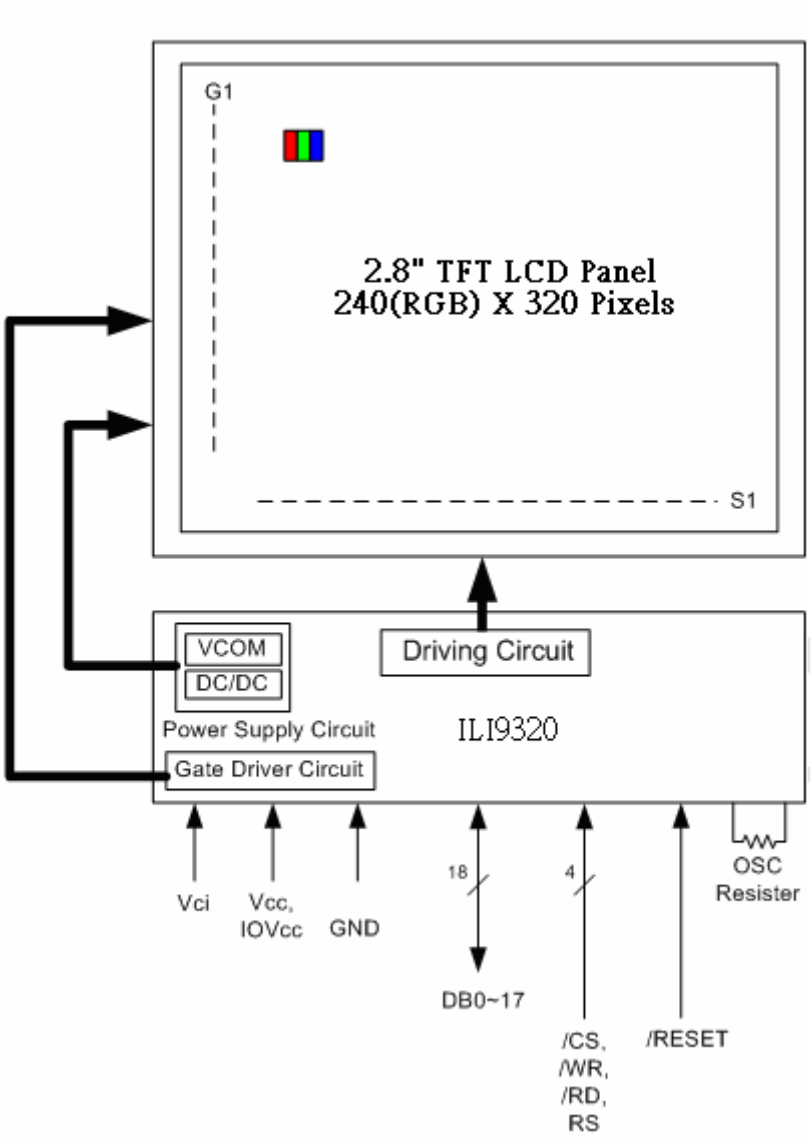
NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format: A-Si TFT transmissive, Normally white type, 12 o'clock.
Display composition: 240 x RGB x 320 dots
LCD Driver : ILI9320
Back light: White LED x 4 (I_{LED}=80mA)



7 Interface specifications

Pin No.	Terminal	Functions
1	DB0	Data Bus Bit 0 Contract to IC Data Bus Bit 1
2	DB1	Data Bus Bit 1 Contract to IC Data Bus Bit 2
3	DB2	Data Bus Bit 2 Contract to IC Data Bus Bit 3
4	DB3	Data Bus Bit 3 Contract to IC Data Bus Bit 4
5	GND	GND-terminal
6	VCC	Power supply for the internal logic circuit. (VCC=2.8~3.3V)
7	/CS	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed.
8	RS	The signal for register index or register command select . Low: Register index or internal status (in read operation); High: Register command.
9	/WR	Write clock terminal , active “L” (80 series interface)
10	/RD	Read clock terminal , active “L” (80 series interface)
11	NC	Not connection (IM0)
12	X+	Touch panel X axis (RIGHT)
13	Y+	Touch panel Y axis (BOTTOM)
14	X-	Touch panel X axis (LEFT)
15	Y+	Touch panel Y axis (TOP)
16	LED A	LED Backlight A terminal
17	LED K1	LED Backlight K1 terminal
18	LED K2	LED Backlight K2 terminal
19	LED K3	LED Backlight K3 terminal
20	LED K4	LED Backlight K4 terminal
21	NC	Not connection (IM3)
22	DB4	Data Bus Bit 4 Contract to IC Data Bus Bit 4
23	DB8	Data Bus Bit 10 Contract to IC Data Bus Bit 8
24	DB9	Data Bus Bit 11 Contract to IC Data Bus Bit 9
25	DB10	Data Bus Bit 12 Contract to IC Data Bus Bit 10
26	DB11	Data Bus Bit 13 Contract to IC Data Bus Bit 11
27	DB12	Data Bus Bit 14 Contract to IC Data Bus Bit 12
28	DB13	Data Bus Bit 15 Contract to IC Data Bus Bit 13
29	DB14	Data Bus Bit 16 Contract to IC Data Bus Bit 14
30	DB15	Data Bus Bit 17 Contract to IC Data Bus Bit 15
31	/RESET	Reset pin. Setting either pin low initializes the LSI.
32	VCI	Power supply for Step-up circuit. (VCi=2.8~3.3V)
33	VCC2	Power supply for I/O circuit
34	GND	GND-terminal
35	DB5	Data Bus Bit 5 Contract to IC Data Bus Bit 5
36	DB6	Data Bus Bit 6 Contract to IC Data Bus Bit 6
37	DB7	Data Bus Bit 7 Contract to IC Data Bus Bit 7

7.1 80-system 16-bit interface

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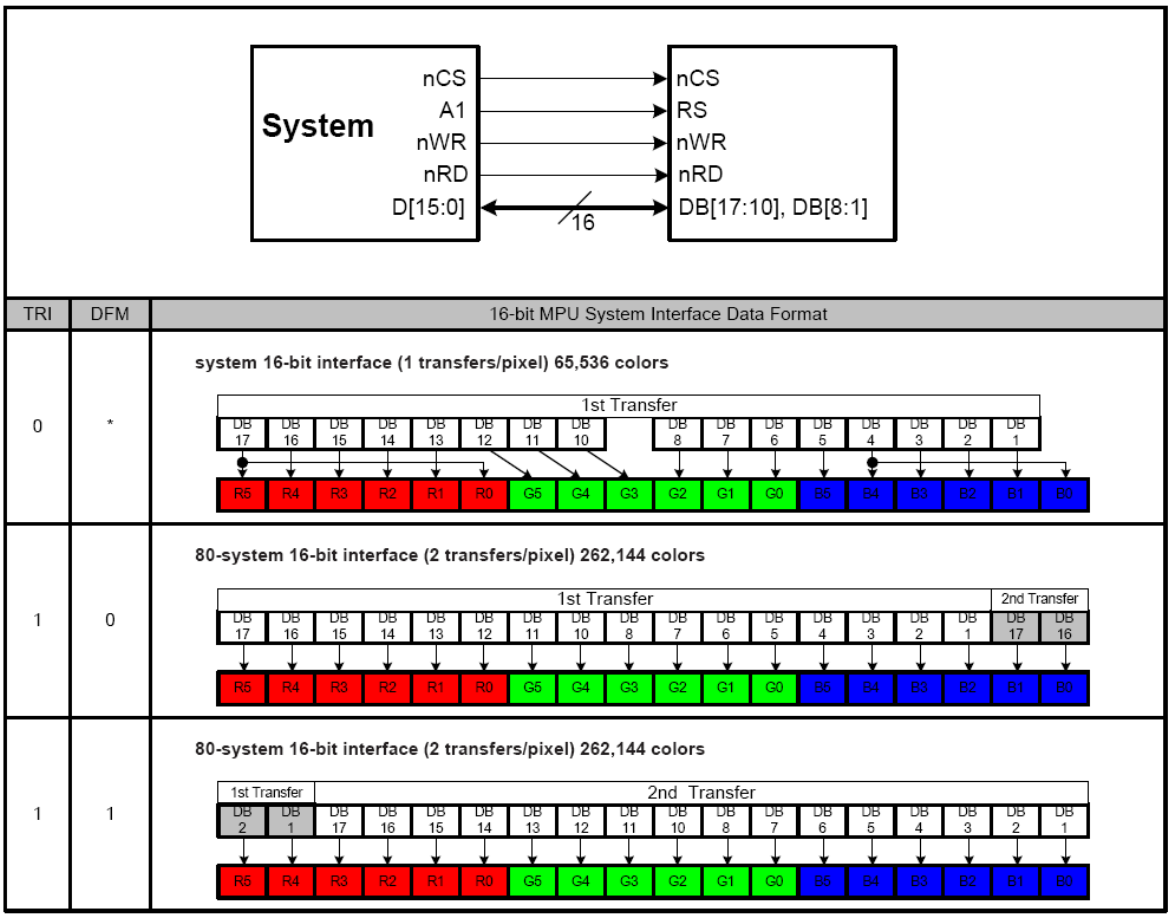
The i80/16-bit system interface is selected by setting the IM[3:0] as “0010” levels. The 262K or 65K color can be display through the 16-bit MPU interface. When the 262K color is displayed, two transfers (1st transfer: 2 bits, 2nd transfer: 16 bits or 1st transfer: 16 bits, 2nd transfer: 2 bits) are necessary for the 16-bit CPU interface.

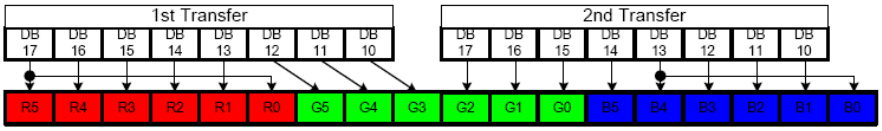
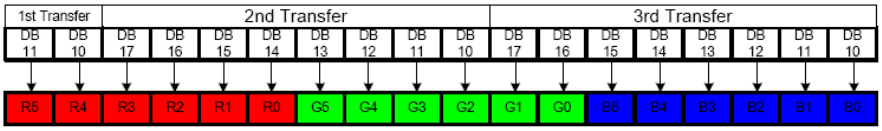
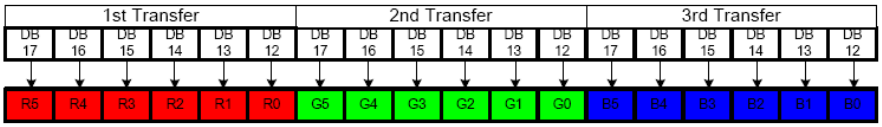


TRI	DFM	16-bit MPU System Interface Data Format
0	*	system 16-bit interface (1 transfers/pixel) 65,536 colors
1	0	80-system 16-bit interface (2 transfers/pixel) 262,144 colors
1	1	80-system 16-bit interface (2 transfers/pixel) 262,144 colors

262,144color are available

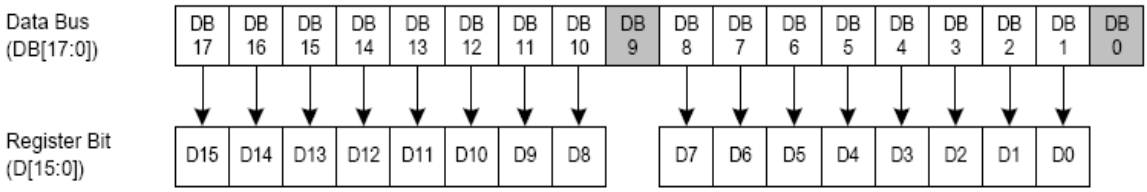
7.2 80-system 8-bit interface

The i80/8-bit system interface is selected by setting the IM[3:0] as “0011” and the DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to either Vcc or AGND.

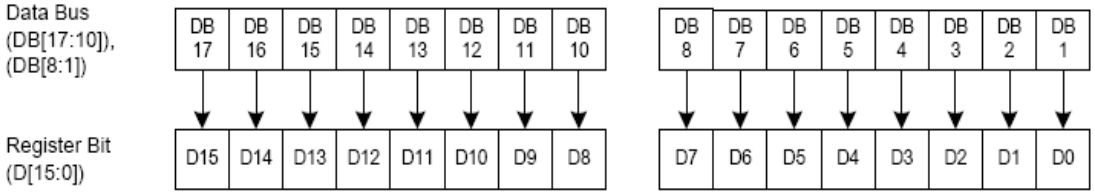
TRI	DFM	8-bit MPU System Interface Data Format
0	*	**system 8-bit interface (2 transfers/pixel) 65,536 colors** 
1	0	**80-system 8-bit interface (3 transfers/pixel) 262,144 colors** 
1	1	**80-system 8-bit interface (3 transfers/pixel) 262,144 colors** 

7.3 Register setting with i80 System Interface

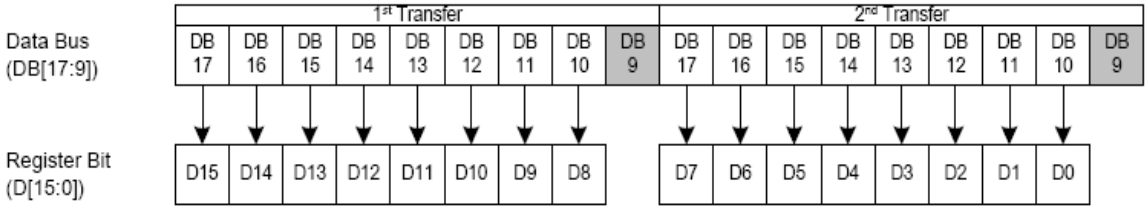
i80/M68 system 18-bit data bus interface



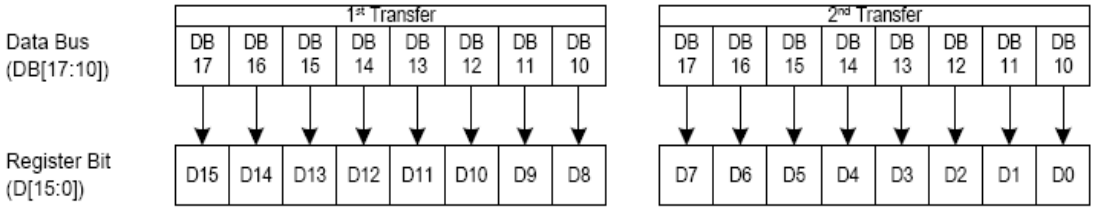
i80/M68 system 16-bit data bus interface



i80/M68 system 9-bit data bus interface



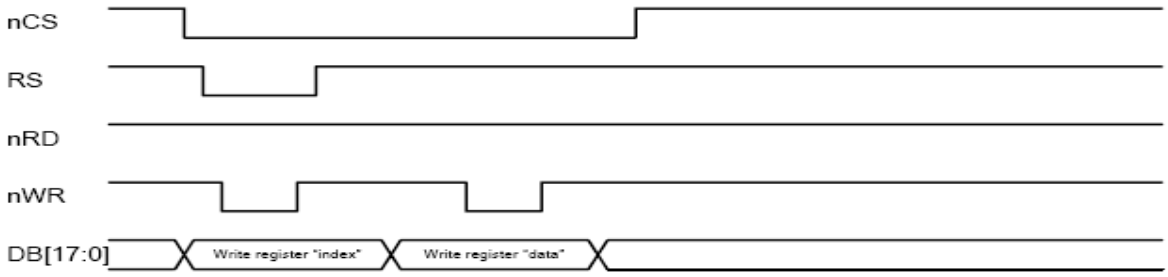
i80/M68 system 8-bit data bus interface/Serial peripheral interface (2/3 transmission)



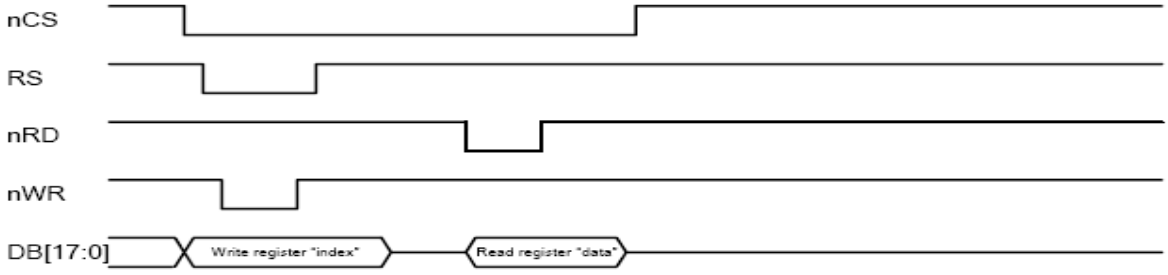
7.4 Register Read / Write Timing of i80 System Interface

i80 18-/16-bit System Bus Interface Timing

(a) Write to register

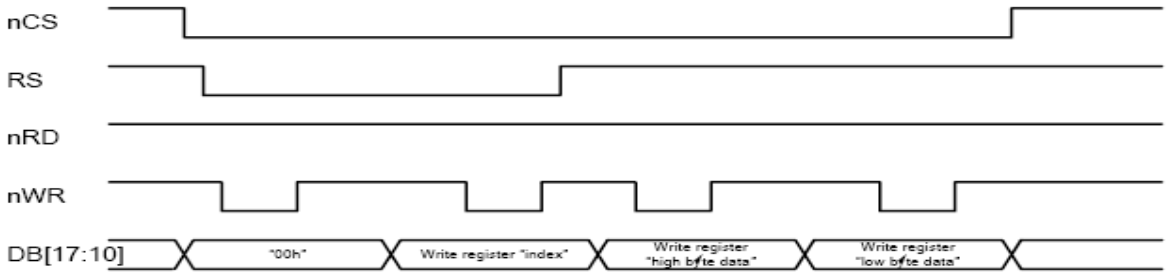


(b) Read from register



i80 9-/8-bit System Bus Interface Timing

(a) Write to register



(b) Read from register

7.5 Instruction List

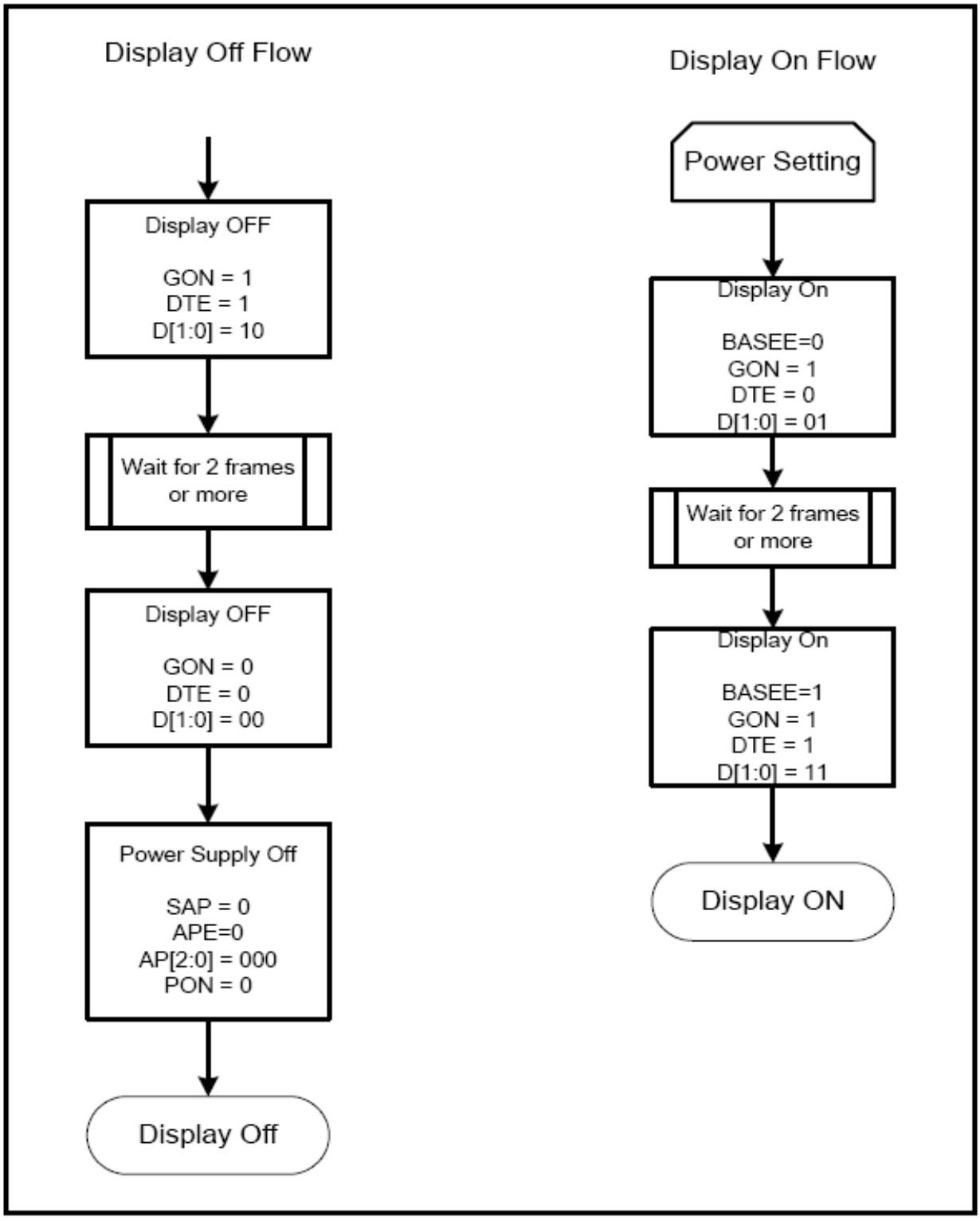
Main LCD Driver IC:ILI920

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
00h	Driver Code Read	R	1	1	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0
00h	Start Oscillation	W	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	OSC
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	HWM	0	ORG	0	I/D1	I/D0	AM	0	0	0
04h	Resize Control	W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	ENC2	ENC1	ENC0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	DPL	EPL
10h	Power Control 1	W	1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	DSTB	SLP	0
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	VCMR	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	EXT_R	0	FR_SEL1	FR_SEL0	0	0	0	0
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]

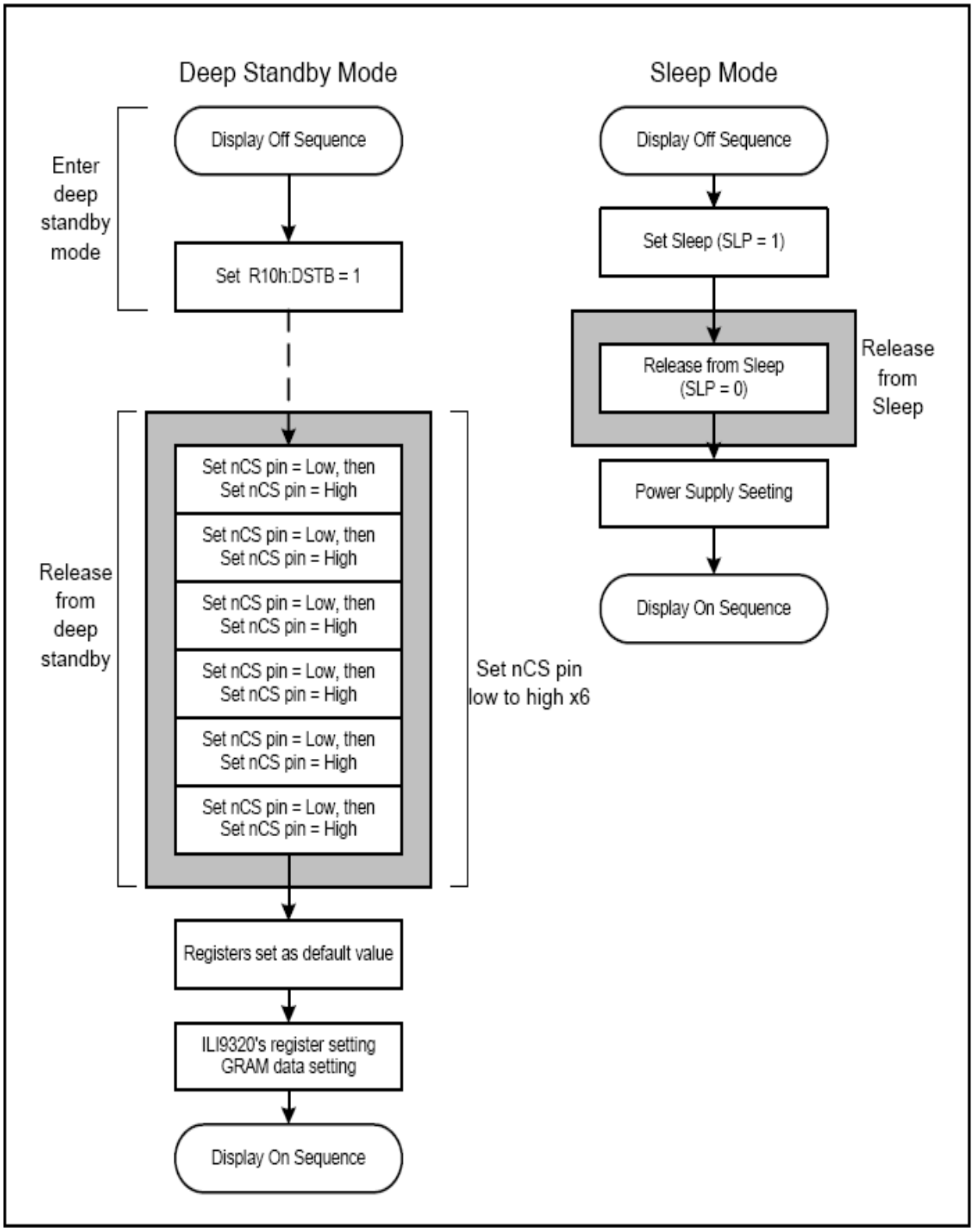
No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI00	0	0	0	0	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0
93h	Panel Interface Control 3	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPI2	MCPI1	MCPI0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
98h	Panel Interface Control 6	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2	MCPE1	MCPE0

8. Application

8.1 Display ON / OFF Sequence

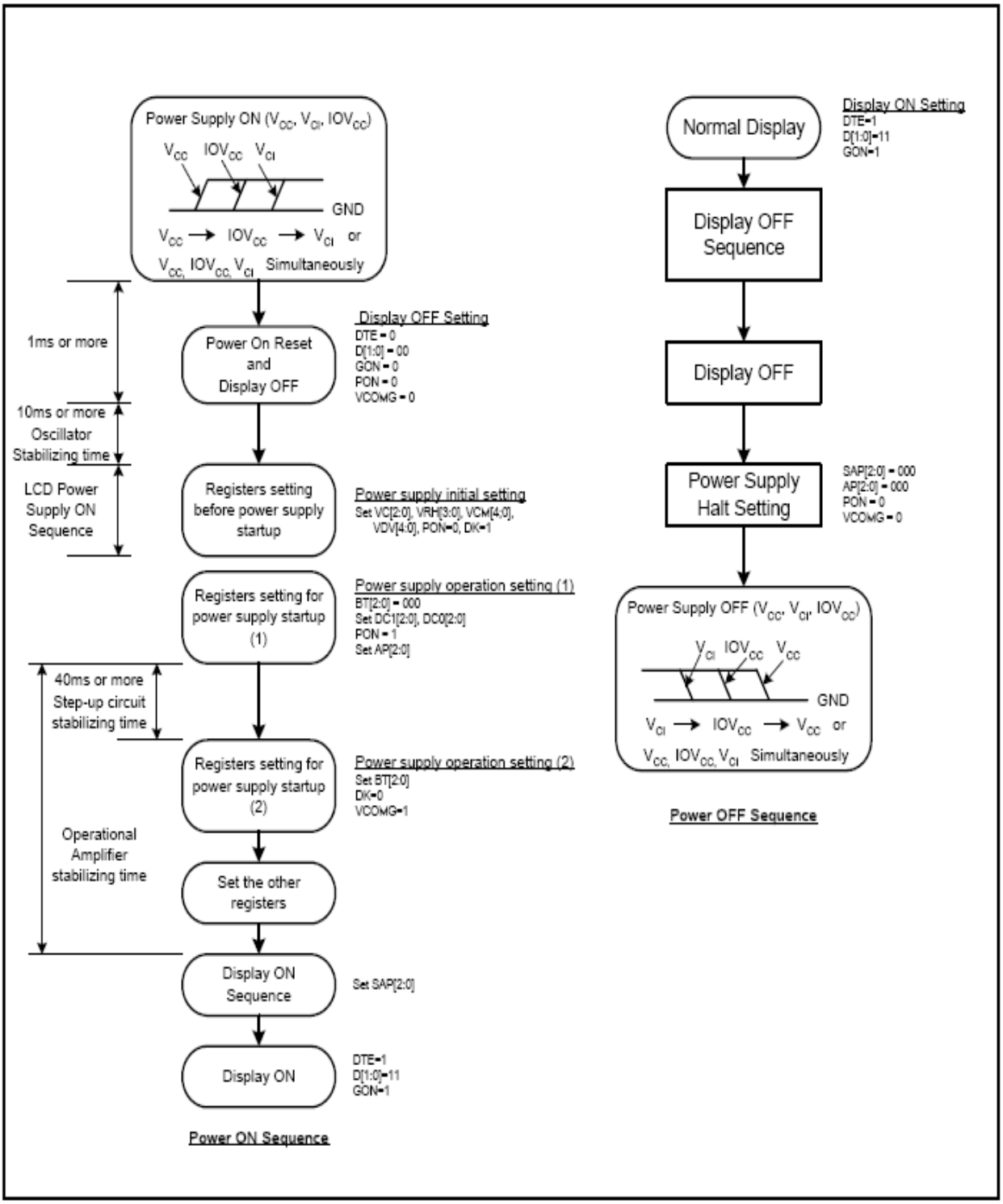


8.2 Deep Standby and Sleep Mode



8.3 Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.



9. Electrical Characteristics

9.1 Clock Characteristics

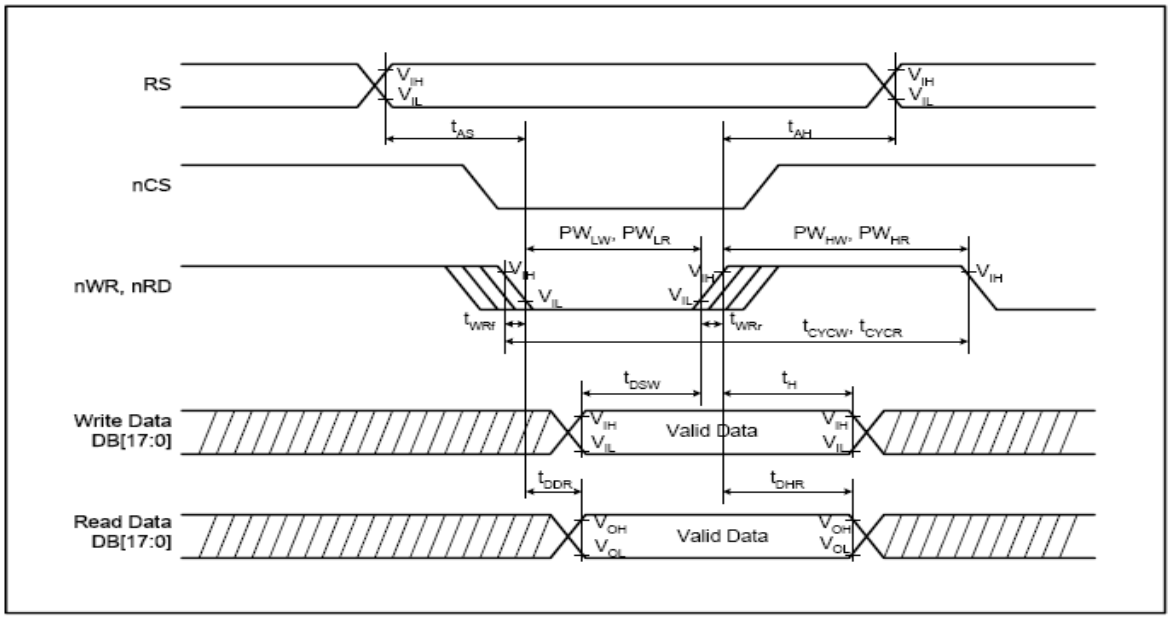
VCC = 2.40 ~ 3.30V, IOVCC = 1.65 ~ 3.30V

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
External Clock Frequency	fcp	VCC = 2.4 ~ 3.3V	450	550	650	KHz
External Clock Duty	f_{Duty}	VCC = 2.4 ~ 3.3V	45	50	55	
External Clock Rising Time	Trcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
External Clock Falling Time	Tfcp	VCC = 2.4 ~ 3.3V	-	-	0.2	µs
RC oscillation clock	f_{osc}	Rf = 100KΩ, VCC = 2.8V	450	550	650	KHz

9.2 AC Characteristics (i80 – system Interface Timing Characteristics)

Normal Write Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	100	-	-	-
	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	50	-	500	-
Write high-level pulse width		PW_{HW}	ns	50	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5	-	-	
Write data set up time		t_{DSW}	ns	10	-	-	
Write data hold time		t_H	ns	15	-	-	
Read data delay time		t_{DDR}	ns	-	-	100	
Read data hold time		t_{DHR}	ns	5	-	-	



10.QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

10.2 SAMPLING PLAN

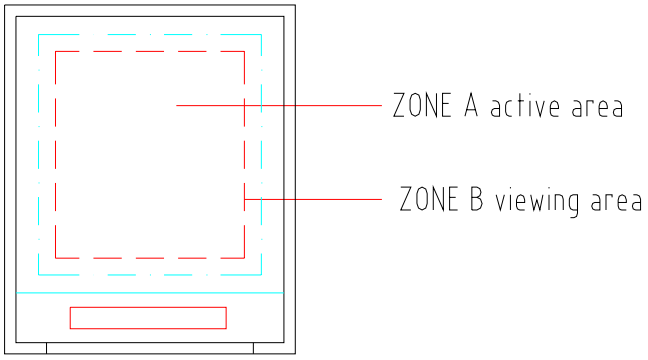
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

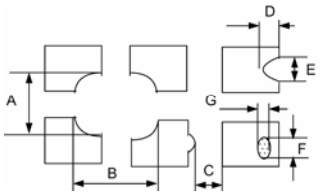
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under florescent light. The inspection area of LCD panel shall be within the range of following limits.



11.5 INSPECTION QUALITY CRITERIA

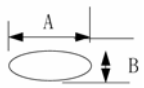
<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Class of Defec</th><th>Accept able level</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td><td>0.65</td></tr>
<tr><td>2</td><td>Scratch,Dent of Plastic Mold</td><td>Serious one is not allowed</td><td>Major</td><td>0.65</td></tr>
<tr><td>3</td><td>Scratch on FPC</td><td>By limited sample</td><td>Major</td><td>0.65</td></tr>
<tr><td>4</td><td>Dot Defect</td><td><table><tr><th>Item</th><th>Number</th></tr><tr><td>Bright dot defect</td><td>N ≦ 0</td></tr><tr><td>Black dot defect</td><td>N ≦ 2</td></tr><tr><td>Total</td><td>N ≦ 2</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
<tr><td>5</td><td>Line Defect</td><td>None</td><td>Minor</td><td>1.5</td></tr>
<tr><td>6</td><td>Uneven Brightness : Line Shape</td><td>None</td><td>Major</td><td>0.65</td></tr>
<tr><td>7</td><td>Uneven Brightness : Dot Shape</td><td>None</td><td>Major</td><td>0.65</td></tr>
<tr><td>8</td><td>Display pattern</td><td> 

Unit:mm
<table><tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr></table>
Note: 1. Acceptable up to 3 damages
2. NG if there’re to two or more pinholes per dot</td><td>Minor</td><td>1.5</td></tr>
<tr><td>9</td><td>Scratch of Polarizer :Dot Shape s

Size:
$D = \frac{A+B}{2}$</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.1
0.1 < D ≤ 0.3
0.3 < D</td><td>Ignore
3
0</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
</table>

<table>
<tr><td>10</td><td>Scratch of Polarizer :

Line Shape

  </td><td><table><tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr><tr><td>W≤0.05</td><td>L ≤ 0.3</td><td>Ignore</td></tr><tr><td>0.1<W≤0.05</td><td>0.3 < L ≤ 2.0</td><td>N≦3</td></tr><tr><td>0.1<W</td><td>-</td><td>See dot shape</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
<tr><td>11</td><td>Bubble in polarizer</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.3</td><td>Ignore</td></tr><tr><td>0.30 < D ≤ 0.50</td><td>1</td></tr><tr><td>0.50 < D</td><td>0</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
<tr><td>12</td><td>Stains inclusion : Line shape</td><td><table><tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr><tr><td>W≤0.04</td><td>Ignore</td><td>Not Allowed</td></tr><tr><td>0.04<W≤0.06</td><td>L ≤ 0.8</td><td>Not Allowed</td></tr><tr><td>0.06<W</td><td>-</td><td>Not Allowed</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
<tr><td>13</td><td>Stains inclusion : dot shape</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.1</td><td>Not Allowed</td></tr><tr><td>0.1 < D ≤ 0.2</td><td>Not Allowed</td></tr><tr><td>0.25< D</td><td>Not Allowed</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
</table>

11.6 RELIABILITY

Test Item	Test Conditions	Note

High Temperature Operation	60±3°C , t=72 hrs	
Low Temperature Operation	-10±3°C , t=72 hrs	
High Temperature Storage	70±3°C , t=72hrs	1,2
Low Temperature Storage	-20±3°C , t=72 hrs	1,2
Humidity Test	40°C , Humidity 90%, 72 hrs	1,2
Thermal Shock Test	-20°C ~ 25°C ~ 70°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge ±5kV, 10times contact discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

12 USE PRECAUTIONS

12.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

12.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

12.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

12.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light

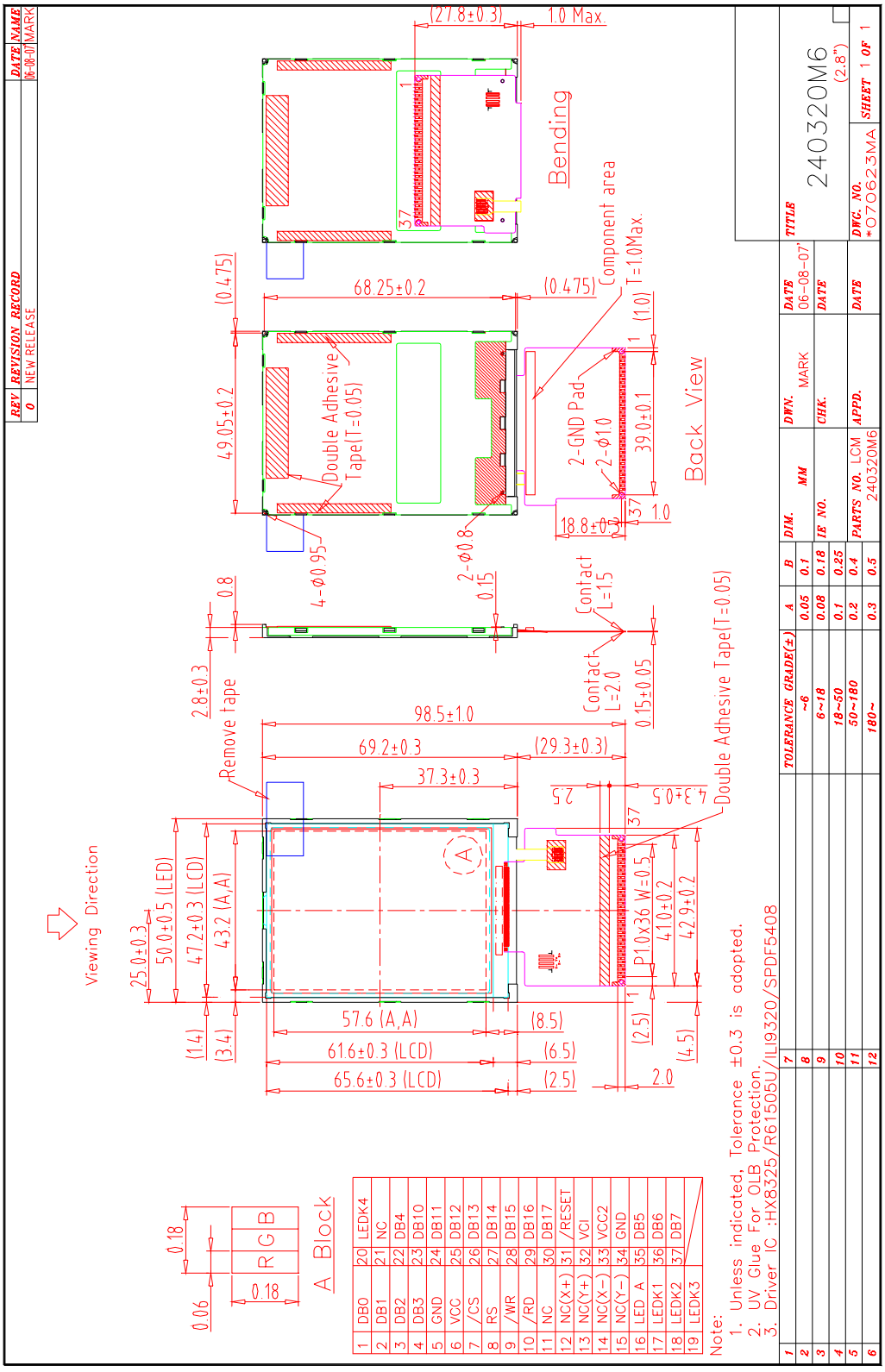
emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

12.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

13. MECHANIC DRAWING



1	DB0	20	LEDK4	1	DB0	20	LEDK4	1	DB0	20	LEDK4	1	DB0	20	LEDK4	1	DB0	20	LEDK4
2	DB1	21	NC	2	DB1	21	NC	2	DB1	21	NC	2	DB1	21	NC	2	DB1	21	NC
3	DB2	22	DB4	3	DB2	22	DB4	3	DB2	22	DB4	3	DB2	22	DB4	3	DB2	22	DB4
4	DB3	23	DB10	4	DB3	23	DB10	4	DB3	23	DB10	4	DB3	23	DB10	4	DB3	23	DB10
5	GND	24	DB11	5	GND	24	DB11	5	GND	24	DB11	5	GND	24	DB11	5	GND	24	DB11
6	VCC	25	DB12	6	VCC	25	DB12	6	VCC	25	DB12	6	VCC	25	DB12	6	VCC	25	DB12
7	/CS	26	DB13	7	/CS	26	DB13	7	/CS	26	DB13	7	/CS	26	DB13	7	/CS	26	DB13
8	RS	27	DB14	8	RS	27	DB14	8	RS	27	DB14	8	RS	27	DB14	8	RS	27	DB14
9	/WR	28	DB15	9	/WR	28	DB15	9	/WR	28	DB15	9	/WR	28	DB15	9	/WR	28	DB15
10	/RD	29	DB16	10	/RD	29	DB16	10	/RD	29	DB16	10	/RD	29	DB16	10	/RD	29	DB16
11	NC	30	DB17	11	NC	30	DB17	11	NC	30	DB17	11	NC	30	DB17	11	NC	30	DB17
12	NC(X+)	31	/RESET	12	NC(X+)	31	/RESET	12	NC(X+)	31	/RESET	12	NC(X+)	31	/RESET	12	NC(X+)	31	/RESET
13	NC(Y+)	32	VCI	13	NC(Y+)	32	VCI	13	NC(Y+)	32	VCI	13	NC(Y+)	32	VCI	13	NC(Y+)	32	VCI
14	NC(X−)	33	VCC2	14	NC(X−)	33	VCC2	14	NC(X−)	33	VCC2	14	NC(X−)	33	VCC2	14	NC(X−)	33	VCC2
15	NC(Y−)	34	GND	15	NC(Y−)	34	GND	15	NC(Y−)	34	GND	15	NC(Y−)	34	GND	15	NC(Y−)	34	GND
16	LED_A	35	DB5	16	LED_A	35	DB5	16	LED_A	35	DB5	16	LED_A	35	DB5	16	LED_A	35	DB5
17	LEDK1	36	DB6	17	LEDK1	36	DB6	17	LEDK1	36	DB6	17	LEDK1	36	DB6	17	LEDK1	36	DB6
18	LEDK2	37	DB7	18	LEDK2	37	DB7	18	LEDK2	37	DB7	18	LEDK2	37	DB7	18	LEDK2	37	DB7
19	LEDK3			19	LEDK3			19	LEDK3			19	LEDK3			19	LEDK3		