TECHNICAL SPECIFICATION

MODEL NO.: PD035OX1

☐ Customer's Confirmation

Customer

Date

By

☐ PVI's Confirmation

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<tr>
<th>Dep</th>
<th>FAE</th>
<th>Panel Design</th>
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<th>Mechanical Design</th>
<th>Product Verification</th>
<th>Prepared by</th>
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Sign


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# TECHNICAL SPECIFICATION

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</table>
1. Application

This technical specification applies to 3.5” color TFT-LCD panel PD035OX1. The TFT LCD panel applies to videophone, door phone and other electronic products which require high quality flat panel displays.

2. Features

. Amorphous silicon TFT-LCD panel with LED Backlight unit

. Support digital 8-bits serial / 24-bits parallel RGB and CCIR601/656 input mode.

. OSD overlay supported in CCIR601/656 input mode.


. Provide source and gate drivers control timing.

. Image Reversion : Up/Down and Left/Right

3. Mechanical Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specifications</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Screen Size</td>
<td>3.5 (diagonal)</td>
<td>inch</td>
</tr>
<tr>
<td>Display Format</td>
<td>320X(RGB) x 234</td>
<td>dot</td>
</tr>
<tr>
<td>Display colors</td>
<td>262,144</td>
<td></td>
</tr>
<tr>
<td>Active Area</td>
<td>71.6 (H) x 62.65 (V)</td>
<td>mm</td>
</tr>
<tr>
<td>Pixel Pitch</td>
<td>0.22375 (H) x 0.225 (V)</td>
<td>mm</td>
</tr>
<tr>
<td>Pixel Configuration</td>
<td>Delta</td>
<td></td>
</tr>
<tr>
<td>Outline Dimension</td>
<td>84.03 (W) x 55.24(H) x 8.43 (D)</td>
<td>mm</td>
</tr>
<tr>
<td>Surface Treatment</td>
<td>Anti – Glare</td>
<td></td>
</tr>
<tr>
<td>Back-light</td>
<td>LED</td>
<td></td>
</tr>
<tr>
<td>Weight</td>
<td>42 ±5</td>
<td>g</td>
</tr>
<tr>
<td>Display model</td>
<td>Normally</td>
<td></td>
</tr>
</tbody>
</table>
4. Mechanical Drawing of TFT-LCD Module
### 5. Input / Output Terminals

**CON1**

FPC Down Connect , 30Pins , Pitch : 0.5 mm

<table>
<thead>
<tr>
<th>Pin No</th>
<th>Symbol</th>
<th>I/O</th>
<th>Description</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D15(G5)</td>
<td>I</td>
<td>Green Data</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>D14(G4)</td>
<td>I</td>
<td>Green Data</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>D13(G3)</td>
<td>I</td>
<td>Green Data</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>D12(G2)</td>
<td>I</td>
<td>Green Data</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>D11(G1)</td>
<td>I</td>
<td>Green Data</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>D10(G0)</td>
<td>I</td>
<td>Green Data(LSB)</td>
<td>Note 5-1</td>
</tr>
<tr>
<td>7</td>
<td>VDD2</td>
<td>I</td>
<td>Analog power supply for source driver</td>
<td>Note 5-2</td>
</tr>
<tr>
<td>8</td>
<td>V8</td>
<td>I</td>
<td>Gamma correction voltage 8</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>V7</td>
<td>I</td>
<td>Gamma correction voltage 7</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>V6</td>
<td>I</td>
<td>Gamma correction voltage 6</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>V5</td>
<td>I</td>
<td>Gamma correction voltage 5</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>V4</td>
<td>I</td>
<td>Gamma correction voltage 4</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>V3</td>
<td>I</td>
<td>Gamma correction voltage 3</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>V2</td>
<td>I</td>
<td>Gamma correction voltage 2</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>V1</td>
<td>I</td>
<td>Gamma correction voltage 1</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>VSS2</td>
<td>I</td>
<td>Analog ground for source driver</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>D07(R7)</td>
<td>I</td>
<td>Red Data(MSB)</td>
<td>Note 5-1</td>
</tr>
<tr>
<td>18</td>
<td>D06(R6)</td>
<td>I</td>
<td>Red Data</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>D05(R5)</td>
<td>I</td>
<td>Red Data</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>D04(R4)</td>
<td>I</td>
<td>Red Data</td>
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</tr>
<tr>
<td>21</td>
<td>D03(R3)</td>
<td>I</td>
<td>Red Data</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>D02(R2)</td>
<td>I</td>
<td>Red Data</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>D01(R1)</td>
<td>I</td>
<td>Red Data</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>D00(R0)</td>
<td>I</td>
<td>Red Data(LSB)</td>
<td>Note 5-1</td>
</tr>
<tr>
<td>25</td>
<td>CLK</td>
<td>I</td>
<td>Clock signal. Latching data at the rising edge</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>HS</td>
<td>I</td>
<td>Horizontal sync input in RGB mode and CCIR601</td>
<td>Note 5-4</td>
</tr>
<tr>
<td>27</td>
<td>VS</td>
<td>I</td>
<td>Vertical sync input in RGB mode and CCIR601</td>
<td>Note 5-5</td>
</tr>
<tr>
<td>28</td>
<td>DEN</td>
<td>I</td>
<td>Input data enable control.(Normally pull low)</td>
<td>Note 5-6</td>
</tr>
<tr>
<td>29</td>
<td>VCC</td>
<td>I</td>
<td>Digital power supply for source driver IC</td>
<td>Note 5-7</td>
</tr>
<tr>
<td>30</td>
<td>VCOM</td>
<td>I</td>
<td>Voltage for common electrode</td>
<td>Note 5-8</td>
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</tbody>
</table>
## CON2

FPC Down Connect, 30Pins, Pitch: 0.5 mm

<table>
<thead>
<tr>
<th>Pin No</th>
<th>Symbol</th>
<th>I/O</th>
<th>Description</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VLED</td>
<td>I</td>
<td>Power supply for LED</td>
<td>Note 5-9</td>
</tr>
<tr>
<td>2</td>
<td>GLED1</td>
<td>I</td>
<td>Ground for LED</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>GLED2</td>
<td>I</td>
<td>Ground for LED</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>-</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>VGH</td>
<td>I</td>
<td>Positive power for gate driver</td>
<td>Note 5-10</td>
</tr>
<tr>
<td>6</td>
<td>VDD1</td>
<td>I</td>
<td>Power supply for gate logic circuit</td>
<td>Note 5-11</td>
</tr>
<tr>
<td>7</td>
<td>VSS1</td>
<td>I</td>
<td>Ground for gate driver</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>VEE</td>
<td>I</td>
<td>Negative power for gate driver</td>
<td>Note 5-12</td>
</tr>
<tr>
<td>9</td>
<td>VDD1</td>
<td>I</td>
<td>Power supply for gate logic circuit</td>
<td>Note 5-11</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>I</td>
<td>Digital ground for source driver IC</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>RESETB</td>
<td>I</td>
<td>Hardware global reset, (low active)</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>VSET</td>
<td>I</td>
<td>Externally/Internally gamma voltage setup</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>U/D</td>
<td>I</td>
<td>Up/Down control for gate driver</td>
<td>Note 5-13</td>
</tr>
<tr>
<td>14</td>
<td>L/R</td>
<td>I</td>
<td>Left/Right control for source driver</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>IF2</td>
<td>I</td>
<td>Select the input data format</td>
<td>Note 5-14</td>
</tr>
<tr>
<td>16</td>
<td>IF1</td>
<td>I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>SPENA</td>
<td>I</td>
<td>Serial port data enable signal (normally pull high)</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>SPCK</td>
<td>I</td>
<td>Serial port clock. (Normally pull high)</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>SPDA</td>
<td>I/O</td>
<td>Serial port data input/output</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>POL</td>
<td>O</td>
<td>Polarity select for the line inversion control signal</td>
<td>Note 5-15</td>
</tr>
<tr>
<td>21</td>
<td>D27(B7)</td>
<td>I</td>
<td>Blue Data(MSB)</td>
<td>Note 5-1</td>
</tr>
<tr>
<td>22</td>
<td>D26(B6)</td>
<td>I</td>
<td>Blue Data</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>D25(B5)</td>
<td>I</td>
<td>Blue Data</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>D24(B4)</td>
<td>I</td>
<td>Blue Data</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>D23(B3)</td>
<td>I</td>
<td>Blue Data</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>D22(B2)</td>
<td>I</td>
<td>Blue Data</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>D21(B1)</td>
<td>I</td>
<td>Blue Data</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>D20(B0)</td>
<td>I</td>
<td>Blue Data(LSB)</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>D17(G7)</td>
<td>I</td>
<td>Green Data(MSB)</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>D16(G6)</td>
<td>I</td>
<td>Green Data</td>
<td></td>
</tr>
</tbody>
</table>
Note 5-1 : Digital data input. DX0 is LSB and DX7 is MSB.

If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G and B data in turn.
If serial RGB or CCIR601/656 input mode is selected, only D07~D00 are used, and others short to Vss.

Note 5-2 : $V_{DD2}$ Typ. = $+5V$

Note 5-3 : The output voltage is determined by the digital input data. If digital RGB or CCIR601/656 input mode is selected, The 8 gamma correction reference voltages can be set to externally or generate internally.
If VSET = "H", the gamma correction voltage generated externally
If VSET = "L", the default value is as below : (When $V_{DD} = +5V$)

<table>
<thead>
<tr>
<th>Default Voltage(V)</th>
<th>V1</th>
<th>V2</th>
<th>V3</th>
<th>V4</th>
<th>V5</th>
<th>V6</th>
<th>V7</th>
<th>V8</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4.29</td>
<td>3.73</td>
<td>3.33</td>
<td>2.94</td>
<td>2.62</td>
<td>2.22</td>
<td>1.51</td>
<td>0.48</td>
</tr>
</tbody>
</table>

Note 5-4 : Horizontal sync input in digital RGB mode. Or HREF input in CCIR601 mode.
( Short to Vss if not used )

Note 5-5 : Vertical sync input in digital RGB mode. Or V123 input in CCIR601 mode.
( Short to Vss if not used )

Note 5-6 : Digital RGB data input format
For digital RGB input data format, both SYNC. Mode and DEN mode are supported. If DEN signal is fixed low, SYNC. Mode is used. Otherwise , DEN mode is used.

Note 5-7 : $V_{CC}$ Typ. = $+3.3V$

Note 5-8 : $V_{COM}$ Typ. = $+6.0Vpp$

Note 5-9 : ILED Typ. = 20mA., VLED Typ. = 9V

Note 5-10 : $V_{GH}$ Typ. = $+15V$.

Note 5-11 : $V_{DD1}$ Typ. = $+3.3V$.

Note 5-12 : $V_{EE}$ Typ. = $-15V$. 

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Note 5-13: The definition of L/R, U/D:
U/D(PIN 13)=Low L/R(PIN 14)=High

U/D(PIN 13)=High L/R(PIN 14)=Low

Note 5-14: IF1, IF2 control the input data format.

<table>
<thead>
<tr>
<th>IF2,IF1</th>
<th>Input data format</th>
</tr>
</thead>
<tbody>
<tr>
<td>L,L (default)</td>
<td>Serial RGB</td>
</tr>
<tr>
<td>L,H</td>
<td>Parallel RGB</td>
</tr>
<tr>
<td>H,L</td>
<td>CCIR601</td>
</tr>
<tr>
<td>H,H</td>
<td>CCIR656</td>
</tr>
</tbody>
</table>

Note 5-15: When POL=L, output voltage is negative polarity.
When POL=H, output voltage is positive polarity.

6. Absolute Maximum Ratings

\[ V_{SS1}=V_{SS2}=0 \text{ V}, \quad Ta = 25 \degree C \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN.</th>
<th>MAX.</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage for source driver</td>
<td>( V_{CC} )</td>
<td>-0.3</td>
<td>+7.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{DD2} )</td>
<td>-0.3</td>
<td>+7.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Supply voltage for gate driver</td>
<td>( V_{DD1} )</td>
<td>-0.3</td>
<td>+7.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>H Level</td>
<td>( V_{GH} )</td>
<td>-0.3</td>
<td>+32.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>L Level</td>
<td>( V_{EE} )</td>
<td>-22.0</td>
<td>+0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{GH-\text{EE}} )</td>
<td>-0.3</td>
<td>+45.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input signal voltage</td>
<td>( V_{IN} )</td>
<td>-0.3</td>
<td>( V_{DD}+0.3 )</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
7. Electrical Characteristics

7-1 Operating condition

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN.</th>
<th>Typ.</th>
<th>MAX.</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage for source driver</td>
<td>Logic</td>
<td>VCC</td>
<td>+3.0</td>
<td>+3.3</td>
<td>+3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Analog</td>
<td>VDD2</td>
<td>+3.8</td>
<td>+5.0</td>
<td>+5.5</td>
<td>V</td>
</tr>
<tr>
<td>Supply voltage for gate driver</td>
<td>Logic</td>
<td>VDD1</td>
<td>+3.0</td>
<td>+3.3</td>
<td>+3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>H level</td>
<td>VGH</td>
<td>+10</td>
<td>+15</td>
<td>+30</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>L level</td>
<td>VEE</td>
<td>-17</td>
<td>-15</td>
<td>-5</td>
<td>V</td>
</tr>
<tr>
<td>Signal input voltage</td>
<td>H level</td>
<td>VIH</td>
<td>0.7VCC</td>
<td>-</td>
<td>VCC</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>L level</td>
<td>VIL</td>
<td>0</td>
<td>-</td>
<td>0.3VCC</td>
<td>V</td>
</tr>
<tr>
<td>Signal output voltage</td>
<td>H level</td>
<td>VOH</td>
<td>0.8VCC</td>
<td>-</td>
<td>VCC</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>L level</td>
<td>VOL</td>
<td>0</td>
<td>-</td>
<td>0.2VCC</td>
<td>V</td>
</tr>
</tbody>
</table>

V_{COM}

- \( V_{COMAC} \) = -6.0 \( V \)
- \( V_{COMDC} \) = 1.0 \( V \)

Note 7-1: PVI strongly suggests that the \( V_{COMDC} \) level shall be adjustable, and the adjustable level range is 1V \( \pm \) 1V, every module’s \( V_{COMDC} \) level shall be carefully adjusted to show a best image performance.

7-2 Recommended driving condition for LED backlight

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage of LED backlight</td>
<td>VLED</td>
<td>9.0</td>
<td>10.0</td>
<td>11.0</td>
<td>V</td>
<td>( i_L = 20 \text{mA} )</td>
</tr>
<tr>
<td>Supply current of LED backlight</td>
<td>ILED</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>mA</td>
<td>Note 7-2</td>
</tr>
<tr>
<td>Backlight Power Consumption</td>
<td>PLED</td>
<td>360</td>
<td>400</td>
<td>440</td>
<td>mW</td>
<td>Note 7-3</td>
</tr>
</tbody>
</table>

Note 7-2: LED B/L applied information, please refer to the appendix at the end.
Note 7-3: \( P_{LED} = 2 \times I_{LED} \times V_{LED} \).

\[ V_{LED} \]

\[ I_{LED} \]

\( G_{LED1} \)

\( G_{LED2} \)
7-3 Power consumption

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current for gate driver (Hi level)</td>
<td>IGH</td>
<td>VGH = +15V</td>
<td>0.2</td>
<td>0.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Supply current for gate driver (Logic)</td>
<td>IDD1</td>
<td>VDD1 = +3.3V</td>
<td>0.05</td>
<td>0.1</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Supply current for gate driver (Low level)</td>
<td>IEE</td>
<td>VEE = -15V</td>
<td>0.2</td>
<td>0.5</td>
<td>mA</td>
<td>VEE center voltage</td>
</tr>
<tr>
<td>Supply current for source driver (Analog)</td>
<td>VDD2</td>
<td>VDD2 = +5V</td>
<td>5.0</td>
<td>8.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Supply current for source driver (Logic)</td>
<td>VCC</td>
<td>VCC = +3.3V</td>
<td>4.5</td>
<td>7.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>LCD panel power consumption</td>
<td>-</td>
<td></td>
<td>48</td>
<td>80</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td>Backlight power consumption</td>
<td>PLED</td>
<td></td>
<td>400</td>
<td>440</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td>Total power consumption</td>
<td>-</td>
<td></td>
<td>0.45</td>
<td>0.52</td>
<td>W</td>
<td></td>
</tr>
</tbody>
</table>

* Above data measured on serial mode:
  
  If on parallel mode, ICC Typ. = 3.0mA, Max. = 5.0mA;
  
  panel power consumption Typ. = 41.5mW Max. = 72.8mW.
  
  If on CCIR601/656 mode, ICC Typ. = 6.0mA, Max. = 10.0mA;
  
  panel power consumption Typ. = 51.4mW Max. = 89.3mW.

7-4 Timing characteristics of input signals

7.4.1 Serial 8 bits RGB interface

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK period</td>
<td>TOSC</td>
<td>-</td>
<td>52</td>
<td>-</td>
<td>ns</td>
<td>Note 7-4</td>
</tr>
<tr>
<td>Data setup time</td>
<td>TSU</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Data hold time</td>
<td>THD</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>HS period</td>
<td>TH</td>
<td>-</td>
<td>1224</td>
<td>-</td>
<td>TOSC</td>
<td></td>
</tr>
<tr>
<td>HS pulse width</td>
<td>THS</td>
<td>5</td>
<td>90</td>
<td>-</td>
<td>TOSC</td>
<td></td>
</tr>
<tr>
<td>HS rising time</td>
<td>TCR</td>
<td>-</td>
<td>-</td>
<td>700</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>HS falling time</td>
<td>TCF</td>
<td>-</td>
<td>-</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>VS pulse width</td>
<td>TVS</td>
<td>1</td>
<td>3</td>
<td>5</td>
<td>T_H</td>
<td></td>
</tr>
<tr>
<td>VS rising time</td>
<td>TVR</td>
<td>-</td>
<td>-</td>
<td>700</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>VS falling time</td>
<td>TVF</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
<td>us</td>
<td></td>
</tr>
<tr>
<td>HS falling to VS falling time for odd field</td>
<td>THVO</td>
<td>0</td>
<td>3</td>
<td>-</td>
<td>TOSC</td>
<td></td>
</tr>
<tr>
<td>VS falling to HS falling time for even field</td>
<td>THVE</td>
<td>0</td>
<td>3</td>
<td>-</td>
<td>TOSC</td>
<td></td>
</tr>
<tr>
<td>VS-DEN time</td>
<td>TVSE</td>
<td>-</td>
<td>21</td>
<td>-</td>
<td>TH</td>
<td></td>
</tr>
<tr>
<td>HS-DEN time</td>
<td>THE</td>
<td>108</td>
<td>204</td>
<td>264</td>
<td>TOSC</td>
<td></td>
</tr>
<tr>
<td>DEN pulse width</td>
<td>TEP</td>
<td>-</td>
<td>960</td>
<td>-</td>
<td>TOSC</td>
<td></td>
</tr>
<tr>
<td>VS period</td>
<td>-</td>
<td>262</td>
<td>-</td>
<td>TH</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 7-4: When SYNC mode is used, 1st data start from 204th CLK after HS fallings.
7.4.2 Parallel 24 bits RGB interface

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK period</td>
<td>T_{OSC}</td>
<td>-</td>
<td>156</td>
<td>-</td>
<td>ns</td>
<td>Note 7-5</td>
</tr>
<tr>
<td>Data setup time</td>
<td>T_{SU}</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Data hold time</td>
<td>T_{HD}</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>HS period</td>
<td>T_{H}</td>
<td>-</td>
<td>408</td>
<td>-</td>
<td>T_{OSC}</td>
<td></td>
</tr>
<tr>
<td>HS pulse width</td>
<td>T_{HS}</td>
<td>5</td>
<td>30</td>
<td>-</td>
<td>T_{OSC}</td>
<td></td>
</tr>
<tr>
<td>HS rising time</td>
<td>T_{Cr}</td>
<td>-</td>
<td>-</td>
<td>700</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>HS falling time</td>
<td>T_{Cf}</td>
<td>-</td>
<td>-</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>VS pulse width</td>
<td>T_{VS}</td>
<td>1</td>
<td>3</td>
<td>5</td>
<td>T_{H}</td>
<td></td>
</tr>
<tr>
<td>VS rising time</td>
<td>T_{Vr}</td>
<td>-</td>
<td>-</td>
<td>700</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>VS falling time</td>
<td>T_{Vf}</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
<td>us</td>
<td></td>
</tr>
<tr>
<td>HS falling to VS falling time for odd field</td>
<td>T_{HVO}</td>
<td>0</td>
<td>3</td>
<td>-</td>
<td>T_{OSC}</td>
<td></td>
</tr>
<tr>
<td>VS falling to HS falling time for even field</td>
<td>T_{HVE}</td>
<td>0</td>
<td>3</td>
<td>-</td>
<td>T_{OSC}</td>
<td></td>
</tr>
<tr>
<td>VS-DEN time</td>
<td>T_{VSE}</td>
<td>-</td>
<td>21</td>
<td>-</td>
<td>T_{H}</td>
<td></td>
</tr>
<tr>
<td>HS-DEN time</td>
<td>T_{HE}</td>
<td>36</td>
<td>68</td>
<td>88</td>
<td>T_{OSC}</td>
<td></td>
</tr>
<tr>
<td>DEN pulse width</td>
<td>T_{EP}</td>
<td>-</td>
<td>320</td>
<td>-</td>
<td>T_{OSC}</td>
<td></td>
</tr>
<tr>
<td>VS period</td>
<td>-</td>
<td>262</td>
<td>-</td>
<td>T_{H}</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 7-5: When SYNC mode is used, 1st data start from 68th CLK after HS fallings.

7.4.3 CCIR601/656 Interface

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK period</td>
<td>T_{OSC}</td>
<td>-</td>
<td>37</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Data setup time</td>
<td>T_{SU}</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Data hold time</td>
<td>T_{HD}</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

7.4.4 Hardware reset timing

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESETB low pulse width</td>
<td>T_{RSB}</td>
<td>200</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
7.5 Timing controller timing chart
7.5.1 Clock and Data waveform

- **CCIR 601 (HS_POL="L" in Register R2)**
  - CLK
    - D00-D07
      - Blanking data
      - Cb0 Y0 Cr0 Y1 Cr2
    - HS

- **CCIR 601**
  - CLK
    - D07-D00
      - Cb Y Cr Y Cb Y Cr

- **Digital Serial RGB**
  - CLK
    - D07-D00
      - Blanking data
      - R G B R G

- **Digital Parallel RGB**
  - CLK
    - D07-D00
      - Blanking data
      - R G B R G B R G B R G B
7.5.2 HS, VS, DEN timing waveform

**HS and VS timing relationship**

Odd field

**HS**

**VS**

Even field

**HS**

**VS**

**HS and DEN timing relationship**

**HS**

**DEN**

**HS, VS and DEN timing relationship**

**HS**

**VS**

**DEN**
7.5.3 CCIR601 timing waveform (VS_POL="H", HS_POL="L" in Register R2)

**ITU-R BT.601 NTSC Input Timing**

Data Blanking

Data

<table>
<thead>
<tr>
<th>HREF</th>
<th>V123</th>
</tr>
</thead>
<tbody>
<tr>
<td>524</td>
<td>523</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>22</td>
<td>23</td>
</tr>
</tbody>
</table>

**ITU-R BT.601 PAL Input Timing**

Data Blanking

Data

<table>
<thead>
<tr>
<th>HREF</th>
<th>V123</th>
</tr>
</thead>
<tbody>
<tr>
<td>622</td>
<td>623</td>
</tr>
<tr>
<td>624</td>
<td>625</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>22</td>
<td>23</td>
</tr>
</tbody>
</table>

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8. Pixel Arrangement

![Pixel Arrangement Diagram]

- 1st Line: RGBRGBRGB
- 2nd Line: BRGBRGBRGB
- 3rd Line: RGBRGBRGBRGB
- 320th Pixel: RGB

1 Pixel = RGB
## 9. Display Color and Gray Scale Reference

<table>
<thead>
<tr>
<th>Color</th>
<th>Input Color Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Red</td>
</tr>
<tr>
<td></td>
<td>R7 R6 R5 R4 R3 R2 R1 R0</td>
</tr>
<tr>
<td>Basic Colors</td>
<td></td>
</tr>
<tr>
<td>Black</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Red (255)</td>
<td>1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>Green</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Blue (255)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Cyan</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Magenta</td>
<td>1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>Yellow</td>
<td>1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>White</td>
<td>1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>Red (00)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Red (01)</td>
<td>0 0 0 0 0 0 1 0</td>
</tr>
<tr>
<td>Red (02)</td>
<td>0 0 0 0 0 0 1 0</td>
</tr>
<tr>
<td>Darker</td>
<td>↓ ↓ ↓ ↓ ↓ ↓ ↓</td>
</tr>
<tr>
<td>Brighter</td>
<td></td>
</tr>
<tr>
<td>Red (253)</td>
<td>1 1 1 1 1 1 0 1</td>
</tr>
<tr>
<td>Red (254)</td>
<td>1 1 1 1 1 1 1 0</td>
</tr>
<tr>
<td>Red (255)</td>
<td>1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>Green (00)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Green (01)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Green (02)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Darker</td>
<td>↓ ↓ ↓ ↓ ↓ ↓ ↓</td>
</tr>
<tr>
<td>Brighter</td>
<td></td>
</tr>
<tr>
<td>Green</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Green</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Green</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Blue (00)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Blue (01)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Blue (02)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Darker</td>
<td>↓ ↓ ↓ ↓ ↓ ↓ ↓</td>
</tr>
<tr>
<td>Brighter</td>
<td></td>
</tr>
<tr>
<td>Blue (253)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Blue (254)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Blue (255)</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
</tbody>
</table>

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10. Block Diagram

- LCD Panel
- H Driver (Source)
  V Driver (Gate)
- Back-light
- 60 PIN Input
11. SPI Register Description and Timing Characteristics

11.1 Function Control Register

Register R0 : Address(A3~A0) → 0000

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>reserve</td>
<td>STHD1</td>
<td>STHD0</td>
<td>STHP4</td>
<td>STHP3</td>
<td>STHP2</td>
<td>STHP1</td>
<td>STHP0</td>
</tr>
<tr>
<td>Default</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

STHD [1:0] : adjust start pulse position by dot

<table>
<thead>
<tr>
<th>STHD1</th>
<th>STHD0</th>
<th>STH position adjust by dot</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>-1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>-2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>+1</td>
</tr>
</tbody>
</table>

STHP [4:0] : adjust start pulse position by pixel

<table>
<thead>
<tr>
<th>STHP4</th>
<th>STHP3</th>
<th>STHP2</th>
<th>STHP1</th>
<th>STHP0</th>
<th>STH position adjust by pixel</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
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<td>-3</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>-5</td>
</tr>
<tr>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>-6</td>
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</tr>
</tbody>
</table>
Register R1: Address (A3~A0) → 0001

<table>
<thead>
<tr>
<th>Bit</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>STVP3</td>
<td>STVP2</td>
<td>STVP1</td>
<td>STVP0</td>
<td>STVNT1</td>
<td>STVNT0</td>
<td>STVPAL1</td>
<td>STVPAL0</td>
</tr>
<tr>
<td>Default</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

STVP [3:0]: adjust first line position by line

<table>
<thead>
<tr>
<th>STVP3</th>
<th>STVP2</th>
<th>STVP1</th>
<th>STVP0</th>
<th>STV position adjust by line</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-1</td>
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<tr>
<td>1</td>
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<td>0</td>
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<td>0</td>
<td>2</td>
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<tr>
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<td>3</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>7</td>
</tr>
</tbody>
</table>

STVNT[1:0]: When NTSC mode, the relationship of first line in Even field and Odd field.
  00: First line in Even field = First line in Odd field.
  01: First line in Even field = First line in Odd field +1.
  10: No use.
  11: First line in Even field = First line in Odd field –1.

STVPAL[1:0]: When PAL mode, the relationship of first line in Even field and Odd field.
  (Only for CCIR601/656 mode)
  00: First line in Even field = First line in Odd field.
  01: First line in Even field = First line in Odd field +1.
  10: No use.
  11: First line in Even field = First line in Odd field –1.
Register R2 :Address(A3~A0)→0010

<table>
<thead>
<tr>
<th>Bit</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>reserved</td>
<td>reserved</td>
<td>reserved</td>
<td>reserved</td>
<td>HS_POL</td>
<td>VS_POL</td>
<td>NPC_IN</td>
<td>NPC_SET</td>
</tr>
<tr>
<td>Default</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**HS_POL**: HS polarity setting.
- **HS_POL** = “L”, negative polarity.
- **HS_POL** = “H”, positive polarity.

**VS_POL**: VS polarity setting.
- **VS_POL** = “L”, negative polarity.
- **VS_POL** = “H”, positive polarity.

**NPC_IN**: Define the NTSC/PAL mode by SPI.
- **NPC_IN** = “L”, PAL. (Only for CCIR601/656 mode)
- **NPC_IN** = “H”, NTSC.

**NPC_SET**: Set the NTSC/PAL auto detection or define by NPC_IN.
- **NPC_SET** = “L”, auto detection.
- **NPC_SET** = “H”, define by SPI.

Register R3 :Address(A3~A0)→0011

<table>
<thead>
<tr>
<th>Bit</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>reserved</td>
<td>reserved</td>
<td>reserved</td>
<td>reserved</td>
<td>PWD_EN</td>
<td>OSDCLK</td>
<td>OSDHSP</td>
<td>OSDVSD</td>
</tr>
<tr>
<td>Default</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**PWD_EN**: Set DAC power saving function.
- **PWD_EN** = “L”, disable. The DAC is always power on.
- **PWD_EN** = “H”, enable.
11-2 SPI timing characteristic

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPCK period</td>
<td>$T_{\text{CK}}$</td>
<td>60</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SPCK high width</td>
<td>$T_{\text{CKH}}$</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SPCK low width</td>
<td>$T_{\text{CKL}}$</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Data setup time</td>
<td>$T_{\text{SU1}}$</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Data hold time</td>
<td>$T_{\text{HD1}}$</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SPENA to SPCK setup time</td>
<td>$T_{\text{CS}}$</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SPENA to SPDA hold time</td>
<td>$T_{\text{CE}}$</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SPENA high pulse width</td>
<td>$T_{\text{CD}}$</td>
<td>50</td>
<td>-</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SPDA output latency</td>
<td>$T_{\text{CR}}$</td>
<td>-</td>
<td>1/2</td>
<td>-</td>
<td>$T_{\text{CK}}$</td>
<td></td>
</tr>
</tbody>
</table>

**SP** "read" timing

**SP** "write" timing

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12. Power On Sequence

The Power on sequence only effect by \( V_{CC}, V_{SS}, V_{DD}, V_{EE} \) and \( V_{GH} \), the others do not care.

1) \( 10 \text{ms} \leq T1 < T2 \)
2) \( 0 \text{ms} < T3 \leq T4 \leq 10 \text{ms} \)

13. Optical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Viewing Angle</td>
<td>( \theta 21, \theta 22 )</td>
<td>Horizontal</td>
<td>45</td>
<td>50</td>
<td>---</td>
<td>deg</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( \theta 11 )</td>
<td></td>
<td>30</td>
<td>35</td>
<td>---</td>
<td>deg</td>
<td>Note 13-1</td>
</tr>
<tr>
<td></td>
<td>( \theta 12 )</td>
<td></td>
<td>10</td>
<td>15</td>
<td>---</td>
<td>deg</td>
<td></td>
</tr>
<tr>
<td>Contrast Ratio</td>
<td>CR</td>
<td>At optimized View angle</td>
<td>200</td>
<td>400</td>
<td>---</td>
<td>---</td>
<td>Note 13-2</td>
</tr>
<tr>
<td>Response Time</td>
<td>Rise</td>
<td>( \theta = 0^\circ )</td>
<td>---</td>
<td>15</td>
<td>30</td>
<td>ms</td>
<td>Note 13-3</td>
</tr>
<tr>
<td></td>
<td>Fall</td>
<td></td>
<td>---</td>
<td>25</td>
<td>50</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Uniformity</td>
<td>U</td>
<td>9 point</td>
<td>70</td>
<td>75</td>
<td>-</td>
<td>%</td>
<td>Note 13-4</td>
</tr>
<tr>
<td>Brightness</td>
<td>-</td>
<td>Center point</td>
<td>200</td>
<td>250</td>
<td>-</td>
<td>cd/m²</td>
<td>Note 13-5</td>
</tr>
<tr>
<td>White</td>
<td>x</td>
<td>( \theta = 0^\circ )</td>
<td>-</td>
<td>0.31</td>
<td>-</td>
<td>-</td>
<td>Note 13-5</td>
</tr>
<tr>
<td>Chromaticity</td>
<td>y</td>
<td>( \theta = 0^\circ )</td>
<td>-</td>
<td>0.33</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>LED Life Time</td>
<td>-</td>
<td>( Ta = 25^\circ )</td>
<td>-</td>
<td>10000</td>
<td>-</td>
<td>hrs</td>
<td>Note 13-6</td>
</tr>
</tbody>
</table>

Ta = 25°C
Note 13-1: The definitions of viewing angles

Note 13-2: \[ \text{CR} = \frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}} \]

Contrast ratio is measured in optimum common electrode voltage.

Note 13-3: The definition of response time:

- 100% White
- 90% Black
- 10% White
- 0% Black

Brightness

\[ \text{Tr} \quad \text{Tf} \]
Note 13-4: The uniformity of LCD is defined as

\[
U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}
\]

Luminance meter: BM-5A or BM-7 fast (TOPCON)
Measurement distance: 500 mm +/- 50 mm
Ambient illumination: < 1 Lux
Measuring direction: Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

Note 13-5: Topcon BM-7(fast) luminance meter 1.0° field of view is used in the testing (use PVI backlight after 5 minutes operating), ILED = 20mA.

Note 13-6: Constant current 20mA for each loop, and the center brightness must more than 50% of initial brightness value.
14. Handling Cautions

14-1) Mounting of module
   a) Please power off the module when you connect the input/output connector.
   b) Please connect the ground pattern of the inverter circuit surely. If the connection
      is not perfect, some following problems may happen possibly.
      1. The noise from the backlight unit will increase.
      2. The output from inverter circuit will be unstable.
      3. In some cases a part of module will heat.
   c) Polarizer which is made of soft material and susceptible to flaw must be handled
      carefully.
   d) Protective film (Laminator) is applied on surface to protect it against scratches
      and dirt. It is recommended to peel off the laminator before use and taking care
      of static electricity.

14-2) Precautions in mounting
   a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled,
      wipe it with soft dry cloth.
   b) Wipe off water drops or finger grease immediately. Long contact with water may
      cause discoloration or spots.
   c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard
      surface. Please handle with care.
   d) Since CMOS LSI is used in the module. So take care of static electricity and
      earth yourself when handling.

14-3) Adjusting module
   a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
   b) Therefore, do not change any adjusted values. If adjusted values are changed, the
      specifications described may not be satisfied.

14-3) Others
   a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many
      hours.
   b) Store the module at a room temperature place.
   c) The voltage of beginning electric discharge may over the normal voltage because of
      leakage current from approach conductor by to draw lump read lead line around.
   d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel.
      Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet.
      Wash it out immediately with soap.
   e) Observe all other precautionary requirements in handling general electronic components.
   f) Please adjust the voltage of common electrode as material of attachment by 1 module.
15. Reliability Test

<table>
<thead>
<tr>
<th>No</th>
<th>Test Item</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>High Temperature Storage Test</td>
<td>Ta = +70℃, 240 hrs</td>
</tr>
<tr>
<td>2</td>
<td>Low Temperature Storage Test</td>
<td>Ta = -20℃, 240 hrs</td>
</tr>
<tr>
<td>3</td>
<td>Low Temperature Operation Test</td>
<td>Ta = 0℃, 240 hrs</td>
</tr>
<tr>
<td>4</td>
<td>High Temperature Operation Test</td>
<td>Ta = 60℃, 240 hrs</td>
</tr>
<tr>
<td>5</td>
<td>High Temperature &amp; High Humidity Operation Test</td>
<td>Ta = +60℃, 90%RH, 240 hrs</td>
</tr>
<tr>
<td>6</td>
<td>Thermal Cycling Test (non-operating)</td>
<td>-20℃ ← → +70℃, 200 Cycles, 30 min → 30 min</td>
</tr>
<tr>
<td>7</td>
<td>Vibration test (non-operating)</td>
<td>Frequency : 10 ~ 55Hz, Amplitude : 1mm, sweep time : 11 mins, Test period : 6 cycles for each direction of X, Y, Z</td>
</tr>
<tr>
<td>8</td>
<td>Shock Test (non-operating)</td>
<td>100G, 6ms, 3 cycles for each direction of X, Y, Z</td>
</tr>
<tr>
<td>9</td>
<td>Electrostatic Discharge Test (non-operating)</td>
<td>200pF, 0Ω, Machine mode = ±200V, 1 time / each terminal</td>
</tr>
</tbody>
</table>

Ta: ambient temperature

Note: The protective film must be removed before temperature test.

[Criteria]
1. Main LCD should normally work under the normally condition no defect of function, screen quality and appearance (including: mura, line defect, no image)

2. After the temperature and humidity test, the luminance and CR (Contrast ratio), should not be lower than minimum of specification.

3. After the vibration and shock test, can't be found chip broken.
16. Packing

**NOTE:**
1. One layer includes: 1 piece of cushion sheet, 12pcs panel & 1 piece of tray.
2. QTY: 120 pcs panel/carton.
3. Dimension: 450*275*190mm.
4. Weight: 7.5 KG.

**TABLE:**

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REMARK</th>
</tr>
</thead>
<tbody>
<tr>
<td>50-0100091</td>
<td>CARTON INTERNAL</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>50-0500041</td>
<td>EPE CUSHION SHEET</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>50-0200059</td>
<td>EPE FOAM</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>50-0300181</td>
<td>TRAY</td>
<td>11</td>
<td></td>
</tr>
</tbody>
</table>

**DRAWING:**

- CARTON INTERNAL
- EPE CUSHION SHEET
- EPE FOAM
- TRAY

Total 11 Layers

**INFORMATION:**
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| Mar.8, 2006 | 1.3 Modify Page 3: 3. Mechanical Specification  
Outline Dimension from 84.15 (W) × 65.3 (H) × 8.45 (D) change to 84.03 (W) × 65.24 (H) × 8.43 (D)  
Page 4: Mechanical Drawing of TFT-LCD Module  
Page 10: 7.4.1 Serial 8 bits RGB interface VS-DEN time from 18T_H change to 21 T_H  
Page 11: 7.4.2 Parallel 24 bits RGB interface VS-DEN time from 18T_H change to 21 T_H |
Appendix

CON 2

VLED (Pin 01) 15+ 0.5V

LED 0.1μF 25V

GLED1 (Pin 02)

VC1

1KVR

0.1μF 25V

2K 5%

2SC2412

20mA, 1V

49.9 Ω, 1%

1/16W

Vb1

Vc2

1KVR

0.1μF 25V

2K 5%

2SC2412

20mA, 1V

49.9 Ω, 1%

1/16W

Vb2

VE1

VE2