Version: 1.3

TECHNICAL SPECIFICATION

MODEL NO. : PD035OX1

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐PVI's Confirmation

Dep	FAE	Panel Design	Electronic Design	Mechanical Design	Product Verification	Prepared by
Sign						

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TECHNICAL SPECIFICATION

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1. Application

This technical specification applies to 3.5” color TFT-LCD panel PD035OX1.

The TFT LCD panel applies to videophone, door phone and other electronic products which require high quality flat panel displays.

2. Features

. Amorphous silicon TFT-LCD panel with LED Backlight unit

. Support digital 8-bits serial / 24-bits parallel RGB and CCIR601/656 input mode.

. OSD overlay supported in CCIR601/656 input mode.

. Optimum viewing direction：6 o’clock.

. Provide source and gate drivers control timing.

. Image Reversion : Up/Down and Left/Right

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	3.5 (diagonal)	inch
Display Format	320×(RGB) x 234	dot
Display colors	262,144	
Active Area	71.6 (H)×52.65 (V)	mm
Pixel Pitch	0.22375 (H)×0.225 (V)	mm
Pixel Configuration	Delta	
Outline Dimension	84.03 (W)×65.24(H)×3.43 (D)	mm
Surface Treatment	Anti – Glare	
Back-light	LED	
Weight	42±5	g
Display model	Normally	

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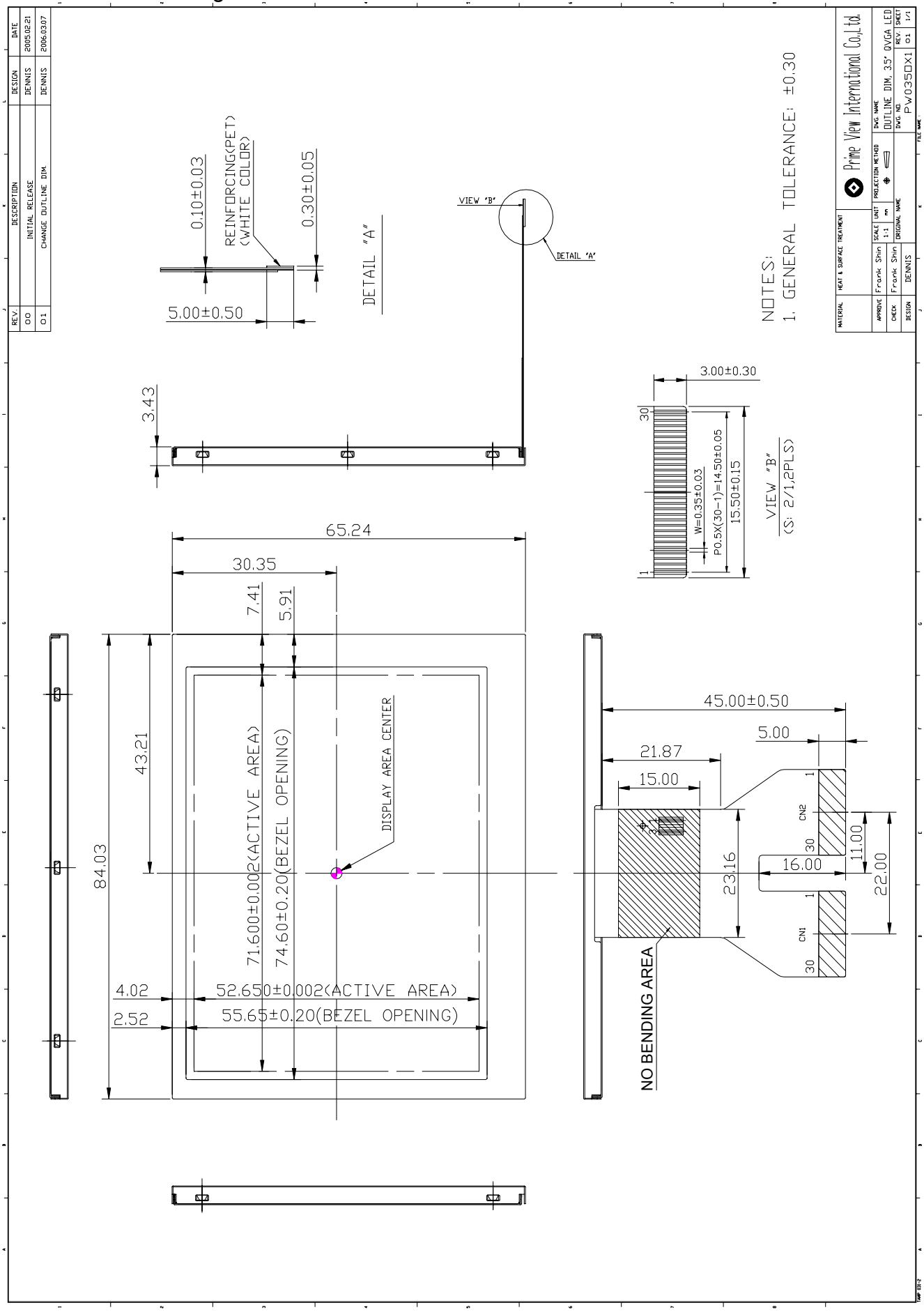
4. Mechanical Drawing of TFT-LCD Module



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5. Input / Output Terminals

CON1

FPC Down Connect , 30Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	D15(G5)	I	Green Data	Note 5-1
2	D14(G4)	I	Green Data	
3	D13(G3)	I	Green Data	
4	D12(G2)	I	Green Data	
5	D11(G1)	I	Green Data	
6	D10(G0)	I	Green Data(LSB)	
7	V_{DD2}	I	Analog power supply for source driver	Note 5-2
8	V8	I	Gamma correction voltage 8	Note 5-3
9	V7	I	Gamma correction voltage 7	
10	V6	I	Gamma correction voltage 6	
11	V5	I	Gamma correction voltage 5	
12	V4	I	Gamma correction voltage 4	
13	V3	I	Gamma correction voltage 3	
14	V2	I	Gamma correction voltage 2	
15	V1	I	Gamma correction voltage 1	
16	V_{SS2}	I	Analog ground for source driver	
17	D07(R7)	I	Red Data(MSB)	Note 5-1
18	D06(R6)	I	Red Data	
19	D05(R5)	I	Red Data	
20	D04(R4)	I	Red Data	
21	D03(R3)	I	Red Data	
22	D02(R2)	I	Red Data	
23	D01(R1)	I	Red Data	
24	D00(R0)	I	Red Data(LSB)	
25	CLK	I	Clock signal. Latching data at the rising edge	
26	HS	I	Horizontal sync input in RGB mode and CCIR601	Note 5-4
27	VS	I	Vertical sync input in RGB mode and CCIR601	Note 5-5
28	DEN	I	Input data enable control.(Normally pull low)	Note 5-6
29	V_{CC}	I	Digital power supply for source driver IC	Note 5-7
30	V_{COM}	I	Voltage for common electrode	Note 5-8

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CON2

FPC Down Connect , 30Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	VLED	I	Power supply for LED	Note 5-9
2	GLED1	I	Ground for LED	
3	GLED2	I	Ground for LED	
4	NC	-	NC	
5	V_{GH}	I	Positive power for gate driver	Note 5-10
6	V_{DD1}	I	Power supply for gate logic circuit	Note 5-11
7	V_{SS1}	I	Ground for gate driver	
8	V_{EE}	I	Negative power for gate driver	Note 5-12
9	V_{DD1}	I	Power supply for gate logic circuit	Note 5-11
10	GND	I	Digital ground for source driver IC	
11	RESETB	I	Hardware global reset, (low active)	
12	VSET	I	Externally/Internally gamma voltage setup	
13	U/D	I	Up/Down control for gate driver	Note 5-13
14	L/R	I	Left/Right control for source driver	
15	IF2	I	Select the input data format	Note 5-14
16	IF1	I	(Serial RGB, Parallel RGB, CCIR601/656)	
17	SPENA	I	Serial port data enable signal (normally pull high)	
`18	SPCK	I	Serial port clock. (Normally pull high)	
19	SPDA	I/O	Serial port data input/output	
20	POL	O	Polarity select for the line inversion control signal	Note 5-15
21	D27(B7)	I	Blue Data(MSB)	Note 5-1
22	D26(B6)	I	Blue Data	
23	D25(B5)	I	Blue Data	
24	D24(B4)	I	Blue Data	
25	D23(B3)	I	Blue Data	
26	D22(B2)	I	Blue Data	
27	D21(B1)	I	Blue Data	
28	D20(B0)	I	Blue Data(LSB)	
29	D17(G7)	I	Green Data(MSB)	
30	D16(G6)	I	Green Data	

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Note 5-1 : Digital data input. DX0 is LSB and DX7 is MSB.

If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G and B data in turn.
If serial RGB or CCIR601/656 input mode is selected, only D07~D00 are used, and others short to Vss.

Note 5-2 : V_{DD2} Typ. = +5V

Note 5-3 : The output voltage is determined by the digital input data. If digital RGB or CCIR601/656 input mode is selected, The 8 gamma correction reference voltages can be set to externally or generate internally.
If VSET = "H", the gamma correction voltage generated externally
If VSET = "L", the default value is as below : (When V_{DD} =+5V)

	V1	V2	V3	V4	V5	V6	V7	V8
Default Voltage(V)	4.29	3.73	3.33	2.94	2.62	2.22	1.51	0.48

Note 5-4 : Horizontal sync input in digital RGB mode. Or HREF input in CCIR601 mode.
(Short to Vss if not used)

Note 5-5 : Vertical sync input in digital RGB mode. Or V123 input in CCIR601 mode.
(Short to Vss if not used)

Note 5-6 : Digital RGB data input format
For digital RGB input data format, both SYNC. Mode and DEN mode are supported. If DEN signal is fixed low, SYNC. Mode is used. Otherwise , DEN mode is used.

Note 5-7 : V_{CC} Typ. = +3.3V

Note 5-8 : V_{COM} Typ.＝+6.0Vpp

Note 5-9 : ILED Typ. = 20mA., VLED Typ. = 9V

Note 5-10 : V_{GH} Typ. =+15V.

Note 5-11 : V_{DD1} Typ.＝+3.3V.

Note 5-12 : V_{EE} Typ. = -15V.

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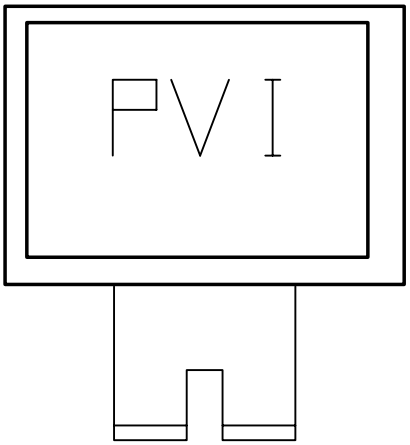
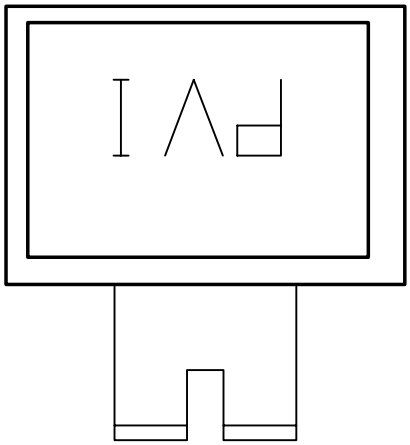
Note 5-13 : The definition of L/R , U/D

U/D(PIN 13)=Low L/R(PIN 14)=High



U/D(PIN 13)=High L/R(PIN 14)=Low



Note 5-14 : IF1,IF2 control the input data format.

IF2,IF1	Input data format
L,L (default)	Serial RGB
L,H	Parallel RGB
H,L	CCIR601
H,H	CCIR656

Note 5-15 : When POL=L, output voltage is negative polarity.
When POL=H, output voltage is positive polarity.

6. Absolute Maximum Ratings

$V_{SS1}=V_{SS2}=0$ V，Ta = 25 ℃

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply voltage for source driver		V_{CC}	-0.3	+7.0	V	
		V_{DD2}	-0.3	+7.0	V	
Supply voltage for gate driver		V_{DD1}	-0.3	+7.0	V	
	H Level	V_{GH}	-0.3	+32.0	V	
	L Level	V_{EE}	-22.0	+0.3	V	
		V_{GH}-V_{EE}	-0.3	+45.0	V	
Input signal voltage		V_{IN}	-0.3	V_{DD}+0.3	V	

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7. Electrical Characteristics

7-1 Operating condition

$V_{SS1}=V_{SS2}=0$ V，Ta = 25 ℃

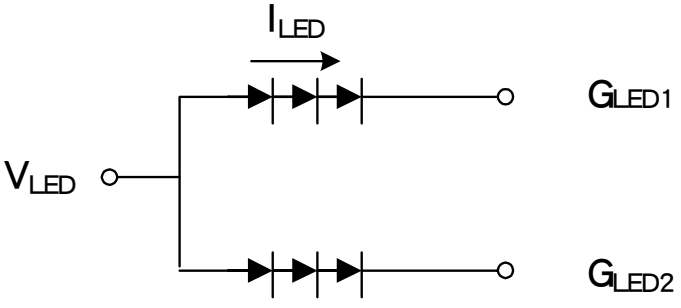
Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply voltage for source driver	Logic	V_{CC}	+3.0	+3.3	+3.6	V	
	Analog	V_{DD2}	+3.8	+5.0	+5.5	V	
Supply voltage for gate driver	Logic	V_{DD1}	+3.0	+3.3	+3.6	V	
	H level	V_{GH}	+10	+15	+30	V	
	L level	V_{EE}	-17	-15	-5	V	
Signal input voltage	H level	V_{IH}	0.7V_{CC}	-	V_{CC}	V	
	L level	V_{IL}	0	-	0.3V_{CC}	V	
Signal output voltage	H level	V_{OH}	0.8V_{CC}	-	V_{CC}	V	
	L level	V_{OL}	0	-	0.2V_{CC}	V	
V_{COM}		V_{COMAC}	-	+6.0	-	V_{P-P}	AC Component of V_{COM}
		V_{COMDC}	-	1.0	-	V	DC Component of V_{COM} Note 7-1

Note 7-1 : PVI strongly suggests that the V_{COMDC} level shall be adjustable , and the adjustable level range is 1V±1V , every module's V_{COMDC} level shall be carefully adjusted to show a best image performance.

7-2 Recommended driving condition for LED backlight

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	VLED	9.0	10.0	11.0	V	I_L = 20 mA
Supply current of LED backlight	ILED	-	20	-	mA	Note 7-2
Backlight Power Consumption	PLED	360	400	440	mW	Note 7-3

Note 7-2 : LED B/L applied information , please refer to the appendix at the end .
Note 7-3 : $P_{LED} = 2*I_{LED}*V_{LED}$.



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7-3 Power consumption

V_{SS1}=V_{SS2}=0 V，Ta = 25 ℃

Parameter	Symbol	Conditions	TYP.	MAX.	Unit	Remark
Supply current for gate driver (Hi level)	I_{GH}	V_{GH} =+15V	0.2	0.5	mA	
Supply current for gate driver(Logic)	I_{DD1}	V_{DD1}=+3.3V	0.05	0.1	mA	
Supply current for gate driver (Low level)	I_{EE}	V_{EE} =-15V	0.2	0.5	mA	VEE center voltage
Supply current for source driver(Analog)	V_{DD2}	V_{DD2}=+5V	5.0	8.0	mA	
Supply current for source driver(Logic)	V_{CC}	V_{CC}=+3.3V	4.5	7.0	mA	
LCD panel power consumption	-		48	80	mW	
Backlight power consumption	P_{LED}		400	440	mW	
Total power consumption	-		0.45	0.52	W	

* Above data measured on serial mode:

If on parallel mode, I_{CC} Typ.= 3.0mA, Max.=5.0mA ;

panel power consumption Typ.= 41.5mW Max.= 72.8mW.

If on CCIR601/656 mode, I_{CC} Typ.= 6.0mA, Max.=10.0mA ;

panel power consumption Typ.= 51.4mW Max.= 89.3mW.

7-4 Timing characteristics of input signals

7.4.1 Serial 8 bits RGB interface

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK period	T_{OSC}	-	52	-	ns	Note 7-4
Data setup time	T_{SU}	12	-	-	ns	
Data hold time	T_{HD}	12	-	-	ns	
HS period	T_H	-	1224	-	T_{OSC}	
HS pulse width	T_{HS}	5	90	-	T_{OSC}	
HS rising time	T_{Cr}	-	-	700	ns	
HS falling time	T_{Cf}	-	-	300	ns	
VS pulse width	T_{VS}	1	3	5	T_H	
VS rising time	T_{Vr}	-	-	700	ns	
VS falling time	T_{Vf}	-	-	1.5	us	
HS falling to VS falling time for odd field	T_{HVO}	0	3	-	T_{OSC}	
VS falling to HS falling time for even field	T_{HVE}	0	3	-	T_{OSC}	
VS-DEN time	T_{VSE}	-	21	-	T_H	
HS-DEN time	T_{HE}	108	204	264	T_{OSC}	
DEN pulse width	T_{EP}	-	960	-	T_{OSC}	
VS period		-	262	-	T_H	

Note 7-4 : When SYNC mode is used, 1st data start from 204th CLK after HS fallings.

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7.4.2 Parallel 24 bits RGB interface

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK period	T_{OSC}	-	156	-	ns	Note 7-5
Data setup time	T_{SU}	12	-	-	ns	
Data hold time	T_{HD}	12	-	-	ns	
HS period	T_H	-	408	-	T_{OSC}	
HS pulse width	T_{HS}	5	30	-	T_{OSC}	
HS rising time	T_{Cr}	-	-	700	ns	
HS falling time	T_{Cf}	-	-	300	ns	
VS pulse width	T_{VS}	1	3	5	T_H	
VS rising time	T_{Vr}	-	-	700	ns	
VS falling time	T_{Vf}	-	-	1.5	us	
HS falling to VS falling time for odd field	T_{HVO}	0	3	-	T_{OSC}	
VS falling to HS falling time for even field	T_{HVE}	0	3	-	T_{OSC}	
VS-DEN time	T_{VSE}	-	21	-	T_H	
HS-DEN time	T_{HE}	36	68	88	T_{OSC}	
DEN pulse width	T_{EP}	-	320	-	T_{OSC}	
VS period		-	262	-	T_H	

Note 7-5 : When SYNC mode is used, 1st data start from 68th CLK after HS fallings.

7.4.3 CCIR601/656 Interface

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK period	T_{OSC}	-	37	-	ns	
Data setup time	T_{SU}	12	-	-	ns	
Data hold time	T_{HD}	12	-	-	ns	

7.4.4 Hardware reset timing

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
RESETB low pulse width	T_{RSB}	200	-	-	ns	

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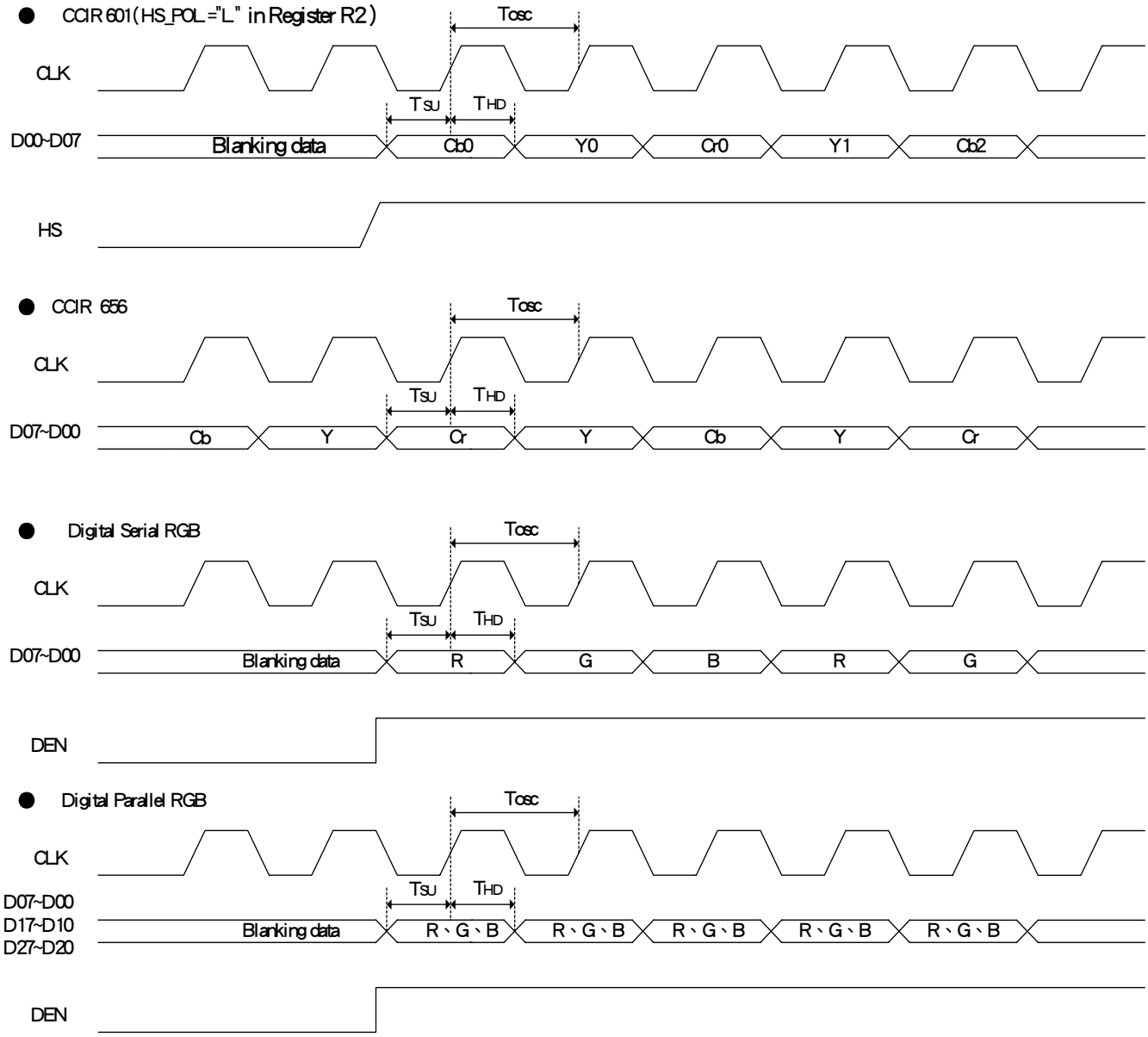
7.5 Timing controller timing chart

7.5.1 Clock and Data waveform



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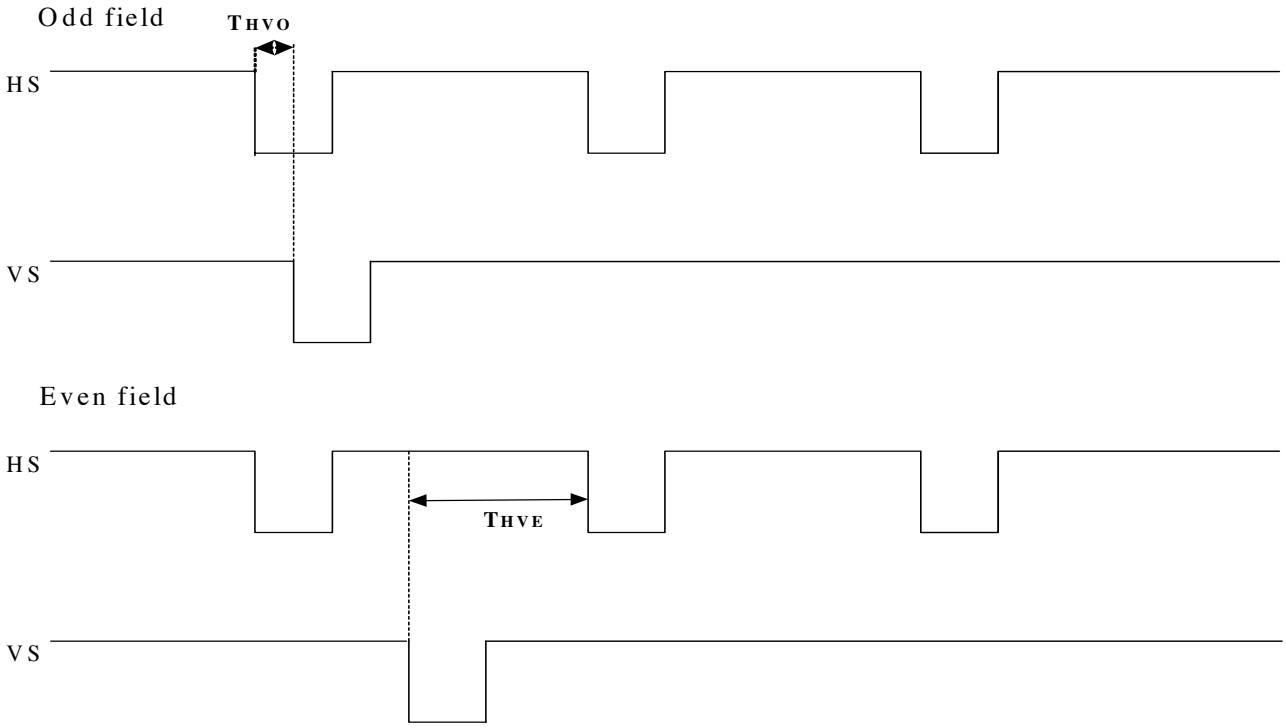
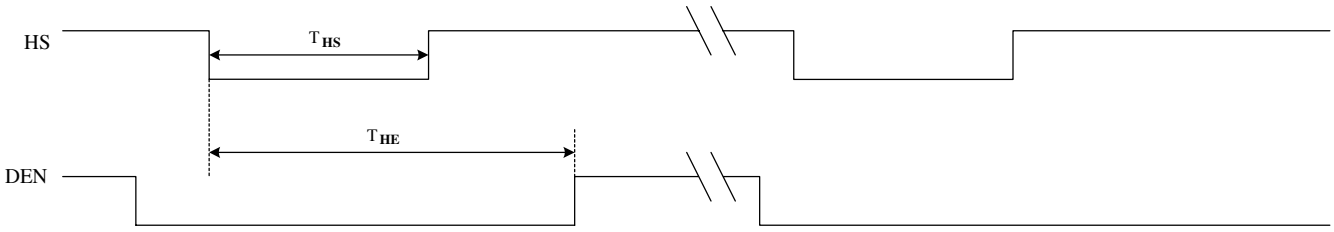
7.5.2 HS,VS,DEN timing waveform

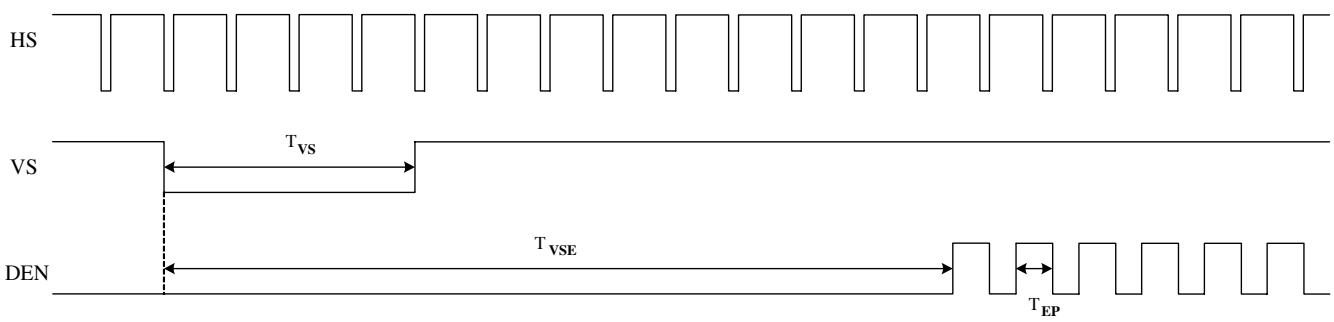
HS and VS timing relationship



HS and DEN timing relationship



HS, VS and DEN timing relationship



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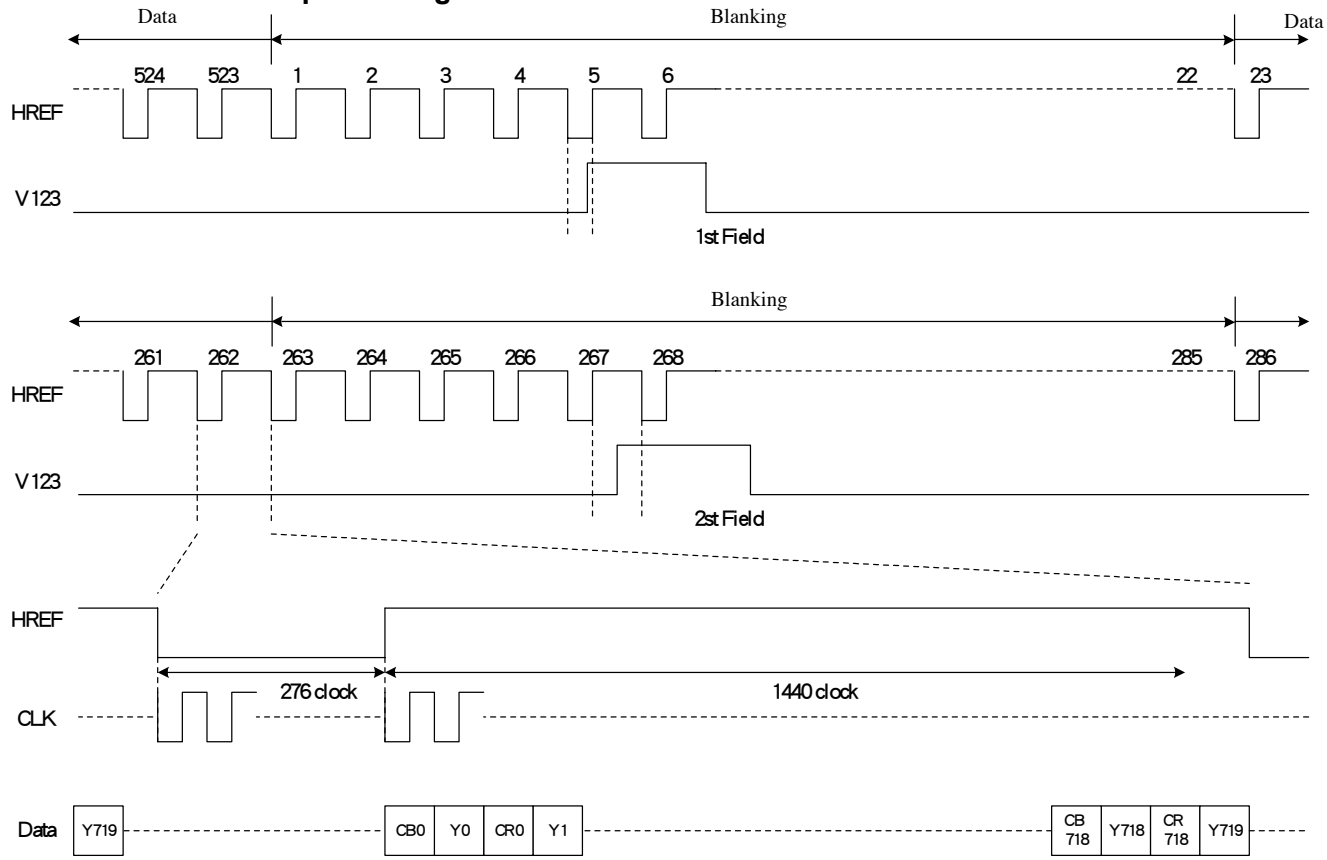
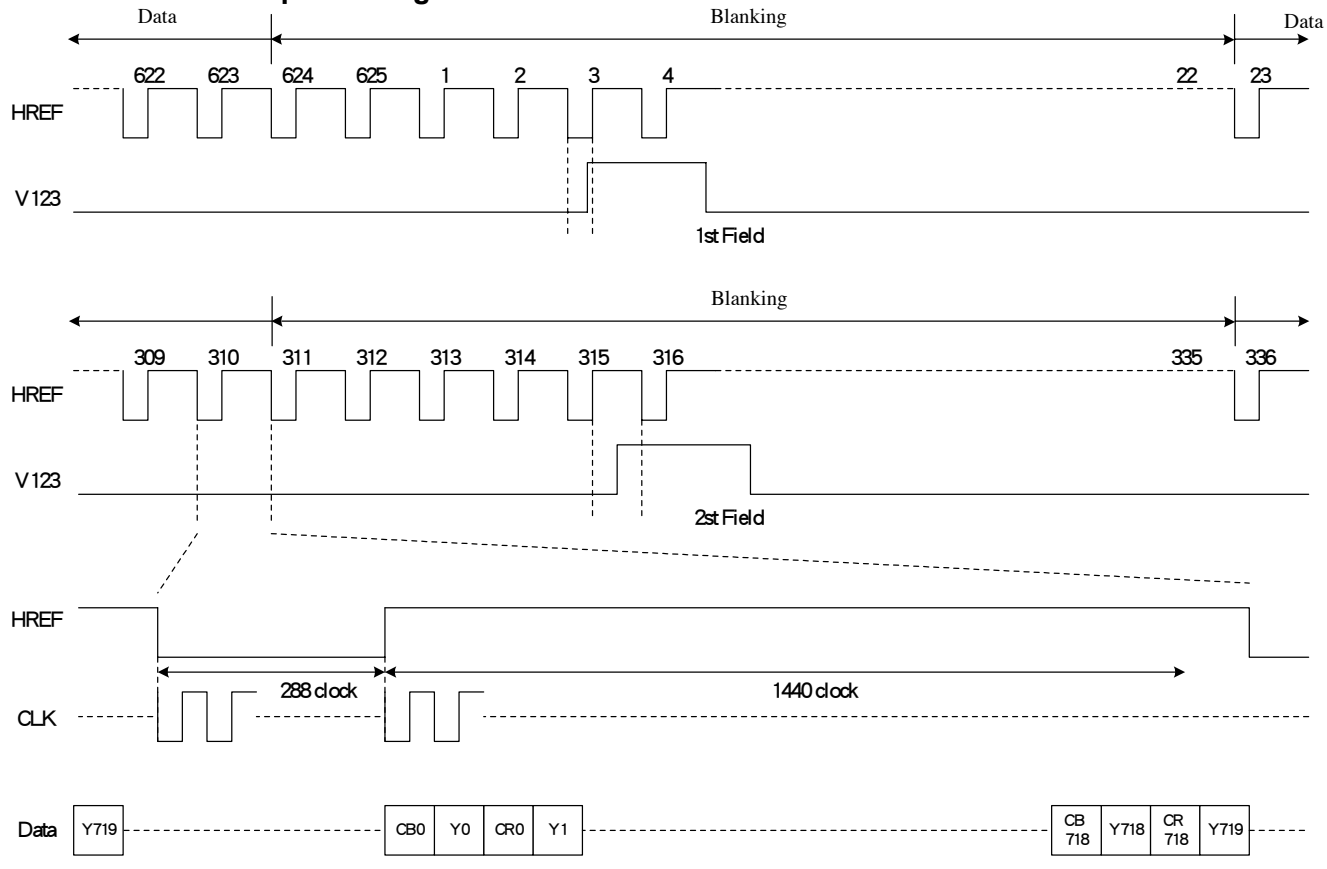
7.5.3 CCIR601 timing waveform (VS_POL="H", HS_POL="L" in Register R2)

ITU-R BT.601 NTSC Input Timing



ITU-R BT.601 PAL Input Timing



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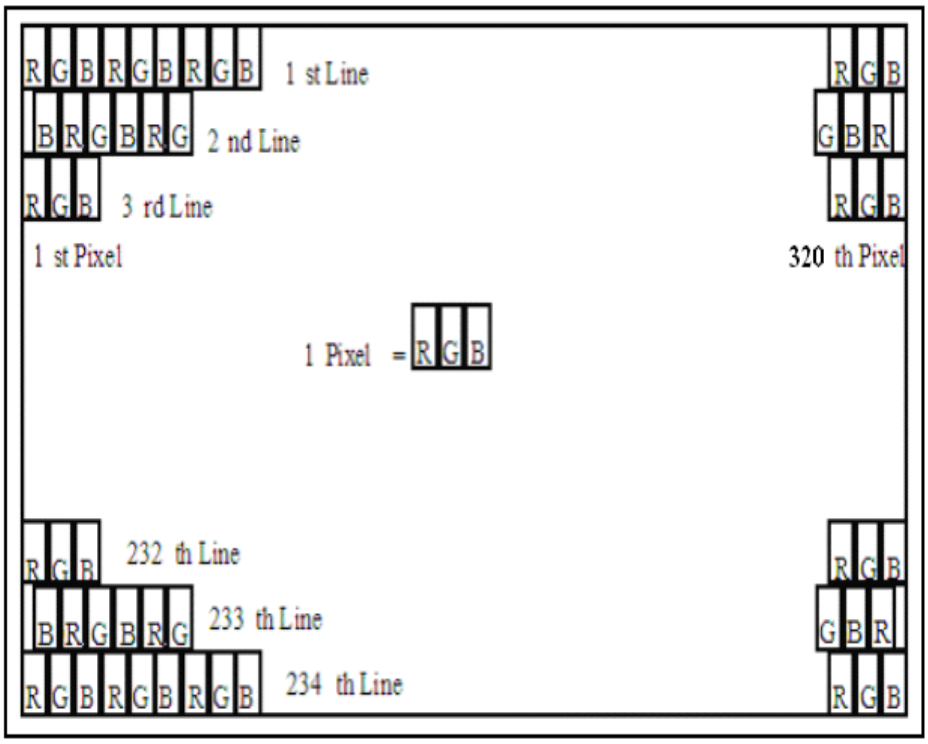
8. Pixel Arrangement



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9. Display Color and Gray Scale Reference

Color		Input Color Data																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

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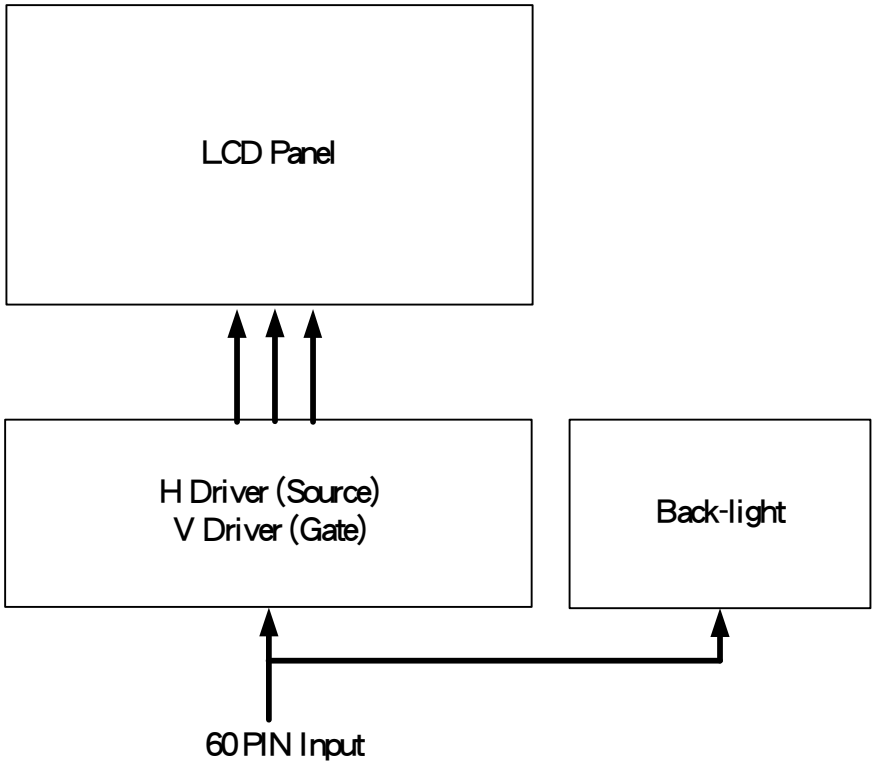
10. Block Diagram



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11. SPI Register Description and Timing Characteristics

11.1 Function Control Register

Register R0 :Address(A3~A0)→0000

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	STHD1	STHD0	STHP4	STHP3	STHP2	STHP1	STHP0
Default	0	0	0	0	0	0	0	0

STHD [1:0] : adjust start pulse position by dot

STHD1	STHD0	STH position adjust by dot
1	1	-1
1	0	-2
0	0	0
0	1	+1

STHP [4:0] : adjust start pulse position by pixel

STHP4	STHP3	STHP2	STHP1	STHP0	STH position adjust by pixel
1	1	1	1	1	-1
1	1	1	1	0	-2
1	1	1	0	1	-3
1	1	1	0	0	-4
1	1	0	1	1	-5
1	1	0	1	0	-6
1	1	0	0	1	-7
1	1	0	0	0	-8
1	0	1	1	1	-9
1	0	1	1	0	-10
1	0	1	0	1	-11
1	0	1	0	0	-12
1	0	0	1	1	-13
1	0	0	1	0	-14
1	0	0	0	1	-15
1	0	0	0	0	-16
0	0	0	0	0	0
0	0	0	0	1	+1
0	0	0	1	0	+2
0	0	0	1	1	+3
0	0	1	0	0	+4
0	0	1	0	1	+5
0	0	1	1	0	+6
0	0	1	1	1	+7
0	1	0	0	0	+8
0	1	0	0	1	+9
0	1	0	1	0	+10
0	1	0	1	1	+11
0	1	1	0	0	+12
0	1	1	0	1	+13
0	1	1	1	0	+14
0	1	1	1	1	+15

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Register R1 :Address(A3~A0)→0001

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	STVP3	STVP2	STVP1	STVP0	STVNT1	STVNT0	STVPAL1	STVPAL0
Default	0	0	0	0	0	0	0	1

STVP [3:0] : adjust first line position by line

STVP3	STVP2	STVP1	STVP0	STV position adjust by line
1	1	1	1	-1
1	1	1	0	-2
1	1	0	1	-3
1	1	0	0	-4
1	0	1	1	-5
1	0	1	0	-6
1	0	0	1	-7
1	0	0	0	-8
0	0	0	0	0
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7

STVNT[1:0]: When NTSC mode, the relationship of first line in Even field and Odd field.
00: First line in Even field = First line in Odd field.
01: First line in Even field = First line in Odd field +1.
10: No use.
11: First line in Even field = First line in Odd field –1.

STVPAL[1:0]: When PAL mode, the relationship of first line in Even field and Odd field.
(Only for CCIR601/656 mode)
00: First line in Even field = First line in Odd field.
01: First line in Even field = First line in Odd field +1.
10: No use.
11: First line in Even field = First line in Odd field –1.

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Register R2 :Address(A3~A0)→0010

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	HS_POL	VS_POL	NPC_IN	NPC_SET
Default	0	0	0	1	0	0	1	0

HS_POL: HS polarity setting.

HS_POL = “L”, negative polarity.

HS_POL = “H”, positive polarity.

VS_POL: VS polarity setting.

VS_POL = “L”, negative polarity.

VS_POL = “H”, positive polarity.

NPC_IN: Define the NTSC/PAL mode by SPI.

NPC_IN = “L”, PAL. (Only for CCIR601/656 mode)

NPC_IN = “H”, NTSC.

NPC_SET: Set the NTSC/PAL auto detection or define by NPC_IN.

NPC_SET = “L”, auto detection.

NPC_SET = “H”, define by SPI.

Register R3 :Address(A3~A0)→0011

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	PWD_EN	OSDCLKP	OSDHSP	OSDVSD
Default	0	0	1	0	1	0	1	1

PWD_EN: Set DAC power saving function.

PWD_EN = “L”, disable. The DAC is always power on.

PWD_EN = “H”, enable.

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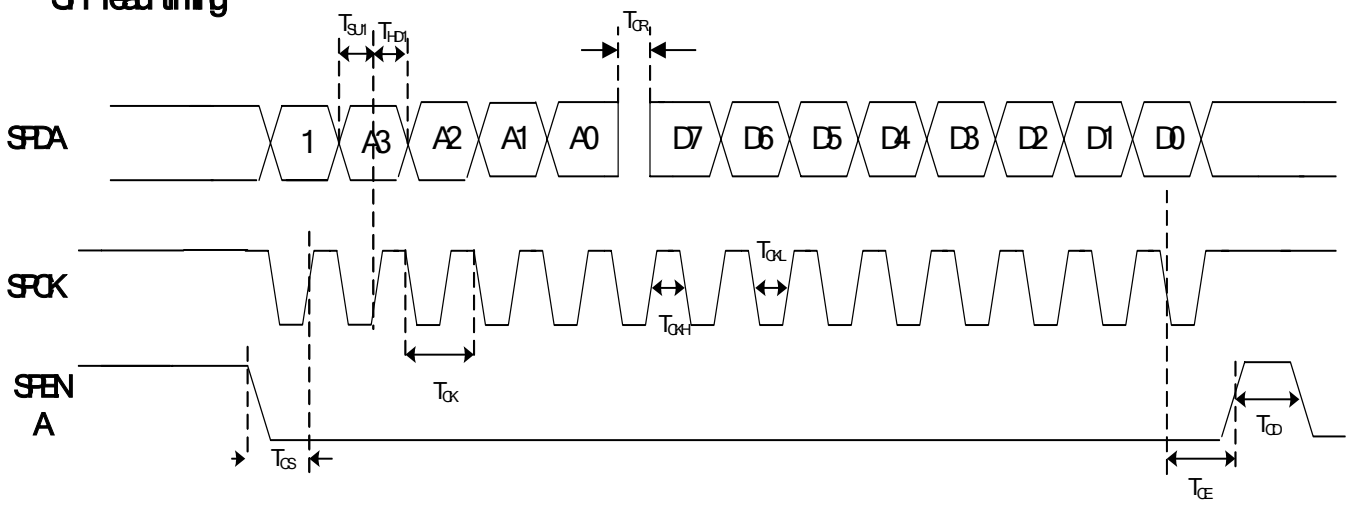
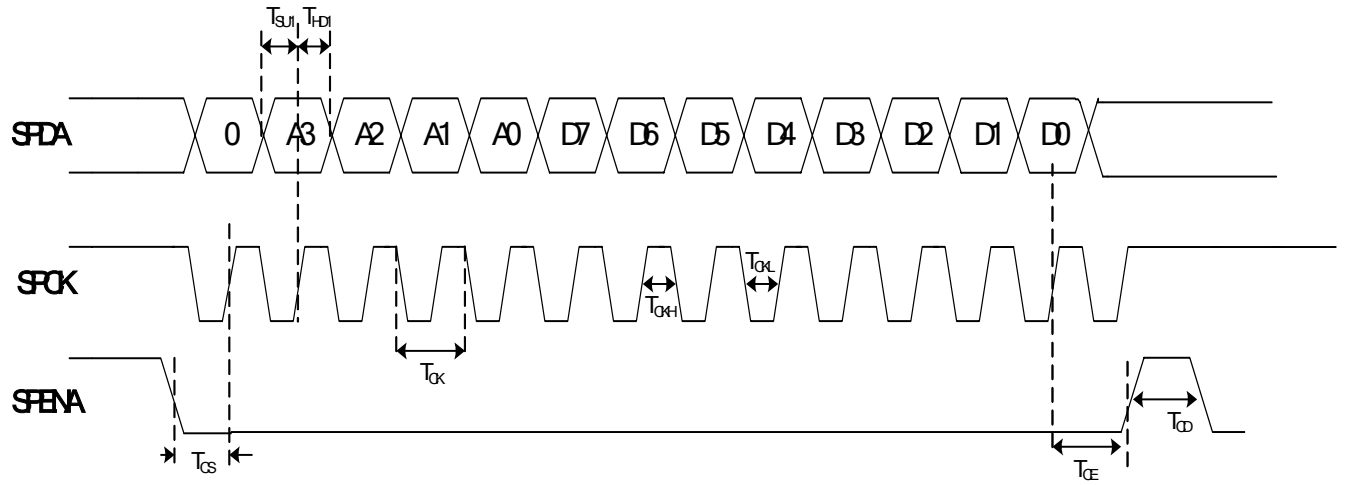
11-2 SPI timing characteristic

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
SPCK period	T_{CK}	60	-	-	ns	
SPCK high width	T_{CKH}	30	-	-	ns	
SPCK low width	T_{CKL}	30	-	-	ns	
Data setup time	T_{SU1}	12	-	-	ns	
Data hold time	T_{HD1}	12	-	-	ns	
SPENA to SPCK setup time	T_{CS}	20	-	-	ns	
SPENA to SPDA hold time	T_{CE}	20	-	-	ns	
SPENA high pulse width	T_{CD}	50	-	-	ns	
SPDA output latency	T_{CR}	-	1/2	-	T_{CK}	

· SPI "read" timing



· SPI "write" timing



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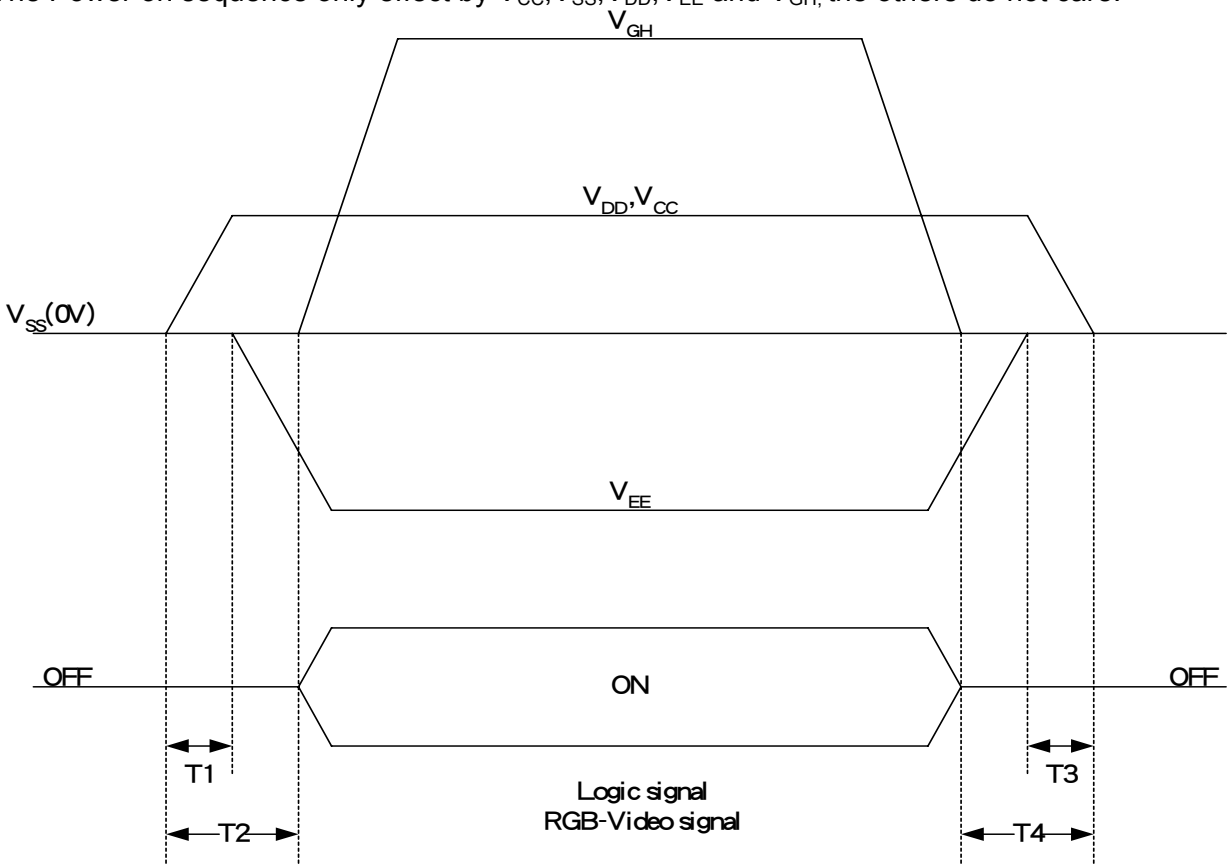
12. Power On Sequence

The Power on sequence only effect by V_{CC},V_{SS},V_{DD},V_{EE} and $V_{GH,}$ the others do not care.



1) 10ms≦T1<T2
2) 0ms<T3≦T4≦10ms

13. Optical Characteristics

Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ21, θ22	CR≧10	45	50	---	deg	Note 13-1
	Vertical	θ11		30	35	---	deg	
		θ12		10	15	---	deg	
Contrast Ratio		CR	At optimized Viewing angle	200	400	---		Note 13-2
Response time	Rise	Tr	θ=0°	---	15	30	ms	Note 13-3
	Fall	Tf		---	25	50	ms	
Uniformity		U	9 point	70	75	-	%	Note 13-4
Brightness		-	Center point	200	250	-	cd/㎡	Note 13-5
White Chromaticity		x	θ=0°	-	0.31	-	-	Note 13-5
		y	θ=0°	-	0.33	-	-	
LED Life Time Ta=25℃		-	-	-	10000	-	hrs	Note13-6

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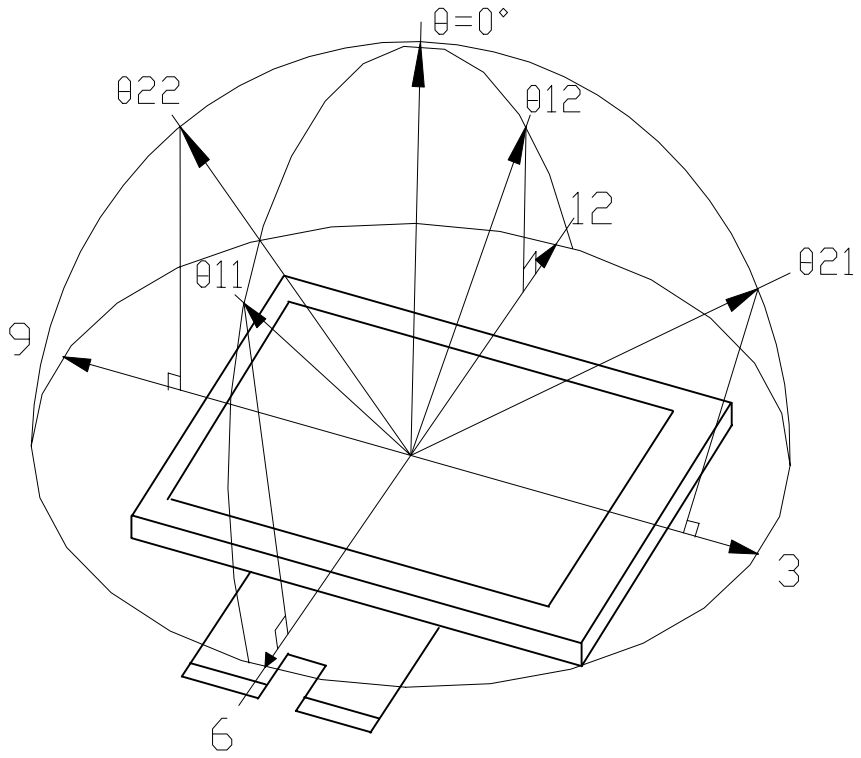
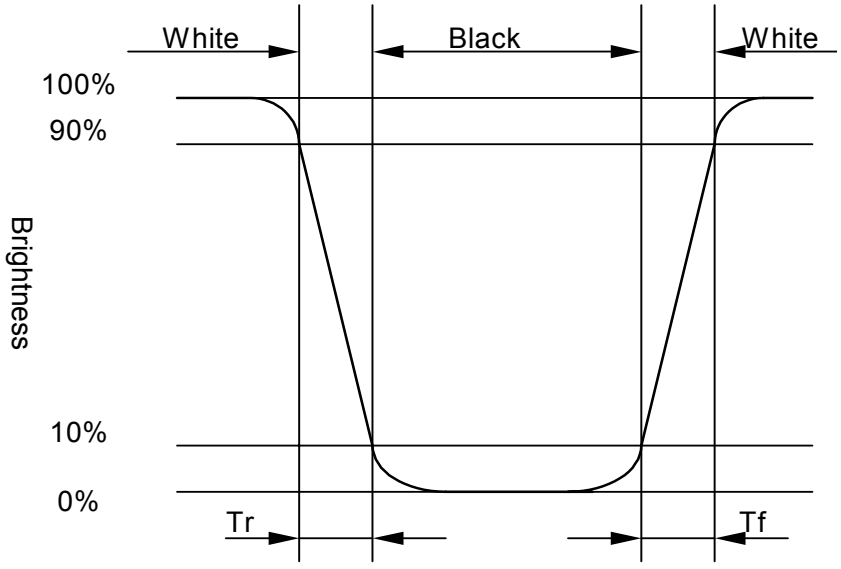
Note 13-1 : The definitions of viewing angles



Note 13-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

Contrast ratio is measured in optimum common electrode voltage.

Note 13-3 : The definition of response time :



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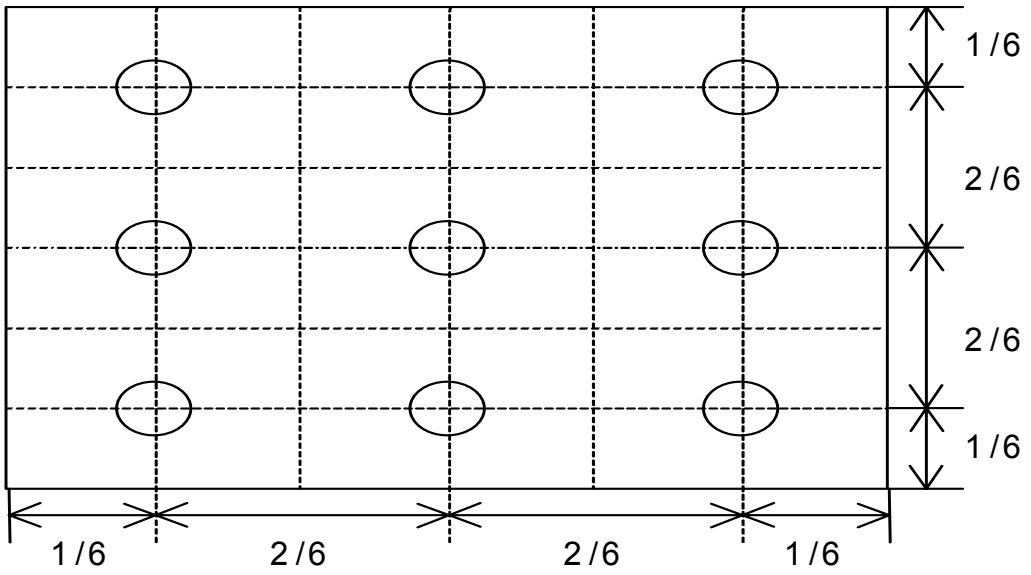
Note 13-4 : The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

Luminance meter : BM-5A or BM-7 fast (TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).



Note 13-5 : Topcon BM-7(fast) luminance meter 1.0° field of view is used in the testing (use PVI backlight after 5 minutes operating), ILED = 20mA.

Note 13-6 : Constant current 20mA for each loop , and the center brightness must more than 50% of initial brightness value .

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14. Handling Cautions

14-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
1.The noise from the backlight unit will increase.
2. The output from inverter circuit will be unstable.
3. In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirts. It is recommended to peel off the laminator before use and taking care of static electricity.

14-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

14-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.

b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

14-3) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

f)Please adjust the voltage of common electrode as material of attachment by 1 module.

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15. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +70℃, 240 hrs
2	Low Temperature Storage Test	Ta = -20℃, 240 hrs
3	Low Temperature Operation Test	Ta = 0℃, 240 hrs
4	High Temperature Operation Test	Ta=60℃,240hrs
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-20℃ ← → +70℃ , 200 Cycles 30 min 30 min
7	Vibration test (non-operating)	Frequency : 10 ~ 55Hz Amplitude : 1mm , sweep time : 11 mins Test period : 6 cycles for each direction of X,Y, Z
8	Shock Test(non-operating)	100G , 6ms , 3cycles for each direction of X,Y,Z
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω Machine mode = ±200V 1 time / each terminal

Ta: ambient temperature

Note : The protective film must be removed before temperature test.

[Criteria]

1. Main LCD should normally work under the normally condition no defect of function,screen quality and appearance (including : mura ,line defect ,no image)

2. After the temperature and humidity test, the luminance and CR (Contrast ratio) ,should not be lower than minimum of specification.

3. After the vibration and shock test , can't be found chip broken.

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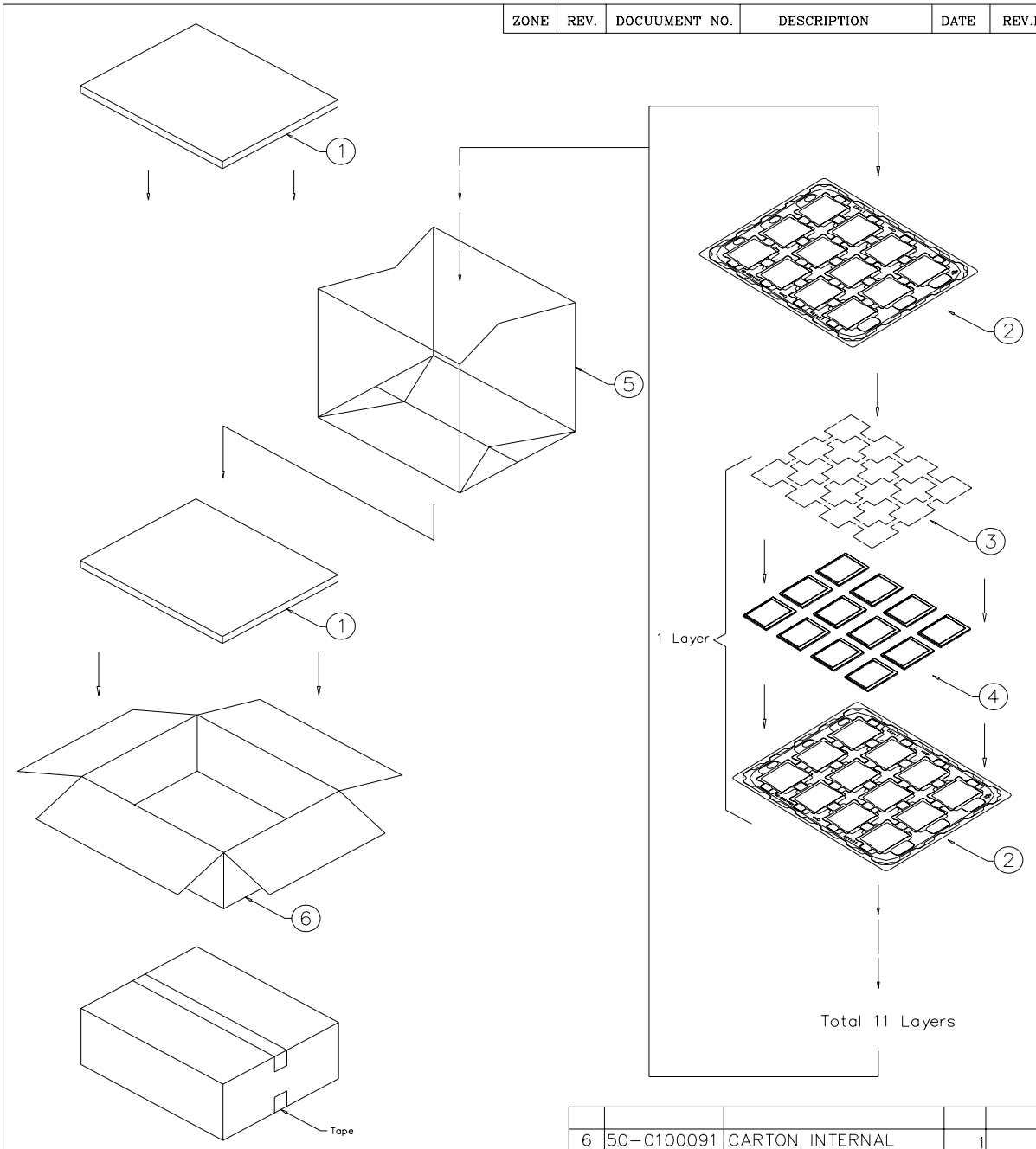
16. Packing

ZONE	REV.	DOCUUMENT NO.	DESCRIPTION	DATE	REV.BY



NOTE:
1. One layer include: 1 piece of cushion sheet, 12pcs panel & 1 piece of tray.
2. Q'TY: 120 pcs panel/carton.
3. Dimension: 455*375*190mm
4. Weight: 7.5 KG

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
6	50-0100091	CARTON INTERNAL	1	
5	50-0500041	摺口袋450*380*700mm	1	抗靜電
4		PD035OX1	120	
3	50-0200059	EPE CUSHION SHEET	10	抗靜電
2	50-0301181	TRAY	11	抗靜電
1	50-0300491	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK	元太科技股份有限公司 Prime View Internation Co.,ltd.

			SCALE	UNIT	SHEET	DWG.TITLE
APPROVE	Frank Shin	'05.06.08	1:1	mm	1 OF 2	PD035OX1 PACKING Dim
CHECK	Frank Shin	'05.06.08				
DESIGN	Dennis	'05.06.08	MTL.NO.		DWG.NO.	REV. 01 / A4 SIZE

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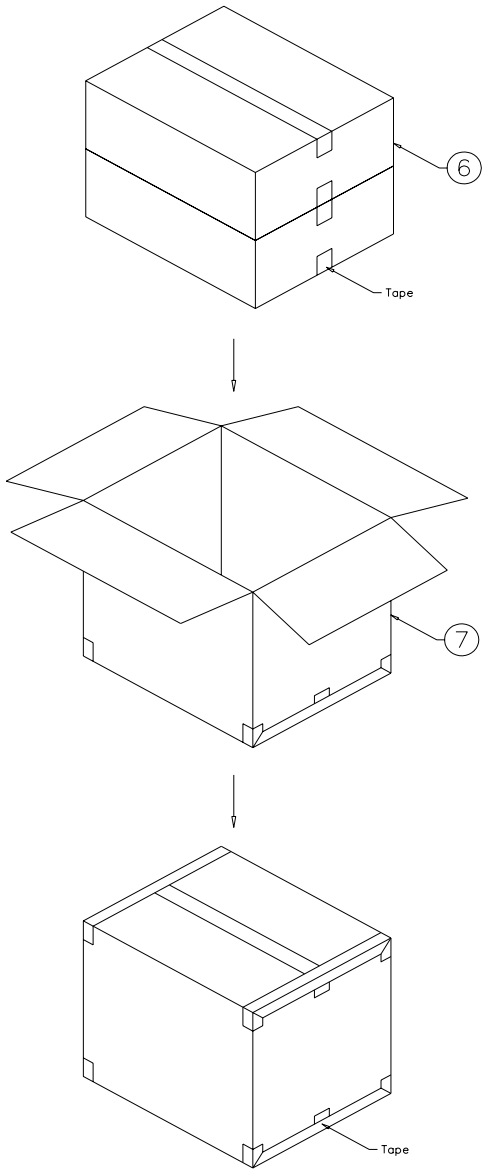
ZONE	REV.	DOCUUMENT NO.	DESCRIPTION	DATE	REV.BY



NOTE:

1. Q'TY: 240 pcs panel/carton.
2. Dimension: 480*396*405mm
3. Weight: 16 KG

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
7	50-0100101	CARTON EXTERNAL	1	

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK	元太科技股份有限公司 Prime View Internation Co.,ltd.

APPROVE	Frank Shin	'05.06.08	SCALE 1:1	UNIT mm	SHEET 2 OF 2	DWG.TITLE PD035OX1 PACKING Dim
CHECK	Frank Shin	'05.06.08				
DESIGN	Dennis	'05.06.08	MTL.NO.	DWG.NO.	REV. 01	A4 SIZE

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Revision History

Rev.	Issued Date	Revised Contents
0.1	Jan .03 , 2005	Preliminary
0.2	Feb .02 , 2005	Modify: Page07: Note5-2 V_{GH} Typ.= +15V. Page16: Register R2 – bit D5, D4 change to reserved, Register R3 – bit D6,D5,D4 change to reserved. Page18: Absolute Max. ratings – storage and operation temperature. Delete: Page21: 9.4.4 Output signal character for Digital/Analog RGB mode.
0.3	Apr. 15, 2005	Modify: Page04: Mechanical Drawing of TFT-LCD Module (FPC Outline Drawing) Add: Appendix (LED B/L driving reference circuit)
0.4	May.17, 2005	Modify: Page05: POL I/O condition to output. Page25: Uniformity Typ. From 80% to 75%.
1.0	Jun. 07, 2005	Modify: Page31: Packing
1. 1	Jul. 22, 2005	Modify: Page20:9.4.1 Serial 8 bit RGB interface Page21:9.4.2Parallel 24 bits RGB interface Page22: 9.5.1Clock and Data waveform Page23: 9.5.2Digital/Analog RGB timing waveform
1.2	Sep.19,2005	Modify: Page6:5. Input / Output Terminals(CON2) Pin15 Symbol from IF1 change to IF2 Pin16 Symbol from IF2 change to IF1 Page18:11.1 Function Control Register Register R0 : Register R1 : Register R2 : Register R3 : ↓change to Register R0 :Address(A3~A0)→0000 Register R1 :Address(A3~A0)→0001 Register R2 :Address(A3~A0)→0010 Register R3 :Address(A3~A0)→0011 Page21 11-2 SPI timing characteristic 8SPI write timing 8SPI read timing Add: Page16: 9. Display Color and Gray Scale Reference Page26:.15.Reliability test High Temperature Operation Test

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1.3	Mar.8,2006	Modify Page3:3.Mechanical Specification Outline Dimension from 84.15 (W)×65.3 (H)×3.45 (D) change to 84.03 (W)×65.24(H)×3.43 (D) Page4: Mechanical Drawing of TFT-LCD Module Page10:7-4 Timing characteristics of input signals→7.4.1 Serial 8 bits RGB interface→VS-DEN time from $18T_H$ change to 21 T_H Page11: 7.4.2 Parallel 24 bits RGB interface VS-DEN time from $18T_H$ change to 21 T_H

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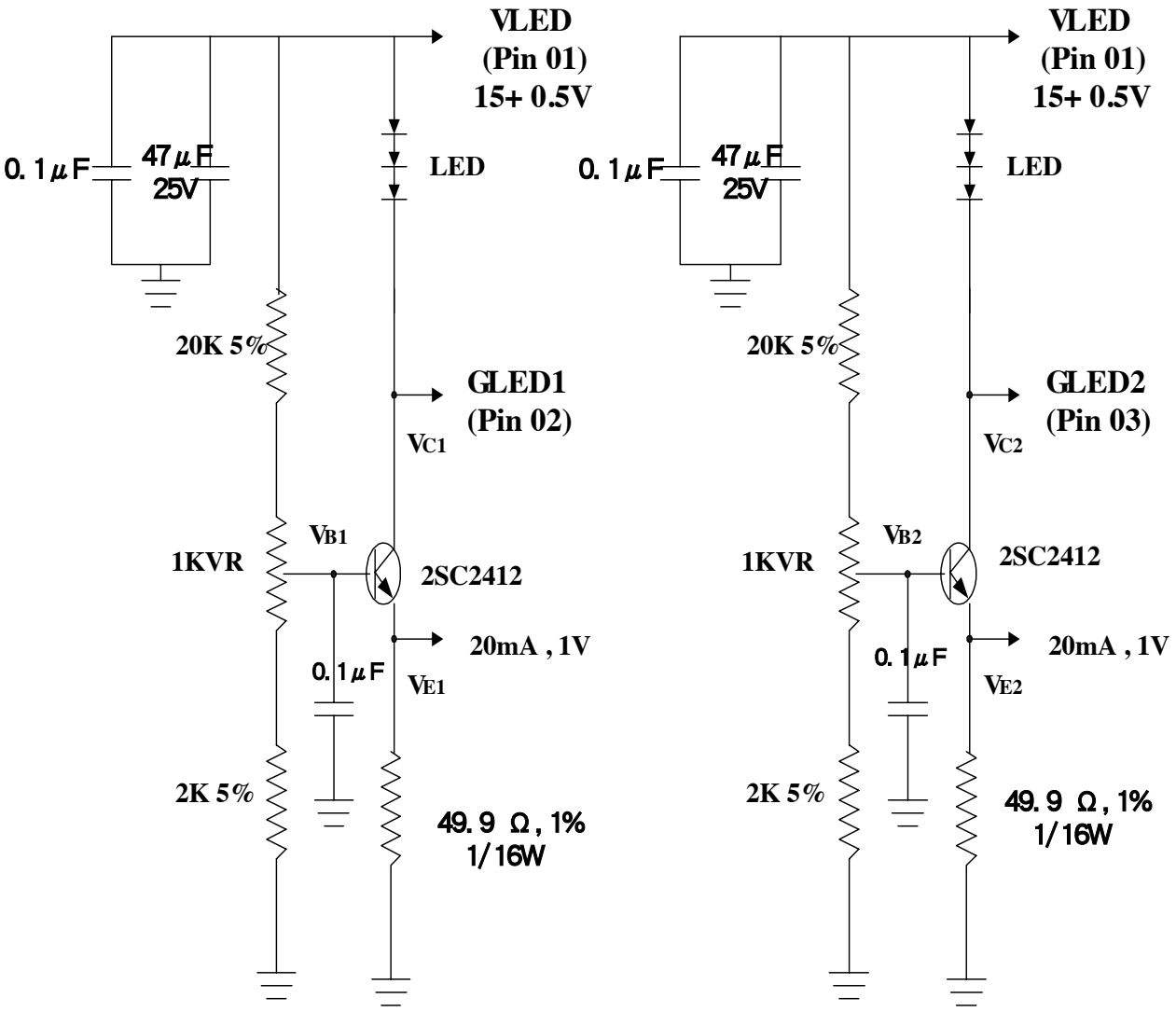
Appendix

CON 2



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