Version :0.1

TECHNICAL SPECIFICATION

MODEL NO : PD035QX2

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Please contact PVI or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐PVI's Confirmation

Dep	FAE	Panel Design	Electronic Design	Mechanical Design	Product Verification	Prepared by
SIGN						

Revision History

Rev.	Eng.	Issued Date	Revised Contents
0.1	Sarah Huang	Nov 19, 2007	Preliminary

TECHNICAL SPECIFICATION
CONTENTS

1.Application

This data sheet applies to a color TFT LCD module, PD035QX2. The module applies to OA product, GPS, which require high quality flat panel display. If you must use in high reliability environment can't over reliability test condition.

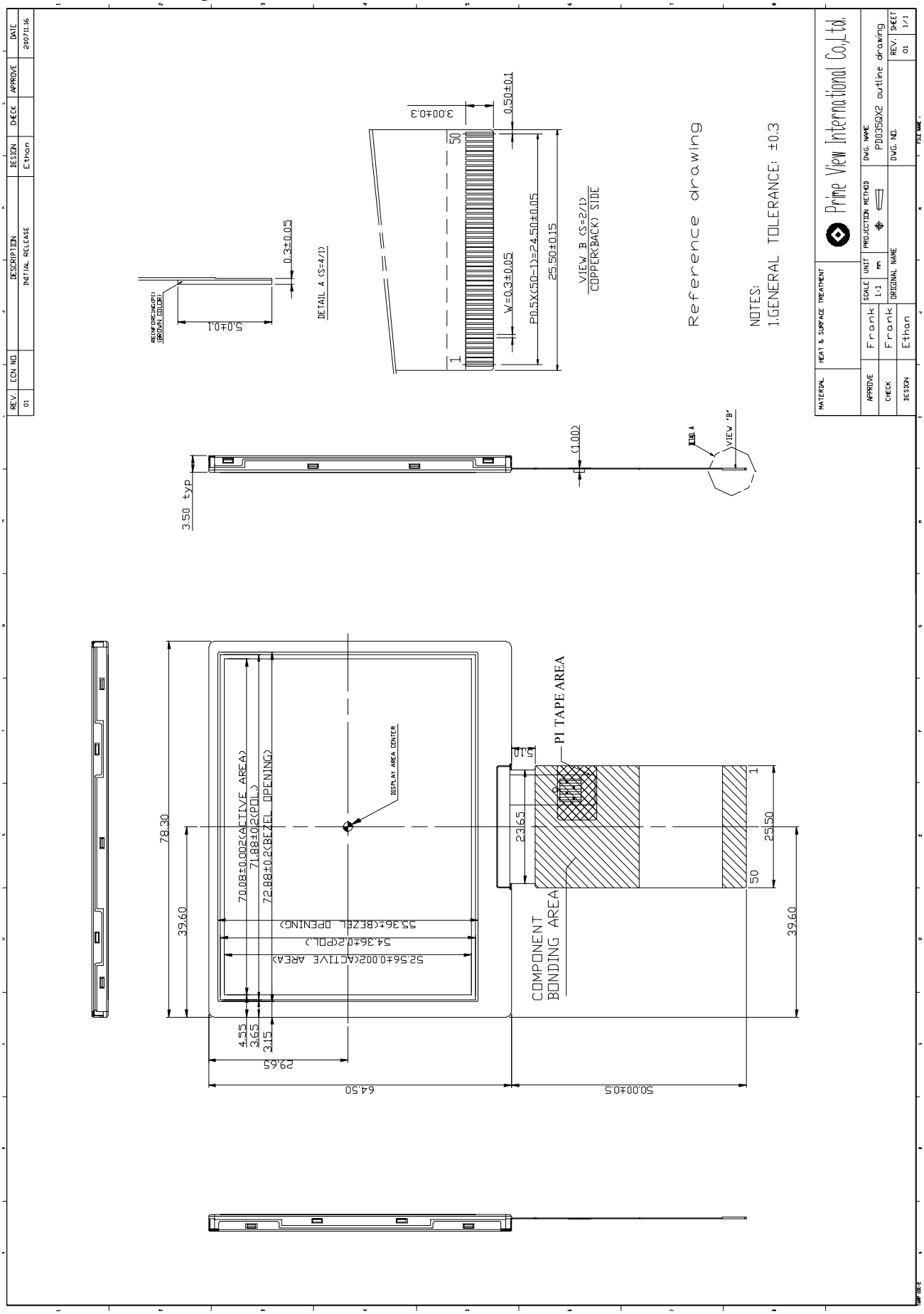
2. Features

. Amorphous silicon TFT LCD panel with LED backlight unit
. Pixel in stripe configuration
. Thin and lightweight
. Display Colors：262K colors
. Optimum Viewing Direction：6 o'clock

3.Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	3.5(diagonal)	inch
Display Format	320×(R, G, B)×240	dot
Display Colors	262K	
Active Area	70.08(H)×52.56(V)	mm
Pixel Pitch	0.219(H)×0.219(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	78.3(H)×64.5(V)×3.5(D)	mm
Weight	TBD	g
Back-light	9-LEDs	
Surface treatment	Anti-glare + EWV	
Display mode	Normally white	
Gray scale inversion direction	6 o'clock [Note 12-1]	

4.Mechanical Drawing of TFT-LCD Module



5.Input / Output Terminals

5-1) TFT-LCD Panel Driving

Pin No.	Symbol	Function	Remark
1	LED+	Supply voltage for LED Backlight	
2	LED-_1	Cathode of LED Backlight	
3	LED-_2	Cathode of LED Backlight	
4	LED-_3	Cathode of LED Backlight	
5	VSS	System Ground	
6	RESB	System Reset	Note 5-1
7	CSB	SPI enable	Note 5-2
8	SCK	SPI clock	
9	SDI	SPI data input	
10	BB0	Blue Data (LSB)	
11	BB1	Blue Data	
12	BB2	Blue Data	
13	BB3	Blue Data	
14	BB4	Blue Data	
15	BB5	Blue Data	
16	BB6	Blue Data	
17	BB7	Blue Data (MSB)	
18	VSS	System Ground	
19	GG0	Green Data (LSB)	
20	GG1	Green Data	
21	GG2	Green Data	
22	GG3	Green Data	
23	GG4	Green Data	
24	GG5	Green Data	
25	GG6	Green Data	
26	GG7	Green Data (MSB)	
27	VSS	System Ground	
28	RR0	Red Data (LSB)	
29	RR1	Red Data	
30	RR2	Red Data	
31	RR3	Red Data	
32	RR4	Red Data	
33	RR5	Red Data	
34	RR6	Red Data	
35	RR7	Red Data (MSB)	
36	VSS	System Ground	
37	DEN	Data enable	Note 5-3
38	HSYNC	Line synchronization signal	Note 5-4
39	VSYNC	Frame synchronization signal	
40	VSS	System Ground	
41	DOTCLK	Clock in	
42	VSS	System Ground	
43	SHUT	Sleep mode work on HI	Note 5-5
44	TB	HI : G0~G239 Low : G239~G0	Note 5-6
45	RL	HI : First RGB data at S0~S2 Low : First RGB data at S959~S957	Note 5-7
46	VSS	System Ground	
47	VDD	Power supply for Logic Circuit	Note 5-8
48	VSSA	Grounding for analog circuit	
49	VDDA	Voltage supply pin for analog circuit	Note 5-9
50	VSSA	Grounding for analog circuit	

Note 5-1: Low active, connect to VDD when not used
Note 5-2: Refer to Serial Interface block. Leave it OPEN when not used.
Note 5-3: Connect to VDD or floating if not used
Note 5-4: Fixed to VDD or floating if not used
Note 5-5: Connect to VDD for sleep mode, VSS for normal operation mode
Note 5-6: Connect to VDD for scan from G0 to G239(normal scan), VSS for G239 to G0(reverse scan)
Note 5-7: Connect to VDD for display first RGB data at S0-S2, VSS for S959-S957
Note 5-8: VDD (Typ.) = +3.3V
Note 5-90: VDDA (Typ.) = +3.3V.Requires a noise free path for providing accurate LCD driving voltage

6.Absolute Maximum Ratings:

The followings are maximum values, which if exceeded, may cause faulty operation or damage to the unit.

Item	Symbol	Value	Unit
Supply voltage (Analog)	VDDA	VSS- 0.3 to 3.6	V
Supply voltage (Logic)	VDD	-0.3 ~ +3.6	V

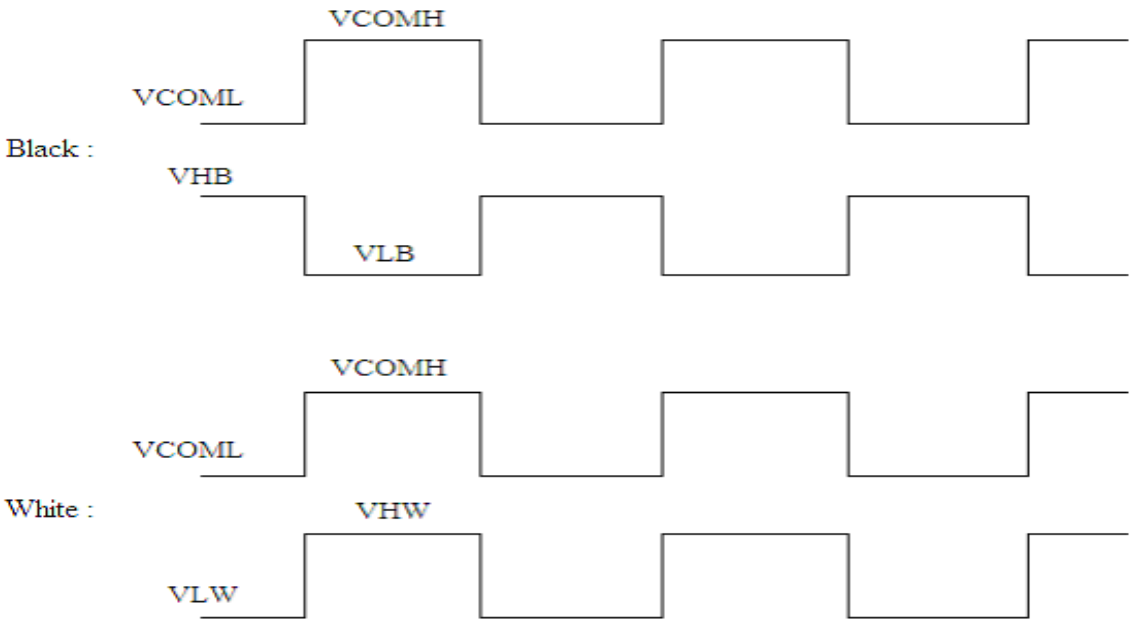
7.Electrical Characteristics

7-1) Recommended Operating Conditions:

Item	Symbol	Min.	Typ.	Max.	Unit	**Remark**
Supply voltage (Analog)	VDDA	-	TBD	-	V	
Supply voltage (Logic)	VDD	-	TBD	-	V	
TFT Common Electrode Voltage	VCOMH	-	TBD	-	V	Note 7-1
	VCOML	-	TBD	-	V	
Black of Video Low Voltage	VLB	-	TBD	-	V	Note 7-2
Black of Video High Voltage	VHB	-	TBD	-	V	
White of Video Low Voltage	VLW	-	TBD	-	V	
White of Video High Voltage	VHW	-	TBD	-	V	

Note7-1：VCOM must be adjusted optimize display quality, crosstalk, contrast ration and etc.

Note7-2：



7-2) Recommended Driving Condition for Back Light

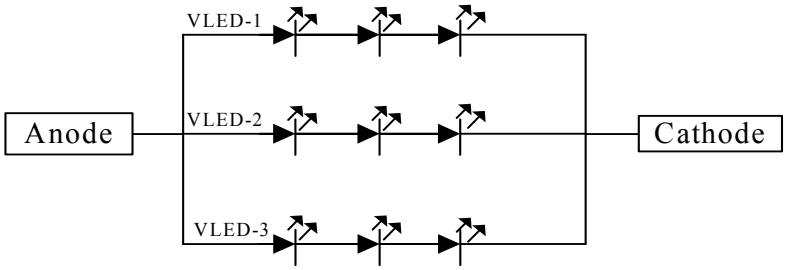
Ta = 25℃

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	V_{LED}	-	-	(10.5)	V	Note 7-3
Supply current of LED backlight	I_{LED}	-	20	-	mA	Note 7-4
Backlight Power Consumption	P_{LED}	-	-	630	mW	Note 7-3/7-5

Note 7-3 : I_{LED}= 20mA,constant current

Note 7-4 : The LED driving condition is defined for each LED module. (3 LED Serial)
Input current = 20mA * 3 = 60mA

Note 7-5 : $P_{LED} = V_{LED-1} * I_{LED-1} + V_{LED-2} * I_{LED-2} \ldots\ldots + V_{LED-3} * I_{LED-3}$



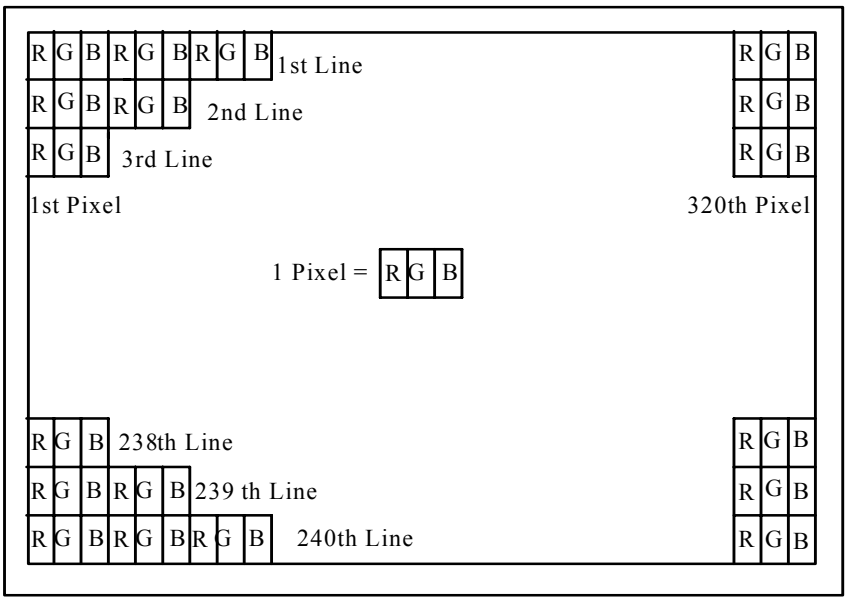
7-3) Power Consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply current for source driver and gate driver	I_{DD}	V_{DD}= TBD V	-	TBD	mA	
Back Light Power Consumption			-	630	mW	
Total Power Consumption			-	TBD	mW	Note 7-6

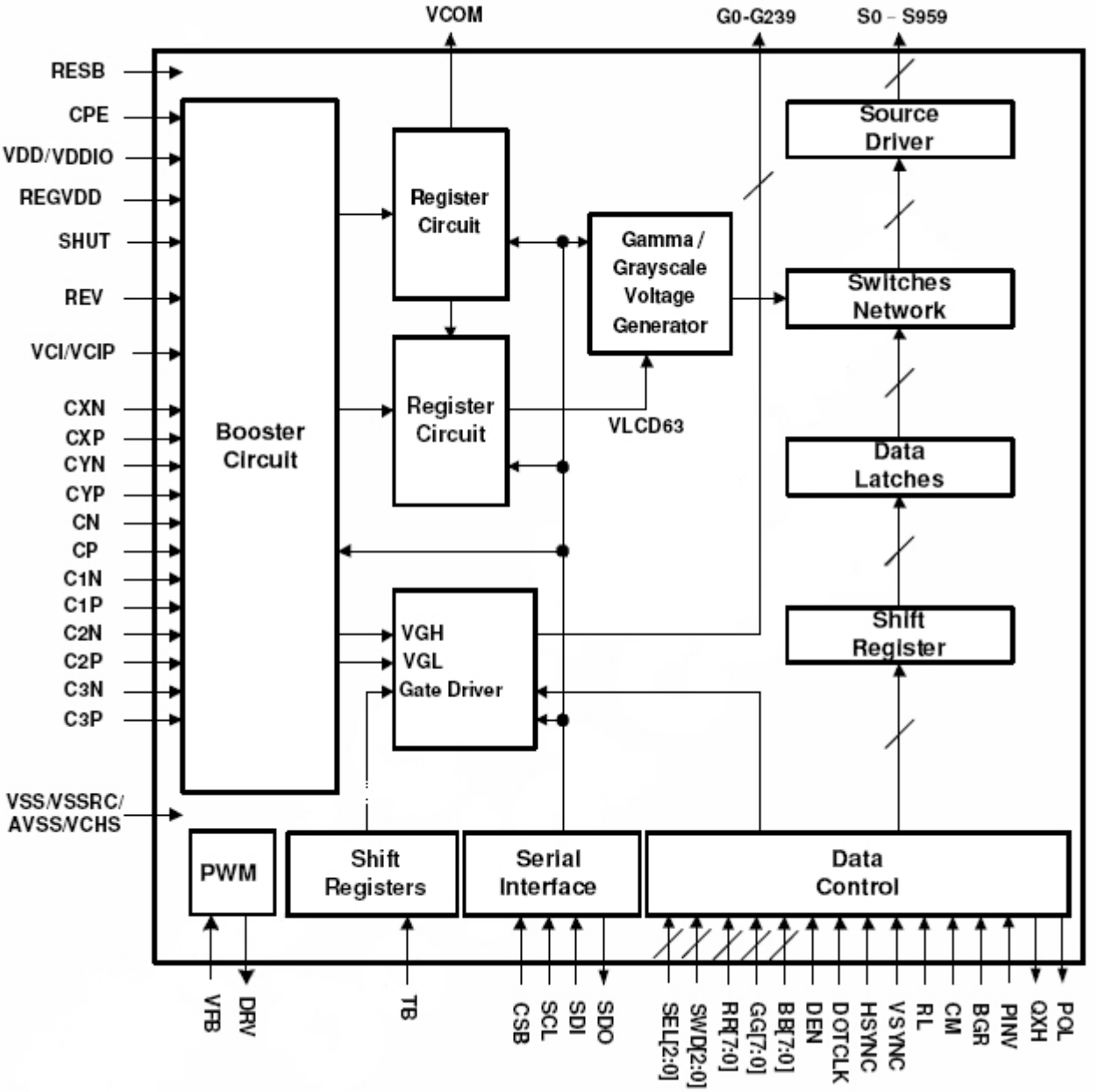
Note 7-6: Back light power consumption is calculated by $I_L \times V_L$.

8. Pixel Arrangement

The LCD module pixel arrangement is the stripe.



9. Block Diagram



10. AC Characteristics

(Unless otherwise specified, Voltage Referenced to Vss, VDD = 3.3V, TA = 25℃)

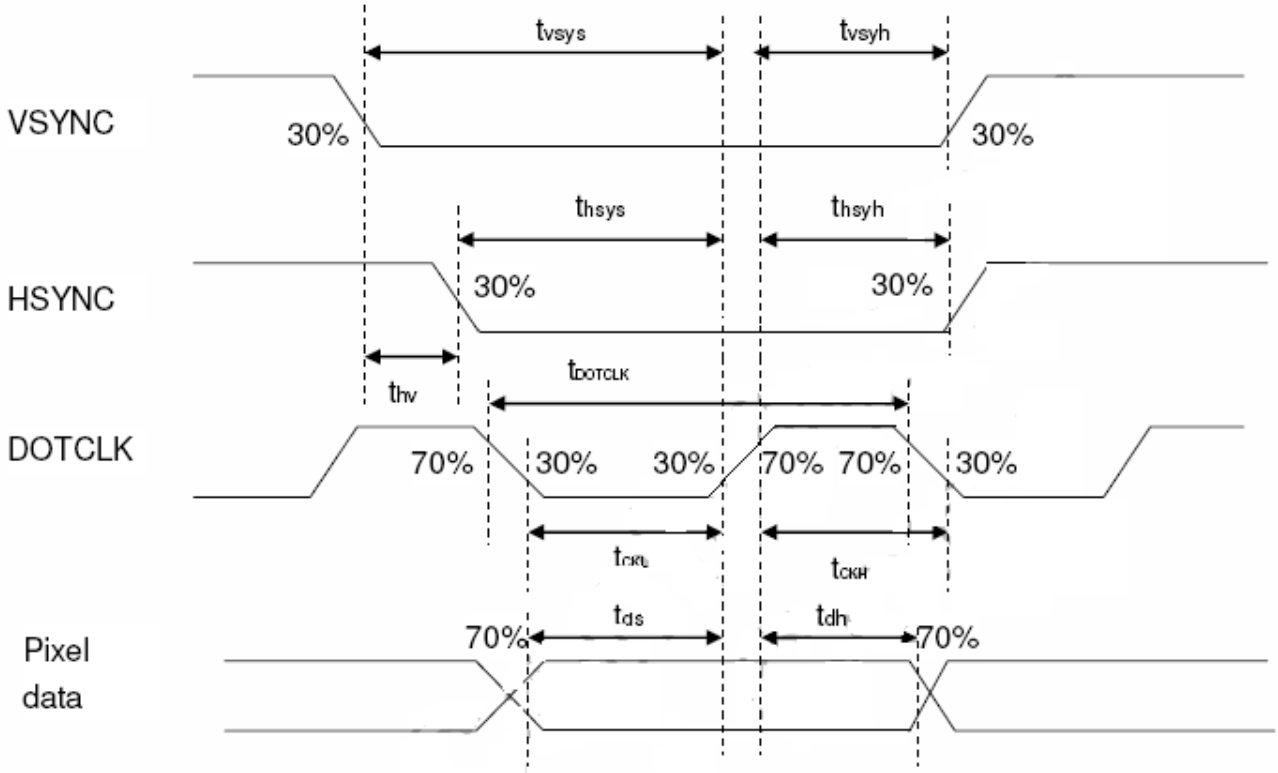


Figure 10.1 Pixel Timing

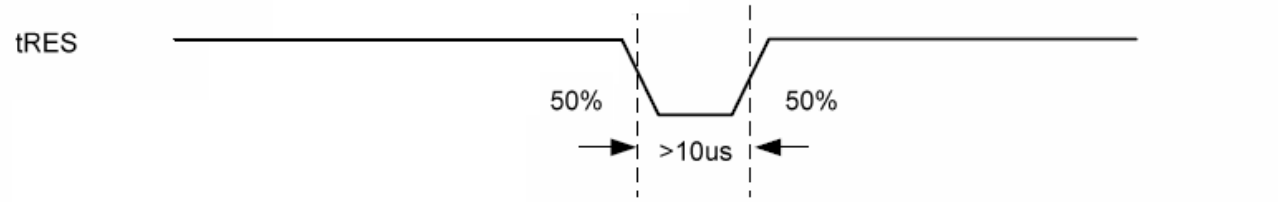
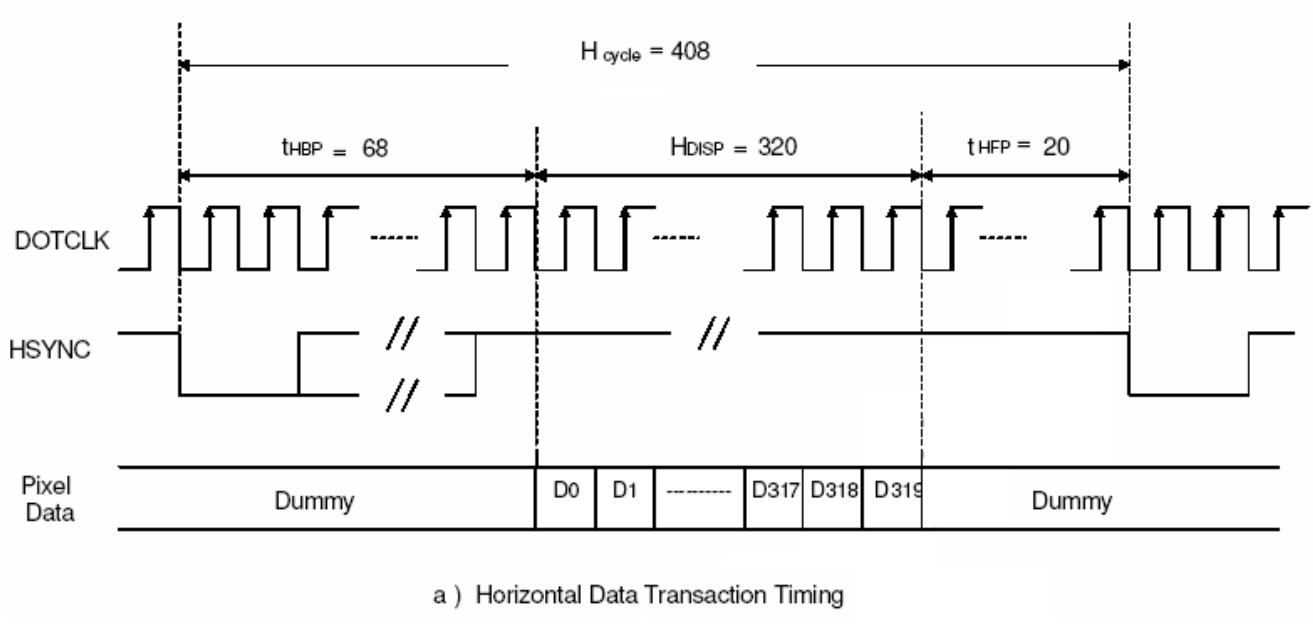


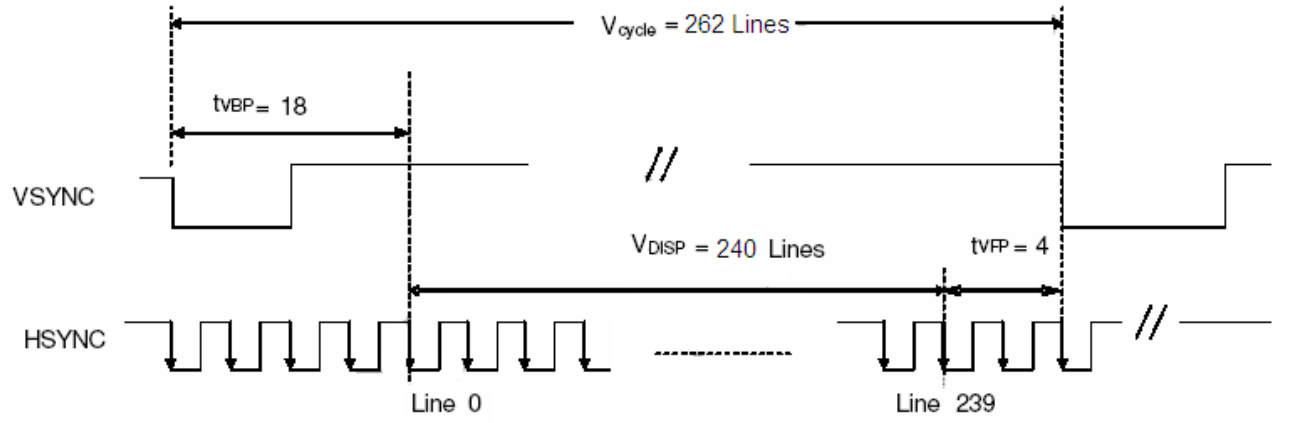
Figure 10. 2 tRES Timing

Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	fDOTCLK	-		6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Vertical Sync Setup Time	tvsys	20	10	-	-	-	-	ns
Vertical Sync Hold Time	tvsyh	20	10	-	-	-	-	ns
Horizontal Sync Setup Time	thsys	20	10	-	-	-	-	ns
Horizontal Sync Hold Time	thsyh	20	10	-	-	-	-	ns
Phase difference of Sync Signal Falling Edge	thv	1		-		240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-	-	-	-	ns
DOTCLK High Period	tCKH	50	15	-	-	-	-	ns
Data Setup Time	tds	12	8	-	-	-	-	ns
Data hold Time	tdh	12	8	-	-	-	-	ns
Reset pulse width	tRES	10		-		-		us

Table 10.1 Pixel & tRES Timing



a) Horizontal Data Transaction Timing



b) Vertical Data Transaction Timing

Figure 10.3 Data Transaction Timing in Parallel RGB (24 bit) Interface (SYNC Mode)

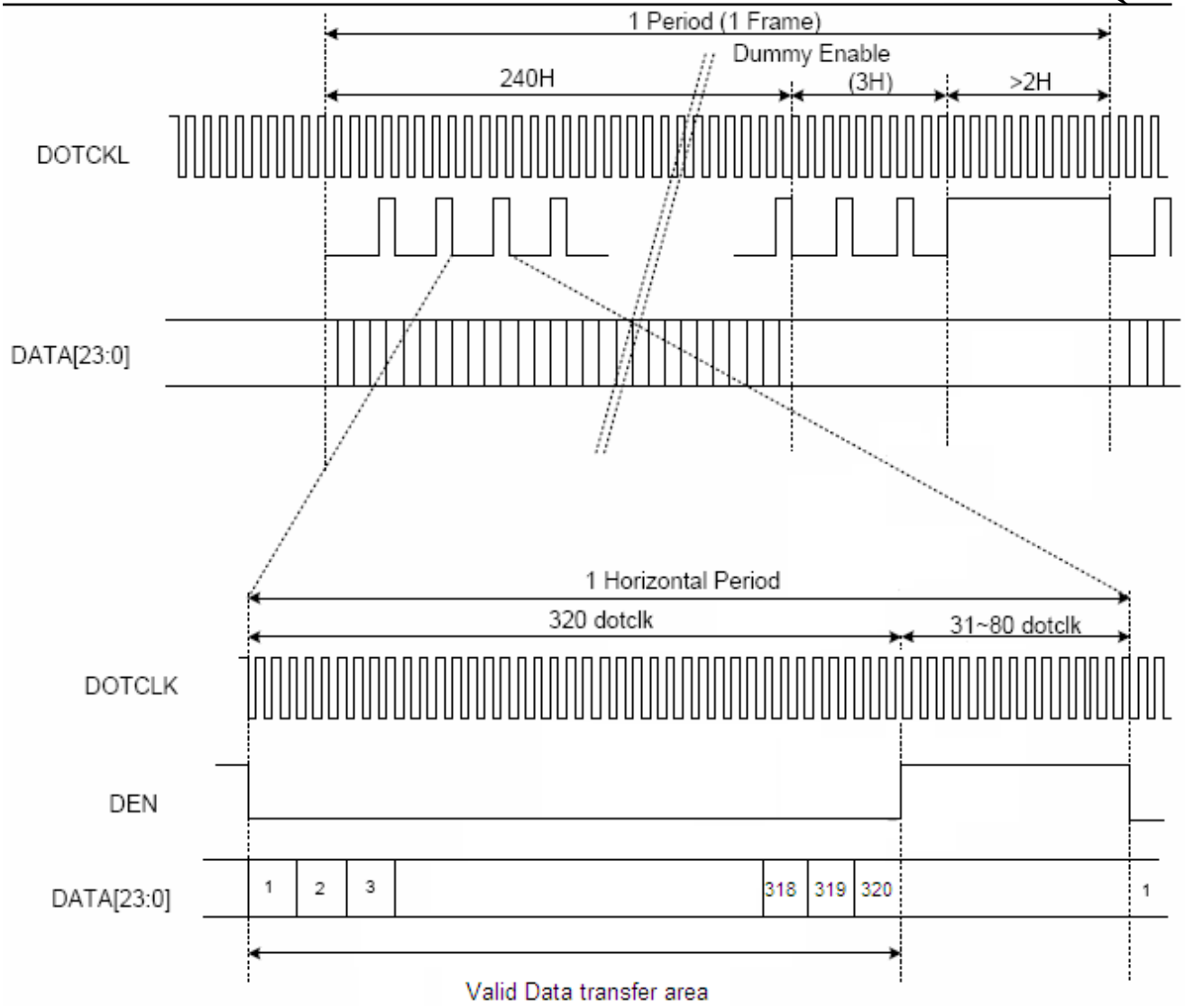


Figure 10. 4 Data Transaction Timing in Parallel RGB (24 bit) Interface (DE Mode)

Characteristics		Symbol	Min.		Typ.		Max.		Unit
			24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency		tDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period		tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Frequency (Line)		fH	-		15.72		22.35		KHz
Vertical Frequency (Refresh)		fV	-		60		90		Hz
Horizontal Back Porch		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Front Porch		tHFP	-	-	20	60	-	-	tDOTCLK
Horizontal Data Start Point		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Blanking Period		tHBP + tHFP	-	-	88	264	-	-	tDOTCLK
Horizontal Display Area		HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle		Hcycle	-	-	408	1224	450	1350	tDOTCLK
Vertical Back Porch		tVBP	-		18		-		Lines
Vertical Front Porch		tVFP	-		4		-		Lines
Vertical Data Start Point		tVBP	-		18		-		Lines
Vertical Blanking Period		tVBP + tVFP	-		22		-		Lines
VS pulse width		tWV	-		4		-		Lines
Vertical Display Area	NTSC	VDISP	-		240		-		Lines
	PAL				280(PALM=0)				
					288(PALM=1)				
Vertical Cycle	NTSC	Vcycle	-		262		350		Lines
	PAL				313				

Table 10. 2 Data Transaction Timing in Normal Operating Mode

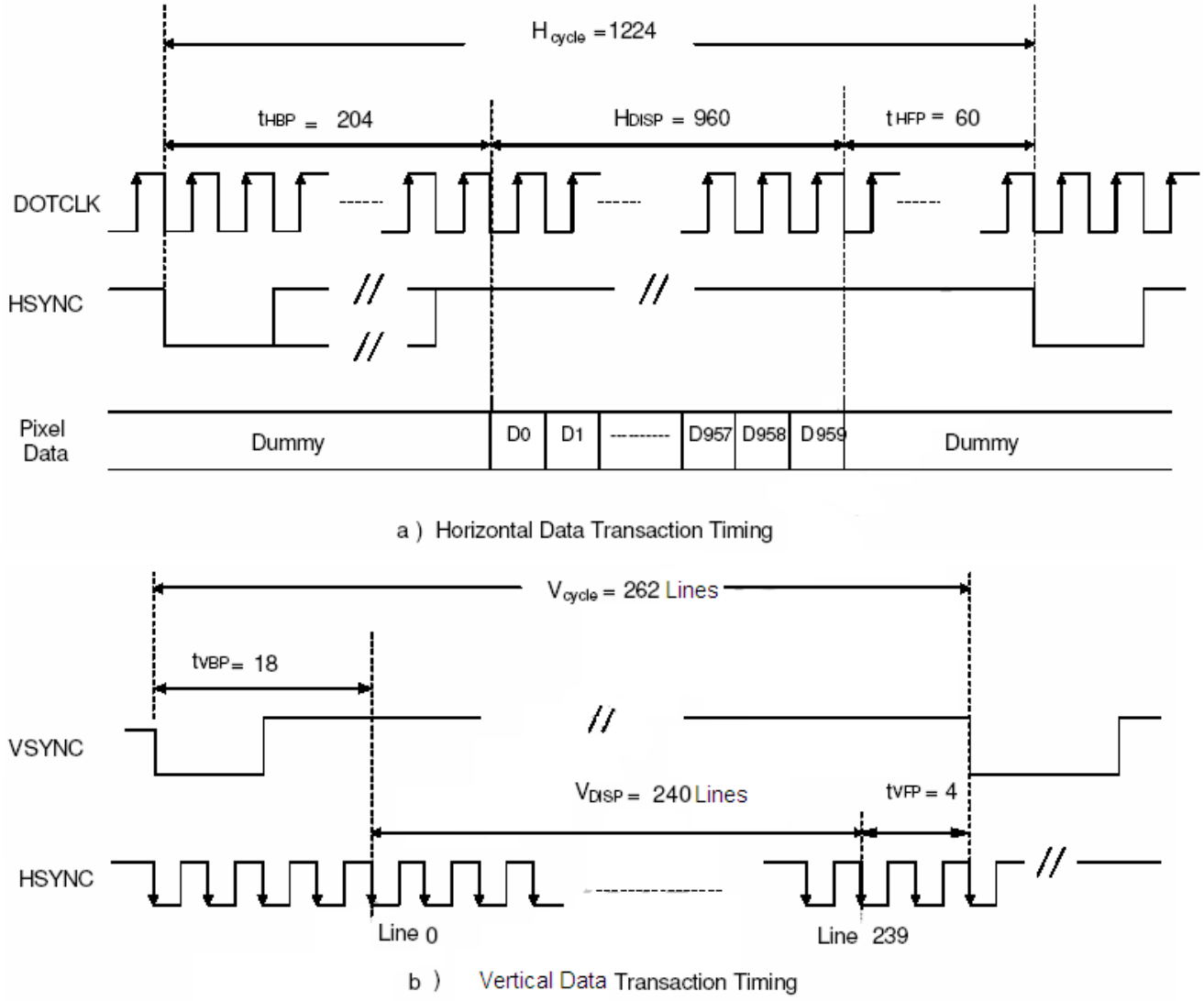


Figure 10.5 Data Transaction Timing in Serial RGB (8 bit) Interface (SYNC Mode)

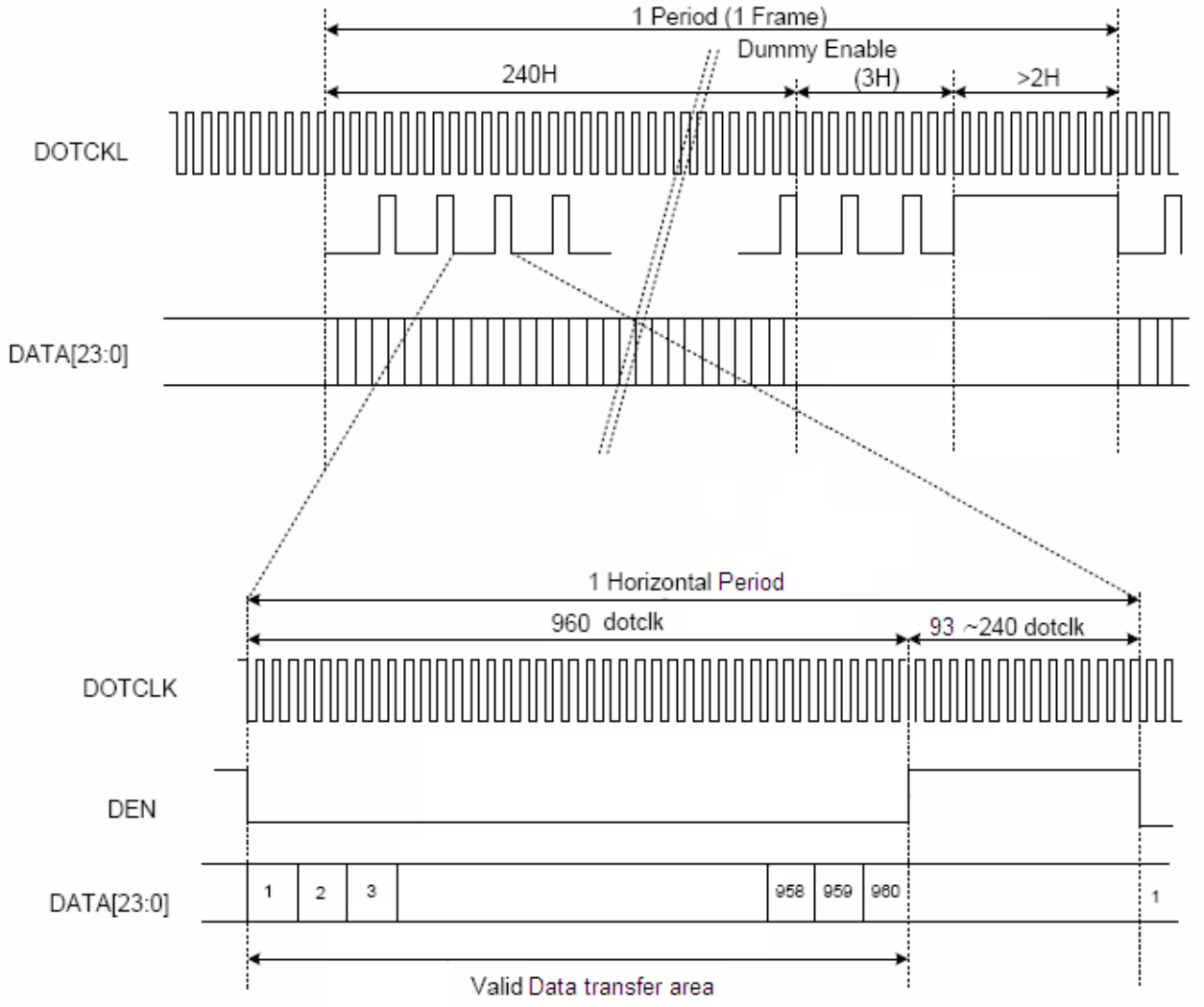
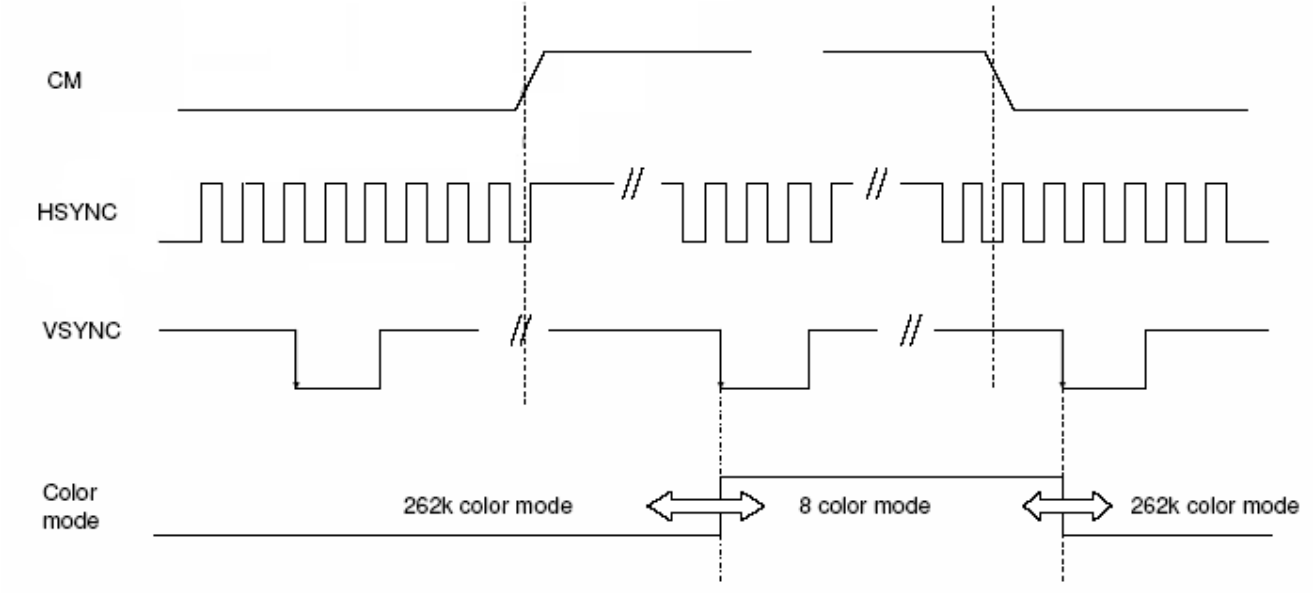


Figure 10. 6 Data Transaction Timing in Serial RGB (8 bit) Interface (DE Mode)



Note: The color mode conversion starts at the first falling edge of VSYNC after stage change of CM.

Figure 10. 7 Color Mode Conversion Timing

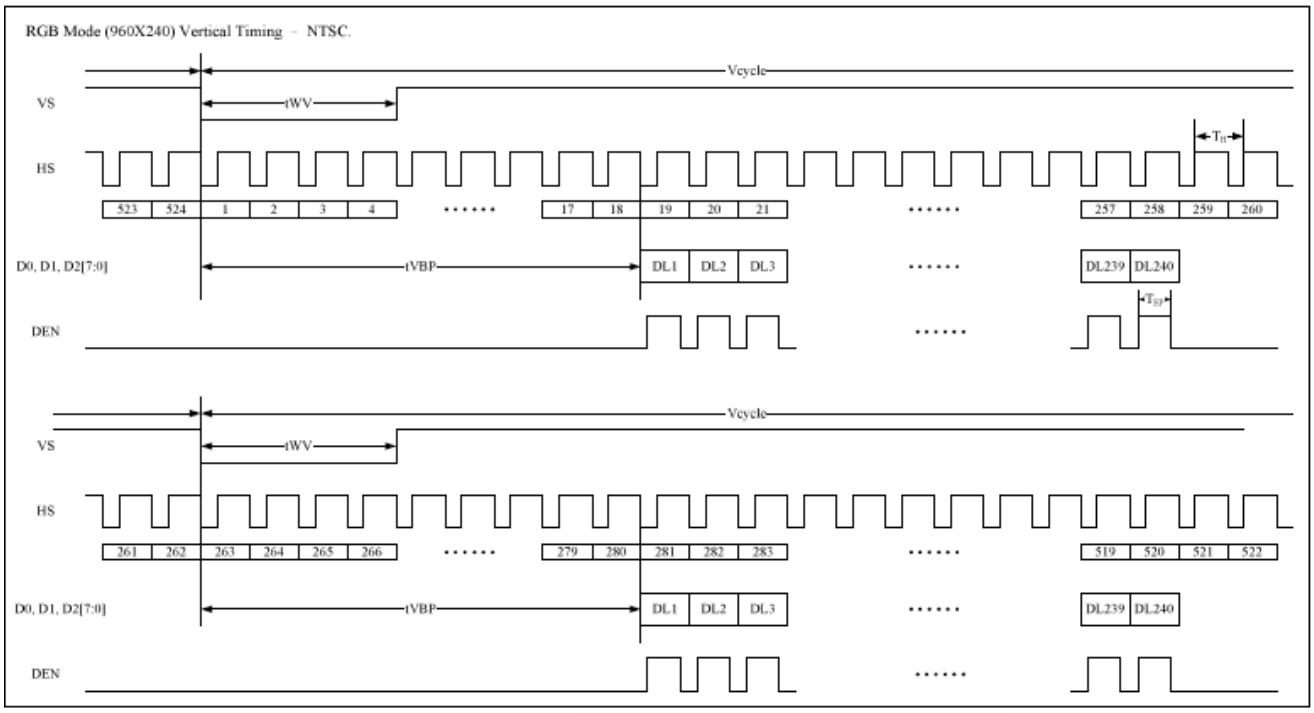


Figure 10. 8 Digital RGB NTSC mode Vertical Data Format for $262T_H$

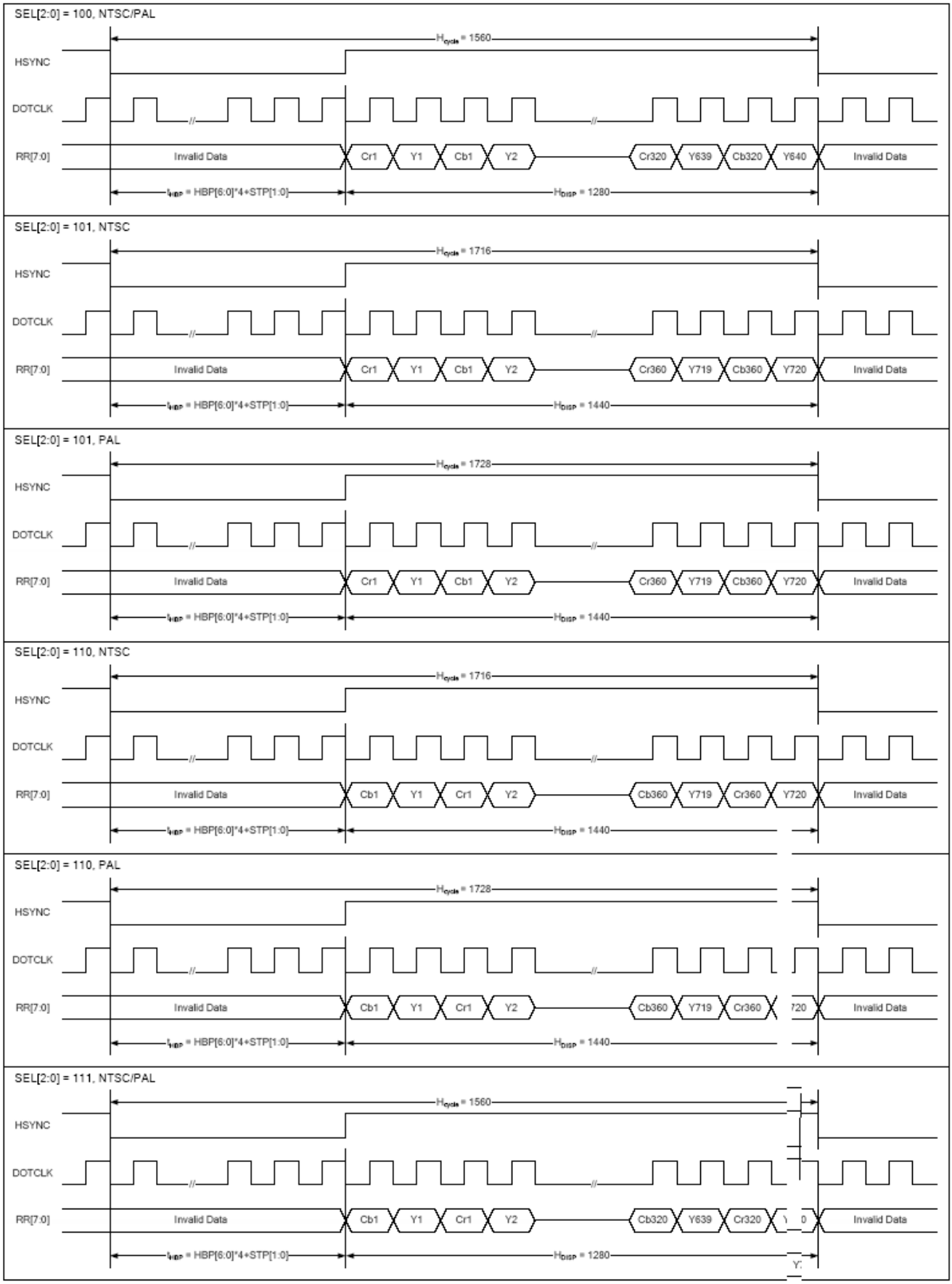


Figure 10. 9 CCIR601 Horizontal Timing

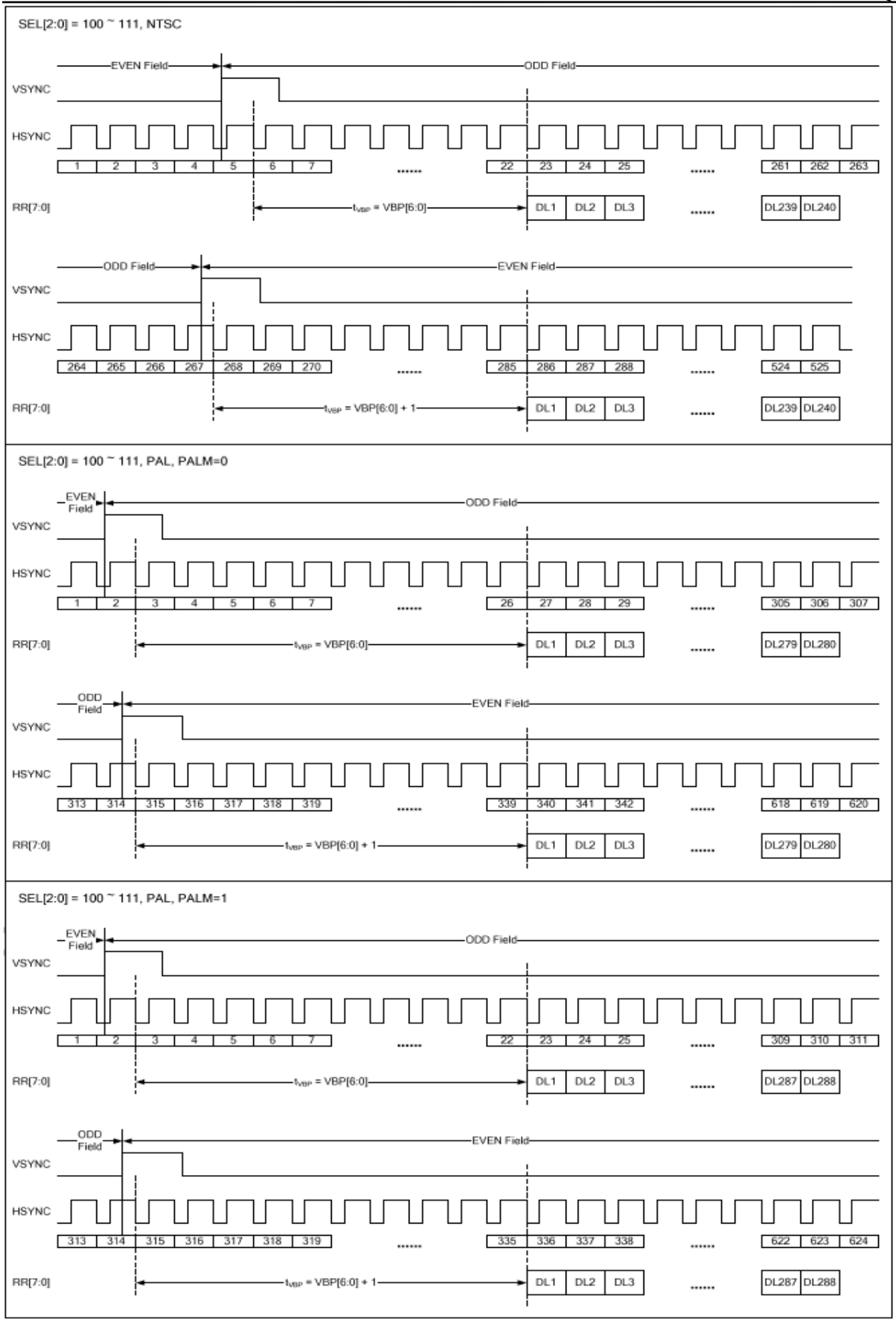


Figure 10. 10 CCIR601 Vertical Timing

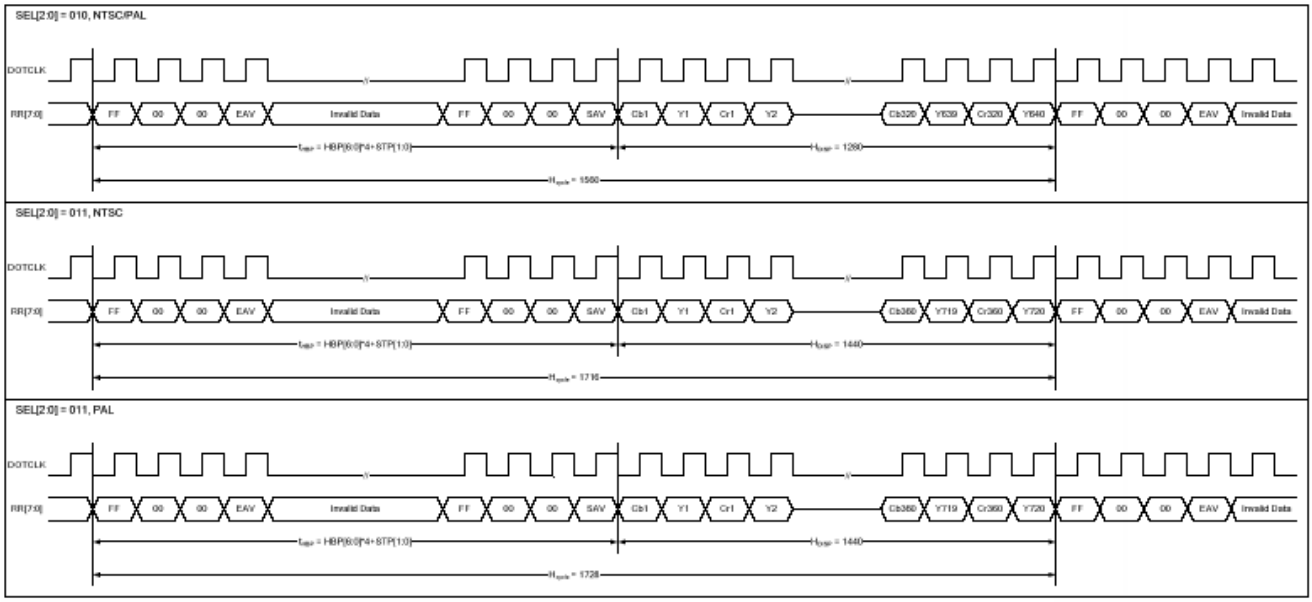


Figure 10. 11 CCIR656 Horizontal Timing

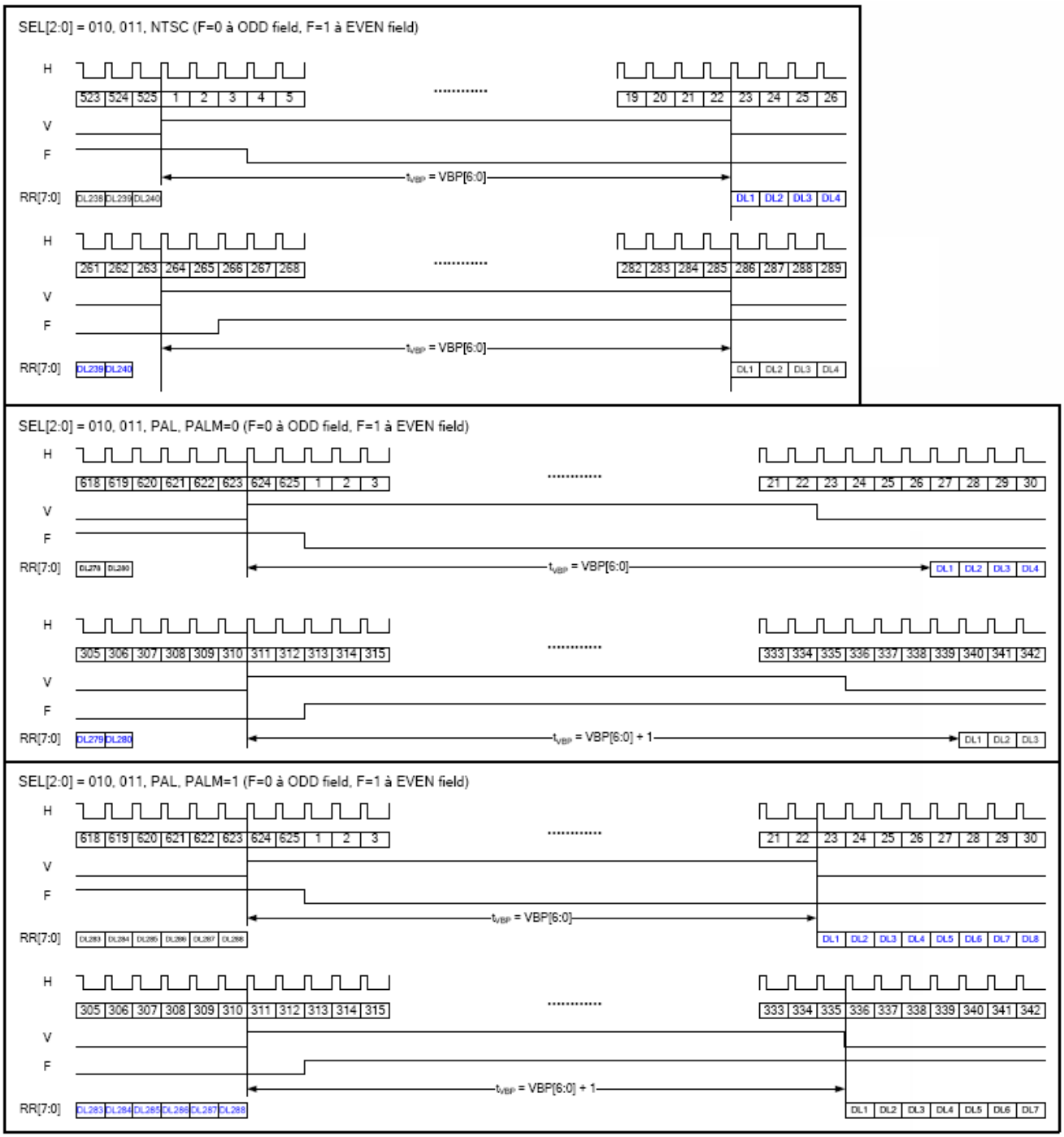
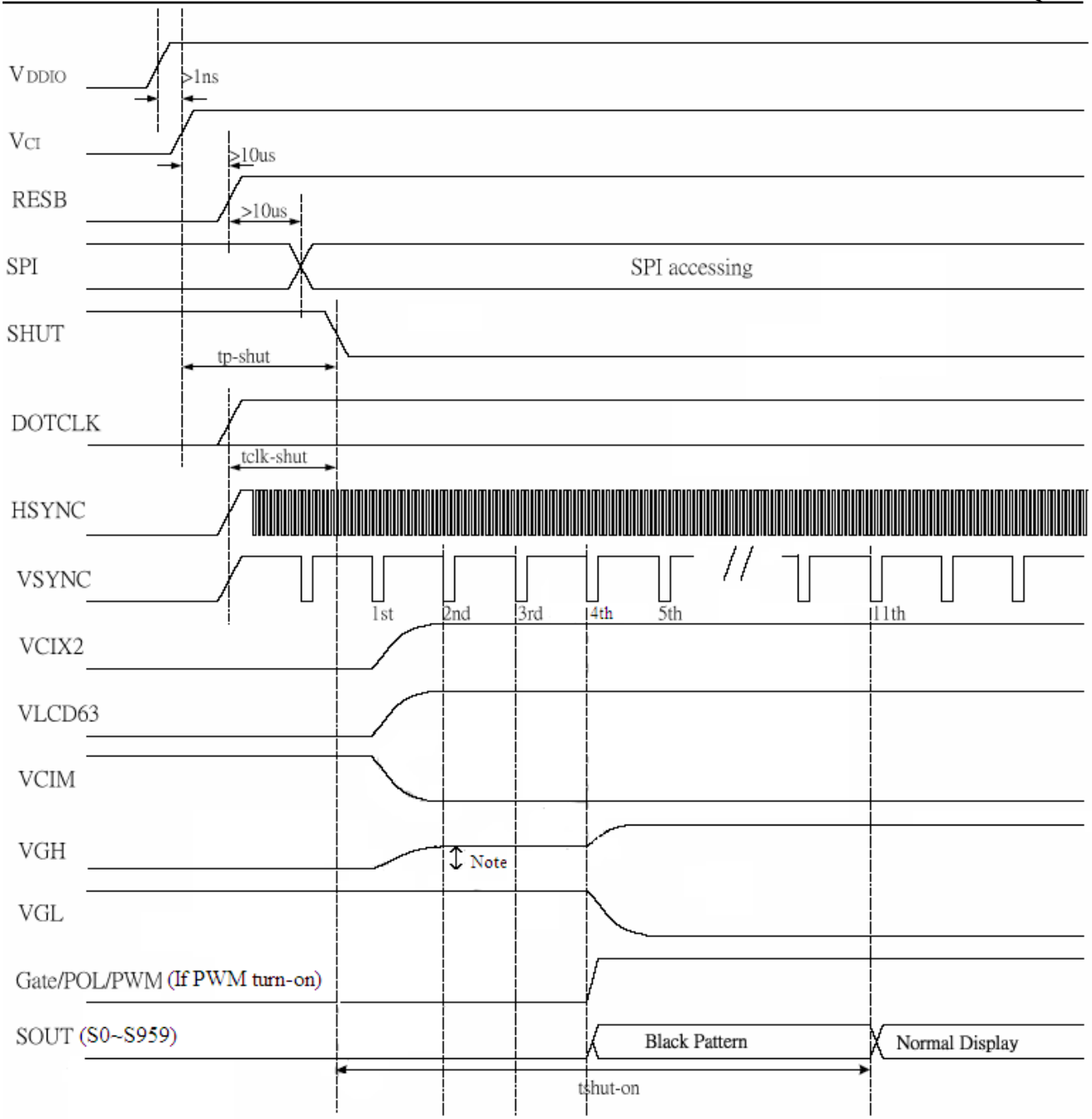


Figure 10. 12 CCIR656 Vertical Timing



Note: There is a diode between VCIX2 and VGH. Switch on VCIX2 will move VGH up.

Figure 10. 13 Power Up Sequence

Characteristics	Symbol	Min.	Typ.	Max.	Unit
VCI/ VDDIO on to falling edge of SHUT	tp-shut	1	-	-	us
DOTCLK to falling edge of SHUT	tclk-shut (Note1)	1	-	-	clk
Falling edge of SHUT to display start - 1 line: 408 clk - 1 frame: 262 line -DOTCLK = 6.5MHz	tshut-on (Note2)	-	-	11	frame

Table 10. 3 Power Up Sequence

Note1: It is necessary to input DOTCLK before the falling edge of SHUT.
Note2: Display starts at 11th falling edge of VSTNC after the falling edge of SHUT. The display starts at the falling edge of VSYNC which is determined by BLT[1:0] of R04h.

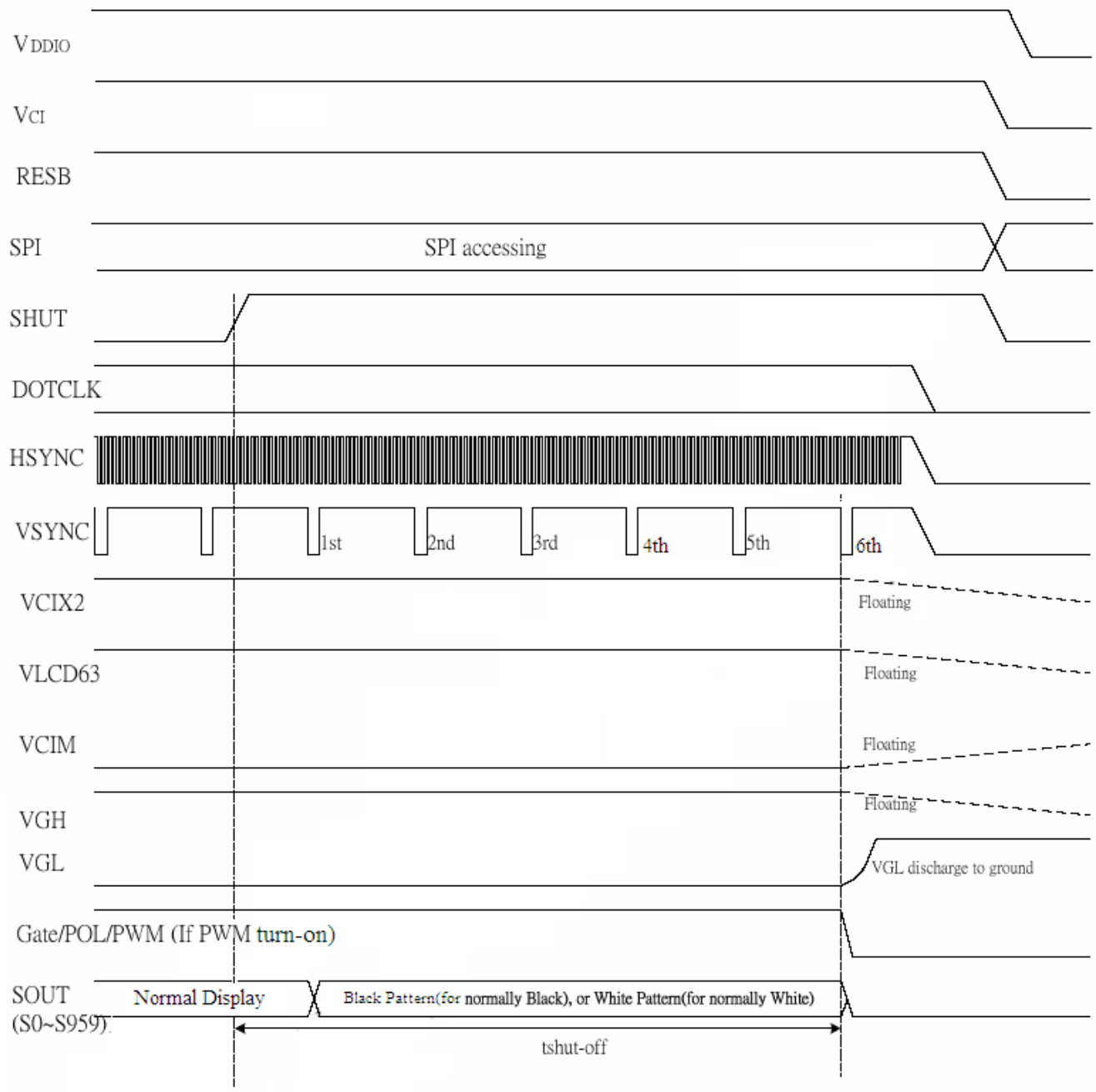


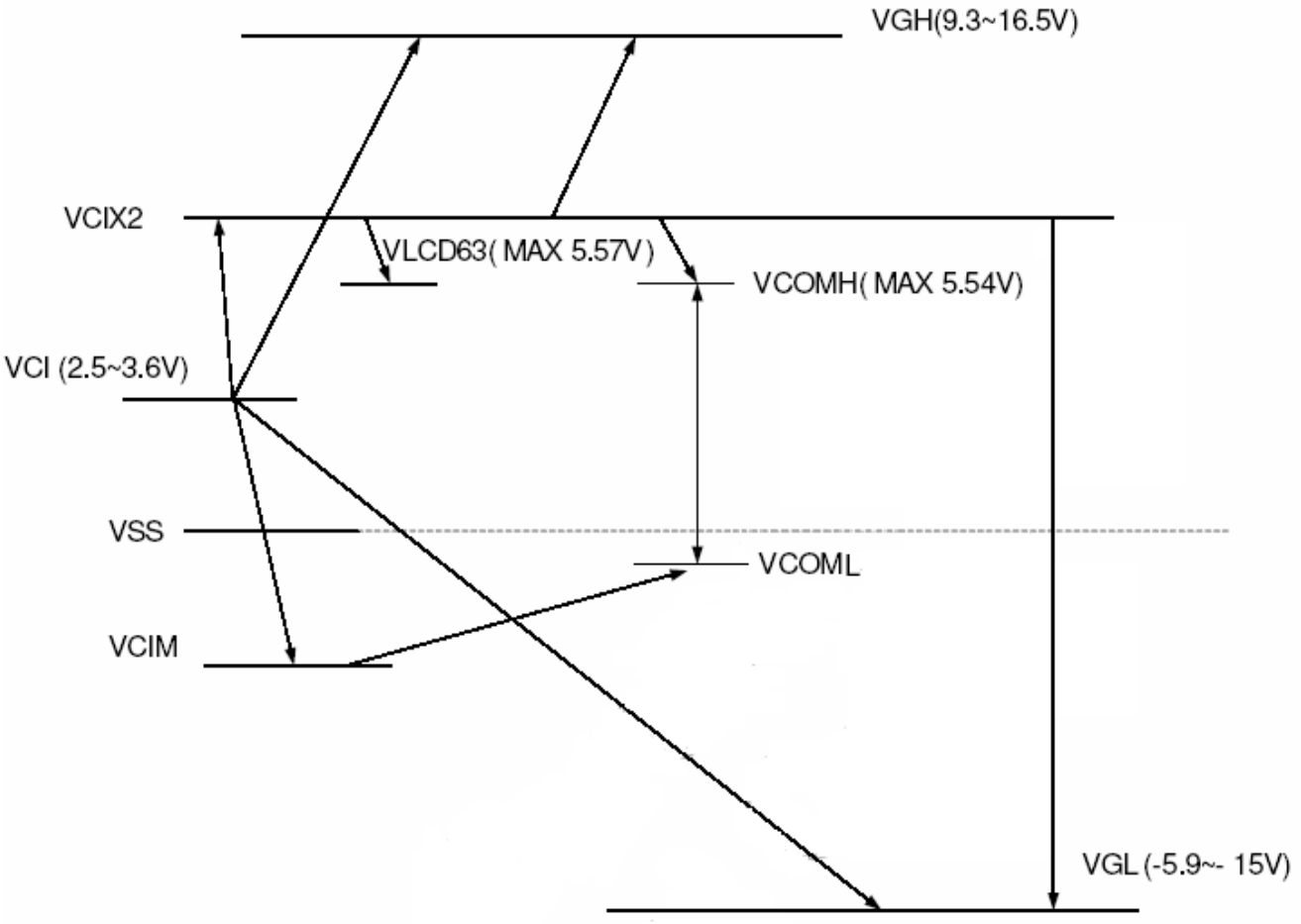
Figure 10. 14 Power Down Sequence

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Rising edge of SHUT to display off - 1 line: 408 clk - 1 frame: 262 line - DOTCLK = 6.5MHz	tshut-off	-	-	6	frame

Note: DOTCLK must be maintained at lease 6 frames after the rising edge of SHUT.
Display become off at the 6nd falling edge of VSTNC after the falling edge of SHUT.
If RESET signal is necessary for power down, provide it after the 6-frames-cycle of the SHUT period.

Table 10. 4 Power Down Sequence

11. Power On Sequence



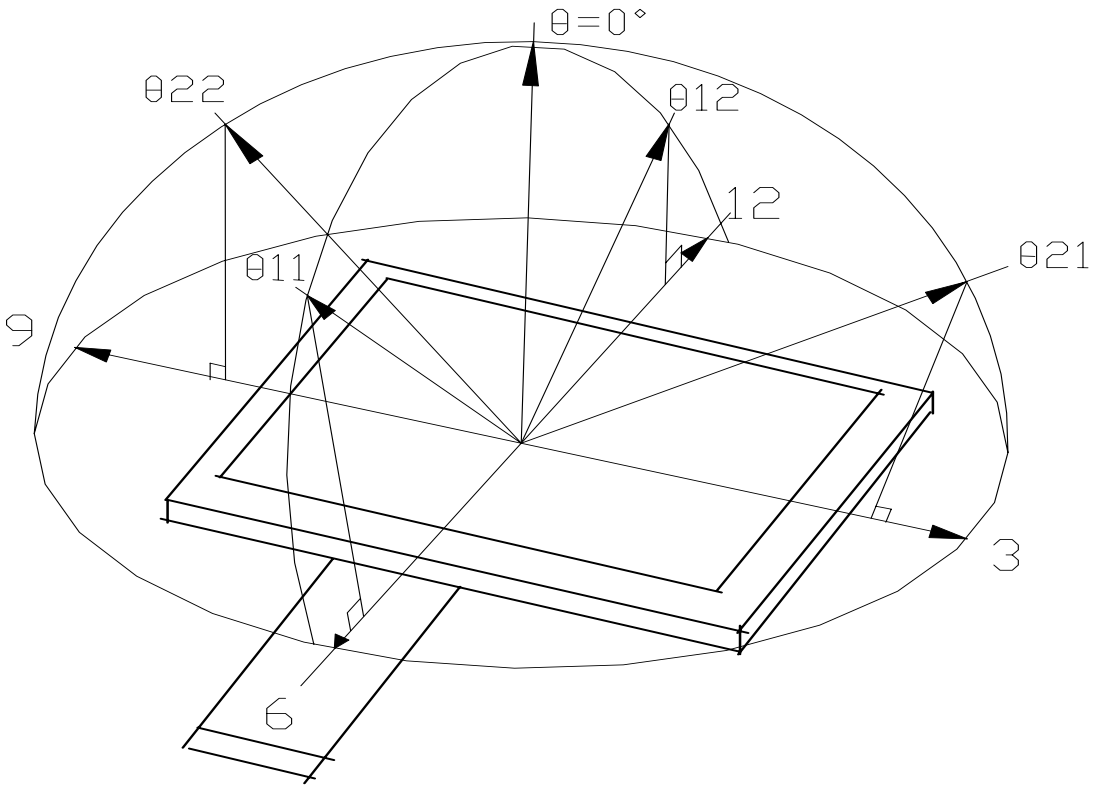
12. Optical Characteristics

12-1) Specification:

Ta=25℃

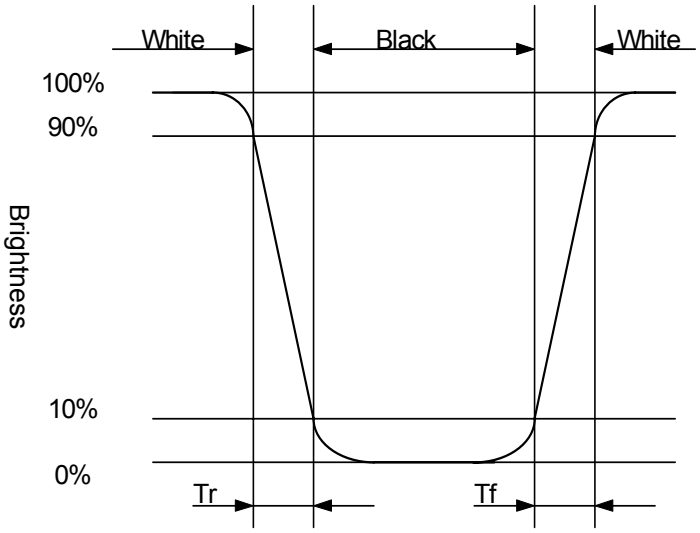
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ (Horizontal)	CR＞10	55	60	--	deg	Note 12-1
	Vertical	θ (12 o'clock)		35	40	--	deg	
		θ (6 o'clock)		50	55	--	deg	
Contrast Ratio		CR		--	400	--	-	Note 12-2
Response time	Rise	Tr	θ =0°	--	15	30	ms	Note 12-3
	Fall	Tf		--	25	50	ms	
Brightness		L	θ =0°/ ϕ =0	--	450	-	cd/㎡	Note 12-4
Luminance Uniformity		U	-	--	TBD	--	%	Note 12-6
White Chromaticity		x	θ =0°/ ϕ =0	--	TBD	--	-	
		y		--	TBD	--	-	
LED Life Time			+25℃	20000	--	--	hrs	Note 12-5
Cross Talk			θ =0°	--	--	3.5	%	Note 12-7

Note 12-1: The definitions of viewing angles are as follow



Note 12-2: The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 12-3: Definition of Response Time Tr and Tf



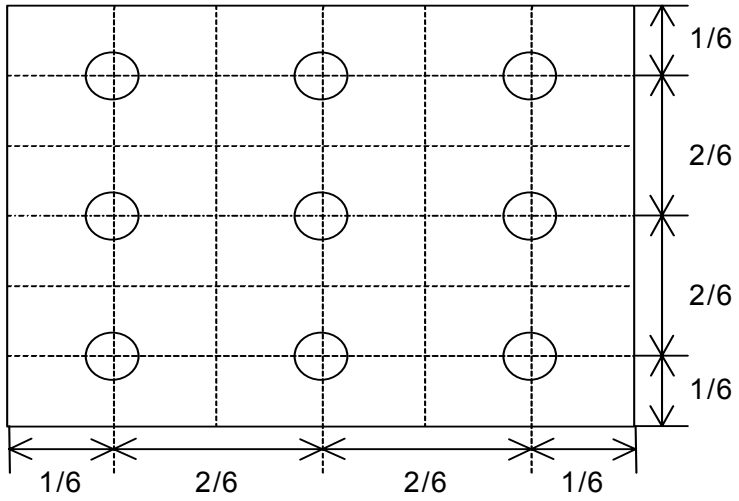
Note 12-4: Topcon BM-5A or BM-7 fast luminance meter 1°field of view is used in the testing

Note 12-5: The "LED Life time " is defined as the module brightness decrease to 50% original Brightness that the ambient temperature is 25℃ and I_{LED} =20mA.

Note 12-6: The uniformity of LCD is defined as

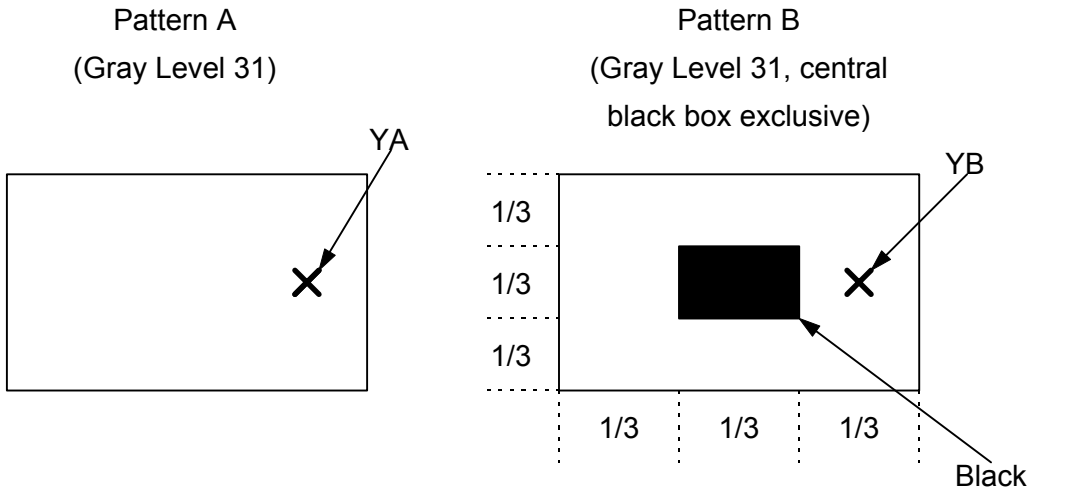
$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

Luminance meter : BM-5A or BM-7 fast(TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module
The test pattern is white (Gray Level 63).



Note 12-7: Cross Talk (CTK) = $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A
YB: Brightness of Pattern B
Luminance meter : BM 5A or BM-7 fast (TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module



13. Handling Cautions

13-1) Mounting of module

a) Please power off the module when you connect the input/output connector.
b) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
c) Protective film (Laminator) is applied on surface to protect it against scratches and dirt's. It is recommended to peel off the laminator before use and taking care of static electricity.

13-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

13-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

13-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
b) Store the module at a room temperature place.
c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
e) Observe all other precautionary requirements in handling general electronic components.
f) Please adjust the voltage of common electrode as material of attachment by 1 module.

13-5) Polarizer mark

The polarizer mark is to describe the direction of wide view angle film how to mach up with the rubbing direction.

14. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = 95℃, 240 hrs
2	Low Temperature Storage Test	Ta = -40℃, 240 hrs
3	High Temperature Operation Test	Ta = 85℃, 240 hrs
4	Low Temperature Operation Test	Ta = -30℃, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = 60℃, 90%RH, 240 hrs (No Condensation)
6	Thermal Cycling Test (non-operating)	-25℃→70℃, 200 Cycles 30min 30min
7	Vibration Test (non-operating)	Frequency：10 ~ 55 H_Z, Amplitude：1 mm Sweep time: 11 min Test Period: 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
9	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal

Ta: ambient temperature

Note : The protective film must be removed before temperature test.

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image).All the cosmetic specification is judged before the reliability stress.

15. Packing Diagram

TBD