## TECHNICAL SPECIFICATION

## MODEL NO : PD040QX1

The content of this information is subject to be changed without notice.
Please contact PVI or its agent for further information.
$\square$ Customer's Confirmation

Customer

Date

By
$\square$ PVI's Confirmation



## Revision History

| Rev. | Issued $\quad$ Date | Revised Contents |
| :--- | :--- | :--- |
| 1.0 | December, 5, 2007 | New |
|  |  | Add |
|  |  | Page 29 15.Handling Cautions <br> $15-1$ item D) |
| 2.0 | March.24.2008 |  |
|  |  | Modify Page 4 3. Mechanical Specifications <br> Page 9 Note 5-2 |

## TECHNICAL SPECIFICATION CONTENTS

| NO. | ITEM | PAGE |
| :---: | :---: | :---: |
| - | Cover | 1 |
| - | Revision History | 2 |
| - | Contents | 3 |
| 1 | Application | 4 |
| 2 | Features | 4 |
| 3 | Mechanical Specifications | 4 |
| 4 | Mechanical Drawing of TFT-LCD module | 5 |
| 5 | Input / Output Terminals | 6 |
| 6 | Absolute Maximum Ratings | 10 |
| 7 | Electrical Characteristics | 10 |
| 8 | Pixel Arrangement | 11 |
| 9 | Display Color and Gray Scale Reference | 12 |
| 10 | Operation description | 13 |
| 11 | AC Characteristics | 21 |
| 12 | Waveform | 22 |
| 13 | Power On Sequence | 26 |
| 14 | Optical Characteristics | 36 |
| 15 | Handling Cautions | 29 |
| 16 | Reliability Test | 30 |
| 17 | Block Diagram | 31 |
| 18 | Packing | 32 |

## 1. Application

This data sheet applies to a color TFT LCD module, PD040QX1.This module applies to OA product(must use Analog to Digital driving board), which requires high quality flat panel display. If you must use in severe reliability environments, please don't extend over PVI's reliability test conditions.

## 2. Features

. Amorphous silicon TFT LCD panel with LED back-light unit
Pixel in stripe configuration
. Slim and compact, designed for O/A application
TTL transmission interface
3. Mechanical Specifications

| Parameter | Specifications | Unit |
| :---: | :---: | :---: |
| Screen Size | $4($ diagonal $)$ | inch |
| Display Format | $320 \times(\mathrm{RGB}) \times 240$ | dot |
| Active Area | $81.12(\mathrm{H}) \times 60.84(\mathrm{~V})$ | mm |
| Pixel Pitch | $0.2535(\mathrm{H}) \times 0.2535(\mathrm{~V})$ | mm |
| Pixel Configuration | Stripe |  |
| Display Colors | 16.7 M |  |
| Surface Treatment | Anti-Glare +EWV |  |
| Back-light | $8-\mathrm{LEDs}$ | mm |
| Outline Dimension | $93.00(\mathrm{~W}) \times 73.50(\mathrm{H}) \times 4.9(\mathrm{D})(\mathrm{typ})$. | g |
| Weight | $46 \pm 5$ |  |
| Display mode | Normally white | o'clock |
| Gray scale inversion direction | 6 <br> (ref to Note $14-1)$ |  |

4. Mechanical Drawing of TFT-LCD Module


The information contained herein is the exclusive property of Prime View International Co., Ltd. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Prime View International Co., Ltd.PAGE:5

PD040QX1
5. Input / Output Terminals

5-1) TFT-LCD Panel Driving
FPC Down Connect, 30 Pins, Pitch: 0.5 mm
CN 1

| Pin No. | Symbol | Function | Remark |
| :---: | :---: | :---: | :---: |
| 1 | D27(B7) | Blue Data | Note 5-1 |
| 2 | D26(B6) | Blue Data |  |
| 3 | D25(B5) | Blue Data |  |
| 4 | D24(B4) | Blue Data |  |
| 5 | D23(B3) | Blue Data |  |
| 6 | D22(B2) | Blue Data |  |
| 7 | D21(B1) | Blue Data |  |
| 8 | D20(B0) | Blue Data |  |
| 9 | GND | Digital ground | Note 5-1 |
| 10 | D17(G7) | Green Data |  |
| 11 | D16(G6) | Green Data |  |
| 12 | D15(G5) | Green Data |  |
| 13 | D14(G4) | Green Data |  |
| 14 | D13(G3) | Green Data |  |
| 15 | D12(G2) | Green Data |  |
| 16 | D11(G1) | Green Data |  |
| 17 | D10(G0) | Green Data |  |
| 18 | GND | Digital ground | Note 5-1 |
| 19 | D07(R7) | Red Data |  |
| 20 | D06(R6) | Red Data |  |
| 21 | D05(R5) | Red Data |  |
| 22 | D04(R4) | Red Data |  |
| 23 | D03(R3) | Red Data |  |
| 24 | D02(R2) | Red Data |  |
| 25 | D01(R1) | Red Data |  |
| 26 | D00(R0) | Red Data |  |
| 27 | GND | Digital ground |  |
| 28 | VEE | Negative power for gate driver | Note 5-8 |
| 29 | VCC2 | Digital power supply for gate driver | Note 5-9 |
| 30 | VGG | Positive power for gate driver | Note 5-10 |

CN 2

| Pin No. | Symbol | Function | Remark |
| :---: | :--- | :---: | :---: |
| 1 | VLED | Voltage for LED |  |
| 2 | GLED2 | LED ground |  |
| 3 | GLED2 | LED ground | Note 5-7 |
| 4 | GND | Digital ground | Note 5-11 |
| 5 | VCOM | Voltage for common electrode |  |
| 6 | VSET | Externally/Internally gamma voltage setup |  |
| 7 | VDDA | Analog power supply for source driver |  |
| 8 | V10 | Gamma correction voltage 10 |  |
| 9 | V9 | Gamma correction voltage 9 |  |
| 10 | V8 | Gamma correction voltage 8 |  |
| 11 | V7 | Gamma correction voltage 7 |  |
| 12 | V6 | Gamma correction voltage 6 |  |
| 13 | V5 | Gamma correction voltage 5 | Note 5-12 |
| 14 | V4 | Gamma correction voltage 4 | Note 5-12 |
| 15 | V3 | Gamma correction voltage 3 | Note 5-6 |
| 16 | V2 | Gamma correction voltage 2 |  |
| 17 | V1 | Gamma correction voltage 1 |  |
| 18 | VSSA | Analog ground for source drive |  |
| 19 | L/R | Left/Right control for source driver |  |
| 20 | U/D | Up/Down control for gate driver | Digital ground |
| 21 | GND | Digital power supply for source driver | Note 5-5 |
| 22 | VCC1 | Hardware global reset | Note 5-3 |
| 23 | RESETB | Serial port data input/output | Note 5-4 |
| 24 | SPDA | Serial port clock |  |
| 25 | SPCK | Serial port data enable signal |  |
| 26 | SPENA | Input data enable control |  |
| 27 | DEN | Horizontal sync input | Vertical sync input |
| 28 | HS | VI |  |
| 29 | VS | Clock signal. Latching data at the rising edge |  |
| 30 | CLK |  |  |

Note 5-1 : Digital data input. DX0 is LSB and DX7 is MSB.
If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G and B data in turn. If serial RGB or CCIR601/656 input mode is selected, only D07~D00 are used, and others short to GND.

Note 5-2 : VDDA Typ. $=9.6 \mathrm{~V}$
Note 5-3 : Horizontal sync input in digital RGB mode and CCIR601 mode. ( Short to GND if not used )
Note 5-4 : Vertical sync input in digital RGB mode and CCIR601 mode. ( Short to GND if not used )

Note 5-5 : The SYNC(HS+VS) Mode and DEN mode are supported. If DEN signal is fixed low, SYNC Mode is used. Otherwise, DEN mode is used.

Note 5-6 : VCC1 Typ. $=3.3 \mathrm{~V}$
Note 5-7 : VCOM Typ. $=3.68 \mathrm{~V}$
Note 5-8 : VEE Typ. = -8V
Note 5-9 : VCC2 Typ. $=3.3 \mathrm{~V}$
Note 5-10 : VGG Typ. $=17 \mathrm{~V}$
Note 5-11 :If.VSET="H",the gamma correction voltage generated externally.
Note 5-12 : The definition of L/R, U/D
U/D CN2 (PIN20) $=$ Low
L/R CN2 (PIN 19) $=$ High
U/D CN2( PIN20) $=$ High
L/R CN2(PIN19)=Low



Typical Application Circuit (When VDDA $=9.6 \mathrm{~V}$ )


The information contained herein is the exclusive property of Prime View International Co., Ltd. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Prime View International Co., Ltd.PAGE:9

PD040QX1
6. Absolute Maximum Ratings:

GND $=0 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}$

| Parameters | Symbol | MIN. | MAX. | Unit | Remark |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltage | VCC2 | -0.3 | 6.0 | V |  |
|  | VCC1 | -0.3 | 7.0 | V |  |
|  | VDDA | -0.3 | 13.5 | V |  |
|  | VGG | -0.3 | 40.0 | V |  |
|  | VGG-VEE | -0.3 | 40.0 | V |  |
|  | VEE | -20 | 0.3 | V |  |

## 7. Electrical Characteristics

7-1) Recommended Operating Conditions:
VSSA $=\mathrm{GND}=0 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltage for Source Driver | VCC1 | 2.7 | 3.3 | 3.6 | V | Note $7-1$ |
|  | VDDA | 6.5 | 9.6 | 13.5 | V |  |
|  | VGG | - | 17 | - | V |  |
|  | VEE | - | -8 | - | V |  |
|  | $\mathrm{VCC2}$ | 2.7 | 3.3 | 3.6 | V |  |
| VCOM Voltage | VCOM | - | 4.1 | - | V |  |
| Digital Input Voltage | $\mathrm{V}_{\mathrm{HH}}$ | $0.7 \mathrm{~V}_{\mathrm{CC}}$ | - | $\mathrm{V}_{\mathrm{CC}}$ | V |  |
|  | $\mathrm{V}_{\mathrm{IL}}$ | 0 | - | $0.3 \mathrm{~V}_{\mathrm{CC}}$ | V |  |

Note 7-1 : To test the current dissipation of $\mathrm{V}_{\mathrm{cc}}$, using the "color bars" testing pattern shown as below.

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 1. White <br> 2. Yellow <br> 3. Cyan <br> 4. Green <br> 5. Magenta <br> 6. Red <br> 7. Blue <br> 8. Black |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

$I_{D D}$ current dissipation testing pattern
7-2) Recommended Driving Condition for Back Light
$\mathrm{Ta}=25^{\circ} \mathrm{C}$

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply voltage of LED backlight | $\mathrm{V}_{\text {LED }}$ | - | - | $(14)$ | V | Note 7-2 |
| Supply current of LED backlight | $\mathrm{I}_{\text {LED }}$ | - | 20 | - | mA | Note 7-3 |
| Backlight Power Consumption | $\mathrm{P}_{\text {LED }}$ | - | - | 560 | mW | Note 7-2, 7-4 |

Note 7-2 : $\mathrm{I}_{\text {LED }}=20 \mathrm{~mA}$, constant current
Note 7-3 : The LED driving condition is defined for each LED module. (4 LED Serial)
Input current $=20 \mathrm{~mA} * 2=40 \mathrm{~mA}$
Note 7-4: $\mathrm{P}_{\text {LED }}=\mathrm{V}_{\text {LED- }-1} * I_{\text {LED- }-1}+\mathrm{V}_{\text {LED- }-2} * \mathrm{I}_{\text {LED- } 2}$


Cathode

PD040QX1
7-3) Power Consumption

| Parameter | Symbol | Condition | Typ. | Max. | Unit | Remark |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Current for Gate Driver (Hi level) | IGG | VGG $=17 \mathrm{~V}$ | 0.1 | 0.3 | mA |  |
| Supply Current for Gate Driver (Low level) | IEE | VEE $=-8 \mathrm{~V}$ | 0.1 | 0.3 | mA |  |
| Supply Current for Gate Driver (Digital) | ICC2 | VCC2 $=3.3 \mathrm{~V}$ | 0.1 | 0.2 | mA |  |
| Supply Current for Source Driver (Digital) | ICC1 | VCC1 $=3.3 \mathrm{~V}$ | 0.9 | 1.8 | mA |  |
| Supply Current for Source Driver (Analog) | IDD | VDD $=9.6 \mathrm{~V}$ | 4.6 | 9.2 | mA |  |
| LCD Panel Power Consumption | - | - | 49.96 | 102.42 | mW | Note 7-5 |
| Backlight LED Power Consumption | PLED | - | 512 | 560 | mW | Note 7-6 |
| Total Power Consumption | - | - | 561.96 | 662.42 | mW |  |

Note 7-5: The power consumption for backlight is not included.
Note 7-6: Back light power consumption is calculated by $I_{\llcorner } \times V_{L}$.

## 8. Pixel Arrangement



PD040QX1
9. Display Color and Gray Scale Reference

| Color |  | Input Color Data |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Red |  |  |  |  |  |  |  | Green |  |  |  |  |  |  |  |  | Blue |  |  |  |  |  |  |  |
|  |  | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G7 | G6 | G5 | G |  | G3 | G2 | G1 | G0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Basic <br> Colors | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
|  | Cyan | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
|  | Magent | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
|  | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Red | Red | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Red | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Red | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Darker |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ |  | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ |
|  | Brighte |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Red | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Green | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Darker |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ |  | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ |
|  | Brighte |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Blue | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
|  | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
|  | Darker |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ |  | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ | $\downarrow$ |
|  | Brighte |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
|  | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
|  | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

10. Operation description

10-1) SPI Register Description

| Register | Test | Address |  |  |  | Data |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Name | RW | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R0 | 0 | 0 | 0 | 0 | 0 | $\triangle$ | $\triangle$ | $\triangle$ | $\triangle$ | $\triangle$ | PSC | STB | RESETB |
|  |  |  |  |  |  | $\triangle$ | $\triangle$ | $\triangle$ | $\triangle$ | $\triangle$ | 0 | 0 | 1 |
| R1 | 0 | 0 | 0 | 0 | 1 | $\triangle$ | $\triangle$ | $\triangle$ | RESL1 | RESLO | IF2 | IF1 | IF0 |
|  |  |  |  |  |  | $\triangle$ | $\triangle$ | $\triangle$ | 1 | 0 | 0 | 0 | 1 |
| R2 | 0 | 0 | 0 | 1 | 0 | $\triangle$ | $\triangle$ | STHD5 | STHD4 | STHD3 | STHD2 | STHD1 | STHDO |
|  |  |  |  |  |  | $\triangle$ | $\triangle$ | 0 | 0 | 0 | 0 | 0 | 0 |
| R3 | 0 | 0 | 0 | 1 | 1 | $\triangle$ | $\triangle$ | STVP3 | STVP2 | STVP1 | STVP0 | FRAD1 | FRADO |
|  |  |  |  |  |  | $\triangle$ | $\triangle$ | 0 | 0 | 0 | 0 | 0 | 0 |
| R4 | 0 | 0 | 1 | 0 | 0 | CS | FRP | FRC | LPF | VS_POL | HS_POL | NPC_SET | NPC_IN |
|  |  |  |  |  |  | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| R5 | 0 | 0 | 1 | 0 | 1 | AUTO_DP | DSIP_ON | A_TIME1 | A_TIME. | B_TIME2 | B_TIME1 | B_TIME0 | 1 |
|  |  |  |  |  |  | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

$\triangle$ RW must always keep low
Register

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Name | reserved | reserved | reserved | reserved | reserved | reserved | reserved | RESETB |
| Default | - | - | - | - | - | - | - | 1 |

## RESETB: Global reset.

RESETB $=$ " $\mathrm{L} "$ ", global reset the whole chip.
RESETB="H", Normal operation.

## Register R1

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Name | reserved | reserved | reserved | RESL1 | RESL0 | IF2 | IF1 | IF0 |
| Default | - | - | - | 1 | 0 | 0 | 0 | 1 |

## Register R1 setting

RESL [1:0]:Display resolution selection

| RESL1 | RESL0 | Resolution |
| :---: | :---: | :---: |
| 0 | 0 | $320 \times \mathrm{RGB} \times 240$ |
| 0 | 1 | reserved |
| 1 | 0 | reserved |
| 1 | 1 | reserved |

Display resolution selection
IF[2:0]:Data input mode selection

| IF2 | IF1 | IF0 | Data input format | operating freq |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | reserved | reserved |
| 0 | 0 | 1 | 24-bis parallel RGB | $25.175 \mathrm{MHz}(\mathrm{MAX})$ |
| 0 | 1 | 0 | reserved | reserved |
| 0 | 1 | 1 | reserved | reserved |
| 1 | 0 | 0 | reserved | reserved |
| 1 | 0 | 1 | reserved | reserved |
| 1 | 1 | 0 | reserved | reserved |
| 1 | 1 | 1 | reserved | reserved |

Data input mode selection
Register R2

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Name | reserved | reserved | STHD5 | STHD4 | STHD3 | STHD2 | STHD1 | STHD0 |
| Default | - | - | 0 | 0 | 0 | 0 | 0 | 0 |

## Register $\mathbf{R 2}$ setting

## STHD[5:0]: adjust start pulse position by dot

| STHD5 | STHD4 | STHD3 | STHD2 | STHD1 | STHD0 | STH position sdjust | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | TCPH |
| 0 | 0 | 0 | 0 | 0 | 1 | +1 | TCPH |
| 0 | 0 | 0 | 0 | 1 | 0 | +2 | TCPH |
| 0 | 0 | 0 | 0 | 1 | 1 | +3 | TCPH |
| 0 | 0 | 0 | 1 | 0 | 0 | +4 | TCPH |
| 0 | 0 | 0 | 1 | 0 | 1 | +5 | TCPH |
| 0 | 0 | 0 | 1 | 1 | 0 | +6 | TCPH |
| 0 | 0 | 0 | 1 | 1 | 1 | +7 | TCPH |
|  |  |  |  |  |  |  |  |
| 0 | 1 | 1 | 0 | 0 | 0 | +24 | TCPH |
| 0 | 1 | 1 | 0 | 0 | 1 | $+25$ | TCPH |
| 0 | 1 | 1 | 0 | 1 | 0 | +26 | TCPH |
| 0 | 1 | 1 | 0 | 1 | 1 | +27 | TCPH |
| 0 | 1 | 1 | 1 | 0 | 0 | +28 | TCPH |
| 0 | 1 | 1 | 1 | 0 | 1 | +29 | TCPH |
| 0 | 1 | 1 | 1 | 1 | 0 | +30 | TCPH |
| 0 | 1 | 1 | 1 | 1 | 1 | +31 | TCPH |
| 1 | 0 | 0 | 0 | 0 | 0 | -1 | TCPH |
| 1 | 0 | 0 | 0 | 0 | 1 | -2 | TCPH |
| 1 | 0 | 0 | 0 | 1 | 0 | -3 | TCPH |
| 1 | 0 | 0 | 0 | 1 | 1 | -4 | TCPH |
| 1 | 0 | 0 | 1 | 0 | 0 | -5 | TCPH |
| 1 | 0 | 0 | 1 | 0 | 1 | -6 | TCPH |
| 1 | 0 | 0 | 1 | 1 | 0 | -7 | TCPH |
| 1 | 0 | 0 | 1 | 1 | 1 | -8 | TCPH |
|  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | 0 | -25 | TCPH |
| 0 | 0 | 0 | 0 | 0 | 1 | -26 | TCPH |
| 0 | 0 | 0 | 0 | 1 | 0 | -27 | TCPH |
| 0 | 0 | 0 | 0 | 1 | 1 | -28 | TCPH |
| 0 | 0 | 0 | 1 | 0 | 0 | -29 | TCPH |
| 0 | 0 | 0 | 1 | 0 | 1 | -30 | TCPH |
| 0 | 0 | 0 | 1 | 1 | 0 | -31 | TCPH |
| 0 | 0 | 0 | 1 | 1 | 1 | -32 | TCPH |

The information contained herein is the exclusive property of Prime View International Co., Ltd. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Prime View International Co., Ltd.PAGE:15

## Register R3

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Name | reserved | reserved | STVP3 | STVP2 | STVP1 | STVP0 | FRAD1 | FRAD0 |
| Default | - | - | 0 | 0 | 0 | 0 | 0 | 0 |

Register R3 setting

| STVP3 | STVP2 | STVP1 | STVP0 | STV position adjust | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | $T_{H}$ |
| 0 | 0 | 0 | 1 | +1 | $T_{H}$ |
| 0 | 0 | 1 | 0 | +2 | $T_{H}$ |
| 0 | 0 | 1 | 1 | +3 | $T_{H}$ |
| 0 | 1 | 0 | 0 | +4 | $T_{H}$ |
| 0 | 1 | 0 | 1 | +5 | $T_{H}$ |
| 0 | 1 | 1 | 0 | +7 | $T_{H}$ |
| 0 | 1 | 1 | 1 | -1 | $T_{H}$ |
| 1 | 0 | 0 | 0 | -2 | $T_{H}$ |
| 1 | 0 | 0 | 1 | -3 | $T_{H}$ |
| 1 | 0 | 1 | 0 | -4 | $T_{H}$ |
| 1 | 0 | 1 | 1 | -5 | $T_{H}$ |
| 1 | 1 | 0 | 0 | -6 | $T_{H}$ |
| 1 | 1 | 0 | 1 | -7 | $T_{H}$ |
| 1 | 1 | 1 | 0 | 1 | -8 |

Adjust first line position by line
FRAD[1:0]:Odd frame or Even frame advance control

| FRAD1 | FRAD0 | Advance Frame | Notes |
| :---: | :---: | :---: | :---: |
| 0 | 0 | reserved | reserved |
| 0 | 1 | reserved | reserved |
| 1 | 0 | Even Frame | Odd frame Tstv=STVP setting +1 H |
| 1 | 1 | Reserve | Reserve |

Odd frame or Even frame Advance control

## Register R4

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Name | reserved | reserved | reserved | reserved | VS_POL | HS_POL | NPC_SET | NPC_IN |
| Default | - | - | - | - | 0 | 0 | 0 | 1 |

## Register R4 setting

VS_POL: VS polarity setting.
VS_POL=L, negative polarity,
VS_POL=H, positive polarity.
Note: Please set the VS_POL=H when CCIR601 mode for video decoder SAA7114.
(Please refer the input timing of the "13-4) Data input format for CCIR601 Mode")

HS_POL: HS polarity setting.
HS_POL=L, negative polarity,
HS_POL=H, positive polarity.

NPC_SET; Set the NTSC/PAL auto detection or define by NPC_IN. NPC_SET=L, auto detection. NPC_SET $=H$, define by NPC_IN.

NPC_IN: Define the NTSC/PAL mode by SPI.
NPC_IN=L, PAL.
NPC_IN=H, NTSC.

## Register R5

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Name | AUTO_DP | SISP_ON | A_TIME1 | A_TIME0 | B_TIME2 | B_TIME2 | B_TIME0 | reserved |
| Default | 1 | 0 | 0 | 1 | 0 | 1 | 0 | - |

Register R5 setting
AUTO_DP: When power on, select blank image display time decided by A_TIME (bit 5,4 ) or DISP_ON (bit 6).
AUTO_DP $=$ "L", Blank image display time decided by DISP ON (bit 6). AUTO_DP $=$ "H", Blank image display time decided by A TIME (bit 5,4 ).

DISP_ON: When AUTO_DP (bit 7) = "L", and DISP_ON = "H", blank image display off, then display normal image.

A_TIME [1:0]: When AUTO_DP(bit 7$)=$ "H". the blank image display time is decided by A_TIME
00 : blank image display time is 8 VS time
01: blank image display time is 16 VS time
10: blank image display time is 32 VS time
11: blank image display time is 64 VS time

B_TIME [2:0]: When into STB mode the blank image display time is decided by B_TIME.
000 : blank image display time is 3 VS time.
001: blank image display time is 4 VS time.
010: blank image display time is 5 VS time.
011: blank image display time is 6 VS time.
100: blank image display time is 7 VS time.
101: blank image display time is 8 VS time.
110: blank image display time is 9 VS time.
111: blank image display time is 10 VS time.

PD040QX1
10-2) Power ON/OFF sequence
To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power ON: VCC1, GND $\rightarrow$ VDDA, VSSA $\rightarrow$ V1 to V10
Power OFF: V1 to V10 $\rightarrow$ VDDA, VSSA $\rightarrow$ VCC1, GND
10-3) Power ON Control
Source drive has a power ON sequence control function. There are two kinds of the mode. One is auto mode, and another is manual mode.

Auto Mode: When power is ON, blank data is outputted for 16 -frames(default value) first, from the falling edge of the following VS signal. The blank data would be gray level 255 for normally white panel.
It can be defined in register R5 A_TiME1 (bit 5) and ATIMEO (bit 4) when
AUTO_DP(bit 7) $=$ " $\mathrm{H}^{\prime}$


RESETB


Manual Mode: When power is ON, you should set the register R5 AUTO_DP(bit 7) $=$ "L" to stay at the manual mode. Blank data is outputted until the DISP_D $\mathrm{O}($ bit 6$)=$ H then display the normal image.


Power on control for Mariual Mode

Source dive has a standby ON/OFF sequence control function. When STB pin is "L", blank data is outputted for 5 -frames (default value) first, from the falling edge of the following VSYNC signal. The blank data would be gray level 255 for normally white panel. It can be defined in register R5 B_TIME[2:0] to adjust the frame number of the biank data.


10-5) Reset when power on
Source drive is internally initialized by the global reset signal. RESETB. The reset input must be held for at least 1 ms after power is stable.


## RESETB control after power stable

PD040QX1

## 11.AC Characteristics

11-1) SPI timing characteristics

| PARAMETER |  | Symbol | Unit |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Max. |  |
| SPCK period | $T_{C K}$ | 60 | - | - | ns |
| SPCK high width | $T_{C K H}$ | 30 | - | - | ns |
| SPCK low width | $T_{\text {CKL }}$ | 30 | - | - | ns |
| Data setup time | $\mathrm{T}_{\text {SUI }}$ | 12 | - | - | ns |
| Data hold time | $T_{H D I}$ | 12 | - | - | ns |
| SPENA to SPCK setup time | $T_{C E}$ | 20 | - | - | ns |
| SPENA to SPDA hold time | $T_{C E}$ | 20 | - | - | ns |
| SPENA high pulse width | $T_{C D}$ | 50 |  | - | ns |

11-2) Digital Parallel RGB interface

| PARAMETER |  | Symbol | Spec. |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Unit |  |  |  |  |  |
|  |  | Min. | Typ. | Max. |  |
| CLK frequency | $\mathrm{F}_{\text {CPH }}$ | - | 6.43 | - | MHz |
| CLK period | $T_{\text {CPH }}$ | - | 155.62 | - | nS |
| CLK pulse duty | $T_{\text {CWH }}$ | 40 | 50 | 60 | $\%$ |
| HS period | $T_{H}$ | - | 408 | - | $T_{\text {CPH }}$ |
| HS pulse width | $T_{\text {WH }}$ | 5 | 30 | - | $T_{\text {CPH }}$ |
| HS-first horizontal data time | $T_{\text {HS }}$ | 36 | 68 | 99 | $T_{\text {CPH }}$ |
| DEN pulse width | $T_{\text {EF }}$ | - | 320 | - | $T_{\text {CPH }}$ |
| VS pulse width | $T_{\text {WV }}$ | 1 | 3 | 5 | $T_{H}$ |
| VS-DEN time | NTSC | $T_{\text {STV }}$ | - | 18 | - |
|  | PAL | $T_{\text {STV }}$ | - | 26 | - |

Note: When SYNC mode is used, 1st data start from 204th CLK after HS falling (when STHD[5.0]=000000)

| PARAMETER | Symbol | Spec. |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. |  |
| OEV pulse width | Toev | - | 26 | - | TCPH |
| CKV pulse width | Tciv | - | 24 | - | $\mathrm{T}_{\text {CPH }}$ |
| HS-CKV time | T | - | 16 | - | $\mathrm{T}_{\mathrm{CPH}}$ |
| HS-OEV time | $\mathrm{T}_{2}$ | - | 8 | - | $\mathrm{T}_{\text {CPH }}$ |
| HS-POL time | T3 | - | 25 | - | $\mathrm{T}_{\mathrm{CPH}}$ |
| STV setup time | Tsuv | - | 10 | - | $\mathrm{T}_{\mathrm{CPH}}$ |
| STV pulse width | Twsty | - | 1 | - | $\mathrm{T}_{\mathrm{H}}$ |

12. Waveform

Timing Controller Timing Chart
12-1) SPI timing


## SPI timing

12-2) Clock and Data input waveforms


Clock and Data input waveforms.

12-3) Data input format for RGB Mode


Parallel RGB Horizontal Data Format


Digital RGB NTSC mode Vertical Data Format for $\mathbf{2 6 2 . 5}_{\mathrm{H}}$


Figu Digital RGB PAL mode Vertical Data Format for $312.5 T_{\mathrm{H}}$


Digital RGB NTSC mode Vertical Data Format for $\mathbf{2 6 2} \mathrm{T}_{\mathrm{H}}$


Digital RGB PAL mode Vertical Data Format for $312 \mathrm{~T}_{\mathrm{H}}$

12-4) The HS \& VS timing of the ODD/EVEN field


Define the HSYNC to VSYNC timing for RGB mode

## 13.Power On Sequence



1. $0<\mathrm{t} 1 \leqq 20 \mathrm{~ms}$
2. $0<\mathrm{t} 2 \leqq 50 \mathrm{~ms}$
3. $0<\mathrm{t} 3 \leqq 1$ s

## 14. Optical Characteristics

## 14-1) Specification:

$\mathrm{Ta}=25^{\circ} \mathrm{C}$

| Parameter |  | Symbol | Condition | MIN. | TYP. | MAX. | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Viewing Angle | Horizontal | Ө21, $\theta 22$ | $C R \geqq 10$ | 75 | 80 | --- | deg | Note 14-1 |
|  | Vertical | $\theta 12$ |  | 45 | 50 | --- | deg |  |
|  |  | $\theta 11$ |  | 55 | 60 | --- | deg |  |
| Contrast Ratio |  | CR | At optimized Viewing angle | 200 | 400 | --- |  | Note 14-2 |
| Luminance |  | L | $\theta=0^{\circ}$ | 300 | 350 | --- | $\mathrm{cd} / \mathrm{m}^{2}$ |  |
| White Chromaticity |  | X | $\theta=0^{\circ}$ | 0.26 | 0.30 | 0.34 |  |  |
|  |  | y | $\theta=0^{\circ}$ | 0.29 | 0.33 | 0.37 |  |  |
| Response time | Rise | Tr | $\theta=0^{\circ}$ | --- | 15 | 30 | ms | Note 14-3 |
|  | Fall | Tf |  | --- | 25 | 50 | ms |  |
| Uniformity |  | U | - | 75 | 80 | --- | \% | Note 14-5 |
| Cross Talk Ratio |  | CTK | - | --- | --- | 3.5 | \% | Note 14-6 |
| LED Life Time |  |  | $+25^{\circ} \mathrm{C}$ | 20000 | 30000 | --- | hrs | Note 14-4 |

Note 14-1: The definitions of viewing angles


Note 14-2 : CR $=\frac{\text { Luminance when Testing point is White }}{\text { Luminance when Testing point is Black }}$
Contrast Ratio is measured in optimum common electrode voltage.

Note 14-3 : The definition of response time :


Note 14-4: The "LED Life time" is defined as the module brightness decrease to $50 \%$ original Brightness that the ambient temperature is $25^{\circ} \mathrm{C}$ and $\mathrm{I}_{\text {LED }}=20 \mathrm{~mA}$

Note 14-5: The uniformity of LCD is defined as
$\mathrm{U}=$ The Minimum Brightness of the 9 testing Points
The Maximum Brightness of the 9 testing Points
Luminance meter : BM-5A or BM-7 fast(TOPCON)
Measurement distance : $500 \mathrm{~mm}+/-50 \mathrm{~mm}$
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module
The test pattern is white (Gray Level 63).


Note 14-6: Cross Talk (CTK) $=\frac{|\mathrm{YA}-\mathrm{YB}|}{\mathrm{YA}} \times 100 \%$
YA: Brightness of Pattern A
YB: Brightness of Pattern B
Luminance meter : BM 5A (TOPCON)
Measurement distance : $500 \mathrm{~mm}+/-50 \mathrm{~mm}$
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module

Pattern A
(Gray Level 31)

Pattern B
(Gray Level 31, central black box exclusive)


X: Measuring Point ( $A$ and $B$ are at the same point.)
(Gray Level 0)

## 15. Handling Cautions

15-1) Mounting of module
A)Please power off the module when you connect the input/output connector.
B)Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
C)Protective film (Laminator) is applied on surface to protect it against scratches and dirt.
D)Please following the tear off direction as figure15-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.
15-2) Precautions in mounting
A) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
B) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
C) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
D) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.
15-3) Adjusting module
A) Adjusting volumes on the rear face of the module have been set optimally before shipment.
B) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.
15-4) Others
A) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
B) Store the module at a room temperature place.
C) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
D) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel.

Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
E) Observe all other precautionary requirements in handling general electronic components.
F) Please adjust the voltage of common electrode as material of attachment by 1 module.

15-5) Polarizer mark
The polarizer mark is to describe the direction of view angle film how to mach up with the rubbing direction.


Protective film

Figure 15-1 the way to peel off protective film
16. Reliability Test

| No | Test Item | Test Condition |
| :---: | :---: | :---: |
| 1 | High Temperature Storage Test | $\mathrm{Ta}=+80^{\circ} \mathrm{C}, 240 \mathrm{hrs}$ |
| 2 | Low Temperature Storage Test | $\mathrm{Ta}=-40^{\circ} \mathrm{C}, 240 \mathrm{hrs}$ |
| 3 | High Temperature Operation Test | $\mathrm{Ta}=+80^{\circ} \mathrm{C}, 240 \mathrm{hrs}$ |
| 4 | Low Temperature Operation Test | $\mathrm{Ta}=-30^{\circ} \mathrm{C}, 240 \mathrm{hrs}$ |
| 5 | High Temperature \& High Humidity Operation Test | $\mathrm{Ta}=+60^{\circ} \mathrm{C}, 90 \% \mathrm{RH}, 240 \mathrm{hrs}$ |
| 6 | Thermal Cycling Test (non-operating) | $\begin{aligned} & \hline-30^{\circ} \mathrm{C} \rightarrow+80^{\circ} \mathrm{C}, 200 \mathrm{Cycles}, \\ & 30 \mathrm{~min} 30 \mathrm{~min} \\ & \hline \end{aligned}$ |
| 7 | Vibration Test (non-operating) | Frequency: $10 \sim 55 \mathrm{H}_{\mathrm{Z}}$ Amplitude: 1.5 mm Sweep time: 11 mins Test Period:6 Cycles for each direction of $\mathrm{X}, \mathrm{Y}, \mathrm{Z}$ |
| 8 | Shock Test (non-operating) | $100 \mathrm{G}, 6 \mathrm{~ms}$ Direction: $\pm X, \pm Y, \pm Z$ Cycle : 3 times |
| 9 | Electrostatic Discharge Test (non-operating) | $\begin{gathered} 200 \mathrm{pF}, 0 \Omega \pm 200 \mathrm{~V} \\ 1 \text { time / each terminal } \\ \hline \end{gathered}$ |

Ta: ambient temperature
Note : The protective film must be removed before temperature test.
[Criteria]
In the standard conditions, there is not display function NG issue occurred. (including : line defect , no image).All the cosmetic specification is judged before the reliability stress.
17. Block Diagram


## © PRIME VIEW

PD040QX1
18. Packing


The information contained herein is the exclusive property of Prime View International Co., Ltd. and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of Prime View International Co., Ltd.PAGE:32

