Version : 1.0

TECHNICAL SPECIFICATION

MODEL NO : PD050QX1

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Please contact PVI or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐PVI's Confirmation

Confirmed By _____

Prepared By _____

Revision History

Rev.	Eng.	Issued Date	Revised Content
0.1	黃秀晶	Mar 19,2007	Preliminary
1.0	黃秀晶	May 07, 2007	Add Page 34 15. Optical Characteristics data

TECHNICAL SPECIFICATION

CONTENTS

1. Application

This data sheet applies to a color TFT LCD module, PD050QX1.This module applies to OA product, computer peripheral, industrial meter, image communication and multi-media. If you must use in severe reliability environment, please don't extend over PVI's reliability test conditions.

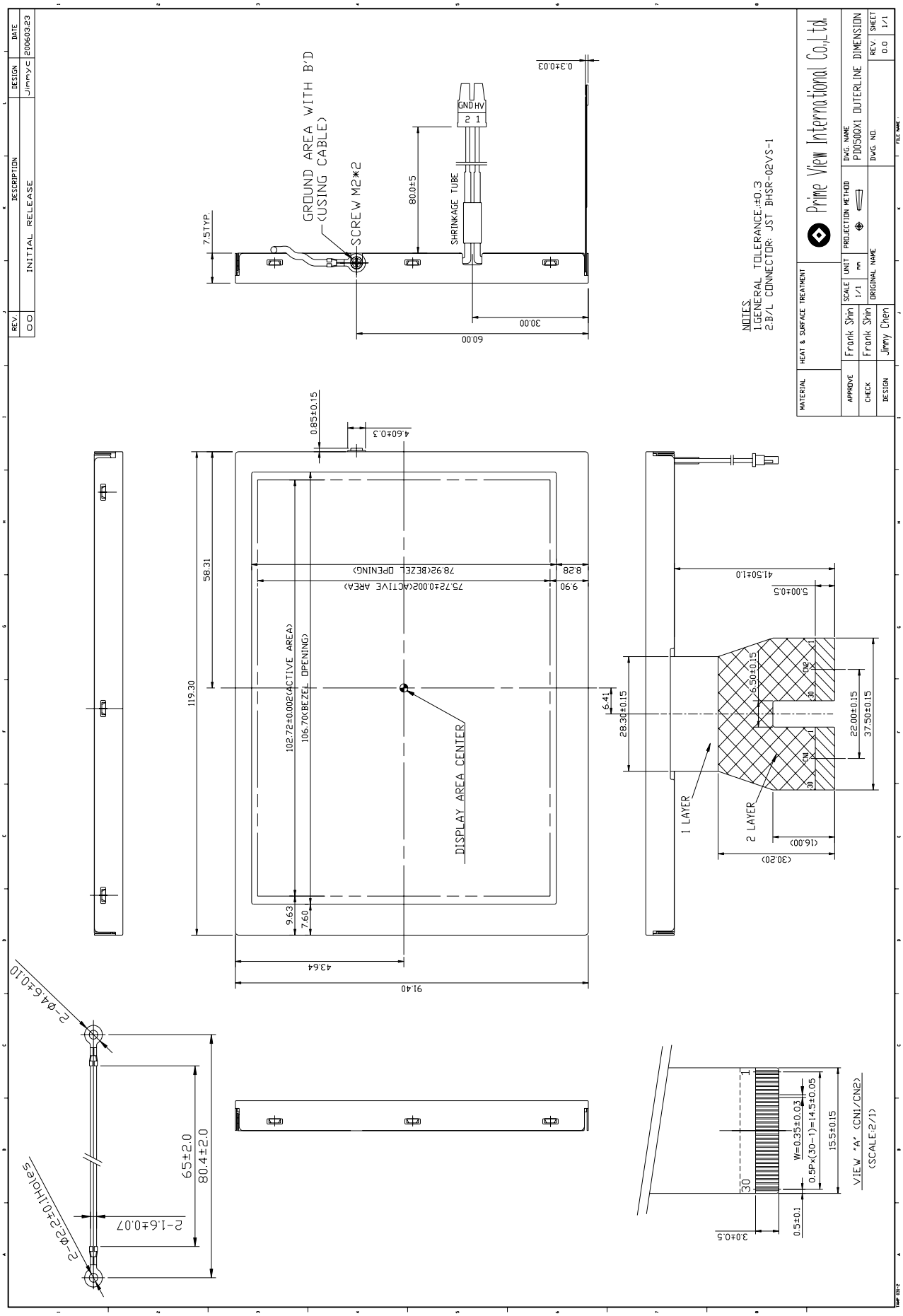
2. Features

. Amorphous silicon TFT LCD panel with backlight unit
. Pixel in stripe configuration
. Slim and compact, designed for O/A application
. Backlight driving DC/AC inverter not included in this module
. Long Life Lamp

3.Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	5.0" (diagonal)	inch
Display Format	320×(RGB)×240	dot
Display Colors	ref. "9. Display Color and Gray Scale Reference"	
Active Area	102.72 (H)×75.72 (V)	mm
Pixel Pitch	0.3210(H)×0.3155 (V)	mm
Pixel Configuration	Stripe	
Outline Dimension	119.3(H)×91.4(V)×7.5(D)	mm
Weight	116.6±10	g
Back-light	CCFL, 1 tubes	
Surface treatment	Anti-Glare+SWV	
Display mode	Normally white	
Gray scale inversion direction	6 (ref to Page 34 viewing angle)	o'clock

4. Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

5-1) TFT-LCD Panel Driving

FPC Down Connect, 30 Pins, Pitch: 0.5 mm

CN 1

Pin No.	Symbol	Function	Remark
1	D27(B7)	Blue Data	Note 5-1
2	D26(B6)	Blue Data	
3	D25(B5)	Blue Data	
4	D24(B4)	Blue Data	
5	D23(B3)	Blue Data	
6	D22(B2)	Blue Data	
7	D21(B1)	Blue Data	
8	D20(B0)	Blue Data	
9	GND	Digital ground	
10	D17(G7)	Green Data	Note 5-1
11	D16(G6)	Green Data	
12	D15(G5)	Green Data	
13	D14(G4)	Green Data	
14	D13(G3)	Green Data	
15	D12(G2)	Green Data	
16	D11(G1)	Green Data	
17	D10(G0)	Green Data	
18	GND	Digital ground	
19	D07(R7)	Red Data	Note 5-1
20	D06(R6)	Red Data	
21	D05(R5)	Red Data	
22	D04(R4)	Red Data	
23	D03(R3)	Red Data	
24	D02(R2)	Red Data	
25	D01(R1)	Red Data	
26	D00(R0)	Red Data	
27	GND	Digital ground	
28	VEE	Negative power for gate driver	Note 5-8
29	VCC2	Digital power supply for gate driver	Note 5-9
30	VGG	Positive power for gate driver	Note 5-10

CN 2

Pin No.	Symbol	Function	Remark
1	VCOM	Voltage for common electrode	Note 5-7
2	VSET	Externally/Internally gamma voltage setup	Note 5-11
3	VDDA	Analog power supply for source driver	Note 5-2
4	V14	Gamma correction voltage 14	
5	V13	Gamma correction voltage 13	
6	V12	Gamma correction voltage 12	
7	V11	Gamma correction voltage 11	
8	V10	Gamma correction voltage 10	
9	V9	Gamma correction voltage 9	
10	V8	Gamma correction voltage 8	
11	V7	Gamma correction voltage 7	
12	V6	Gamma correction voltage 6	
13	V5	Gamma correction voltage 5	
14	V4	Gamma correction voltage 4	
15	V3	Gamma correction voltage 3	
16	V2	Gamma correction voltage 2	
17	V1	Gamma correction voltage 1	
18	VSSA	Analog ground for source drive	
19	L/R	Left/Right control for source driver	Note 5-12
20	U/D	Up/Down control for gate driver	Note 5-12
21	GND	Digital ground	
22	VCC1	Digital power supply for source driver	Note 5-6
23	RESETB	Hardware global reset	
24	SPDA	Serial port data input/output	
25	SPCK	Serial port clock	
26	SPENA	Serial port data enable signal	
27	DEN	Input data enable control	Note 5-5
28	HS	Vertical sync input	Note 5-3
29	VS	Horizontal sync input	Note 5-4
30	CLK	Clock signal. Latching data at the rising edge	

Note 5-1 : Digital data input. DX0 is LSB and DX7 is MSB.
If parallel RGB input mode is used, D0X, D1X, and D2X indicate R, G and B data in turn.
If serial RGB or CCIR601/656 input mode is selected, only D07~D00 are used, and others short to GND.

Note 5-2 : VDDA Typ. = 8.6V

Note 5-3 : Horizontal sync input in digital RGB mode and CCIR601 mode.
(Short to GND if not used)

Note 5-4 : Vertical sync input in digital RGB mode and CCIR601 mode.
(Short to GND if not used)

Note 5-5 : The SYNC(HS+VS) Mode and DEN mode are supported. If DEN signal is fixed low, SYNC Mode is used. Otherwise , DEN mode is used.

Note 5-6 : VCC1 Typ. = 3.3V

Note 5-7 : VCOM Typ.＝3.68V

Note 5-8 : VEE Typ. = -5V

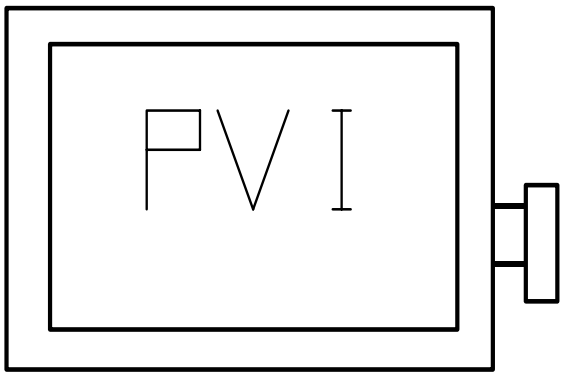
Note 5-9 : VCC2 Typ.＝3.3V

Note 5-10 : VGG Typ. =19.6V

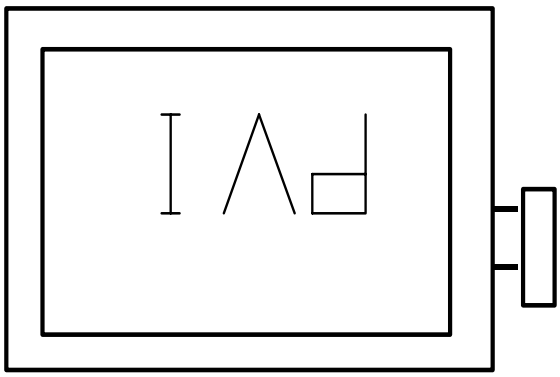
Note 5-11 :If.VSET=”H”,the gamma correction voltage generated externally.

Note 5-12 : The definition of L/R , U/D

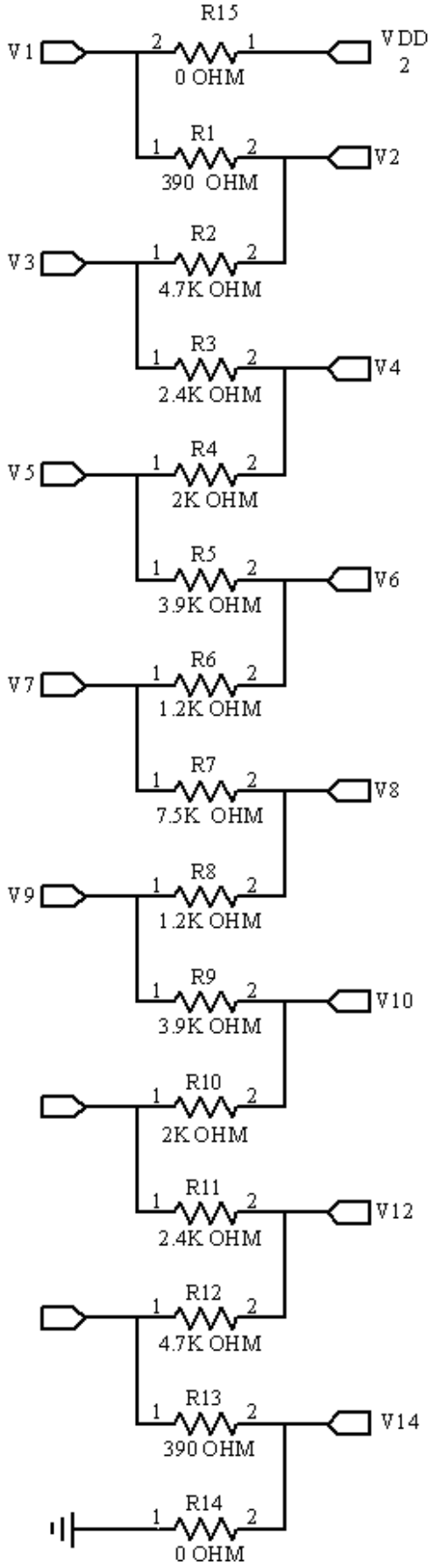
U/D CN2(PIN 20)=Low
L/R CN2(PIN 19)=High



U/D CN2(PIN 20)=High
L/R CN2(PIN 19)=Low



Typical Application Circuit (When VDDA = 8.6V)



6. Absolute Maximum Ratings:

VSSA=GND=0V, Ta=25℃

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	VCC2	-0.3	6.0	V	
	VCC1	-0.3	7.0	V	
	VDDA	-0.3	13.5	V	
	VGG	-0.3	40.0	V	
	VGG-VEE	-0.3	40.0	V	
	VEE	-20	0.3	V	

7.Electrical Characteristics

7-1) Recommended Operating Conditions :

VSSA=GND=0V, Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	VCC1	2.7	3.3	3.6	V	
	VDDA	6.5	8.6	13.5	V	
Supply Voltage for Gate Driver	VGG	-	19.6	-	V	
	VEE	-	-5	-	V	
	VCC2	2.7	3.3	3.6	V	
VCOM Voltage	VCOM	-	3.68	-	V	
Digital Input Voltage	V_{IH}	0.7 V_{CC}	-	V_{CC}	V	
	V_{IL}	0	-	0.3 V_{CC}	V	

7-2) Recommended Driving Condition for Back Light

Ta=25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	392	436	480	Vrms	
Lamp current	I_L	3	6	8	mA	Note 7-1
Lamp frequency	P_L	40	43	80	KHz	Note 7-2
Starting voltage(25℃) (Reference Value)	Vs	-	-	890	Vrms	Note 7-3
Starting voltage(0℃) (Reference Value)	Vs	-	-	1180	Vrms	Note 7-3

Note 7-1: In order to satisfy the quality of B/L, no matter use what kind of inverter, the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 7-2: The waveform of lamp driving voltage should be as closed to a perfect sine wave As possible.

Note 7-3: The “Starting voltage” means the minimum voltage of inverter to turn on the CCFL. and it should be applied to the lamp for more than 1 second start up. Otherwise the lamp may not be turned on.

7-3) Power Consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	IGG	VGG= 19.6V	0.115	0.345	mA	
Supply Current for Gate Driver (Low level)	IEE	VEE= -5V	0.12	0.36	mA	
Supply Current for Source Driver (Digital)	ICC1	VCC1= 3.3V	1.74	3.48	mA	
Supply Current for Source Driver (Analog)	IDDA	VDDA= 8.6V	7.45	14.9	mA	
Supply Current for Gate Driver (Digital)	ICC2	VCC2= 3.3V	0.006	0.018	mA	
LCD Panel Power Consumption	-	-	72.68	148.23	mW	Note 7-4
Backlight Lamp Power Consumption	P_{CCFL}	-	2.62	3.84	W	Note 7-5
Total Power Consumption	-	-	2.70	4	W	

Note 7-4: The power consumption for backlight is not included.

Note 7-5: Back light lamp power consumption is calculated by $I_L \times V_L$.

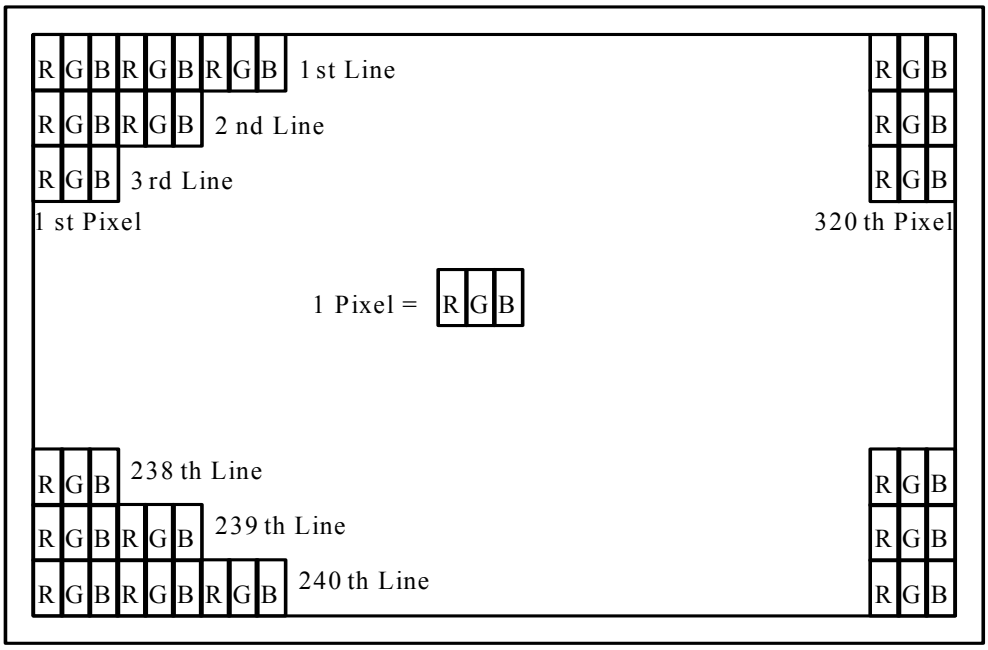
7-4) Backlight driving

Connector type : “JST BHSR-02VS-1” of Japan Solder less Terminal MFG Co. LTD

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	
2	VL2	Input terminal (Low voltage side)	Note 7-6

Note 7-6: Low voltage side of backlight inverter connects with ground of inverter circuits.

8. Pixel Arrangement

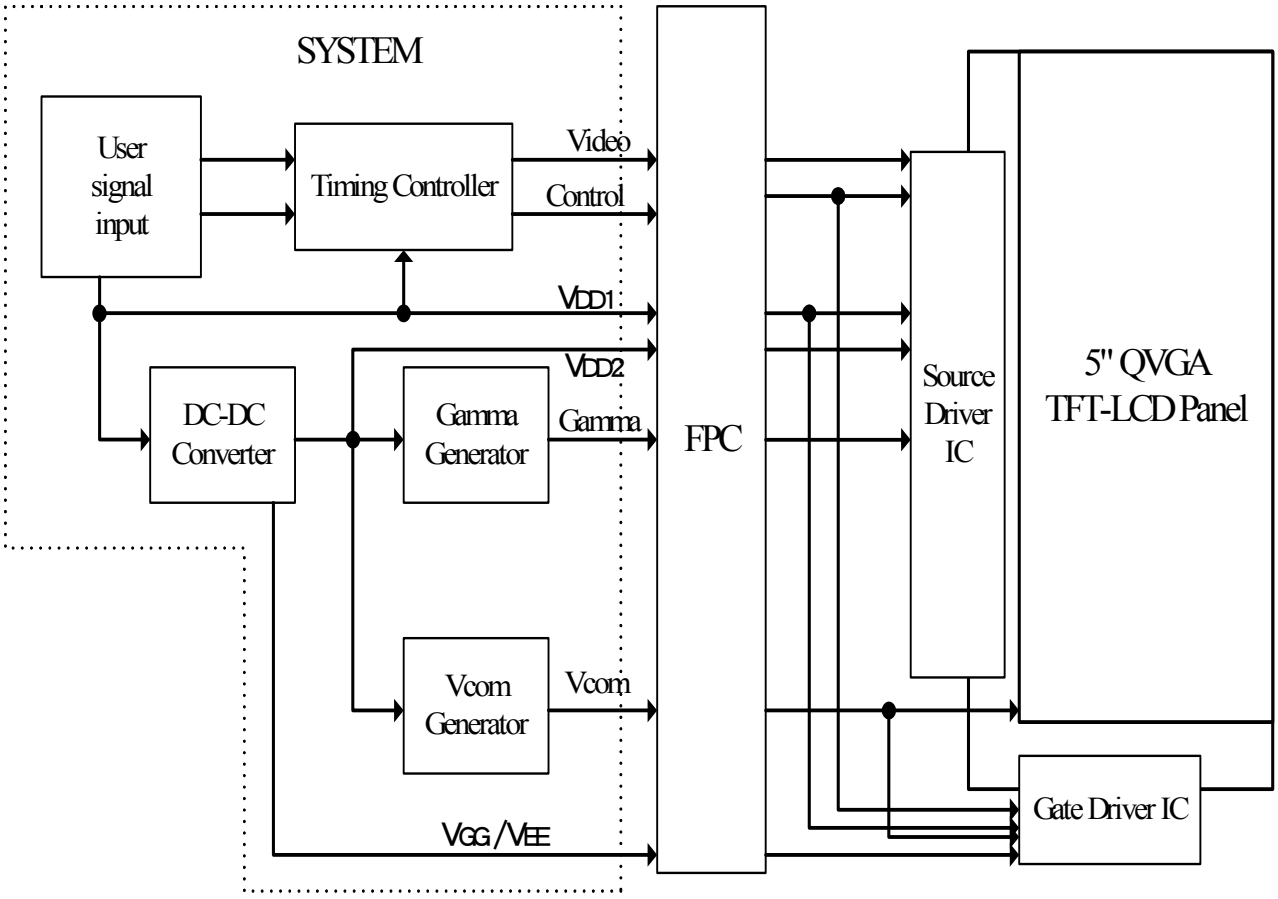


9. Display Color and Gray Scale Reference

Color		Input Color Data																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Red	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

10. Block Diagram

10-1) TFT-module Block Diagram



11. Operation description

11-1) SPI Register Description

Register Name	Test RW	Address A3	A2	A1	A0	Data D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	1	1	1	1	1	PSC	STB	RESETB
						1	1	1	1	1	0	0	1
R1	0	0	0	0	1	1	1	1	RESL1	RESL0	IF2	IF1	IF0
						1	1	1	1	0	0	0	1
R2	0	0	0	1	0	1	1	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
						1	1	0	0	0	0	0	0
R3	0	0	0	1	1	1	1	STVP3	STVP2	STVP1	STVP0	FRAD1	FRAD0
						1	1	0	0	0	0	0	0
R4	0	0	1	0	0	CS	FRP	FRC	LPF	VS_POL	HS_POL	NPC_SET	NPC_IN
						1	0	1	1	0	0	0	1
R5	0	0	1	0	1	AUTO_DP	DISP_ON	A_TIME1	A_TIME0	B_TIME2	B_TIME1	B_TIME0	1
						1	0	0	1	0	1	0	1

1 RW must always keep low.

- **Register R0**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	reserved	PSC	STB	RESETB
Default	-	-	-	-	-	0	0	1

Table 11.1 Register R0 setting

PSC: Operating mode setting by input pin or SPI register.
PSC="H", set STB, FRP, CS, IF[2:0],RESL[1:0] by SPI register.

STB: Standby mode setting.
STB="L", TCON and source driver are off
STB="H", all the functions are on.

RESETB: Global reset.
RESETB="L", global reset the whole chip.
RESETB="H", Normal operation.

- **Register R1**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	RESL1	RESL0	IF2	IF1	IF0
Default	–	–	–	1	0	0	0	1

Table 11.2 Register R1 setting

RESL [1:0]: Display resolution selection.

RESL1	RESL0	Resolution
0	0	320x RGB x240
0	1	reserved
1	0	reserved
1	1	reserved

Table 11.3 Display resolution selection

IF [2:0]: Data input mode selection.

IF2	IF1	IF0	Data input format	Operating freq
0	0	0	8-bit serial RGB	38.4MHz (Max)
0	0	1	24-bit parallel RGB	25.175MHz (Max)
0	1	0	CCIR601(YUV mode A)	24.54MHz
0	1	1	CCIR601(YUV mode B)	24.54MHz
1	0	0	CCIR601(YUV mode A)	27MHz
1	0	1	CCIR601(YUV mode B)	27MHz
1	1	0	CCIR656(YUV mode A)	27MHz
1	1	1	CCIR656(YUV mode B)	27MHz

Table 11.4 Data input mode selection

- **Register R2**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	STHD5	STHD4	STHD3	STHD2	STHD1	STHD0
Default	—	—	0	0	0	0	0	0

Table 11.5 Register R2 setting

STHD [5:0]: adjust start pulse position by dot

STHD5	STHD4	STHD3	STHD2	STHD1	STHD0	STH position adjust	Unit
0	0	0	0	0	0	0	T_{CPH}
0	0	0	0	0	1	+1	T_{CPH}
0	0	0	0	1	0	+2	T_{CPH}
0	0	0	0	1	1	+3	T_{CPH}
0	0	0	1	0	0	+4	T_{CPH}
0	0	0	1	0	1	+5	T_{CPH}
0	0	0	1	1	0	+6	T_{CPH}
0	0	0	1	1	1	+7	T_{CPH}
⋮							
0	1	1	0	0	0	+24	T_{CPH}
0	1	1	0	0	1	+25	T_{CPH}
0	1	1	0	1	0	+26	T_{CPH}
0	1	1	0	1	1	+27	T_{CPH}
0	1	1	1	0	0	+28	T_{CPH}
0	1	1	1	0	1	+29	T_{CPH}
0	1	1	1	1	0	+30	T_{CPH}
0	1	1	1	1	1	+31	T_{CPH}
1	0	0	0	0	0	-1	T_{CPH}
1	0	0	0	0	1	-2	T_{CPH}
1	0	0	0	1	0	-3	T_{CPH}
1	0	0	0	1	1	-4	T_{CPH}
1	0	0	1	0	0	-5	T_{CPH}
1	0	0	1	0	1	-6	T_{CPH}
1	0	0	1	1	0	-7	T_{CPH}
1	0	0	1	1	1	-8	T_{CPH}
⋮							
1	1	1	0	0	0	-25	T_{CPH}
1	1	1	0	0	1	-26	T_{CPH}
1	1	1	0	1	0	-27	T_{CPH}
1	1	1	0	1	1	-28	T_{CPH}
1	1	1	1	0	0	-29	T_{CPH}
1	1	1	1	0	1	-30	T_{CPH}
1	1	1	1	1	0	-31	T_{CPH}
1	1	1	1	1	1	-32	T_{CPH}

Table 11.6 Adjust start pulse position by dot

- **Register R3**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	STVP3	STVP2	STVP1	STVP0	FRAD1	FRAD0
Default	—	—	0	0	0	0	0	0

Table 11.7 Register R3 setting

STVP [3:0]: adjust first line position by line

STVP3	STVP2	STVP1	STVP0	STV position adjust	Unit
0	0	0	0	0	T_H
0	0	0	1	+1	T_H
0	0	1	0	+2	T_H
0	0	1	1	+3	T_H
0	1	0	0	+4	T_H
0	1	0	1	+5	T_H
0	1	1	0	+6	T_H
0	1	1	1	+7	T_H
1	0	0	0	-1	T_H
1	0	0	1	-2	T_H
1	0	1	0	-3	T_H
1	0	1	1	-4	T_H
1	1	0	0	-5	T_H
1	1	0	1	-6	T_H
1	1	1	0	-7	T_H
1	1	1	1	-8	T_H

Table 11.8 Adiust first line position by line

FRAD [1:0]: Odd frame or Even frame advance control

FRAD1	FRAD0	Advance Frame	Notes
0	0	Default	Odd/Even frame Tstv are the same
0	1	Odd frame	Even frame Tstv = STVP setting + 1H
1	0	Even frame	Odd frame Tstv = STVP setting + 1H
1	1	Reserve	Reserve

Note : Please set the FRAD[1:0]=0.1 when CCIR601 NTSC/PAL、CCIR656 PAL mode；set the PRAD[1:0]=00 when CCIR656 NTSC mode for video decoder SAA7114。(Please refer the input timing of the "13-4) Data input format for CCIR601 Mode")

Table 11.9 Odd frame or Even frame advance control

- **Register R4**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CS	FRP	FRC	LPF	VS_POL	HS_POL	NPC_SET	NPC_IN
Default	1	0	1	1	0	0	0	1

Table 11.10 Register R4 setting

CS: Charge share function control.
CS=L, disable charge share function.
CS=H, enable charge share function.

FRP: Select normally white or normally black panel.
FRP=L, pass the input data for normally white panel.
FRP=H, inverse the input data for normally black panel.

FRC: Dithering ON/OFF control.
FRC=L, Dithering function disable.
FRC=H, Dithering function enable

LPF: Low pass filter function enable/disable in CCIR656/CCIR601 mode
LPF="L", Low pass filer function disable.
LPF="H", Low pass filer function enable

VS_POL: VS polarity setting.
VS_POL=L, negative polarity.
VS_POL=H, positive polarity.

Note: Please set the VS_POL=H when CCIR601 mode for video decoder SAA7114.
(Please refer the input timing of the "13-4) Data input format for CCIR601 Mode")

HS_POL: HS polarity setting.
HS_POL=L, negative polarity.
HS_POL=H, positive polarity.

NPC_SET: Set the NTSC/PAL auto detection or define by NPC_IN.
NPC_SET=L, auto detection.
NPC_SET=H, define by NPC_IN.

NPC_IN: Define the NTSC/PAL mode by SPI.
NPC_IN=L, PAL.
NPC_IN=H, NTSC.

- **Register R5**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	AUTO_DP	DISP_ON	A_TIME1	A_TIME0	B_TIME2	B_TIME1	B_TIME0	reserved
Default	1	0	0	1	0	1	0	—

Table 11.11 Register R5 setting

AUTO_DP: When power on, select blank image display time decided by A_TIME (bit 5, 4) or DISP_ON (bit 6).
AUTO_DP ="L", Blank image display time decided by DISP ON (bit 6).
AUTO_DP ="H", Blank image display time decided by A TIME (bit 5, 4).

DISP_ON: When AUTO_DP (bit 7) = "L", and DISP_ON = "H", blank image display off, then display normal image.

A_TIME [1:0]: When AUTO_DP(bit 7) = "H". the blank image display time is decided by A_TIME
00: blank image display time is 8 VS time
01: blank image display time is 16 VS time
10: blank image display time is 32 VS time
11: blank image display time is 64 VS time

B_TIME [2:0]: When into STB mode. the blank image display time is decided by B_TIME.
000: blank image display time is 3 VS time.
001: blank image display time is 4 VS time.
010: blank image display time is 5 VS time.
011: blank image display time is 6 VS time.
100: blank image display time is 7 VS time.
101: blank image display time is 8 VS time.
110: blank image display time is 9 VS time.
111: blank image display time is 10 VS time.

11-2) Power ON/OFF sequence

To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power ON: VCC1, GND → VDDA, VSSA → V1 to V10
Power OFF: V1 to V10 → VDDA, VSSA → VCC1, GND

11-3) Power ON Control

Source drive has a power ON sequence control function. There are two kinds of the mode. One is auto mode, and another is manual mode.

Auto Mode: When power is ON, blank data is outputted for 16-frames (default value) first, from the falling edge of the following VS signal. The blank data would be gray level 255 for normally white panel.
It can be defined in register R5 A_TIME1(bit 5) and A TIME0 (bit 4) when AUTO_DP(bit 7) = "H"

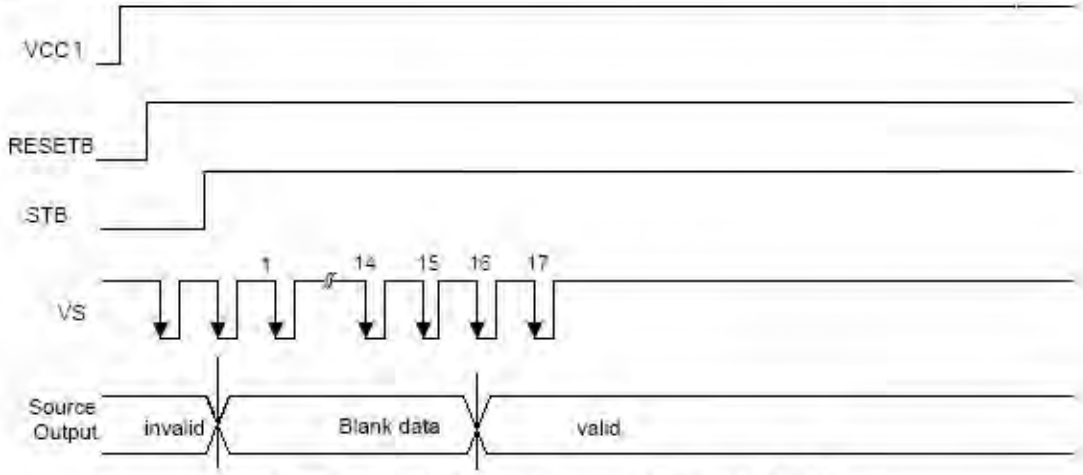


Figure 11-1 Power on control for Auto Mode

Manual Mode: When power is ON, you should set the register R5 AUTO_DP(bit 7) = "L" to stay at the manual mode. Blank data is outputted until the DISP_ON(bit 6) = H then display the normal image.

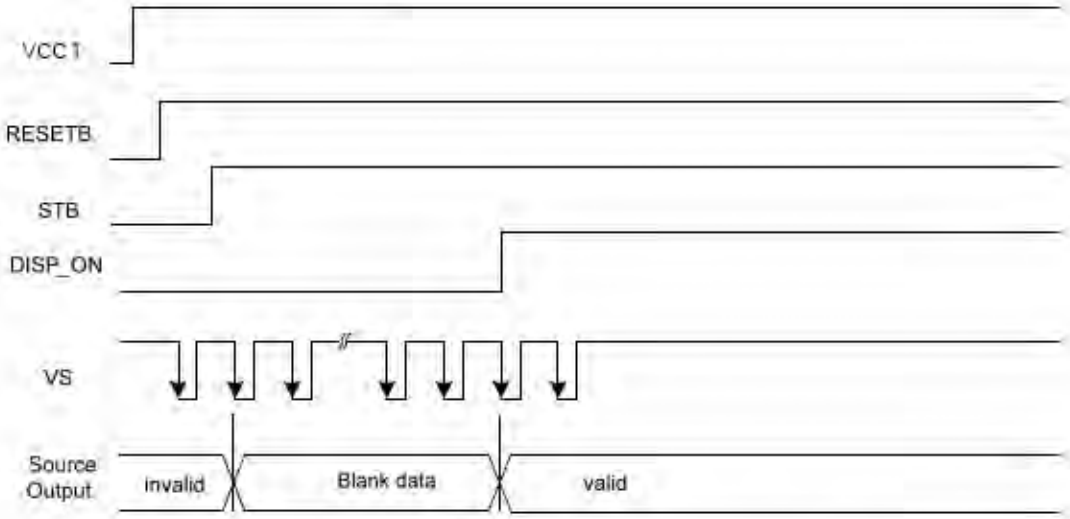


Figure 11-2 Power on control for Manual Mode

11-4) Standby ON/OFF Control

Source drive has a standby ON/OFF sequence control function. When STB pin is "L", blank data is outputted for 5-frames (default value) first, from the falling edge of the following VSYNC signal. The blank data would be gray level 255 for normally white panel. It can be defined in register R5 B_TIME[2:0] to adjust the frame number of the blank data.

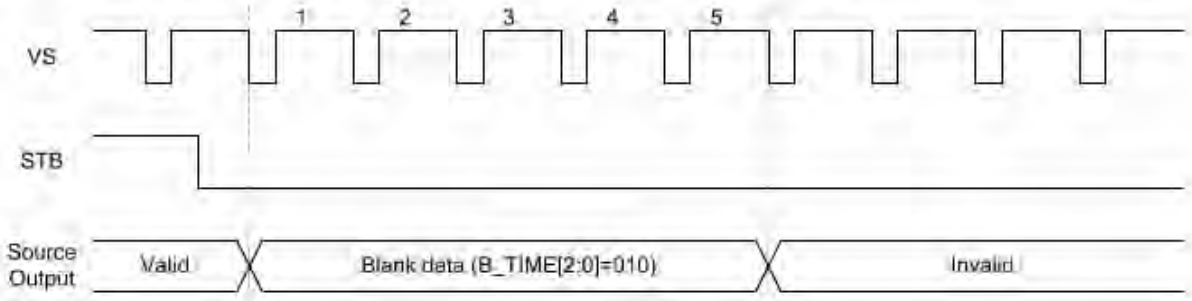


Figure 11-3 Standby ON/OFF Control

11-5) Reset when power on

Source drive is internally initialized by the global reset signal. RESETB. The reset input must be held for at least 1ms after power is stable.

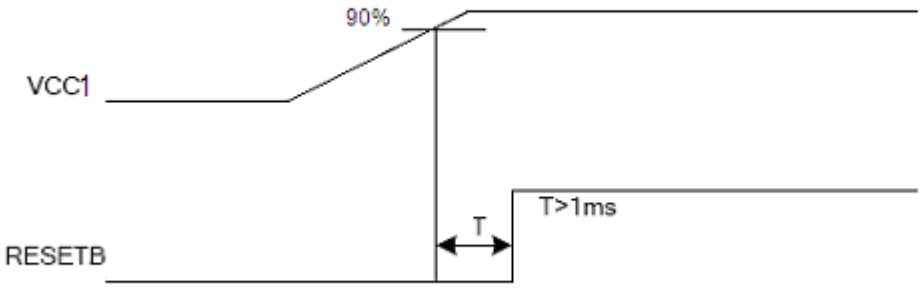


Figure 11-4 RESETB control after power stable

12. AC Characteristics

12-1) SPI timing characteristics

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPCK period	T_{CK}	60	-	-	ns
SPCK high width	T_{CKH}	30	-	-	ns
SPCK low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
SPENA to SPCK setup time	T_{CS}	20	-	-	ns
SPENA to SPDA hold time	T_{CE}	20	-	-	ns
SPENA high pulse width	T_{CD}	50	-	-	ns

12-2) Digital Serial RGB interface

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{CPH}	-	19.28	-	MHz
CLK period		T_{CPH}	-	51.87	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period		T_H	-	1224	-	T_{CPH}
HS pulse width		T_{WH}	5	90	-	T_{CPH}
HS-first horizontal data time		T_{HS}	172	204	235	T_{CPH}
DEN pulse width		T_{EP}	-	960	-	T_{CPH}
VS pulse width		T_{WV}	1	3	5	T_H
VS-DEN time	NTSC	T_{STV}	-	18	-	T_H
	PAL	T_{STV}	-	26	-	T_H
VS period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

Note: When SYNC mode is used, 1st data start from 204th CLK after HS falling (when STHD[5:0]=000000)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	100	-	T_{CPH}
CKV pulse width	T_{CKV}	-	72	-	T_{CPH}
HS-CKV time	T_1	-	48	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	81	-	T_{CPH}
STV setup time	T_{SUV}	-	42	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

12-3) Digital Parallel RGB interface

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{CPH}	-	6.43	-	MHz
CLK period		T_{CPH}	-	155.62	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period		T_H	-	408	-	T_{CPH}
HS pulse width		T_{WH}	5	30	-	T_{CPH}
HS-first horizontal data time		T_{HS}	36	68	99	T_{CPH}
DEN pulse width		T_{EP}	-	320	-	T_{CPH}
VS pulse width		T_{WV}	1	3	5	T_H
VS-DEN time	NTSC	T_{STV}	-	18	-	T_H
	PAL	T_{STV}	-	26	-	T_H
VS period	NTSC	T_V	-	262.5 / 262	-	T_H
	PAL	T_V	-	312.5 / 312	-	T_H

Note: When SYNC mode is used, 1st data start from 204th CLK after HS falling (when STHD[5:0]=000000)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	26	-	T_{CPH}
CKV pulse width	T_{CKV}	-	24	-	T_{CPH}
HS-CKV time	T_1	-	16	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	25	-	T_{CPH}
STV setup time	T_{SUV}	-	10	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

12-4) CCIR601 interface

(For 24.54MHz, NTSC mode)

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
CLK frequency	F_{CPH}	-	24.54	-	MHz
CLK period	T_{CPH}	-	40.7	-	ns
CLK pulse duty	T_{CWH}	40	50	60	%
HS period	T_H	-	1560	-	T_{CPH}
Horizontal active data area	T_{HA}	-	1280	-	T_{CPH}
VS pulse width	T_{WV}	-	1.5	-	T_H
VS-1st Data input time	T_{STV}	-	17	-	T_H
VS period	T_V	-	262.5	-	T_H

(For 27MHz)

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{CPH}	-	27	-	MHz
CLK period		T_{CPH}	-	37	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period	NTSC	T_H	-	1716	-	T_{CPH}
	PAL	T_H	-	1728	-	T_{CPH}
Horizontal active data area		T_{HA}	-	1440	-	T_{CPH}
VS pulse width		T_{WV}	-	1.5	-	T_H
VS-1st Data input time	NTSC	T_{STV}	-	17	-	T_H
	PAL	T_{STV}	-	24	-	T_H
VS period	NTSC	T_V	-	262.5	-	T_H
	PAL	T_V	-	312.5	-	T_H

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	100	-	T_{CPH}
CKV pulse width	T_{CKV}	-	96	-	T_{CPH}
HS-CKV time	T_1	-	52	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	72	-	T_{CPH}
STV setup time	T_{SUV}	-	46	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

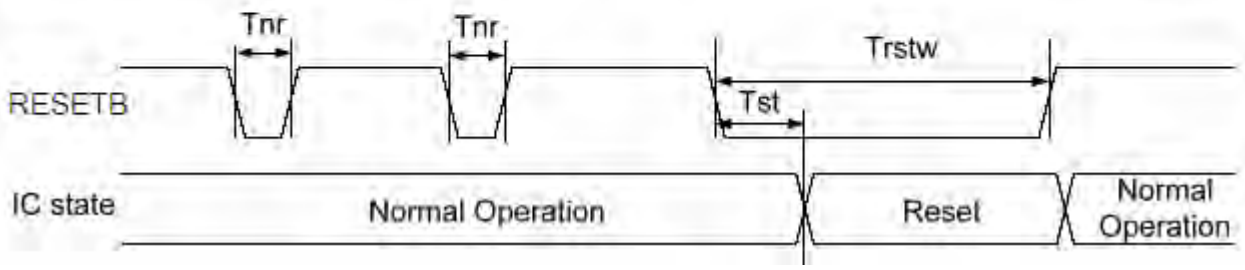
12-5) CCIR656 interface

PARAMETER		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
CLK frequency		F_{CPH}	-	27	-	MHz
CLK period		T_{CPH}	-	37	-	ns
CLK pulse duty		T_{CWH}	40	50	60	%
HS period	NTSC	T_H	-	1716	-	T_{CPH}
	PAL	T_H	-	1728	-	T_{CPH}
Horizontal active data area		T_{HA}	-	1440	-	T_{CPH}
VS-1st Data input time	NTSC	T_{STV}	-	22	-	T_H
	PAL	T_{STV}	-	28	-	T_H
VS period	NTSC	T_V	-	262.5	-	T_H
	PAL	T_V	-	312.5	-	T_H

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
OEV pulse width	T_{OEV}	-	100	-	T_{CPH}
CKV pulse width	T_{CKV}	-	96	-	T_{CPH}
HS-CKV time	T_1	-	52	-	T_{CPH}
HS-OEV time	T_2	-	8	-	T_{CPH}
HS-POL time	T_3	-	72	-	T_{CPH}
STV setup time	T_{SUV}	-	46	-	T_{CPH}
STV pulse width	T_{WSTV}	-	1	-	T_H

12-6) Hardware reset timing

PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
RESETB low pulse width		10	-	-	μs
Negative noise pulse width	T_{nr}	-	-	2	μs
Reset start time	T_{st}	2	-	-	μs



13. Waveform

Timing Controller Timing Chart

13-1) SPI timing

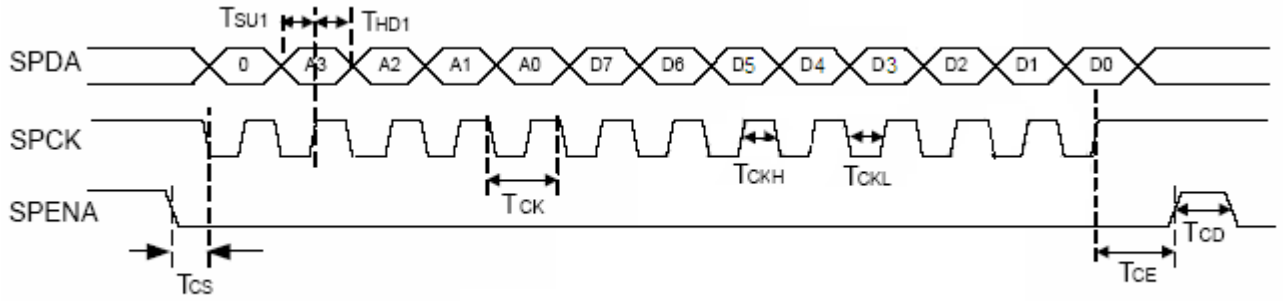


Figure 13-1 SPI timing

13-2) Clock and Data input waveforms

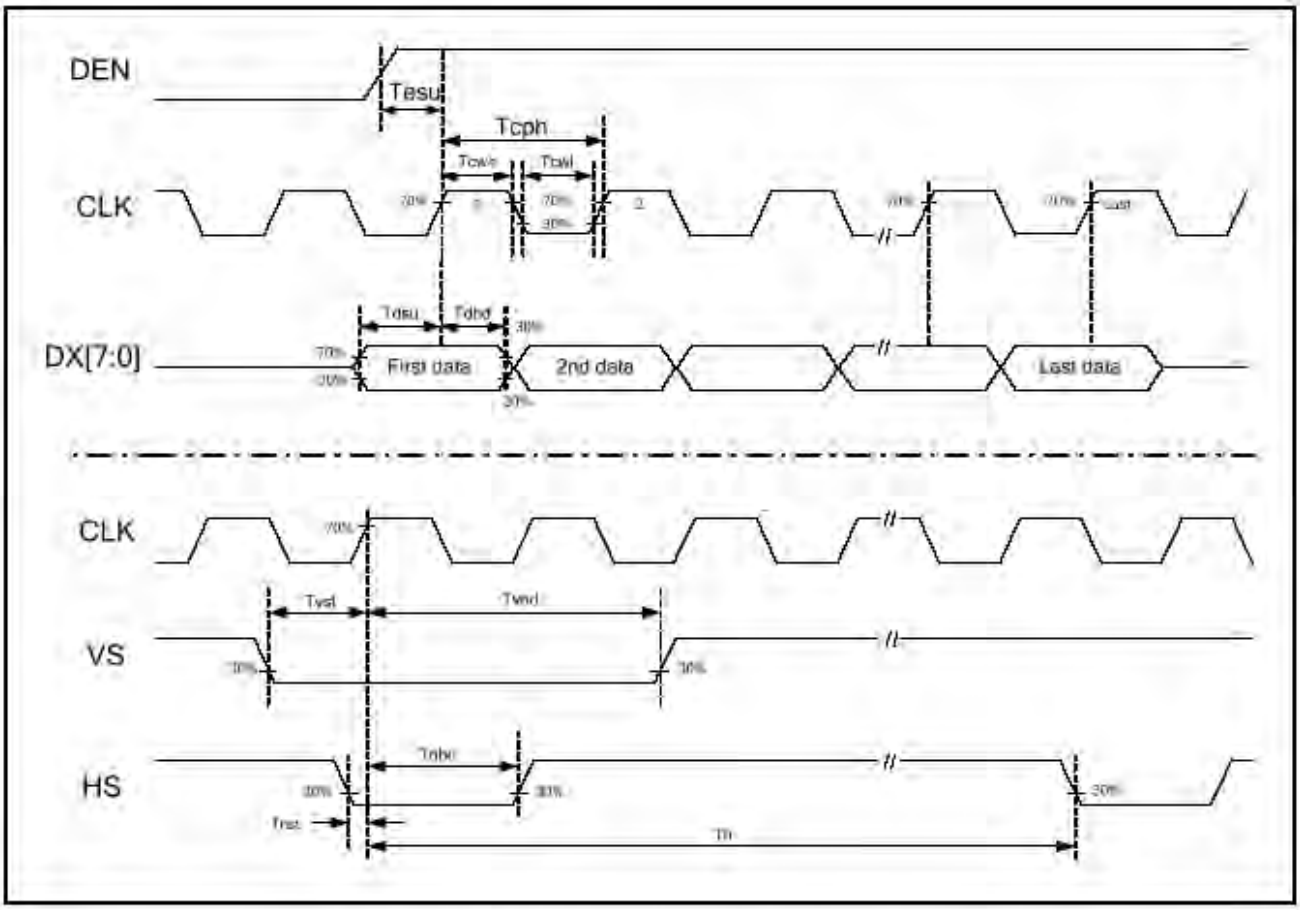


Figure 13-2 Clock and Data input waveforms.

13-3) Data input format for RGB Mode

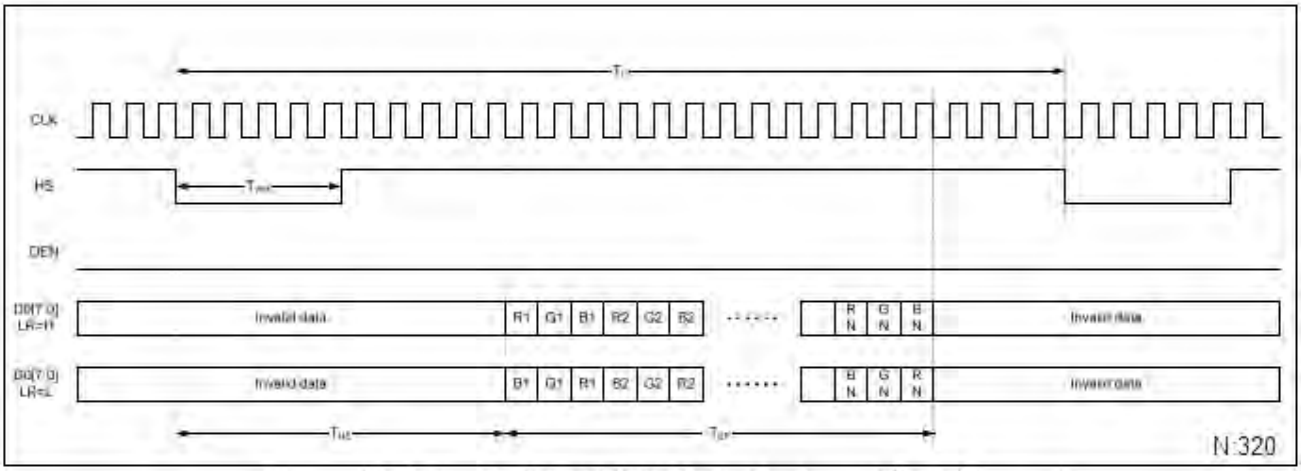


Figure 13-3 Serial RGB SYNC Mode Horizontal Data Format

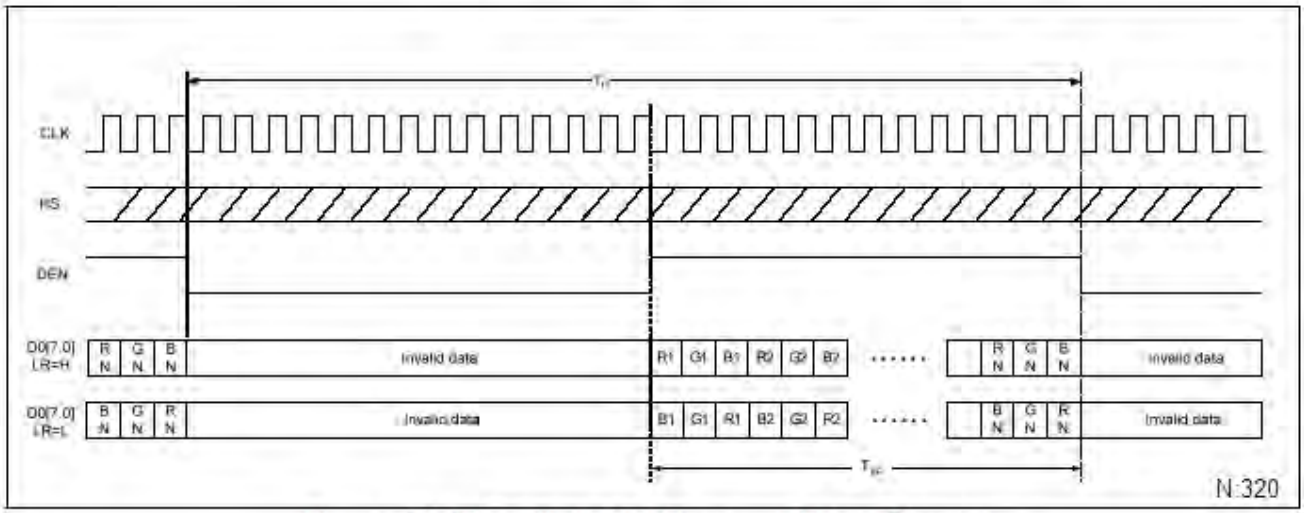


Figure 13-4 Parallel RGB Horizontal Data Format

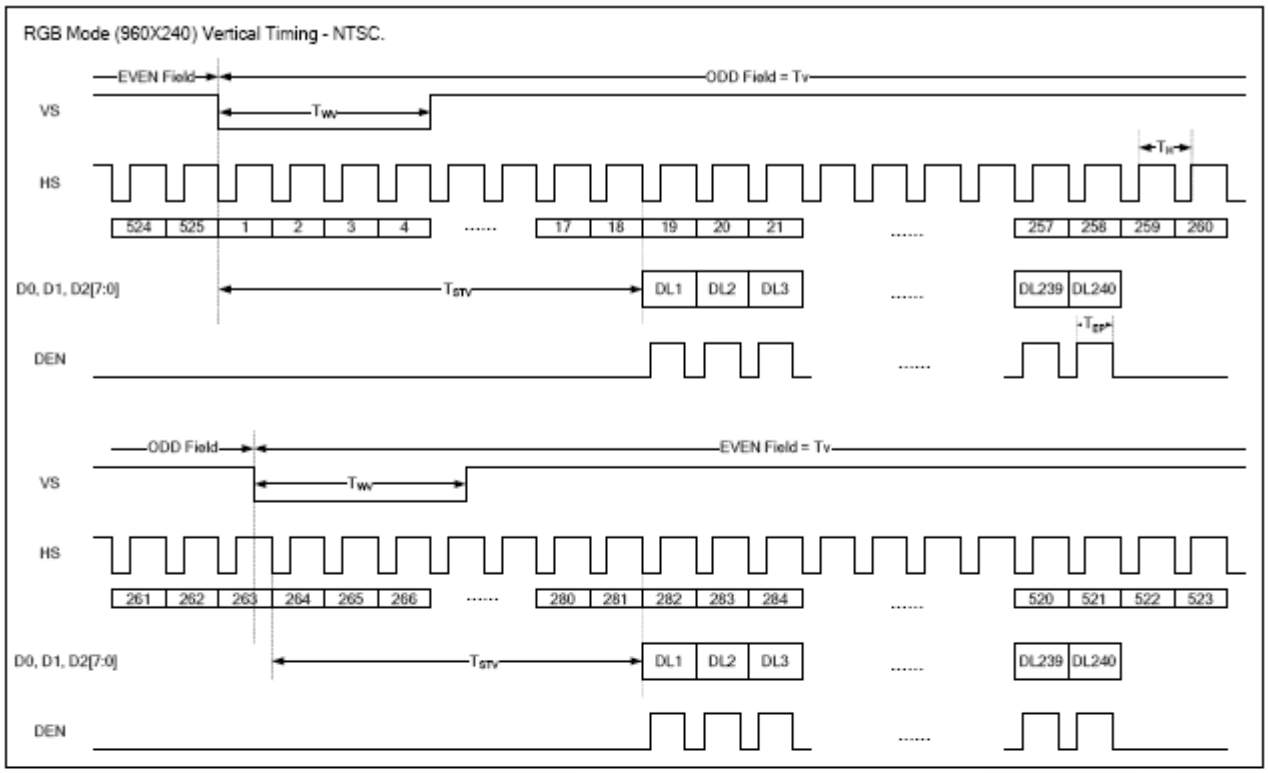


Figure 13-5 Digital RGB NTSC mode Vertical Data Format for 262.5T_H

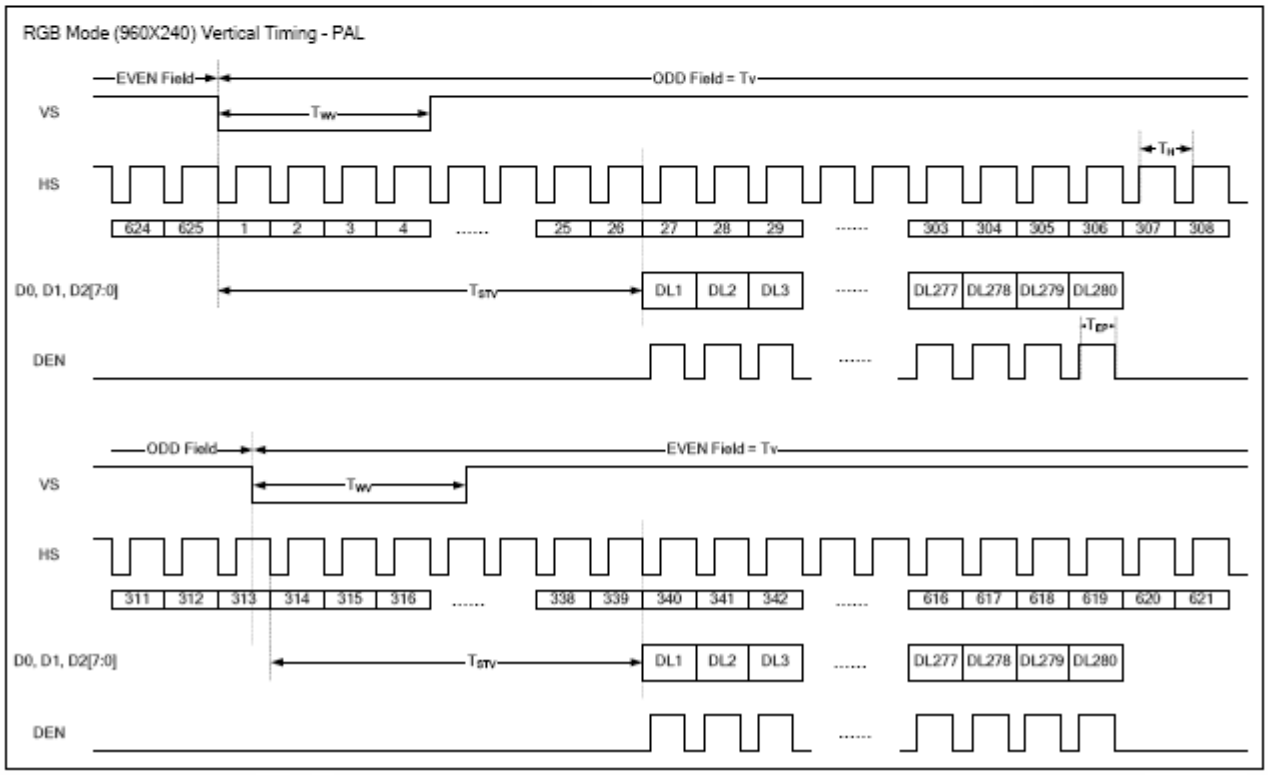


Figure 13-6 Digital RGB PAL mode Vertical Data Format for 312.5T_H

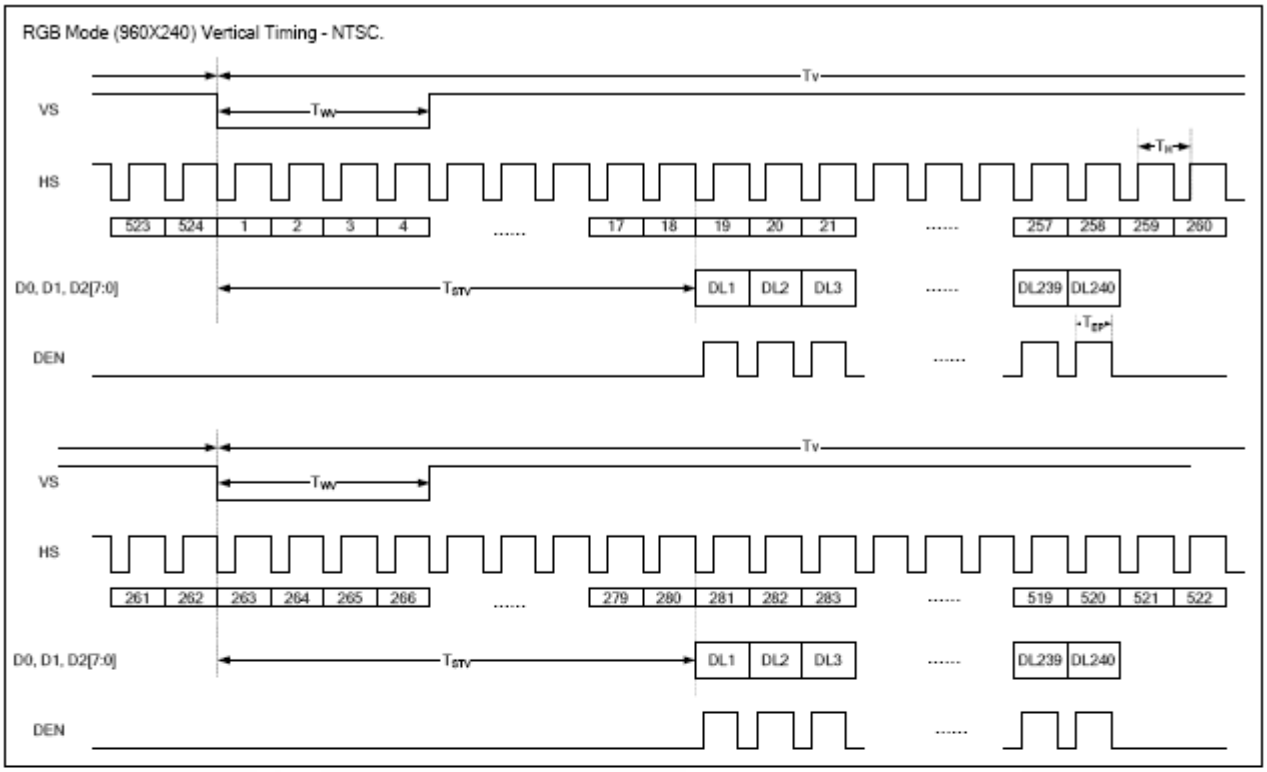


Figure 13-7 Digital RGB NTSC mode Vertical Data Format for 262T_H

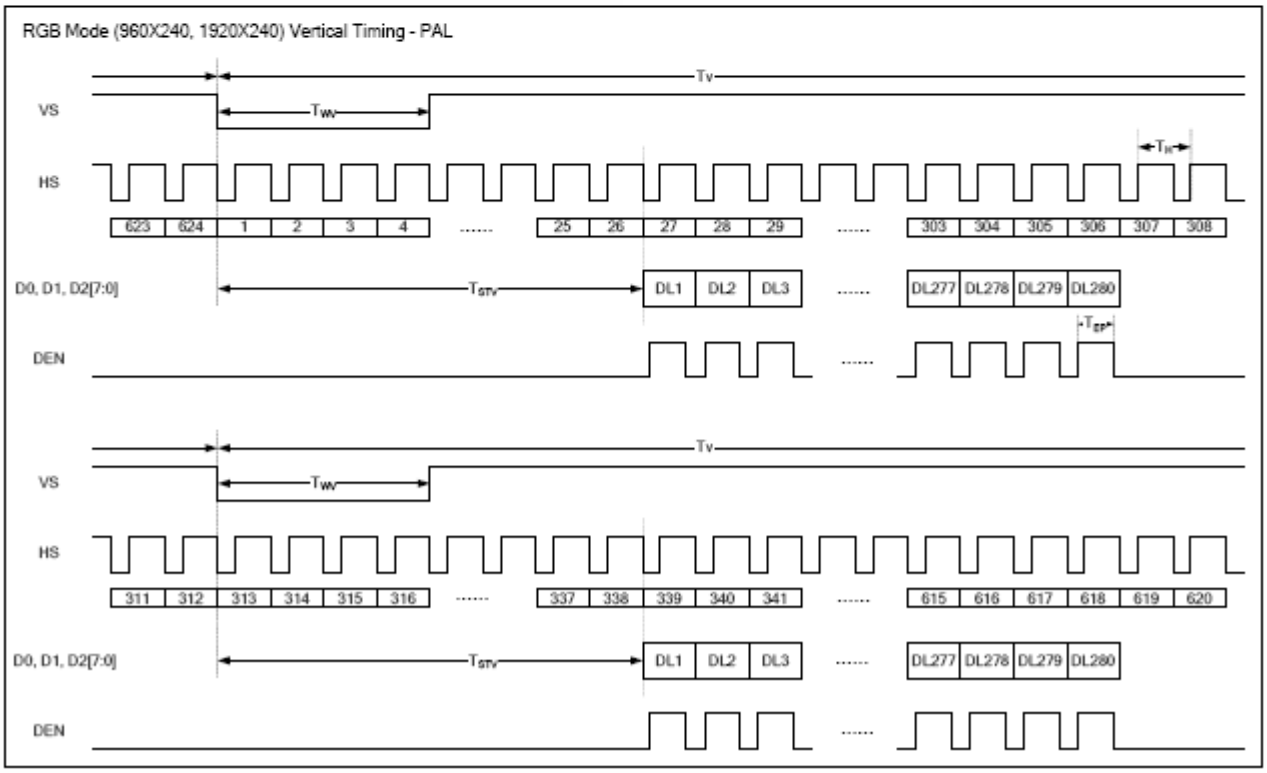


Figure 13-8 Digital RGB PAL mode Vertical Data Format for 312T_H

13-4) Data input format for CCIR601 Mode

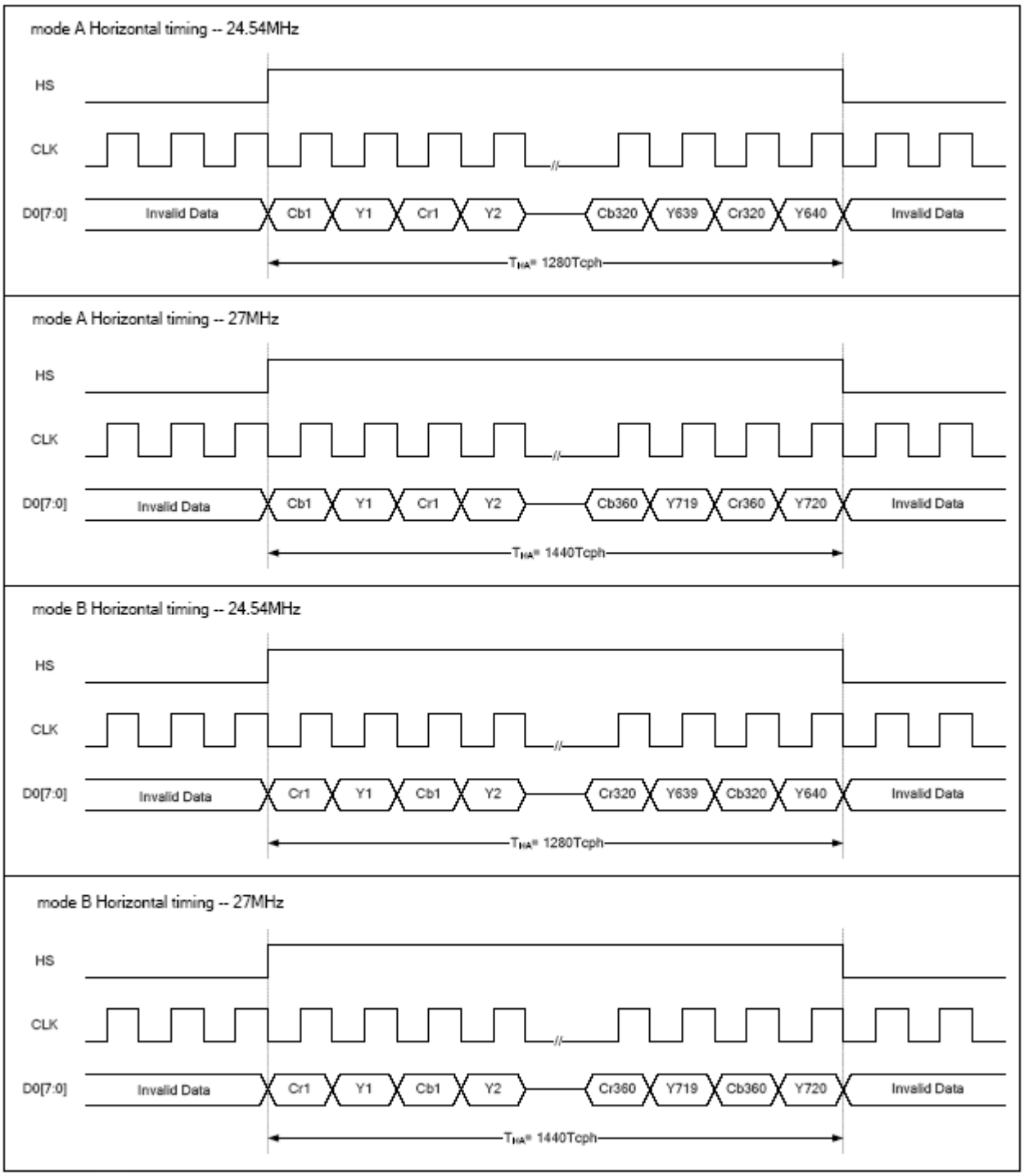


Figure 13-9 CCIR601 Horizontal Data Format

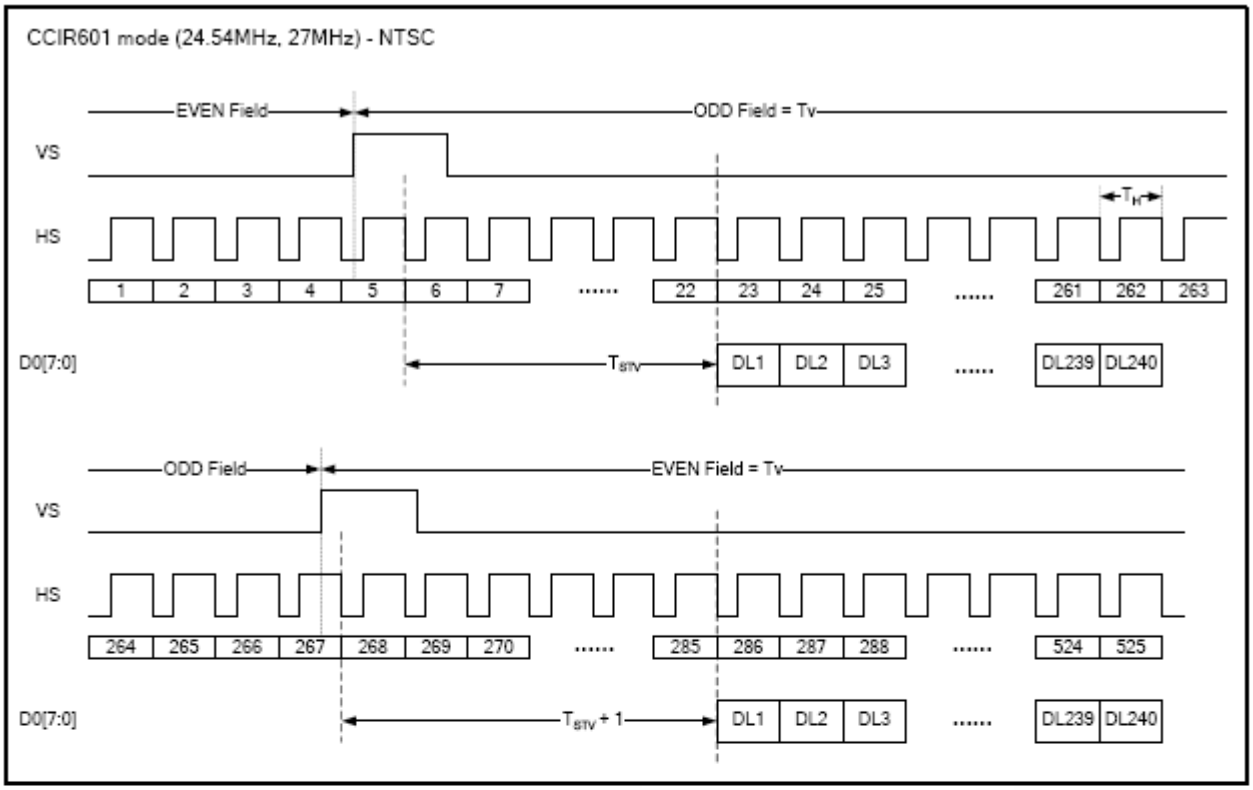


Figure 13-10 CCIR601 Vertical Data Format - NTSC

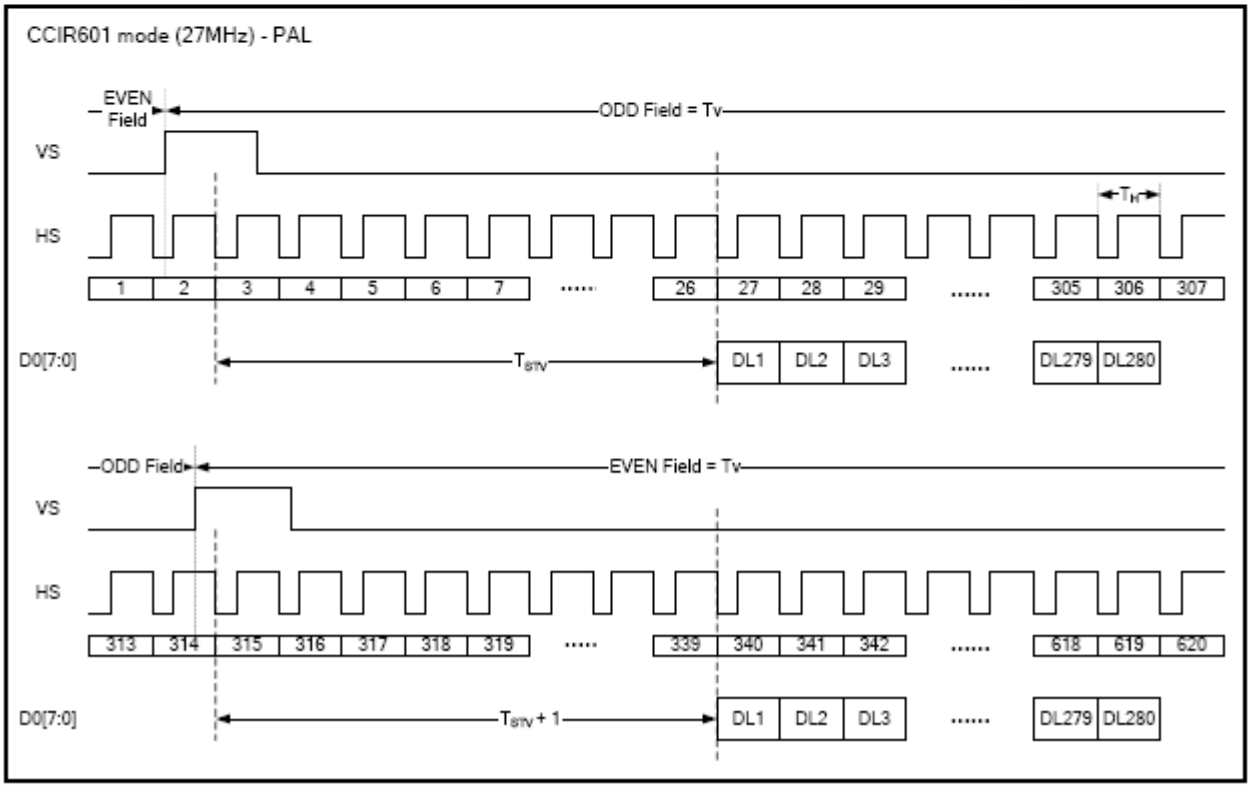


Figure 13-11 CCIR601 Vertical Data Format - PAL

13-5) Data input format for CCIR656 Mode

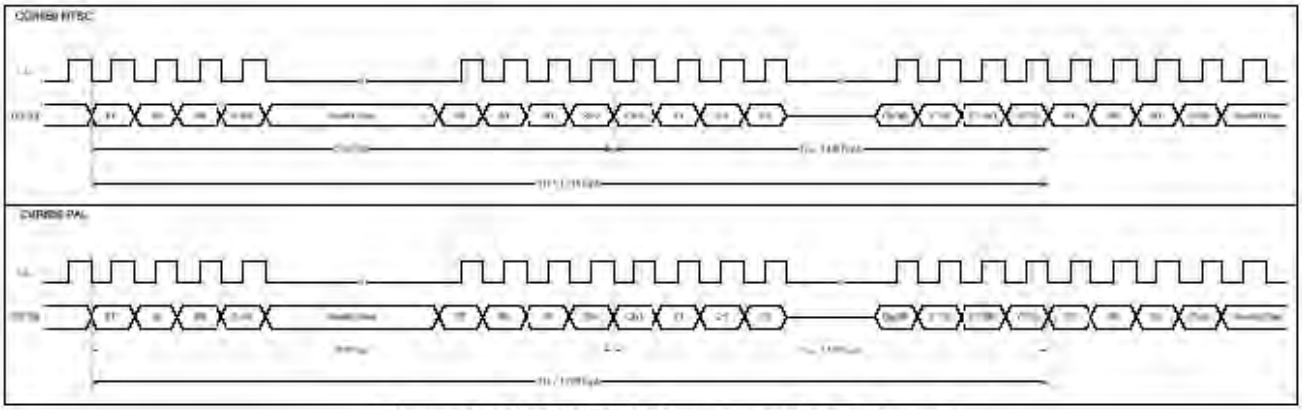


Figure13-12 CCIR656 Horizontal Data Format

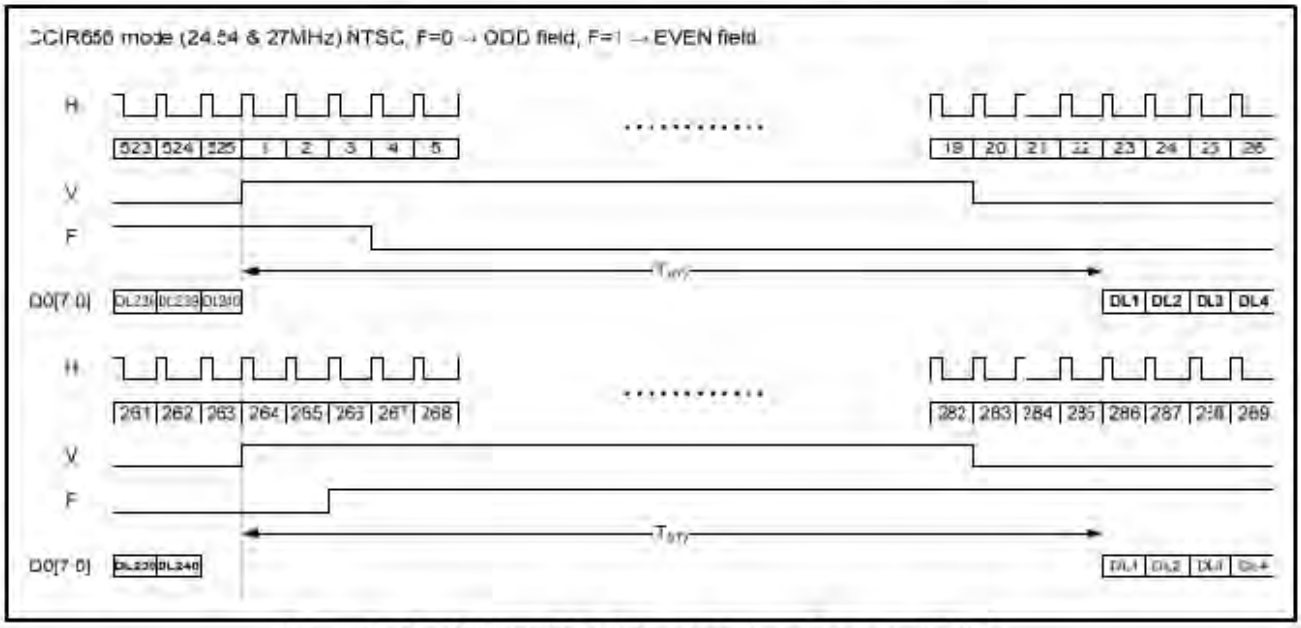


Figure13-13 CCIR656 NTSC Vertical Data Format - NTSC

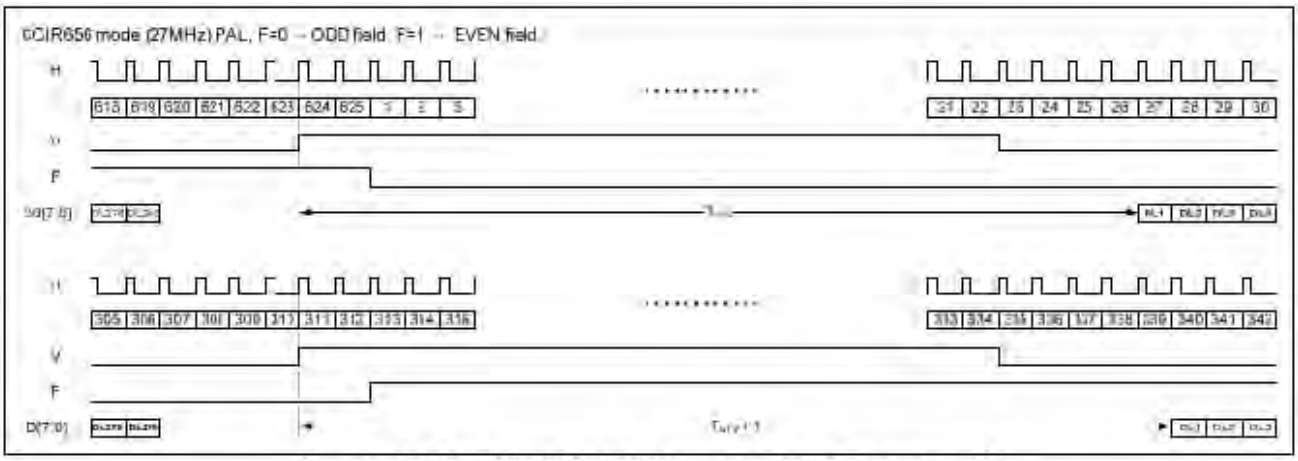


Figure 13-14 CCIR656 NTSC Vertical Data Format - PAL

13-6) The HS & VS timing of the ODD/EVEN field

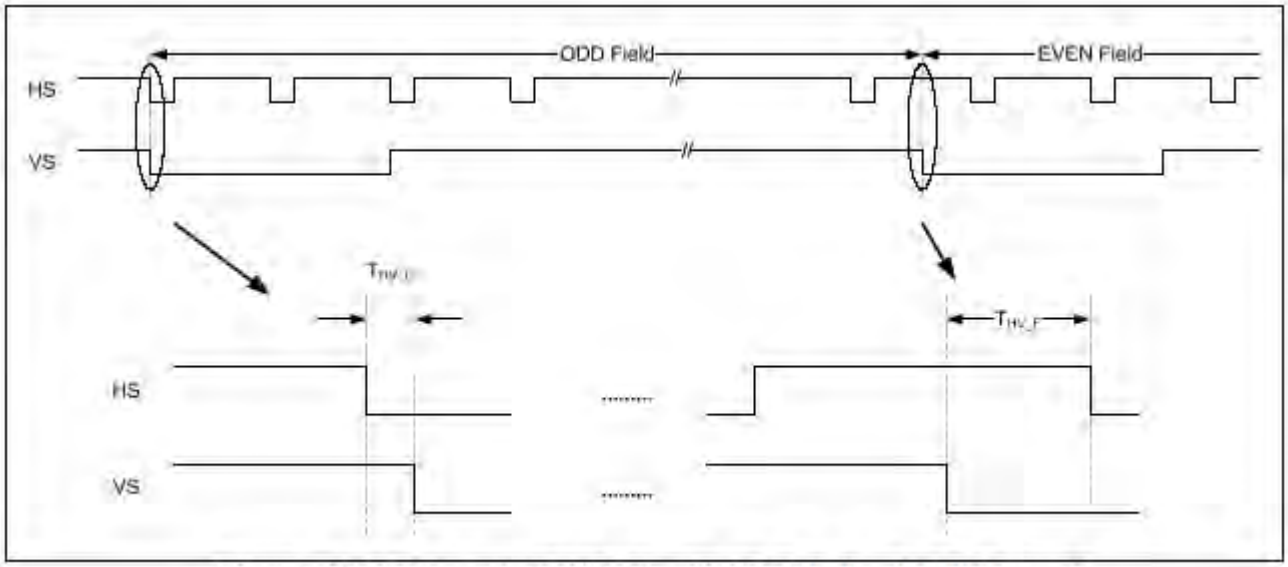
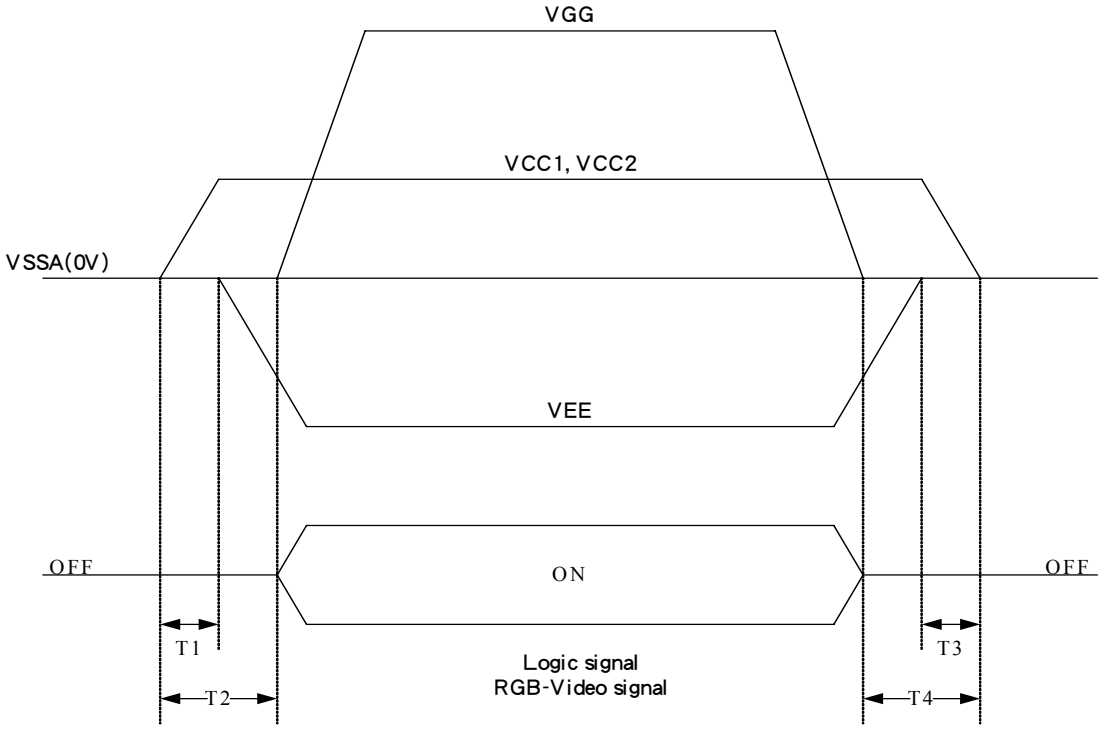


Figure13-15 Define the HSYNC to VSYNC timing for RGB mode

14. Power On Sequence

The Power on Sequence only effect by VCC1, VGG, VCC2, VSSA and VEE, the others do not care.



1) 10ms≦T1<T2
2) 0ms<T3≦T4≦10ms

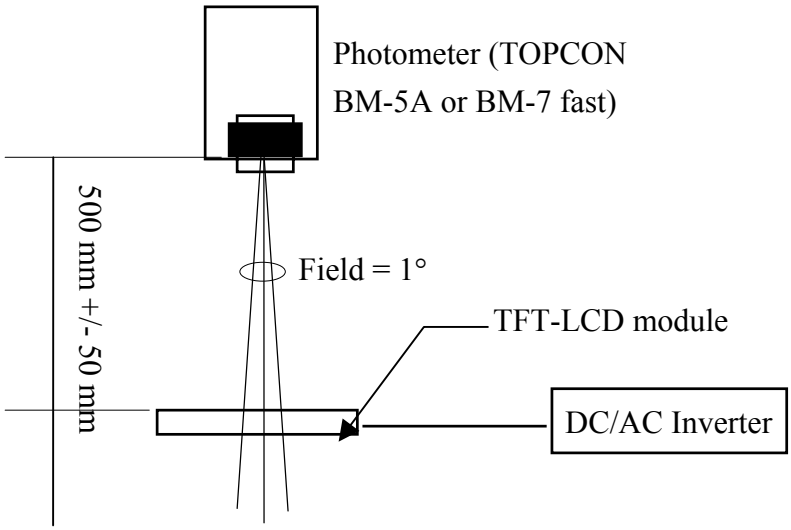
15. Optical Characteristics

15-1) Specification:

Ta = 25℃

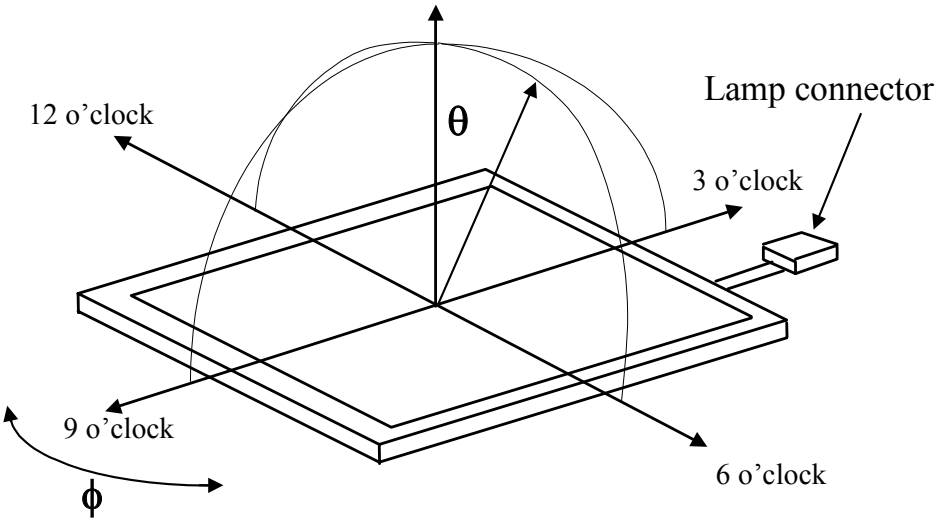
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ	CR≥10	55	60	-	deg	Note 15-1
	Vertical	θ (to 12 'clock)		35	40	-	deg	
		θ (to 6 o'clock)		50	55	-	deg	
Contrast Ratio		CR	Optimum direction	200	350	-	-	Note 15-2
Luminance		L	θ =0°/ ϕ =0°	350	400	-	cd/m²	Note 15-3
White Chromaticity		x	θ =0°/ ϕ =0°	0.27	0.30	0.33	-	
		y		0.31	0.34	0.37	-	
Response time	Rise	Tr	θ =0° ϕ =0°	-	15	30	ms	Note 15-4
	Fall	Tf		-	25	50	ms	
Luminance Uniformity		U	-	70	80	-	%	Note 15-5
Cross Talk Ratio		CTK	-	-	-	3.5	%	Note 15-6
Lamp Life Time			25℃	50000	-	-	hrs	I_{FL}=6mA

All the optical measurement shall be executed 30 minutes after backlight being turn-on. The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.



Optical characteristics measuring configuration

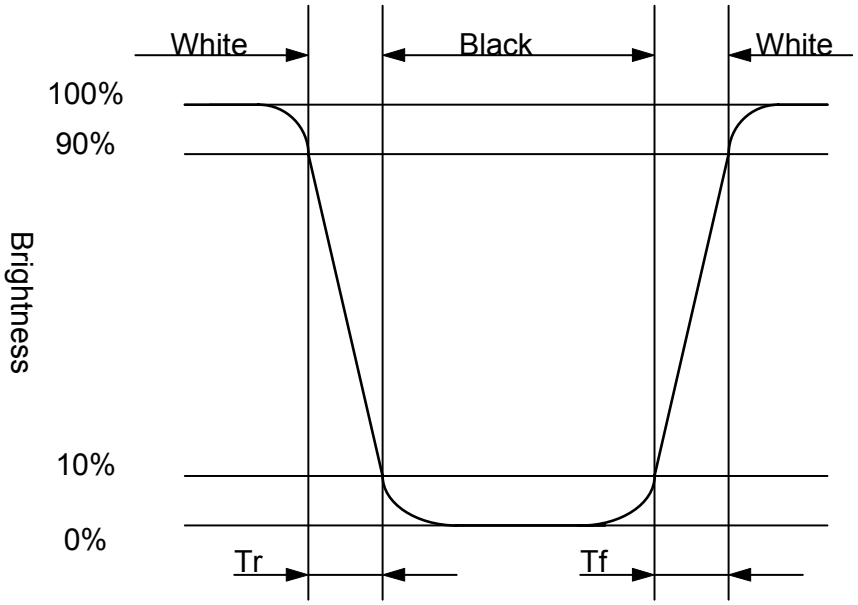
Note 15-1: The definitions of viewing angles are as follow



Note 15-2 : The definition of contrast ratio $CR = \frac{\text{Luminance at gray level 63}}{\text{Luminance at gray level 0}}$

Note 15-3:Topcon BM-5A or BM-7 fast luminance meter 1°field of view is used in the testing (after 30 minutes' operation). The typical luminance value is measured at lamp current 6.0 mA.

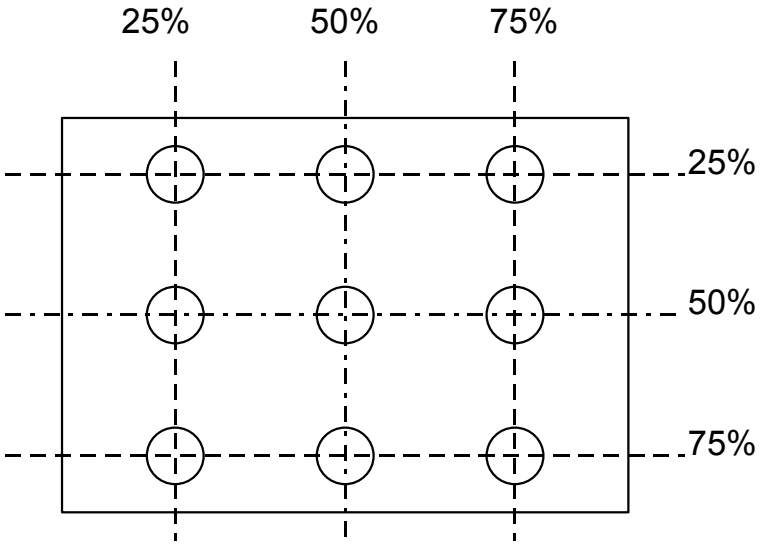
Note 15-4: Definition of Response Time Tr and Tf:



Note 15-5: The uniformity of LCD is defined as

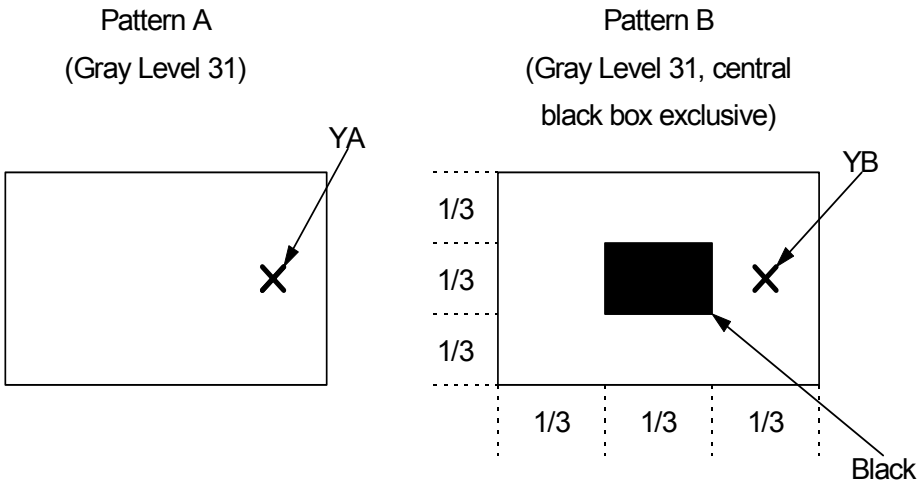
$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

Luminance meter : BM-5A or BM-7 fast(TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module
The test pattern is white (Gray Level 63).



Note 15-6: Cross Talk (CTK) = $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A
YB: Brightness of Pattern B
Luminance meter : BM 5A (TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module



✕: Measuring Point (A and B are at the same point.)

16. Handling Cautions

16-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.

1.The noise from the backlight unit will increase.

2.The output from inverter circuit will be unstable.

3.In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

16-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

16-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.

b) Therefore, do not change any adjusted values. If adjusted values are changed, the Specifications described may not be satisfied.

16-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

f) Please adjust the voltage of common electrode as material of attachment by 1 module.

17. Reliability Test

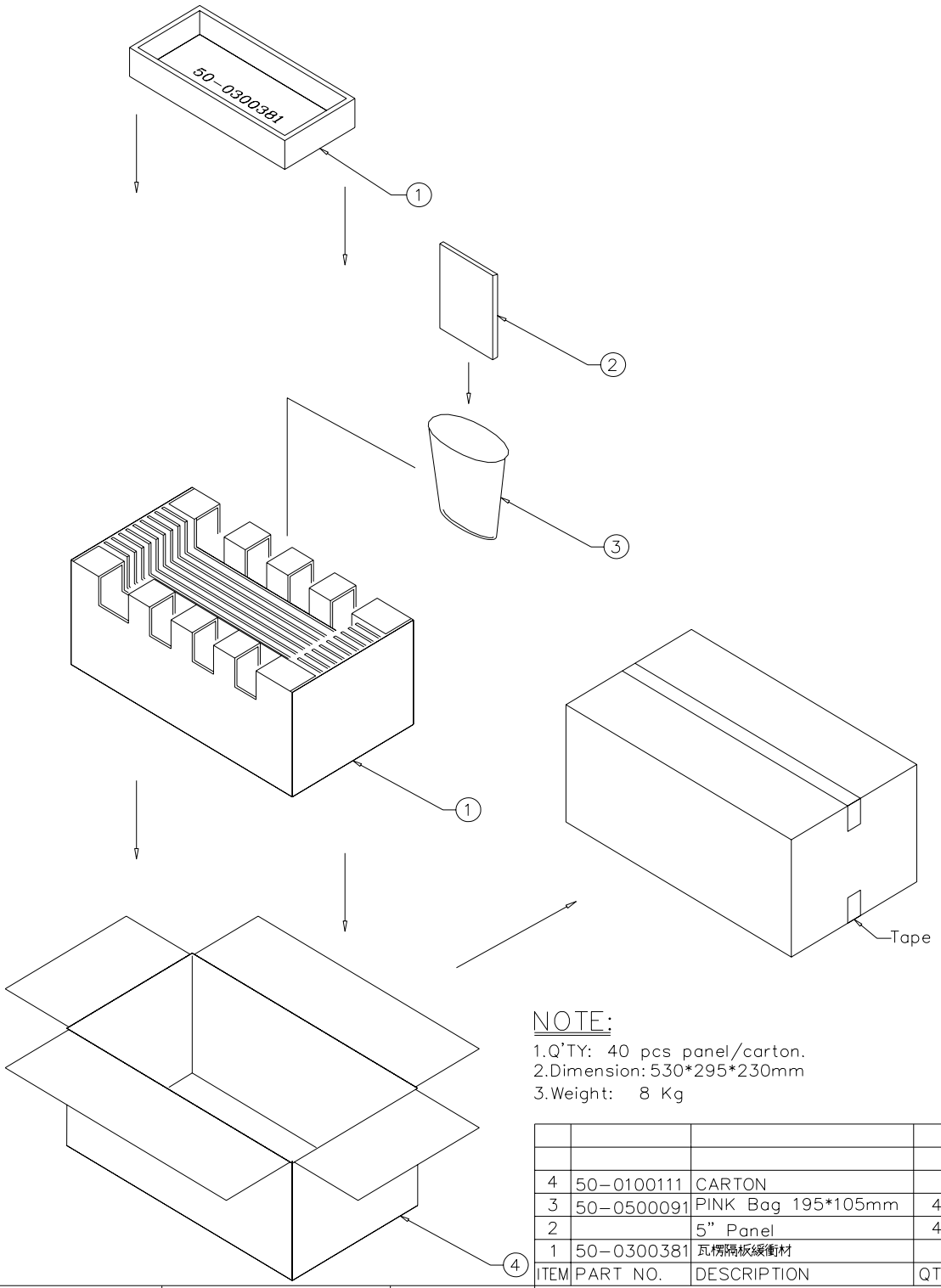
No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80℃, 240 hrs
2	Low Temperature Storage Test	Ta = -30℃, 240 hrs
3	High Temperature Operation Test	Ta = +70℃, 240 hrs
4	Low Temperature Operation Test	Ta = -25℃, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-25℃→ +70℃, 200 Cycles 30 min 30 min
7	Vibration Test (non-operating)	Frequency：10 ~ 55 H_Z Amplitude：1.5 mm Sweep time: 11 mins Test Period : 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction : ±X, ±Y, ±Z Cycle : 3 times
9	Electrostatic Discharge Test (non-operating)	200pF , 0Ω ±200V 1 time / each terminal

Ta: ambient temperature
Note: The protective film must be removed before temperature test

[Criteria]
In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image).All the cosmetic specification is judged before the reliability stress.

18.Packing

ZONE	REV.	DOCUUMENT NO.	DESCRIPTION	DATE	REV.BY



NOTE:

1.Q'TY: 40 pcs panel/carton.
2.Dimension: 530*295*230mm
3.Weight: 8 Kg

ITEM	PART NO.	DESCRIPTION	QTY	REMARK
4	50-0100111	CARTON	1	
3	50-0500091	PINK Bag 195*105mm	40	抗靜電
2		5" Panel	40	
1	50-0300381	瓦楞隔板緩衝材	1	上蓋+ 底座

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK

元太科技工業股份有限公司
Prime View International Co., Ltd.

APPROVE	Franks	'03.03.17	SCALE	UNIT	SHEET 1 OF 1	DWG.TITLE: 5" Model Packing Draw
CHECK	Franks	'03.03.17				
DRAWN	Jimmyc	'03.03.17	MTL.NO.		DWG FILE:	REV. 01 / A4 SIZE