***Version : 1.6***

# TECHNICAL SPECIFICATION

# MODEL NO. : PW045XS1

☐Customer's Confirmation

Customer

Date

By

☐PVI's Confirmation

Confirmed By

Prepared By

**PRIME VIEW INTERNATIONAL CO.,LTD.**
3,LI SHIN RD. 1,SCIENCE-BASED INDUSTRIAL PARK,HSINCHU,TAIWAN,R.O.C.
http://www.pvi.com.tw

Date : Oct. 06, 2004

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# *TECHNICAL SPECIFICATION*

## *CONTENTS*

1. Application

This technical specification applies to 4.5” color TFT-LCD module , PW045XS1. The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system..

2. Features

. Compatible with NTSC & PAL system

. Pixel in stripe configuration

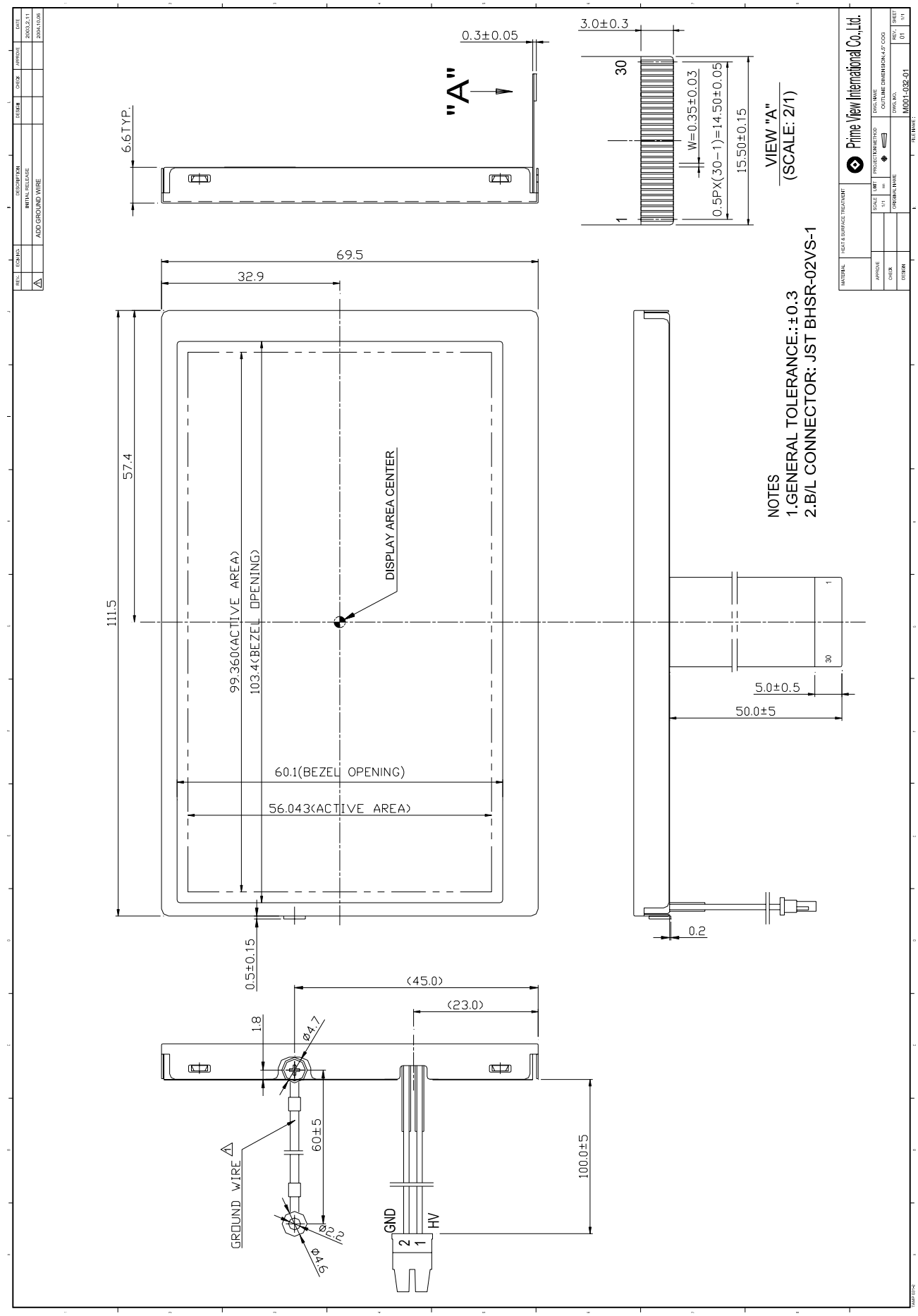
. Slim and compact

. Image Reversion : Up/Down and Left/Right

3. Mechanical Specifications

| Parameter | Specifications | Unit |
|---|---|---|
| Screen Size | 4.5 (diagonal) | inch |
| Display Format | 960×234 | dot |
| Active Area | 99.36(H)× 56.0(V) | mm |
| Dot Pitch | 0.1035 (H)×0.2395 (V) | mm |
| Pixel Configuration | Stripe | |
| Outline Dimension | 111.5(W)× 69.5(H)× 6.6(D)(typ.) | mm |
| Surface Treatment | Anti – Glare | |
| Weight | 84±5 | g |

4. Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

TFT-LCD Module Connector
FPC Down Connect , 30Pins , Pitch : 0.5 mm

| Pin No | Symbol | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | GND | - | Ground for logic circuit | |
| 2 | $V_{CC}$ | I | Supply voltage of logic control circuit for gate driver | Note 5-3 |
| 3 | NC | - | No connection | |
| 4 | $V_{EE}$ | I | Negative power for gate driver | Note 5-4 |
| 5 | NC | - | No connection | |
| 6 | $V_{GH}$ | I | Positive power for gate driver | Note 5-5 |
| 7 | NC | - | No connection | |
| 8 | DIO1 | I/O | Vertical start pulse | Note 5-1 |
| 9 | DIO2 | I/O | Vertical start pulse | |
| 10 | CPV | I | Shift clock for gate driver | |
| 11 | U/D | I | Up / Down Control for gate driver | Note 5-1 |
| 12 | XOE3 | I | Output enable for gate driver | |
| 13 | XOE2 | I | Output enable for gate driver | |
| 14 | XOE1 | I | Output enable for gate driver | |
| 15 | $V_{COM}$ | I | Common electrode voltage | |
| 16 | STH1 | I/O | Start pulse for source driver | Note 5-2 |
| 17 | $V_{SS2}$ | - | Ground for analog circuit | |
| 18 | $V_R$ | I | Video Input R | |
| 19 | $V_G$ | I | Video Input G | |
| 20 | $V_B$ | I | Video Input B | |
| 21 | $V_{SS1}$ | - | Ground for digital circuit | |
| 22 | $V_{DD2}$ | I | Supply power for analog circuit | Note 5-6 |
| 23 | CPH1 | I | Sampling and shift clock for source driver | |
| 24 | CPH2 | I | Sampling and shift clock for source driver | |
| 25 | CPH3 | I | Sampling and shift clock for source driver | |
| 26 | $V_{DD1}$ | I | Supply power for digital circuit | Note 5-7 |
| 27 | R/L | I | Left / Right Control for source driver | Note 5-2 |
| 28 | NC | I | No Connection | |
| 29 | OEH | I | Output enable for source driver | |
| 30 | STH2 | I/O | Start pulse for source driver | Note 5-2 |

Note 5-1

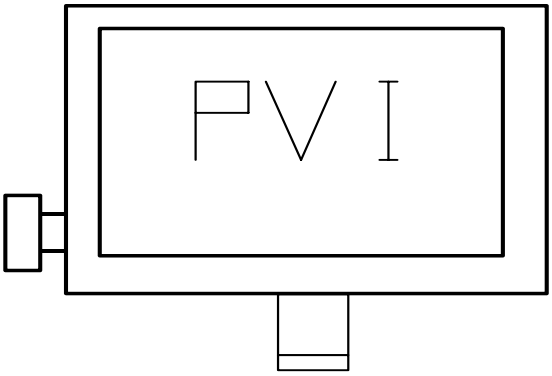
| U/D | DIO1 | DIO2 | scanning direction |
|---|---|---|---|
| Vcc | Input | output | down to up |
| GND | Output | input | up to down |

Note 5-2

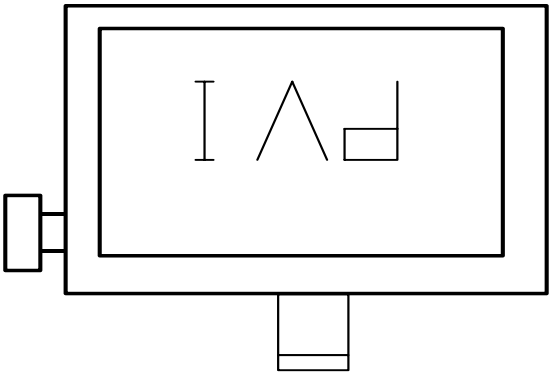
| R/L | STH1 | STH2 | scanning direction |
|---|---|---|---|
| Vcc | output | input | left to right |
| GND | input | output | right to left |

The definitions of Note 5-1,5-2

U/D(PIN 11)=Low R/L(PIN 27)=High



U/D(PIN 11)=High R/L(PIN 27)=Low



Note 5-3 : $V_{CC}$ TYP.＝+5V

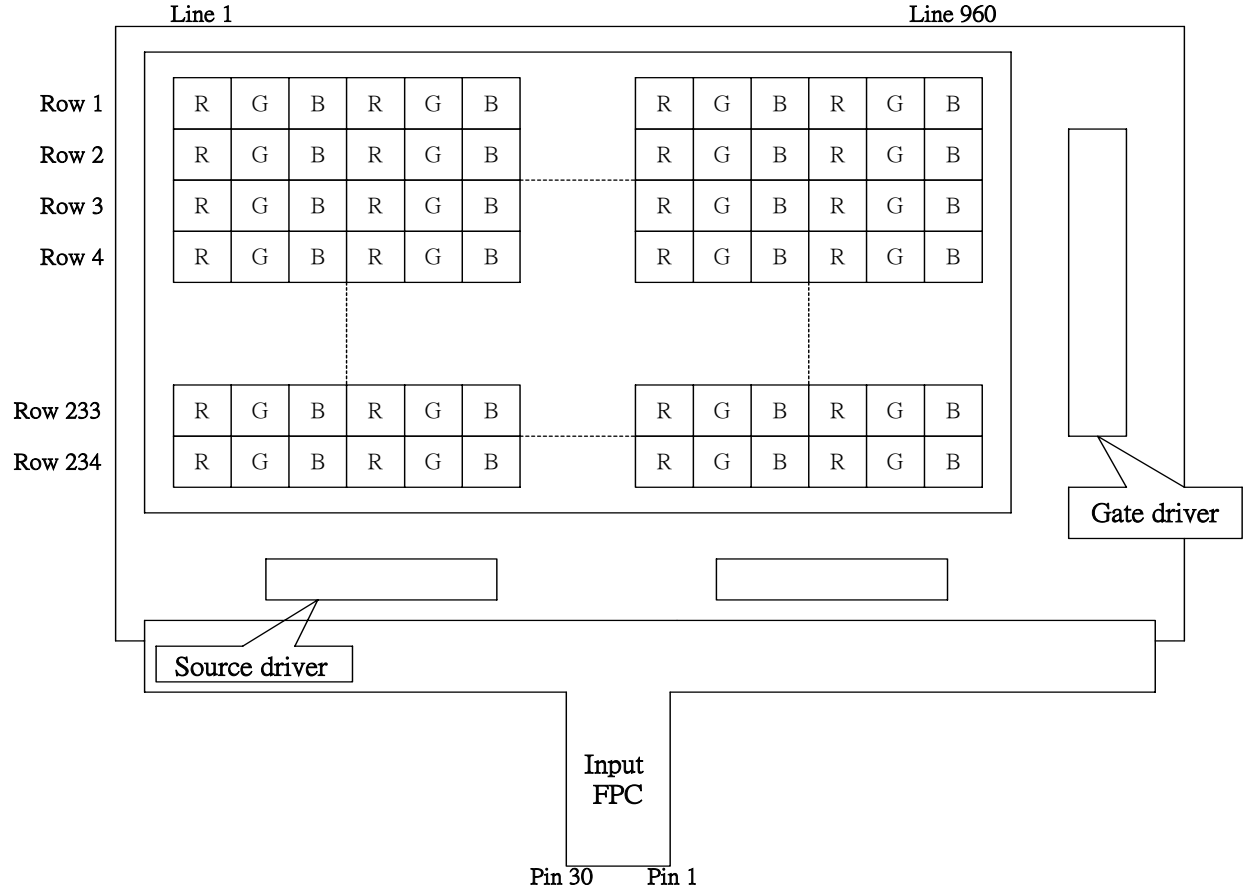
Note 5-4 : $V_{EE}$ TYP.＝-12V

Note 5-5 : $V_{GH}$ TYP.＝+17V

Note 5-6 : $V_{DD2}$ TYP.＝+5V

Note 5-7 : $V_{DD1}$ TYP.＝+3.3V

6. Pixel Arrangement and Input Connector Pin NO.



7. Absolute Maximum Ratings :

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

GND = 0 V， Ta = 25 ℃

| Parameter | | Symbol | MIN. | MAX. | Unit | Remark |
|---|---|---|---|---|---|---|
| Supply Voltage For Source Driver | | $V_{DD2}$ | -0.3 | +5.8 | V | |
| | | $V_{DD1}$ | -0.3 | +7.0 | V | |
| Supply Voltage For Gate Driver | | $V_{CC}$ | -0.3 | +6.0 | V | |
| | | $V_{GH}$-$V_{EE}$ | -0.3 | +40.0 | V | |
| | H Level | $V_{GH}$ | -0.3 | +25.0 | V | |
| | L Level | $V_{EE}$ | -16 | +0.3 | V | |
| Analog Signal Input Level | | $V_R$,$V_G$,$V_B$ | -0.2 | $V_{DD1}$+0.2 | V | Note 7-1 |
| Storage Temperature | | | -10 | +70 | ℃ | |
| Operation Temperature | | | 0 | +60 | ℃ | Note 7-2 |

Notes 7-1 : Analog Input Voltage means $V_R$,$V_G$,$V_B$.

Notes 7-2 : Operating Temperature define that contrast, response time, other display optical character are Ta=+25.

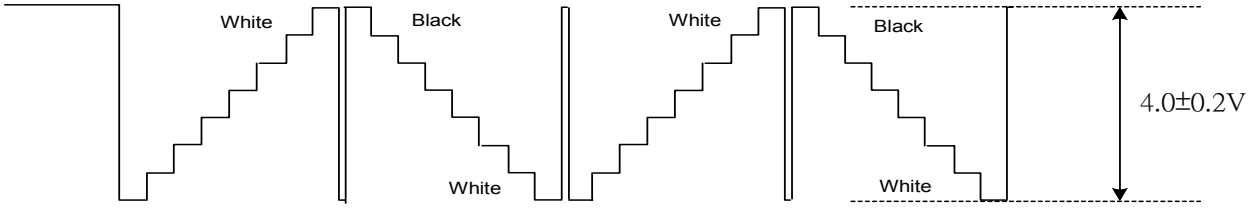
8. Electrical Characteristics

8-1) Operating Condition

| Parameter | | Symbol | MIN. | Typ. | MAX. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Supply Voltage For Source Driver | Analog | $V_{DD2}$ | +4.5 | +5.0 | +5.5 | V | |
| | Logic | $V_{DD1}$ | +3.0 | +3.3 | +3.6 | V | |
| Supply Voltage For Gate Driver | H level | $V_{GH}$ | +15 | +17 | +19 | V | |
| | L level | $V_{EE\ DC}$ | -13 | -12 | -10.5 | V | DC Component of $V_{EE}$ |
| | | $V_{EE\ AC}$ | | +6.0 | | $V_{P-P}$ | AC Component of $V_{EE}$ |
| | Logic | $V_{CC}$ | +4.5 | +5.0 | +5.5 | V | |
| Analog Signal input Level | Amplitu | | +0.3 | | $V_{CC}$-0.3 | V | |
| Digital input voltage | H level | $V_{IH}$ | 0.7 $V_{DD1}$ | - | $V_{DD1}$ | V | |
| | L level | $V_{IL}$ | -0.3 | - | 0.3 $V_{DD1}$ | V | |
| Digital output voltage | H level | $V_{OH}$ | 0.7 $V_{DD1}$ | - | $V_{DD1}$ | V | |
| | L level | $V_{OL}$ | -0.3 | - | 0.3 $V_{DD1}$ | V | |
| $V_{COM}$ | | $V_{COM\ AC}$ | - | +6.0 | - | $V_{P-P}$ | AC Component of $V_{COM}$ |
| | | $V_{COM\ DC}$ | 1.10 | 1.30 | 1.50 | V | DC Component of $V_{COM}$ Note 8-1 |

Note 8-1 : PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is 1.3V±1V , every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

Note 8-2: Both NTSC and PAL system Video Signal input waveform is based on 8 steps gray scale.




8-2) Current Consumption (GND=0V)

Ta= 25 ℃

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Current for Driver | $I_{CC}$ | $V_{CC}$=+5V | - | 0.004 | 0.006 | mA | |
| | $I_{EE}$ | $V_{EE}$=-12V | - | 0.725 | 1.08 | mA | |
| | $I_{GH}$ | $V_{GH}$=+17V | - | 0.08 | 0.12 | mA | |
| | $I_{DD1}$ | $V_{DD1}$=+3.3V | - | 1.2 | 3.0 | mA | |
| | $I_{DD2}$ | $V_{DD2}$=+5V | - | 7.0 | 10.0 | mA | |

8-3) Backlight driving & Power Consumption

| Pin No | Symbol | Description | Remark |
|---|---|---|---|
| 1 | VL1 | Input terminal (Hi voltage side) | |
| 2 | VL2 | Input terminal (Low voltage side) | Note 8-3 |

Note 8-3 : Low voltage side of backlight inverter connects with Ground of inverter circuits.

Ta= 25 ℃

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Lamp voltage | $V_L$ | 350 | 371 | 400 | Vrms | |
| Lamp current | $I_L$ | 3 | 6 | 7 | mA | Note 8-4 |
| Lamp frequency | $P_L$ | 45 | 60 | - | KHz | Note 8-5 |
| Kick-off voltage(25℃) | Vs | - | - | 610 | Vrms | Note 8-6 |
| Kick-off voltage(0℃) | Vs | - | - | 830 | Vrms | Note 8-6 |

Note 8-4 : In order to satisfy the quality of B/L , no matter use what kind of inverter , the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-5 : The waveform of lamp driving voltage should be as closed to a perfect SIN wave as possible.

Note 8-6: This value is not output voltage of inverter.
The voltage of inverter must larger than the starting voltage.
The kick-off time must larger than 1 second.

Power Consumption Ta= 25 ℃

| Parameter | Symbol | Conditions | TYP. | Unit | Remark |
|---|---|---|---|---|---|
| LCD Panel Power Consumption | | | 49.0 | mW | Note 8-7 |
| Backlight Lamp Power Consumption | | | 2.23 | W | Note 8-8 |
| Total Power Consumption | | | 2.28 | W | |

Note 8-7：The power consumption for backlight is not included.

Note 8-8：Backlight lamp power consumption is calculated by $I_L \times V_L$.

8-4) Input / Output Connector

Backlight Connector
JST BHSR-02VS-1,
Pin No. : 2 ,
Pitch : 3.5 mm

8-5) Timing Characteristics Of Input Signals

| Characteristics | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Rising time | $t_r$ | - | - | 10 | ns | |
| Falling time | $t_f$ | - | - | 10 | ns | |
| High and low level pulse width | $t_{CPH}$ | 147 | 156 | 166 | ns | CPH1 |
| CPH pulse duty | $t_{CWH}$ | 30 | 50 | 70 | % | CPH1 |
| STH setup time | $t_{SUH}$ | 20 | - | - | ns | STH1,STH2 |
| STH hold time | $t_{HDH}$ | 20 | - | - | ns | STH1,STH2 |
| STH pulse width | $t_{STH}$ | - | 1 | - | $t_{CPH}$ | STH1,STH2 |
| STH period | $t_H$ | 61.5 | 63.5 | 65.5 | $\mu$s | STH1,STH2 |
| OEH pulse width | $t_{OEH}$ | - | 1.6 | - | $\mu$s | OEH |
| Sample and hold disable time | $t_{DIS1}$ | - | 4.4 | - | $\mu$s | |
| OEV pulse width | $t_{OEV}$ | - | 12 | - | $\mu$s | XOE |
| CKV pulse width | $t_{CKV}$ | - | 32 | - | $\mu$s | CPV |
| Clean enable time | $t_{DIS2}$ | - | 6 | - | $\mu$s | |
| Horizontal display timing range | $t_{DH}$ | - | 960 | - | $t_{CPH}$/3 | |
| STV setup time | $t_{SUV}$ | 400 | - | - | ns | DIO1,DIO2 |
| STV hold time | $t_{HDV}$ | 400 | - | - | ns | DIO1,DIO2 |
| STV pulse width | $t_{STV}$ | - | - | 1 | $t_H$ | DIO1,DIO2 |
| Horizontal lines per field | $t_V$ | 256 | 262 | 268 | $t_H$ | |
| Vertical display start | $t_{SV}$ | | 3 | - | $t_H$ | |
| Vertical display timing range | $t_{DV}$ | | 234 | - | $t_H$ | |
| VCOM rising time | $t_{rCOM}$ | | - | 5 | $\mu$s | |
| VCOM falling time | $t_{fCOM}$ | | - | 5 | $\mu$s | |
| VCOM delay time | $t_{DCOM}$ | | - | 3 | $\mu$s | |
| RGB delay time | $t_{DRGB}$ | | - | 1 | $\mu$s | |

8–6) Signal Timing Waveforms

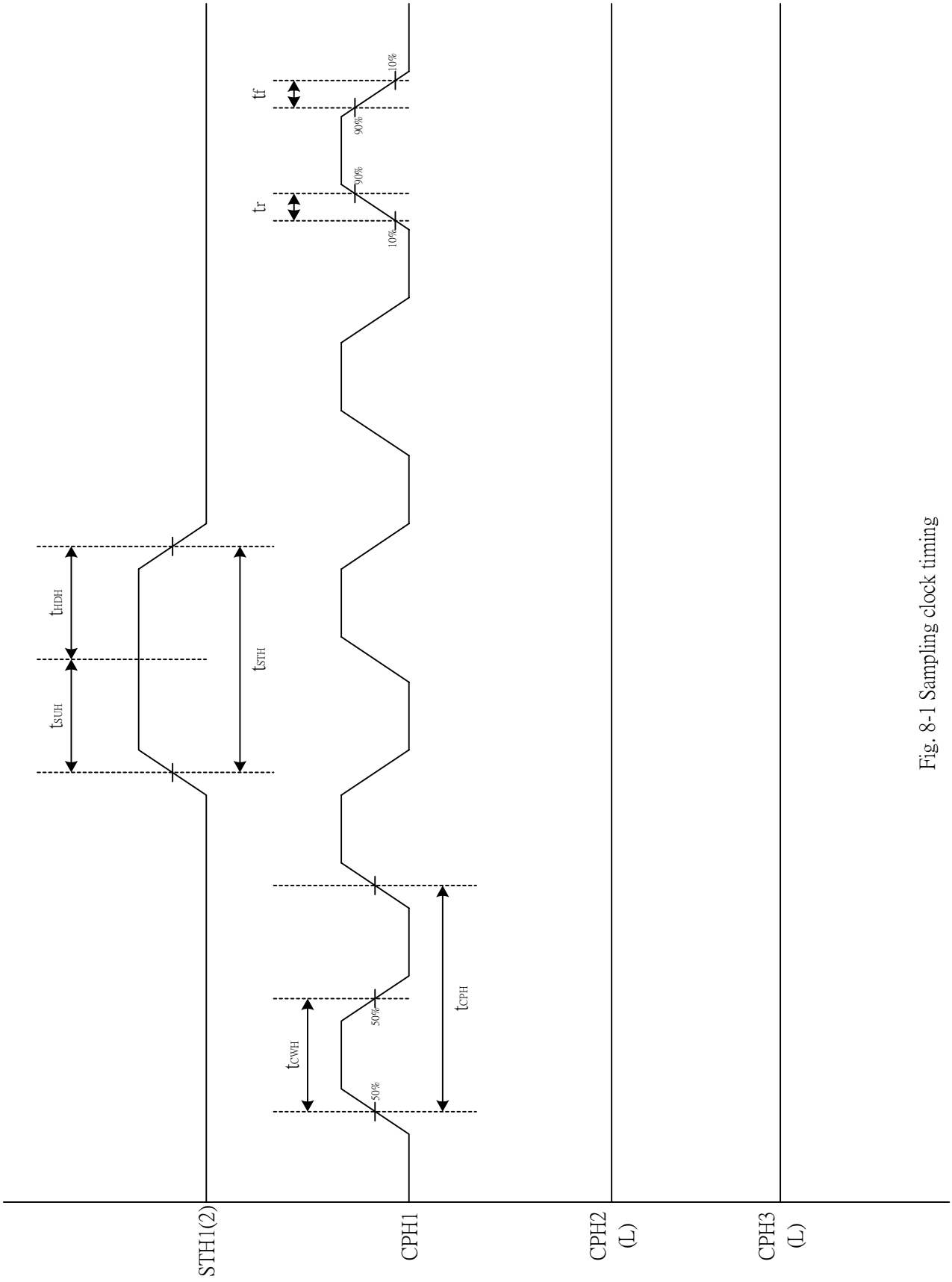



Fig. 8-1 Sampling clock timing

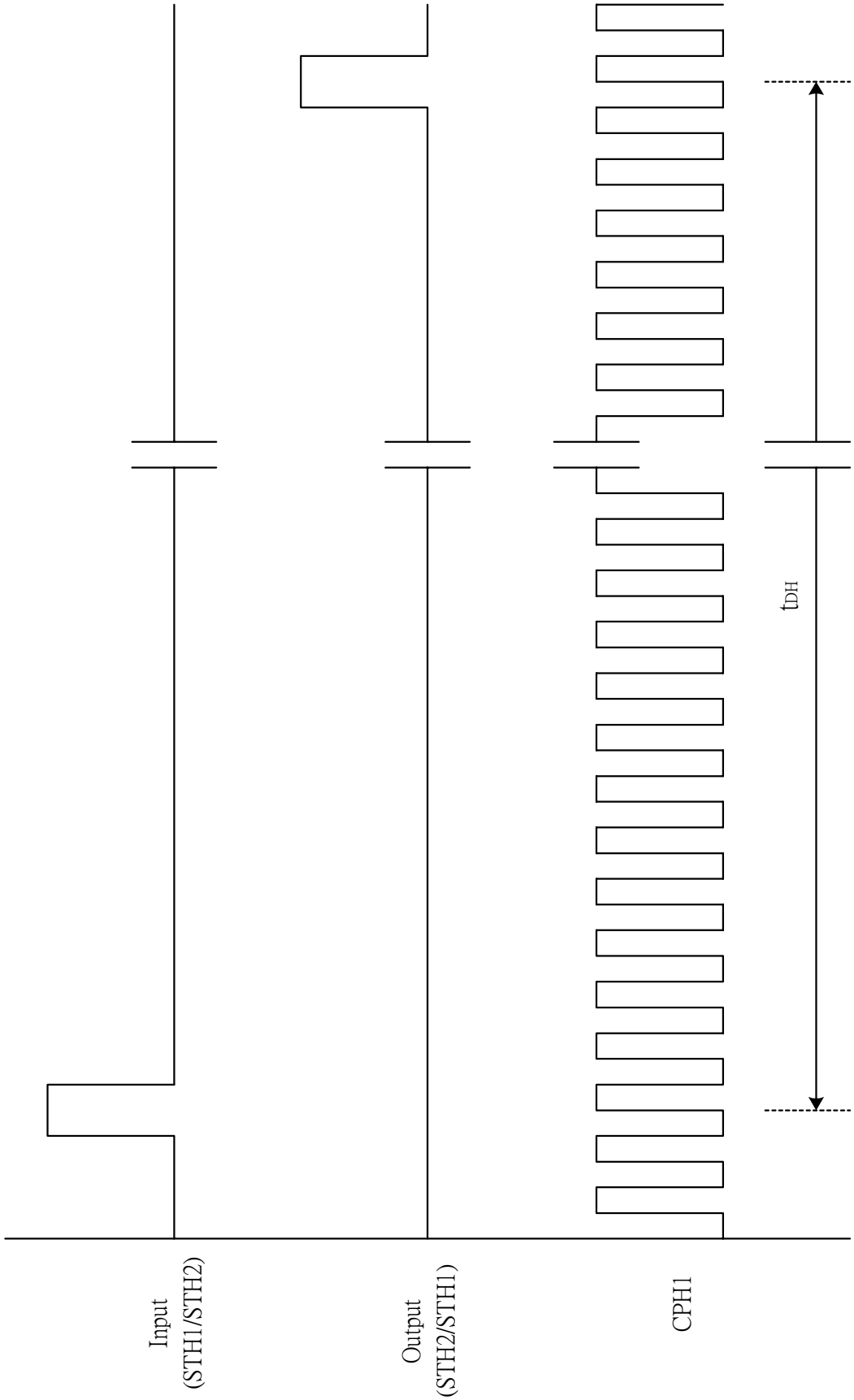



Fig. 8-2 Horizontal display timing range

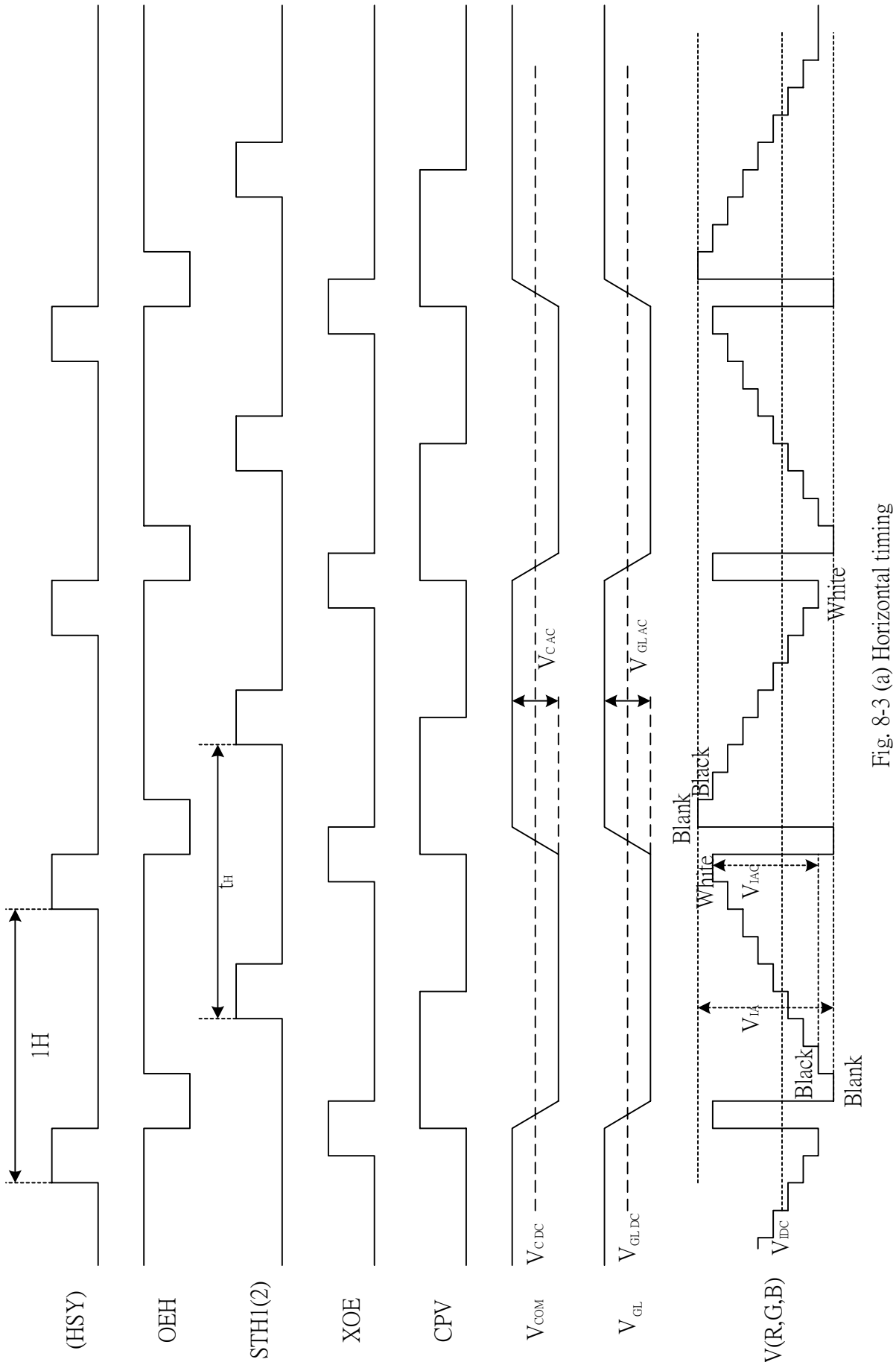
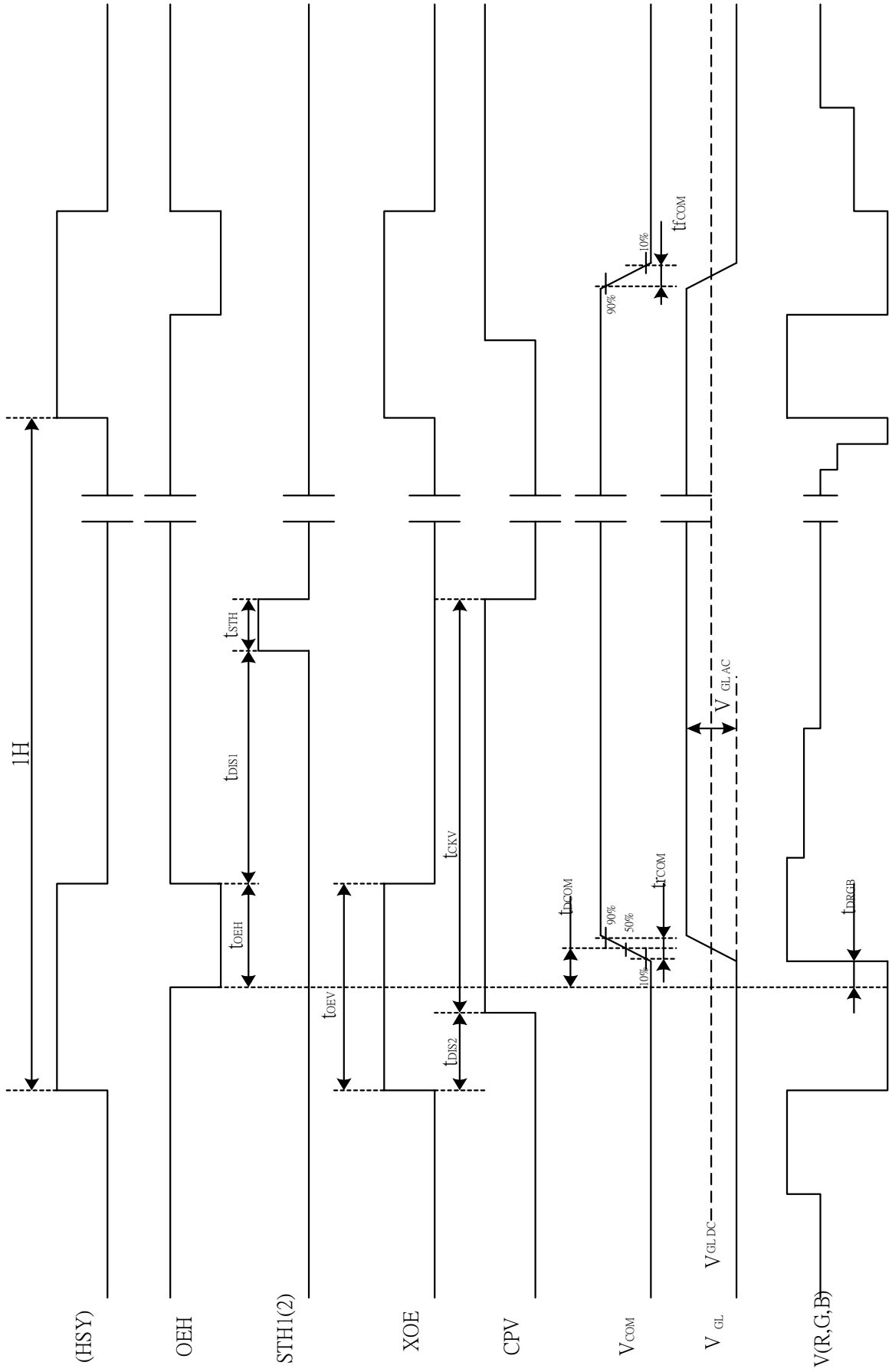



Fig. 8-3 (a) Horizontal timing




Note : The falling edge of OEV should be synchronized with the falling edge of OEH

Fig. 8-3 (b) Detail horizontal timing

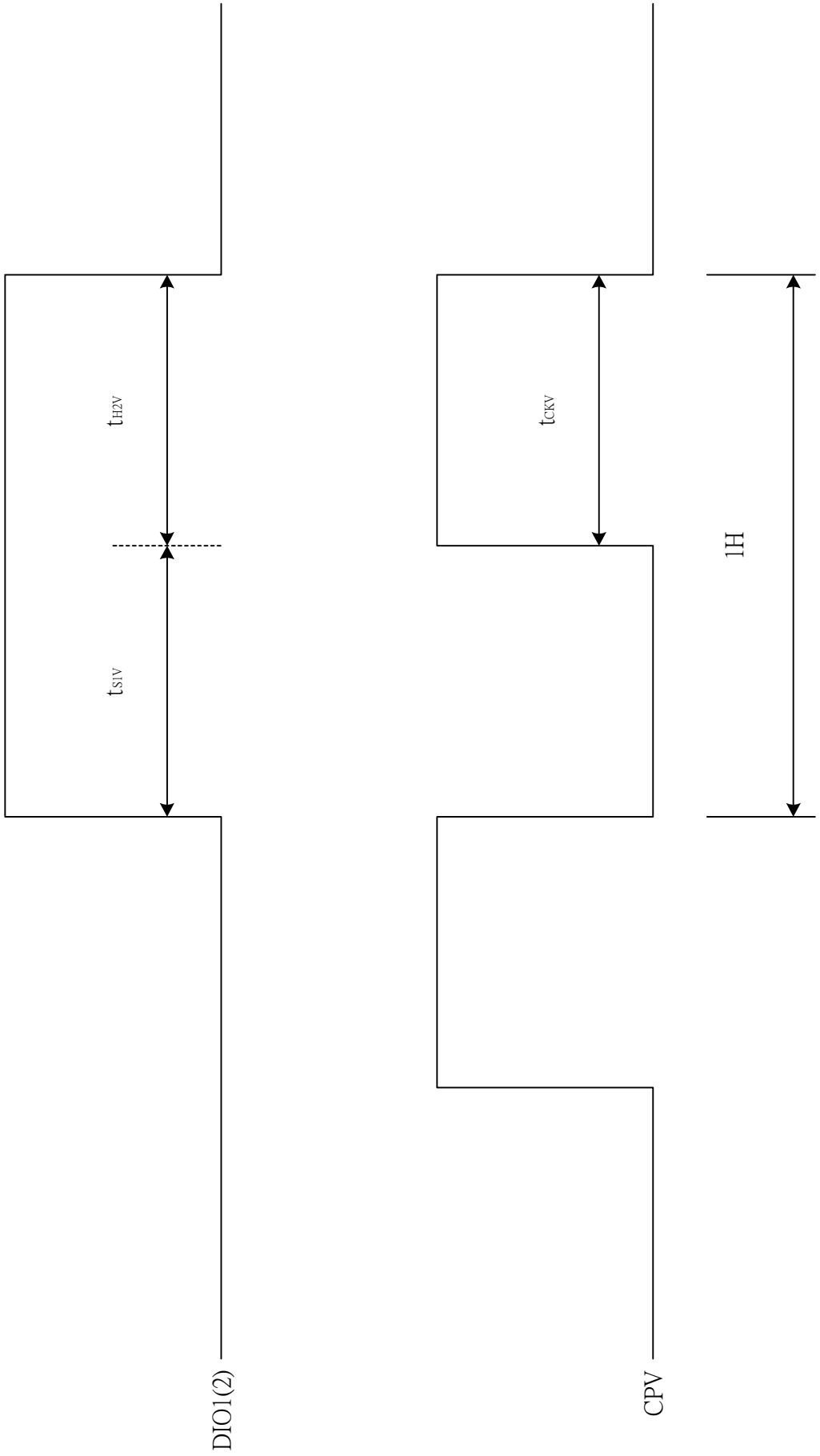



Fig. 8-4 Vertical shift clock timing

Vertical timing (From up to down)

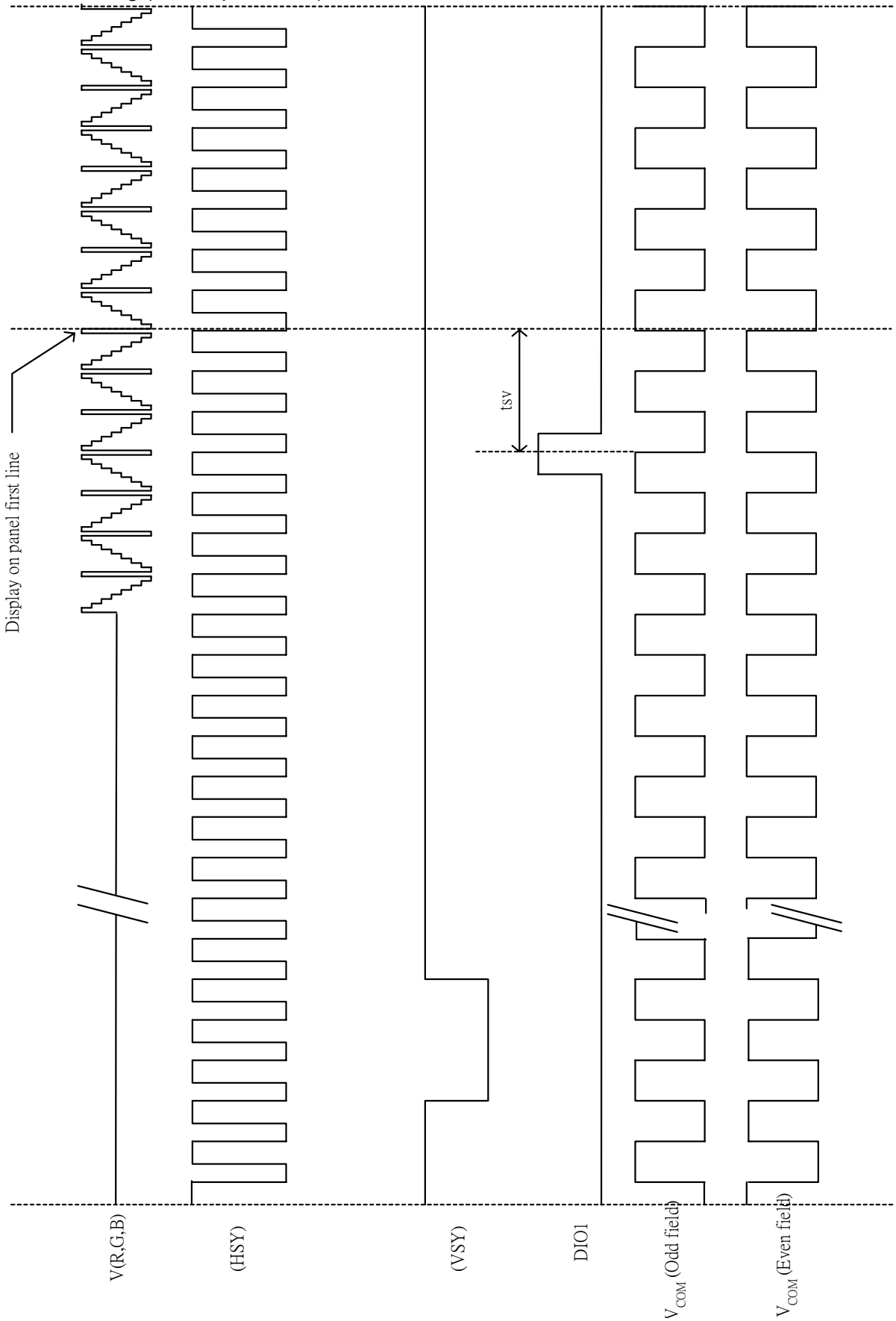



Fig. 8-5 (a) Vertical timing (From Up to Down)

Vertical timing (From down to up)

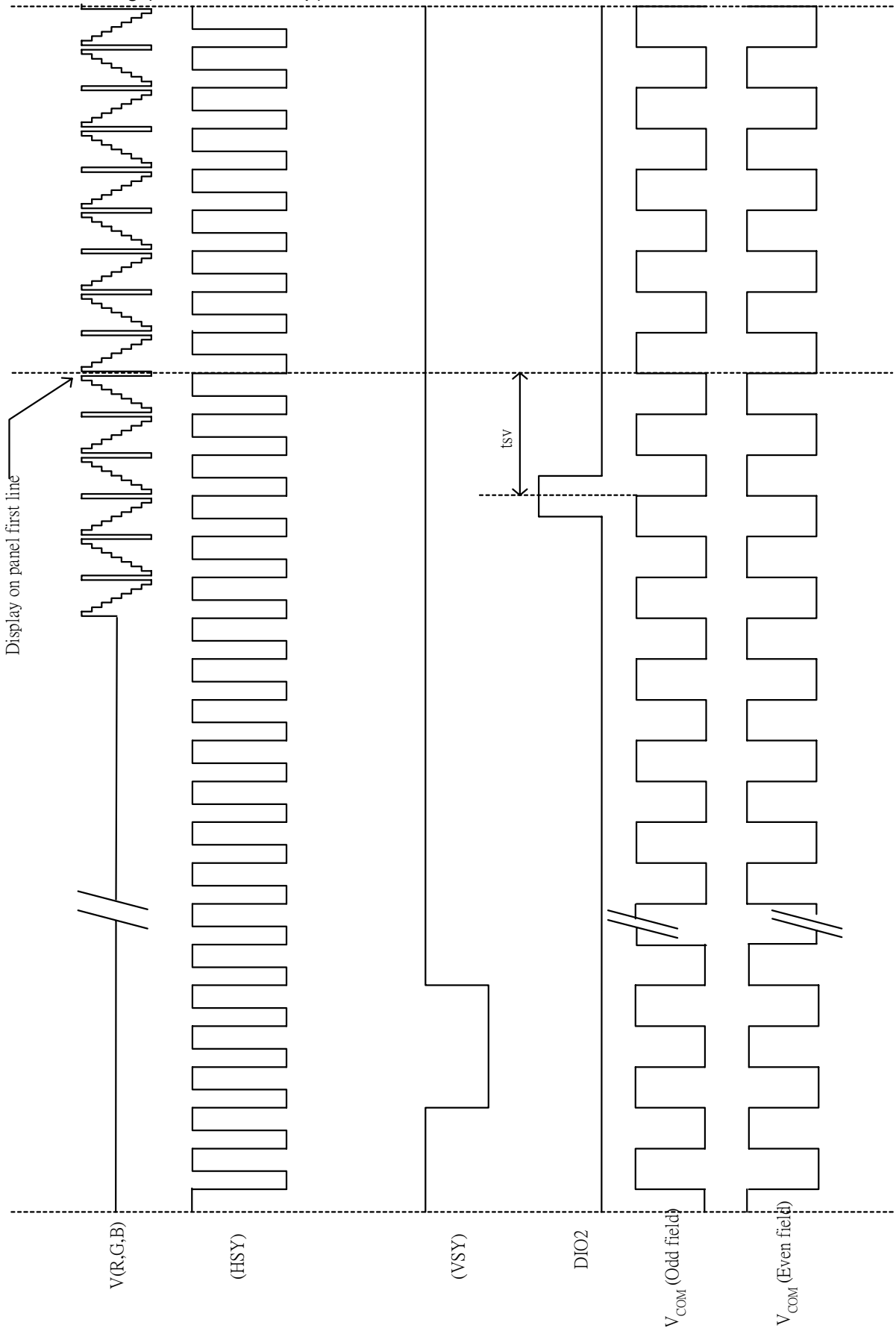
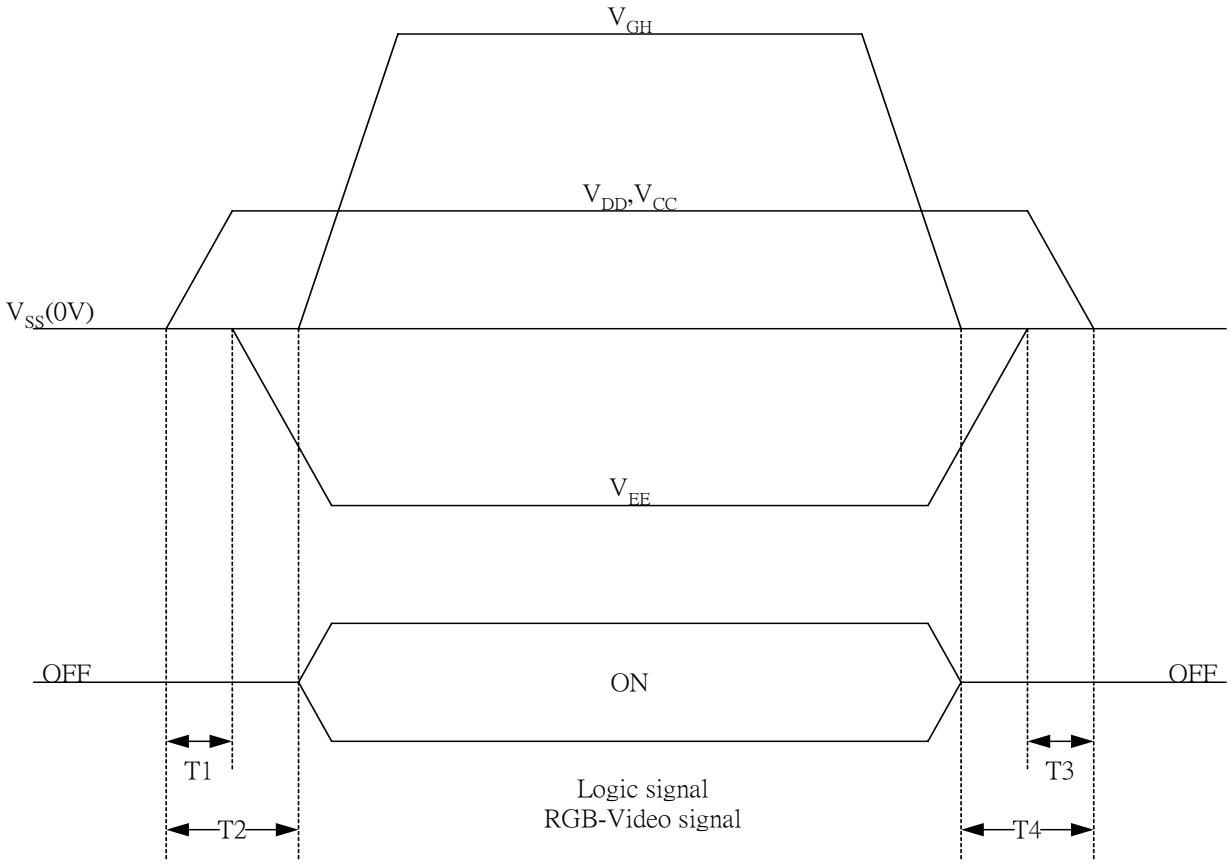



Fig. 8-5 (b) Vertical timing (From Down to Up)

9. Power On Sequence

The Power on Sequence only effect by $V_{CC}$,$V_{SS}$,$V_{DD}$,$V_{EE}$ and $V_{GH,}$ the others do not care.




1) 10ms≦T1<T2
2) 0ms<T3≦T4≦10ms

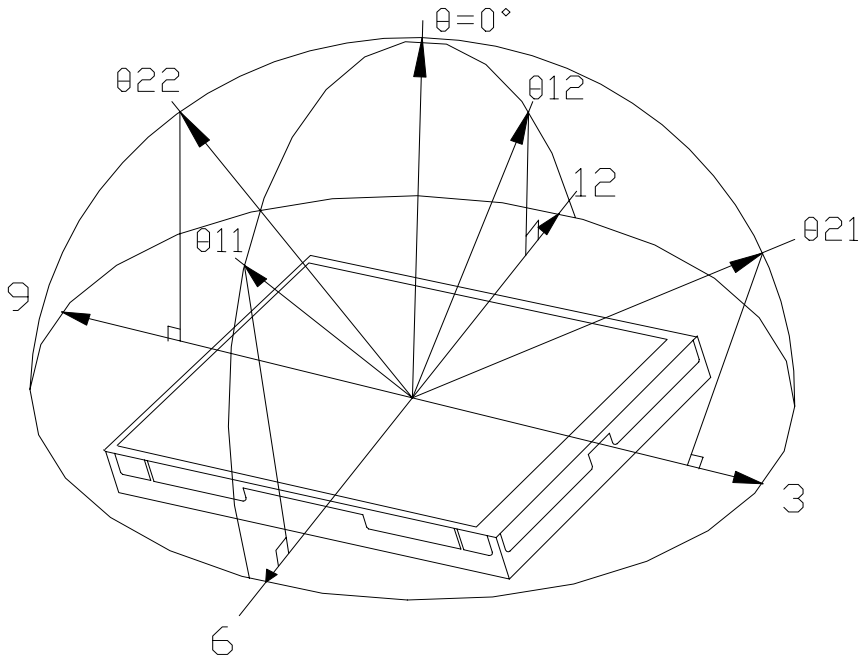
10. Optical Characteristics

10-1) Specification:

Ta = 25℃

| Parameter | | Symbol | Condition | MIN. | TYP. | MAX. | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Viewing Angle | Horizontal | θ21, θ22 | CR≧10 | 45 | 50 | --- | deg | Note 10-1 |
| | Vertical | θ11 | | 30 | 35 | --- | Deg | Note 10-1 |
| | | θ12 | | 10 | 15 | --- | deg | Note 10-1 |
| Contrast Ratio | | CR | At optimized Viewing angle | 200 | 350 | --- | | Note 10-2 |
| Response time | Rise | Tr | θ=0° | --- | 15 | 30 | ms | Note 10-4 |
| | Fall | Tf | | --- | 30 | 50 | ms | |
| Uniformity | | U | | 70 | 85 | --- | % | Note 10-5 |
| Brightness | | | | 350 | 400 | --- | cd/㎡ | Note 10-3 |
| White Chromaticity | | x | θ=0° | 0.271 | 0.301 | 0.331 | | Note 10-3 |
| | | y | θ=0° | 0.280 | 0.310 | 0.340 | | |
| Lamp Life Time +25℃ | | | | | 30000 | --- | hrs | |

Note 10-1 : The definitions of viewing angles




Note 10-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

(Testing configuration see 10-2 )

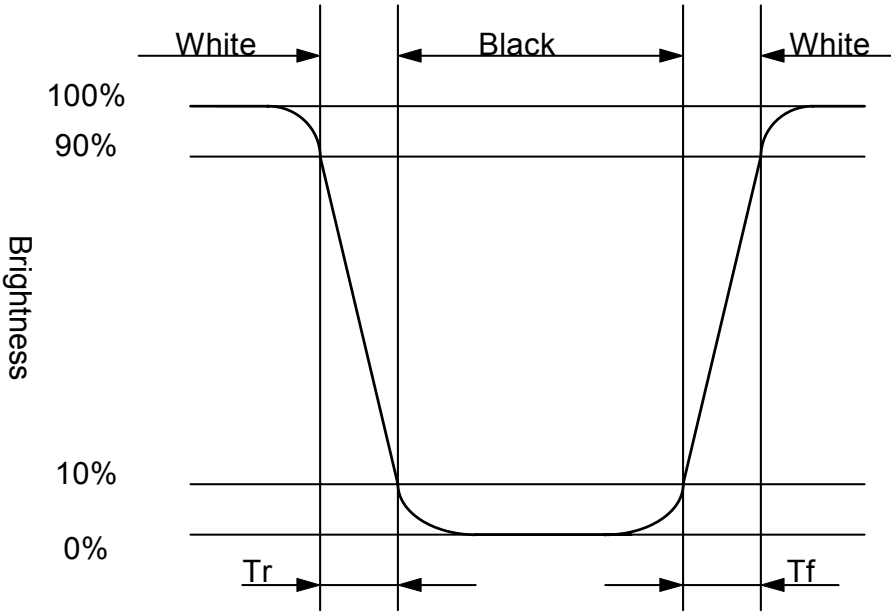
Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : Topcon BM-7(fast) luminance meter 2°field of view is used in the testing (after 20~30 minutes operation).

Lamp Current 6mA

Inverter model : TDK-347

Note 10-4 : The definition of response time :




Note 10-5: The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

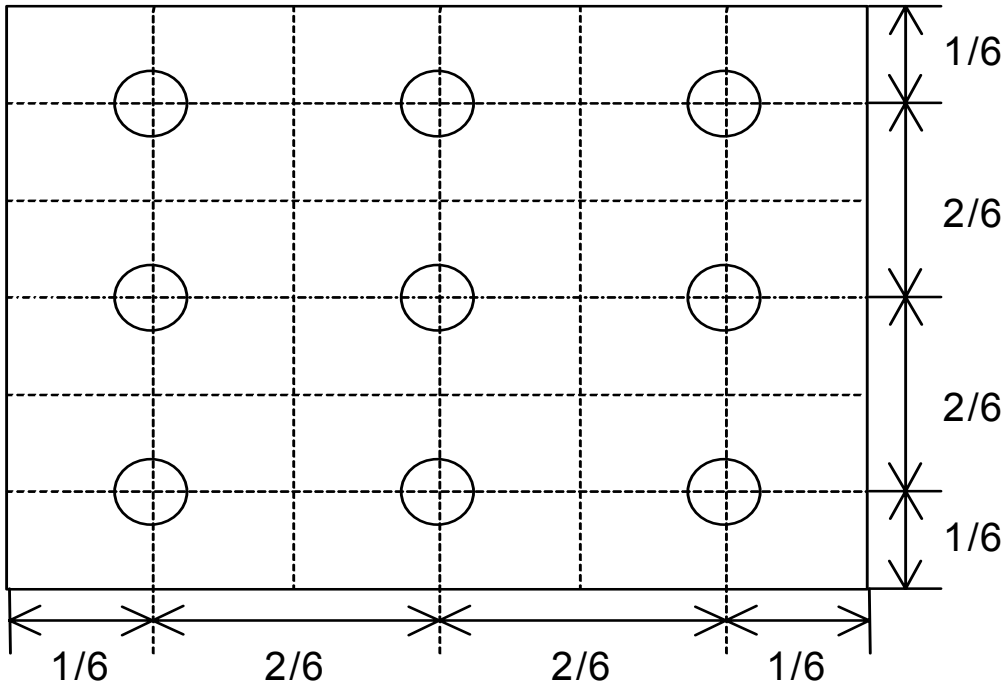
Luminance meter : BM-5A or BM-7 fast(TOPCON)

Measurement distance : 500 mm +/- 50 mm

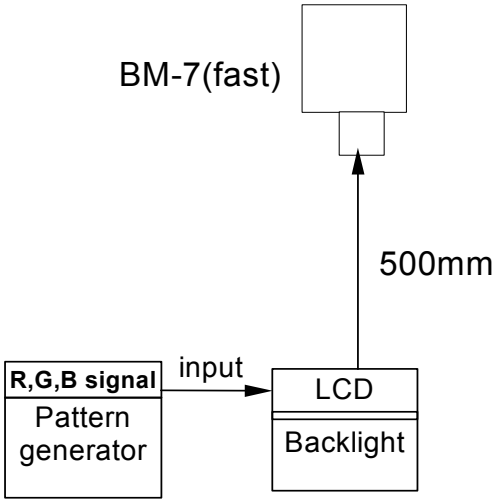
Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).

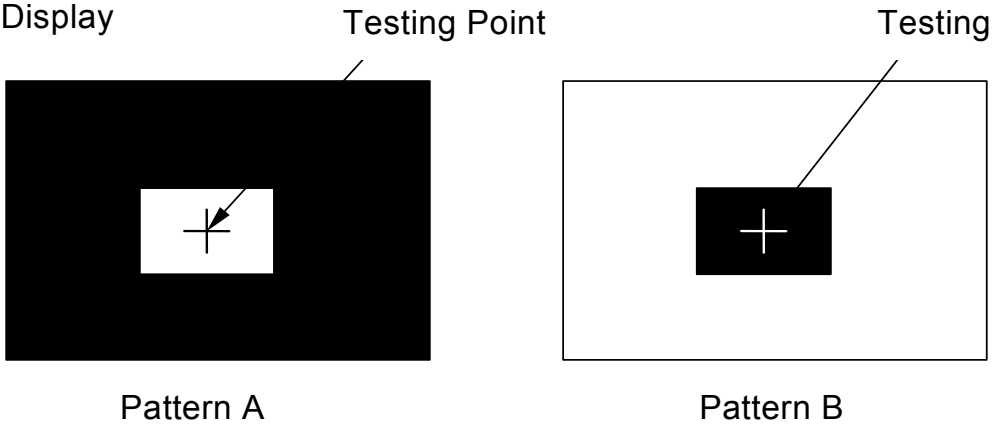


10-2) Testing configuration



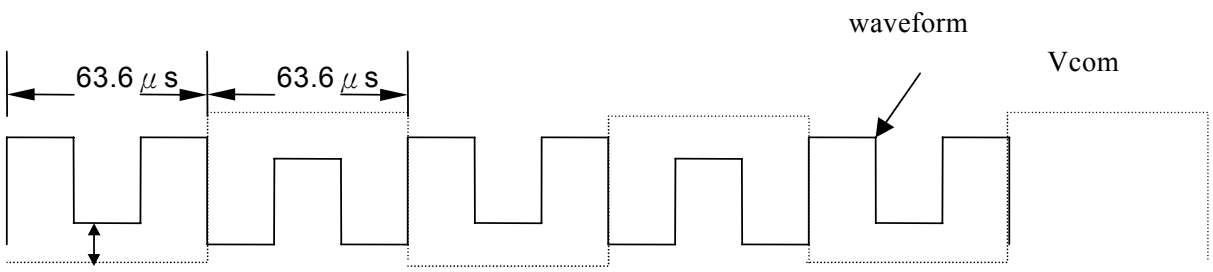

Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display



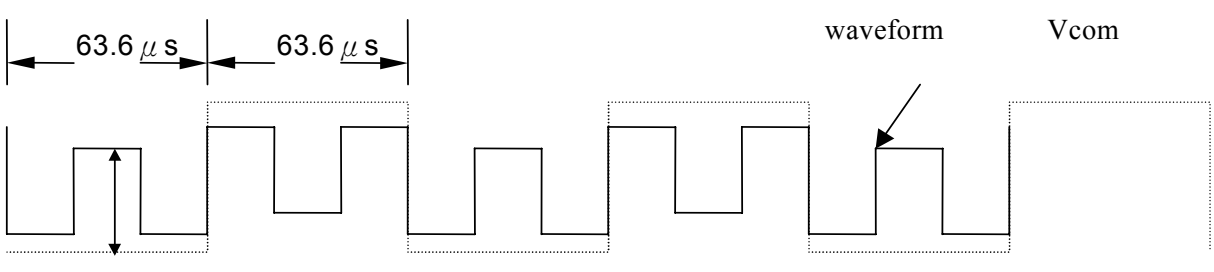

Pattern A Pattern B

- R, G, B Waveform of Pattern A at Testing Point




Vw=1.3V +/- 0.2V

- R, G, B Waveform of Pattern B at Testing Point




Vb=5.0V +/- 0.2V

11. Handling Cautions

11-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.

1. The noise from the backlight unit will increase.
2. The output from inverter circuit will be unstable.
3. In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirts. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.

b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

11-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components.

f) Please adjust the voltage of common electrode as material of attachment by 1 module.

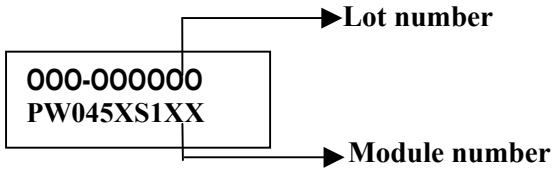
12. Reliability Test

| No | Test Item | Test Condition |
|---|---|---|
| 1 | High Temperature Storage Test | Ta = +70℃, 240 hrs |
| 2 | Low Temperature Storage Test | Ta = -10℃, 240 hrs |
| 3 | High Temperature Operation Test | Ta = +60℃, 240 hrs |
| 4 | Low Temperature Operation Test | Ta = 0℃, 240 hrs |
| 5 | High Temperature & High Humidity Operation Test | Ta = +60℃, 80%RH, 240 hrs |
| 6 | Thermal Cycling Test (non-operating) | -25℃ → +70℃, 200 Cycles<br>30 min 30 min |
| 7 | Vibration Test (non-operating) | Frequency：10 ~ 55 $H_Z$<br>Amplitude：1.5 mm<br>Sweep time: 11 mins<br>Test Period : 6 Cycles for each direction of X, Y, Z |
| 8 | Shock Test (non-operating) | 100G, 6ms<br>Direction : ±X, ±Y, ±Z<br>Cycle : 3 times |
| 9 | Electrostatic Discharge Test (non-operating) | 200pF, 0Ω<br>±200V<br>1 time / each terminal |

Ta: ambient temperature

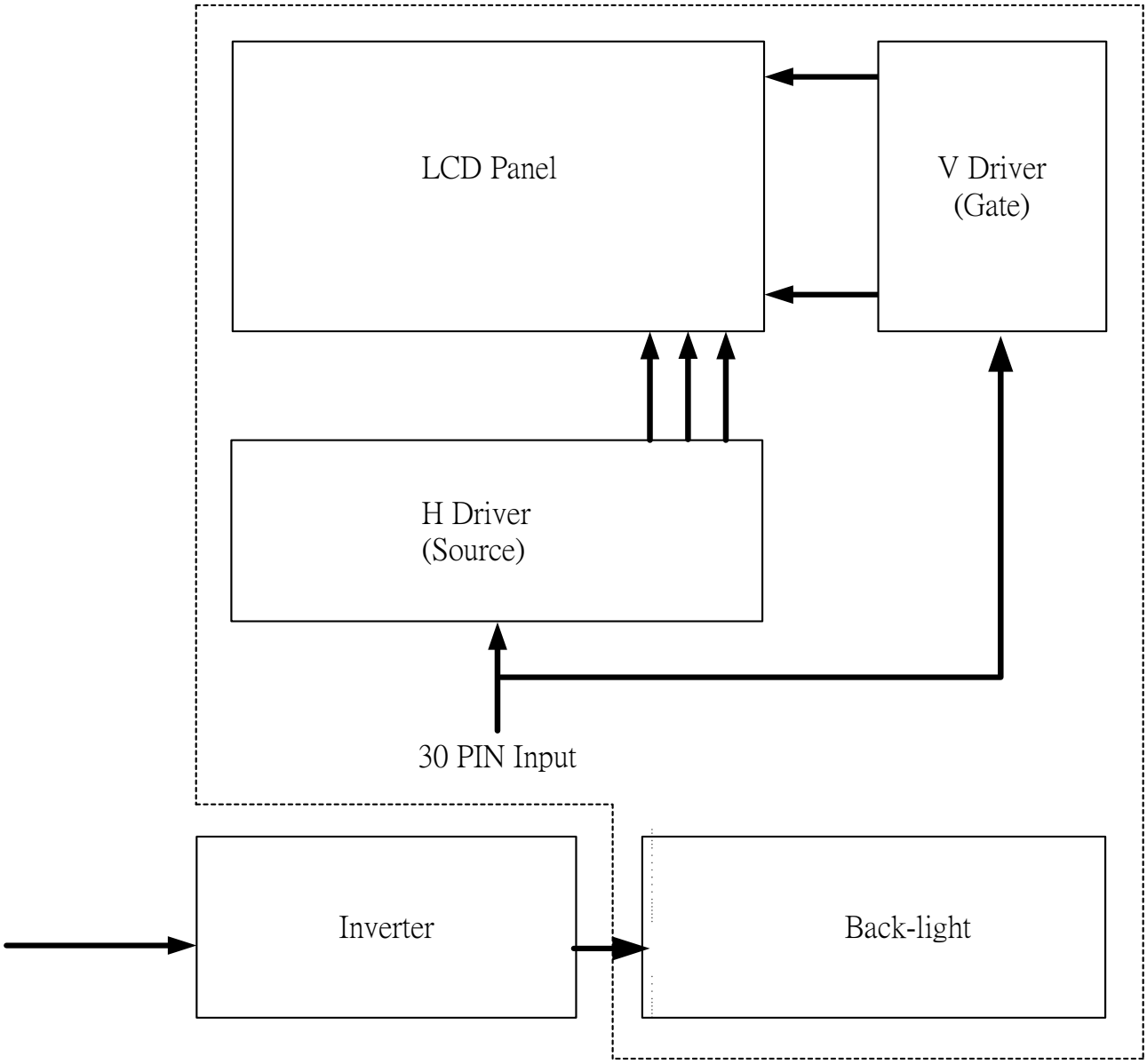
[Criteria]
Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

13. Indication of Lot Number Label
Indicated contents of the label



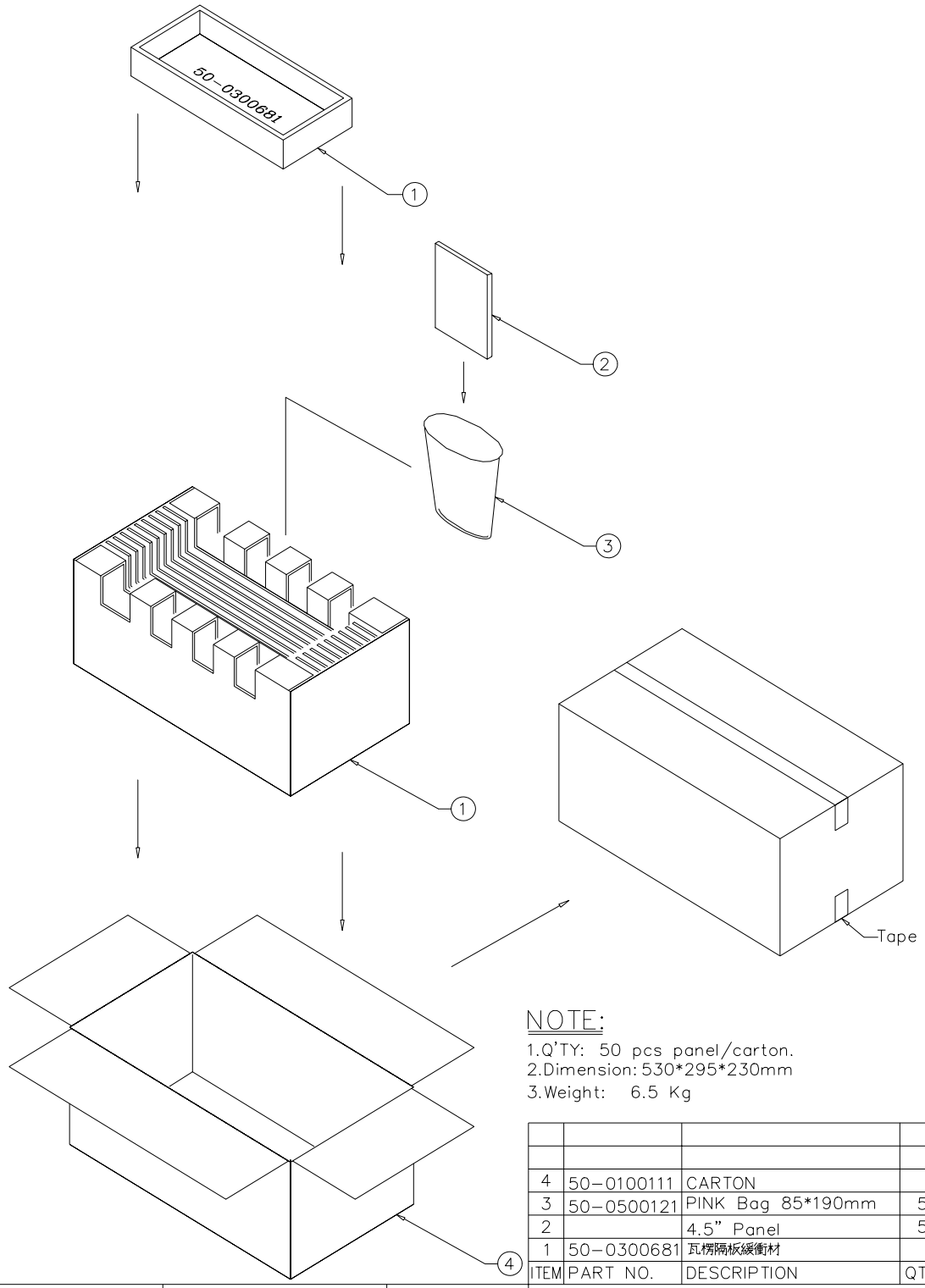

Contents of lot number : $1_{st}$~$3_{rd}$—The OEM product
$5_{th}$—Production year : 1999⇒9, 2000⇒A, 2001⇒B……..
$6_{th}$—Production month : 1, 2, 3,….9, A, B, C
$7_{th}$~$8_{th}$—Production size : 4.5” ⇒45
$9_{th}$~$10_{th}$— Serial numbers : 01~99

14. Block Diagram



15. Packing

| ZONE | REV. | DOCUUMENT NO. | DESCRIPTION | DATE | REV.BY |
|---|---|---|---|---|---|




NOTE:

1.Q'TY: 50 pcs panel/carton.
2.Dimension: 530*295*230mm
3.Weight: 6.5 Kg

| ITEM | PART NO. | DESCRIPTION | QTY | REMARK |
|---|---|---|---|---|
| | | | | |
| | | | | |
| 4 | 50-0100111 | CARTON | 1 | |
| 3 | 50-0500121 | PINK Bag 85*190mm | 50 | 抗靜電 |
| 2 | | 4.5" Panel | 50 | |
| 1 | 50-0300681 | 瓦楞隔板緩衝材 | 1 | 上蓋+ 底座 |

| MTL.SPEC. | UNSPECIFIED TOL'S | REMARK |
|---|---|---|
| | ANGLE | |
| | ROUGHNESS | |

元太科技工業股份有限公司
Prime View International Co., Ltd.

| | | | | | | |
|---|---|---|---|---|---|---|
| APPROVE | | . . | SCALE | UNIT | SHEET 1 OF 1 | DWG.TITLE 4.5" Model Packing Draw |
| CHECK | | . . | | | | |
| DRAWN | Jimmy | '03.06.05 | MTL.NO. | | DWG FILE: | REV. 01 / A4 SIZE |

# Revision History

| Rev. | Issued Date | Revised Contents |
|---|---|---|
| 0.1 | Feb. 13 , 2003 | NEW |
| 0.2 | May 08, 2003 | Page 6 : Add Pixel Arrangement and Input Connector Pin NO. |
| 0.3 | Jun. 05, 2003 | Page 8 : Modify Current Consumption<br>Page 24 : Add Packing Drawing |
| 1.0 | Jun. 13, 2003 | Page 8 : Add Lamp & Power Consumption |
| 1.1 | Aug. 29, 2003 | Page 4 : Modify Mechanical Drawing of TFT-LCD Module<br>Page 7 : Modify Operating Condition(from $V_{GL}$ to $V_{EE}$)<br>Page 8 : Modify Power Consumption (Exchange $V_{DD1}$ & $V_{DD2}$) |
| 1.2 | Sep. 19, 2003 | Page 8: Modify Current Consumption & Power Consumption |
| 1.3 | Nov. 24, 2003 | Page 17: Modify Optical Characteristics<br>(Contrast Ratio Min. from 110 to 200 & Typ. From 150 to 350) |
| 1.4 | Feb. 05, 2004 | Page 4: Modify Mechanical Drawing of TFT-LCD Module |
| 1.5 | Jun. 28, 2004 | Page 9: Modify Input / Output Connector Pitch from 4 to 3.5 mm. |
| 1.6 | Oct. 06, 2004 | Page 4: Modify Mechanical Drawing of TFT-LCD Module(Add GND Wire)<br>Page 8: Add Note about Lamp Kick-off Voltage<br>Page 19: Modify The Test Pattern of Uniformity |