Version : 0.2

TECHNICAL SPECIFICATION

MODEL NO. : PW100XS1

☐Customer's Confirmation

Customer

Date

By

☐PVI's Confirmation

Confirmed By

Prepared By

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Date : Mar.22,2005

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TECHNICAL SPECIFICATION

CONTENTS

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1. Application

This technical specification applies to 10” color TFT-LCD module, PW100XS1. The applications of the panel are car TV, portable DVD, GPS, multimedia applications and others AV system.

2. Features

. Pixel in stripe configuration

. Slim and compact

. High Brightness

. Image Reversion：Up/Down and Left/Right

. Support multi display mode
(If you use this mode, you must use PVI-1005A’s timing controller (mode by PVI))

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	10(15:9 diagonal)	Inch
Display Format	1920*468	dot
Active Area	216.0(H)×29.64 (V)	mm
Dot Pitch	0.112(H)×0.277(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	235.0(W)×145.8(H)×6.1(D)(typ.)	mm
Surface Treatment	Anti-Glare	
Weight	TBD	g

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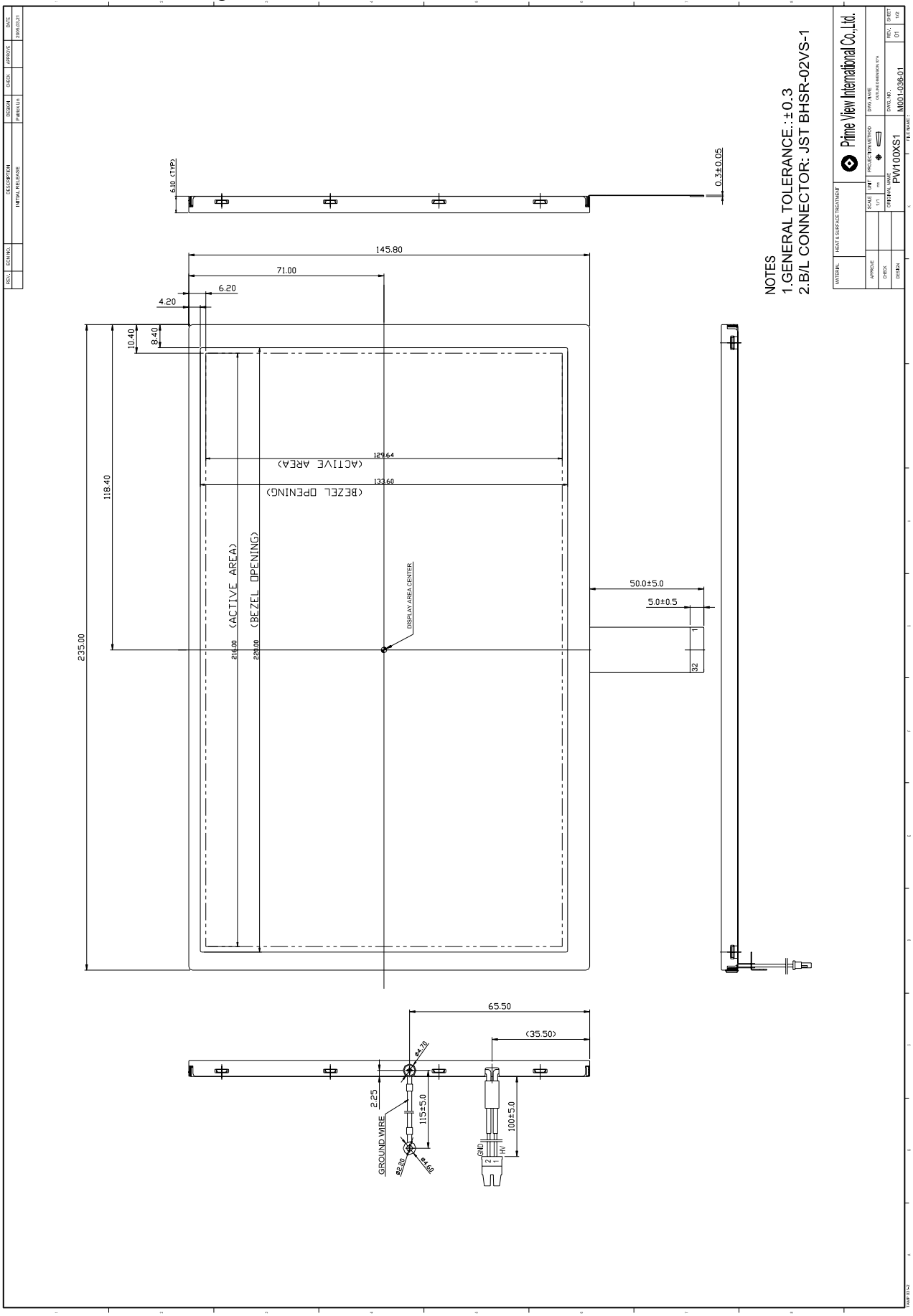
4. Mechanical Drawing of TFT-LCD Module



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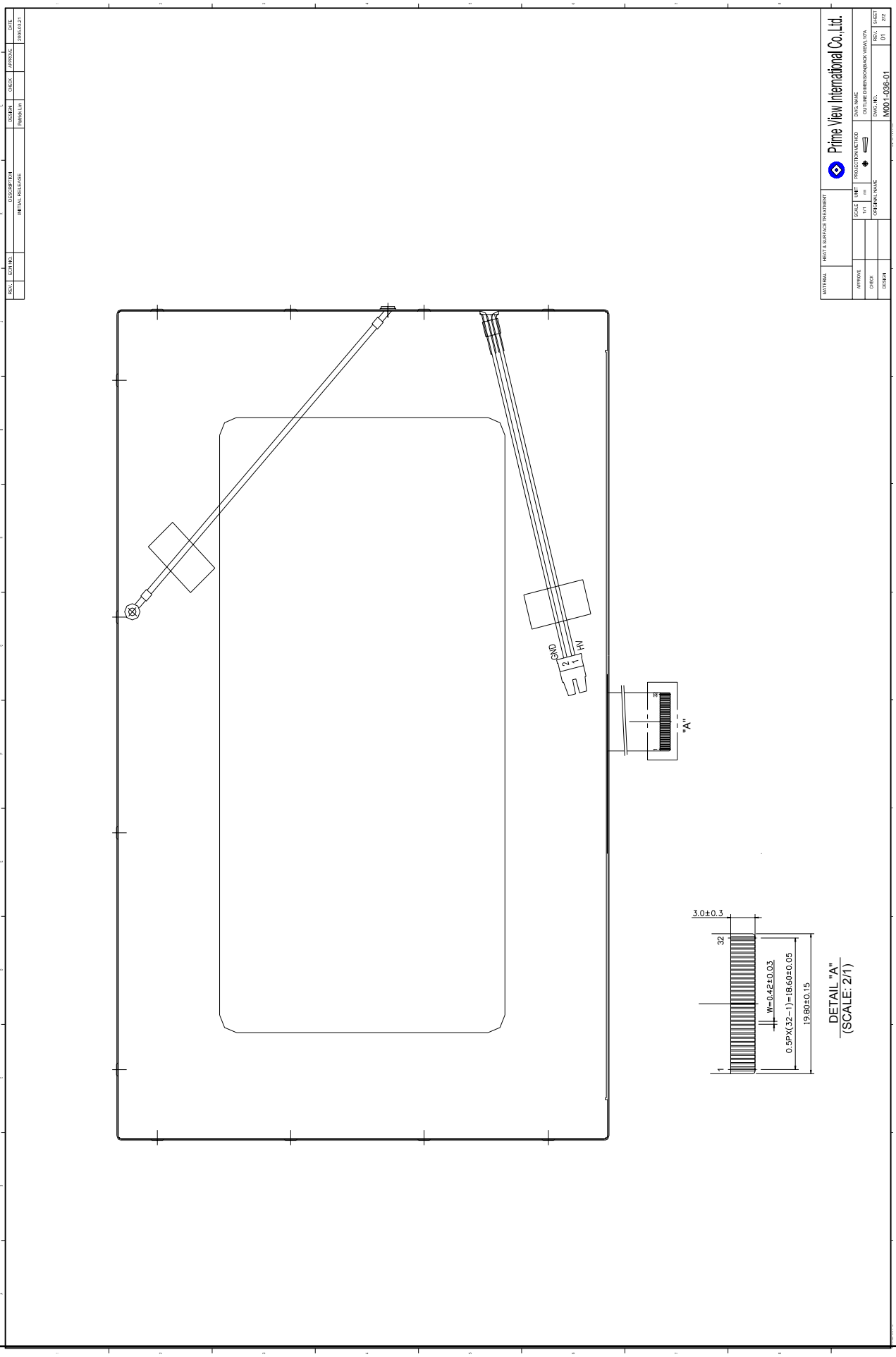

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5. Input / Output Terminals

LCD Module Connector
FPC Down Connect , 32 Pins , Pitch : 0.5 mm

Pin No	Symbol	I/O	Description	Remark
1	GND	-	Ground for gate driver	
2	V_{GH}	-	Positive power gate driver	Note 5-5
3	V_{EE}	-	Negative power gate driver	Note 5-4
4	V_{CC}	-	Power supply for gate driver circuit	
5	STVD	I/O	Vertical start pulse	Note 5-1
6	STVU	I/O	Vertical start pulse	Note 5-3
7	CKV	I	Shift clock for gate driver	
8	U/D	I	Up / Down Control for gate driver	Note 5-1
9	OE3	I	Output enable for gate driver	
10	OE2	I	Output enable for gate driver	
11	OE1	I	Output enable for gate driver	
12	V_{COM}	I	Voltage for common electrode	
13	V_{DD2}	-	Supply voltage of analog circuit for source driver	
14	V_{SS2}	-	Ground for analog circuit for source driver	
15	VB-	I	Video input B for negative polarity	
16	VG-	I	Video input G for negative polarity	
17	VR-	I	Video input R for negative polarity	
18	VB+	I	Video input B for positive polarity	
19	VG+	I	Video input G for positive polarity	
20	VR+	I	Video input R for positive polarity	
21	V_{SS1}	-	Ground of logic circuit for source driver	
22	V_{DD1}	-	Supply voltage of logic circuit for source driver	
23	STH2	I/O	Start pulse for source driver	Note 5-2
24	STH1	I/O	Start pulse for source driver	
25	POL	I	P0larity control for column inversion	
26	CPH1	I	Sample and shift clock for source driver	
27	CPH2	I	Sample and shift clock for source driver	
28	CPH3	I	Sample and shift clock for source driver	
29	OEH	I	Output enable for source driver	
30	MOD	I	Simultaneous/sequential mode select	
31	R/L	I	Left / Right Control for source driver	Note 5-2
32	V_{COM}	I	Voltage for common electrode	

Note 5-1

U/D	STVD	STVU	scanning direction
GND	Input	output	up todown
Vcc	Output	input	down to up

Note 5-2

R/L	STH1	STH2	scanning direction
Vcc	input	output	left to right
GND	output	input	right to left

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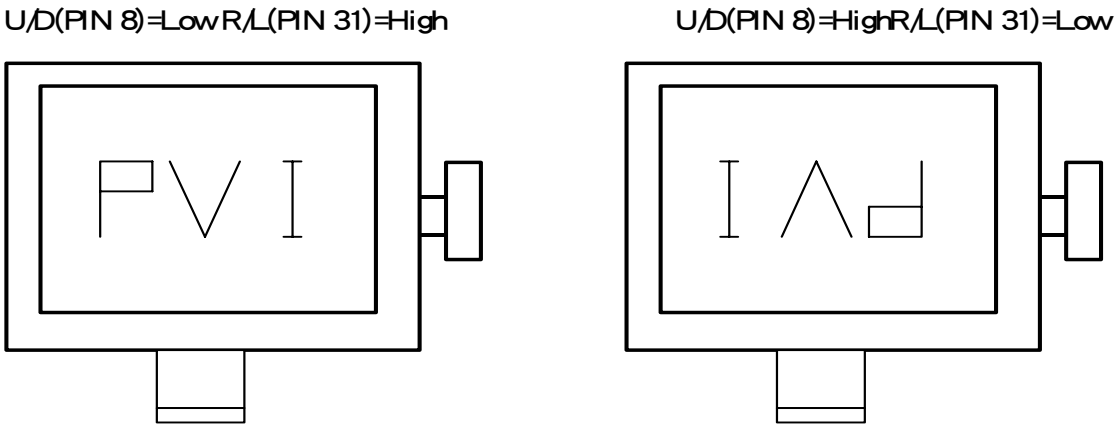
The definitions of Note 5-1,5-2



Note 5-3 : V_{CC} TYP.＝+3.3V

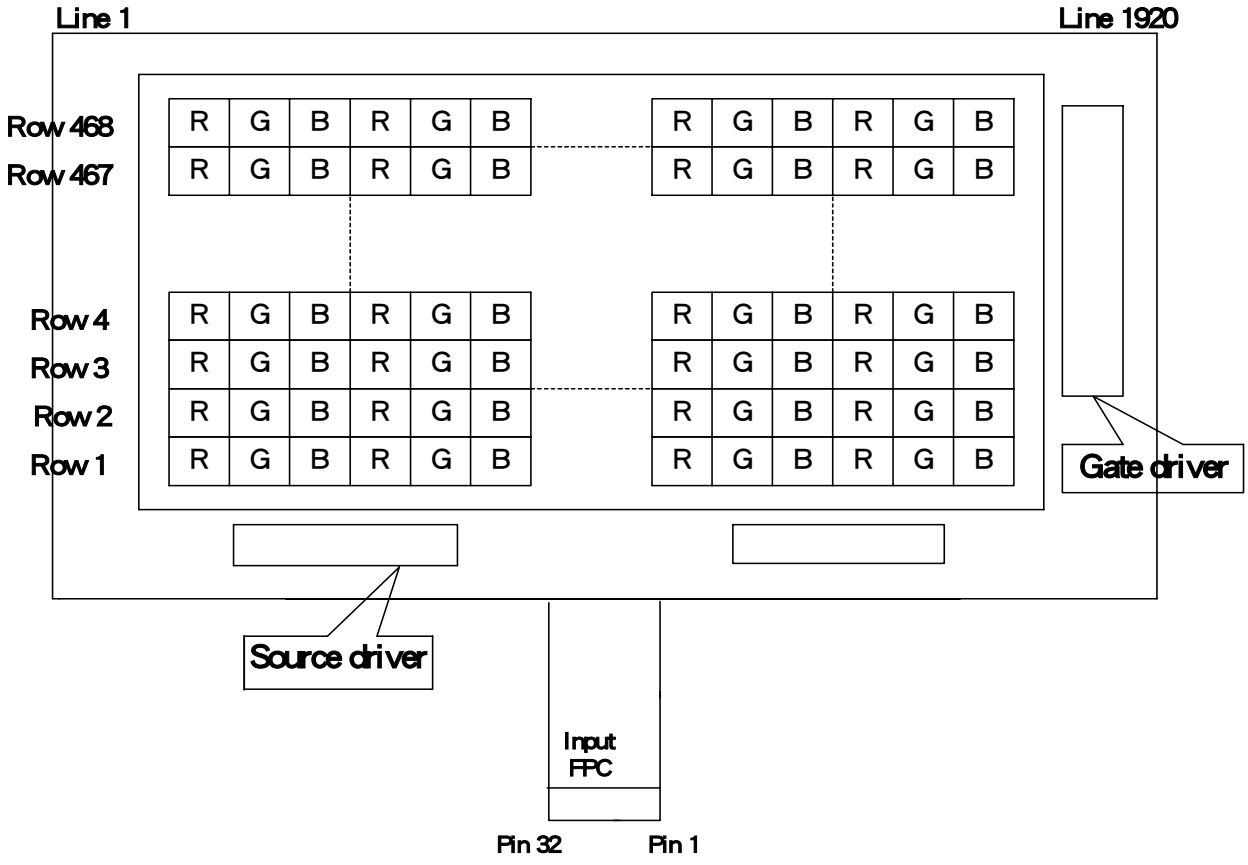
Note 5-4 : V_{EE} TYP.＝-10V

Note 5-5 : V_{GH} TYP.＝+20V

Note 5-6 : V_{DD2} TYP.＝+12V

Note 5-7 : V_{DD1} TYP.＝+3.3V

6. Pixel Arrangement and input connector pin NO.



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7. Absolute Maximum Ratings

The followings are maximum values , which if exceeded, may cause faulty operation or damage to the unit.

Parameter		Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage For Source Driver		V_{DD2}	+9.0	+13.5	V	
		V_{DD1}	-0.3	+7.0	V	
Supply Voltage For Gate Driver		V_{CC}	-0.3	+6.0	V	
		V_{GH}-V_{EE}	-0.3	+40.0	V	
	H Level	V_{GH}	-0.3	+25.0	V	
	L Level	V_{EE}	-16	+0.3	V	
Analog Signal Input Level		V_R+,V_G+,V_B+	+4	+11	V	Note 7-1
		V_R-,V_G-,V_B-	0	5.5	V	
Storage Temperature			-30	+80	℃	
Operation Temperature			-20	+70	℃	Note 7-2

Notes 7-1 : Analog Input Voltage means V_R,V_G,V_B.

Notes 7-2 : Optical characteristics shown in Table 10-1 are measured under Ta=+25℃.

8. Electrical Characteristics

8-1) Recommended Driving condition for TFT-LCD panel

Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply Voltage For Source Driver	Analog	V_{DD2}	+11	+12	+13	V	
	Logic	V_{DD1}	+3.0	+3.3	+3.6	V	
Supply Voltage For Gate Driver	H level	V_{GH}	+18	+20	+22	V	
	L level	$V_{EE\ DC}$	-11	-10	-9	V	
	Logic	V_{CC}	+3.0	+3.3	+3.6	V	
Analog Signal input Level	V_R+,V_G+,V_B+ (Analog video+)	$V_{+,AC}$	-	+4.0	-	O_{P-P}	
		$V_{+,DC}$	7.8	8	8.3	V	
	V_R-,V_G-,V_B- (Analog video-)	$V_{-,AC}$	-	+4.0-	-	O_{P-P}	
		$V_{-,DC}$	2.7	3.0	3.3	V	
Digital input voltage	H level	V_{IH}	0.7	-	V_{DD1}	V	
	L level	V_{IL}	-0.3	-	0.3	V	
Digital output voltage	H level	V_{OH}	0.7	-	V_{DD1}	V	
	L level	V_{OL}	-0.3	-	0.3	V	
Vcom		$V_{COM\ DC}$	3.5	4.0	5.5	V	DC Component of V_{COM} Note 8-1

Note 8-1 : PVI strongly suggests that the $V_{COM\ DC}$ level shall be adjustable , and the adjustable level range is 4.0V±0.5V , every module's $V_{COM\ DC}$ level shall be carefully adjusted to show a best image performance.

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8-2) Back Light driving (JST BHSR-02VS-1 ,Pin No.：2)

Pin No	Symbol	Description	Remark
1	VL1	Input terminal (Hi voltage side)	Wire color: pink
2	VL2	Input terminal (Low voltage side)	Wire color: white Note 8-2

Note 8-2 : Low voltage side of back light inverter connects with Ground of inverter circuits.

Recommended driving condition for back light Ta= 25 ℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	TBD	TBD	TBD	Vrms	
Lamp current	I_L	TBD	TBD	TBD	mA	Note 8-3
Lamp frequency	P_L	TBD	TBD	TBD	KHz	Note 8-4
Starting voltage(25℃) (Reference Value)	Vs			TBD	Vrms	Note 8-5
Starting voltage(0℃) (Reference Value)	Vs			TBD	Vrms	Note 8-5

Note 8-3 : In order to satisfy the quality of B/L , no matter use what kind of inverter , the output lamp current must between Min. and Max. to avoid the abnormal display image caused by B/L.

Note 8-4 : The waveform of lamp driving voltage should be as closed to a perfect sine wave as possible.

Note 8-5 : This value is not output voltage of inverter.
The voltage of inverter must larger than the starting voltage.
The kick-off time must larger than 1 second.

8-3) Power Consumption Ta= 25 ℃

Parameter	Symbol	Conditions	TYP.	MAX	Unit	Remark
Supply current for Gate Driver (Hi level)	I_{GH}	V_{GH} = +20V	TBD	TBD	mA	
Supply current for Gate Driver (Low level)	I_{EE}	V_{EE} = -12V	TBD	TBD	mA	
Supply current for Source Driver(Digital)	I_{DD1}	V_{DD1} = +3.3V	TBD	TBD	mA	
Supply current for Source Driver(Analog)	I_{DD2}	V_{DD2} = +10V	TBD	TBD	mA	
Supply current for Gate Driver (Digital)	I_{CC}	V_{CC} = +3.3V	TBD	TBD	mA	
LCD Panel Power Consumption			TBD	TBD	mW	Note 8-6
Back Light Lamp Power Consumption			TBD		W	Note 8-7

Note 8-6 : The power consumption for back light is not included.

Note 8-7 : Back light lamp power consumption is calculated by $I_L \times V_L$.

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8-4) Timing Characteristics Of Input Signals

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
Rising time	t_r	-	-	10	ns	
Falling time	t_f	-	-	10	ns	
High and low level pulse width	t_{CPH}	12.3	12.8	13.3	MHz	CPH1~CPH3
CPH pulse duty	t_{CWH}	30	50	70	%	CPH1~CPH3
STH setup time	t_{SUH}	20	-	-	ns	STH1,STH2
STH hold time	t_{HDH}	20	-	-	ns	STH1,STH2
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STH1,STH2
STH period	t_H	61.5	63.5	65.5	μs	STH1,STH2
OEH pulse width	t_{OEH}	-	2.08	-	μs	OEH
Sample and hold disable time	t_{DIS1}	-	5.26	-	μs	
OEV pulse width	t_{OEV}	-	16	-	μs	OEV
CKV pulse width	t_{CKV}	-	32	-	μs	CKV
Clean enable time	t_{DIS2}	-	8.02	-	μs	
Horizontal display start	t_{SH}	-	0	-	t_{CPH}/3	
Horizontal display timing range	t_{DH}	-	640	-	t_{CPH}	
STV setup time	t_{SUV}	400	-	-	ns	STVD,STVU
STV hold time	t_{HDV}	400	-	-	ns	STVD,STVU
STV pulse width	t_{STV}	-	-	1	t_H	STVD,STVU
Horizontal lines per field	t_V	256	262	268	t_H	
Vertical display start	t_{SV}		3	-	t_H	
Vertical display timing range	t_{DV}		234	-	t_H	

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8-5) Signal Timing Waveforms

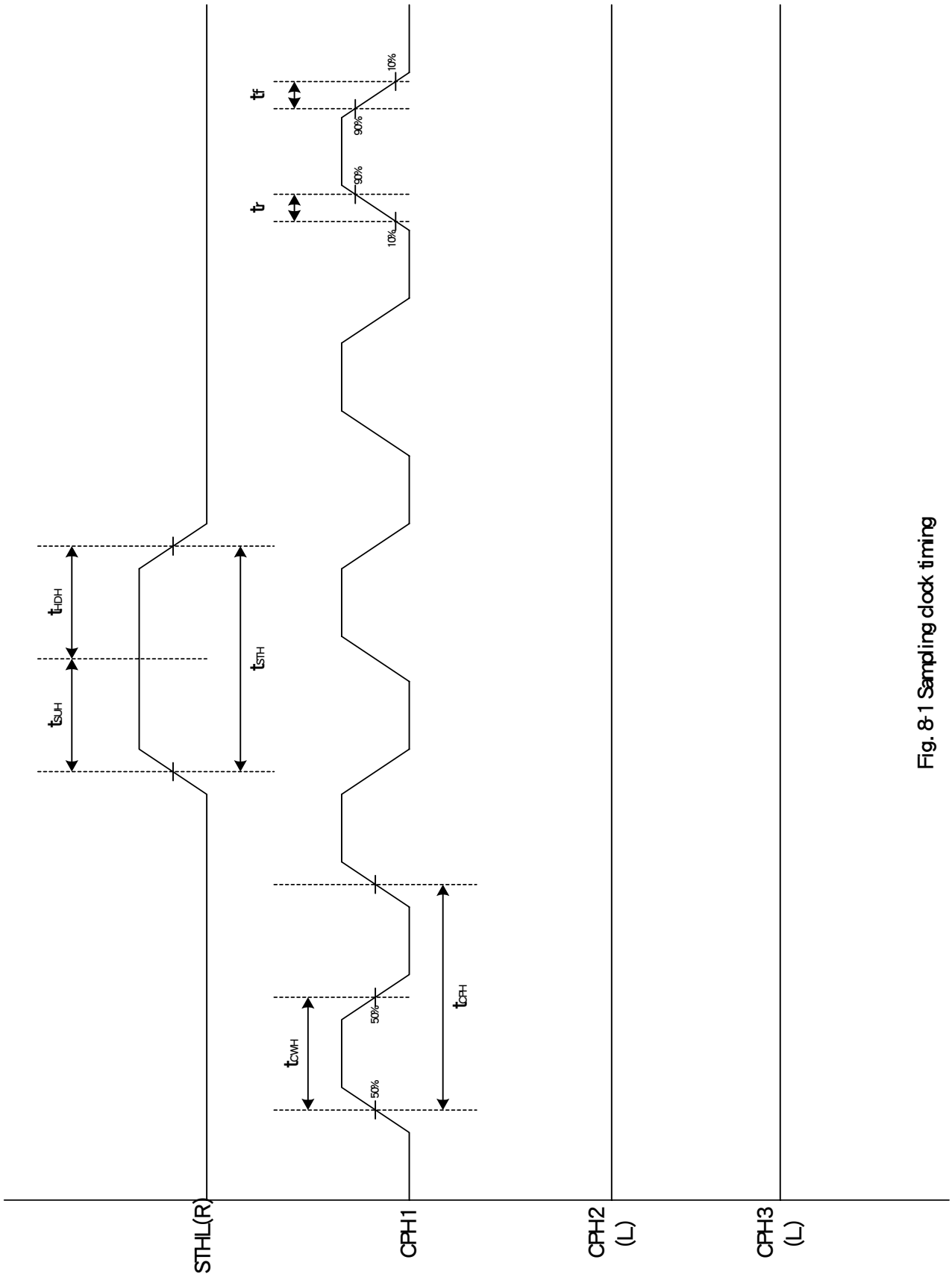

Fig. 8-1 Sampling clock timing

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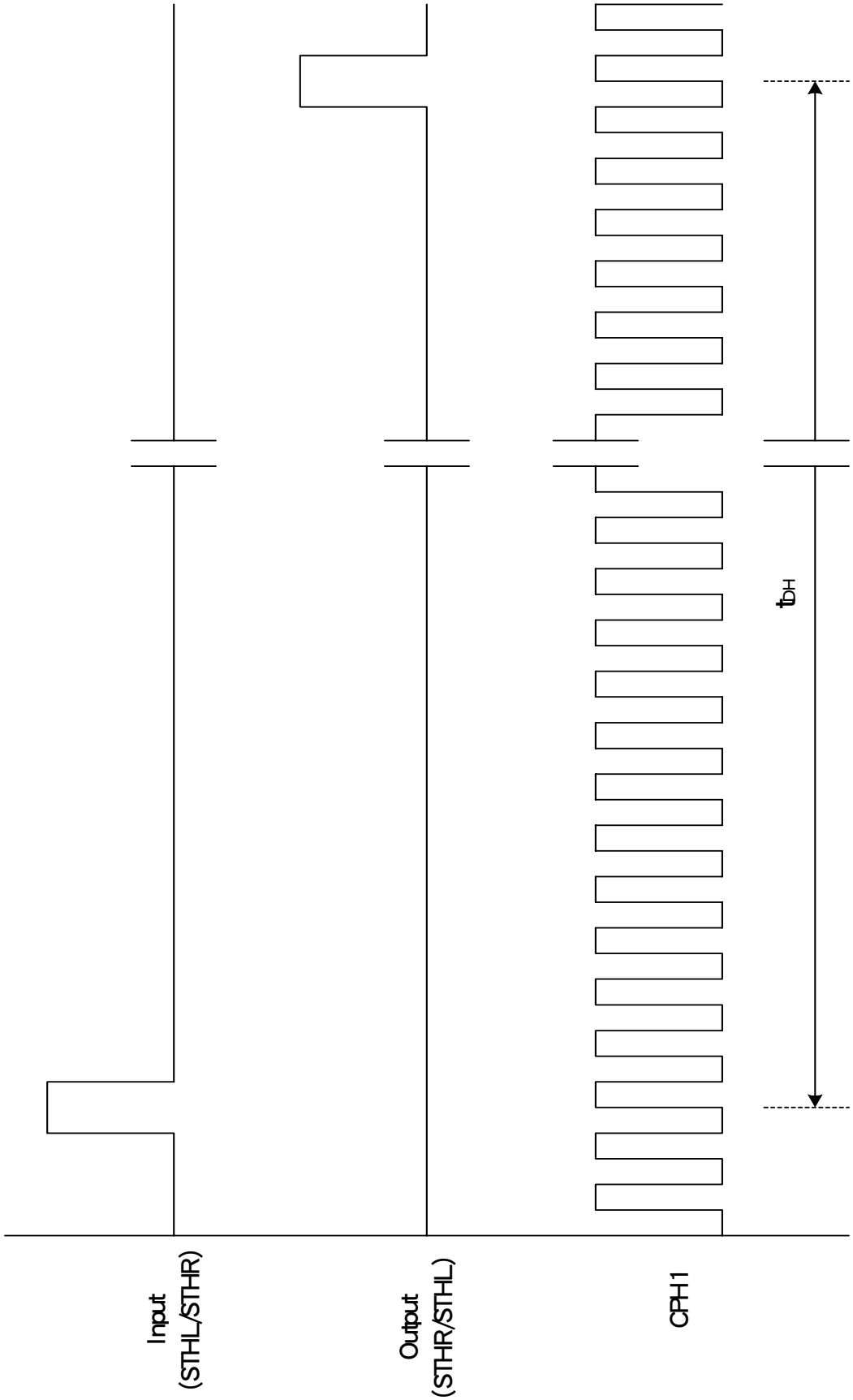

Fig. 8-2 Horizontal display timing range

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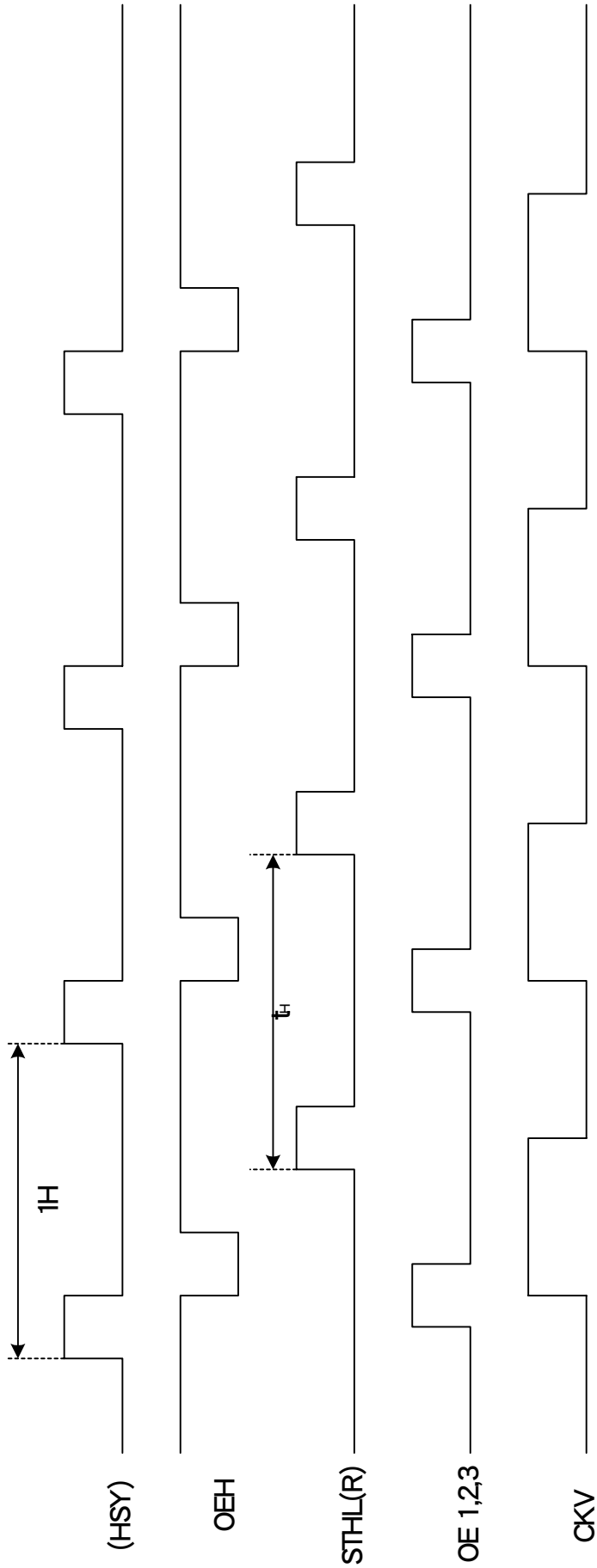

Fig. 8-3(a) Horizontal timing

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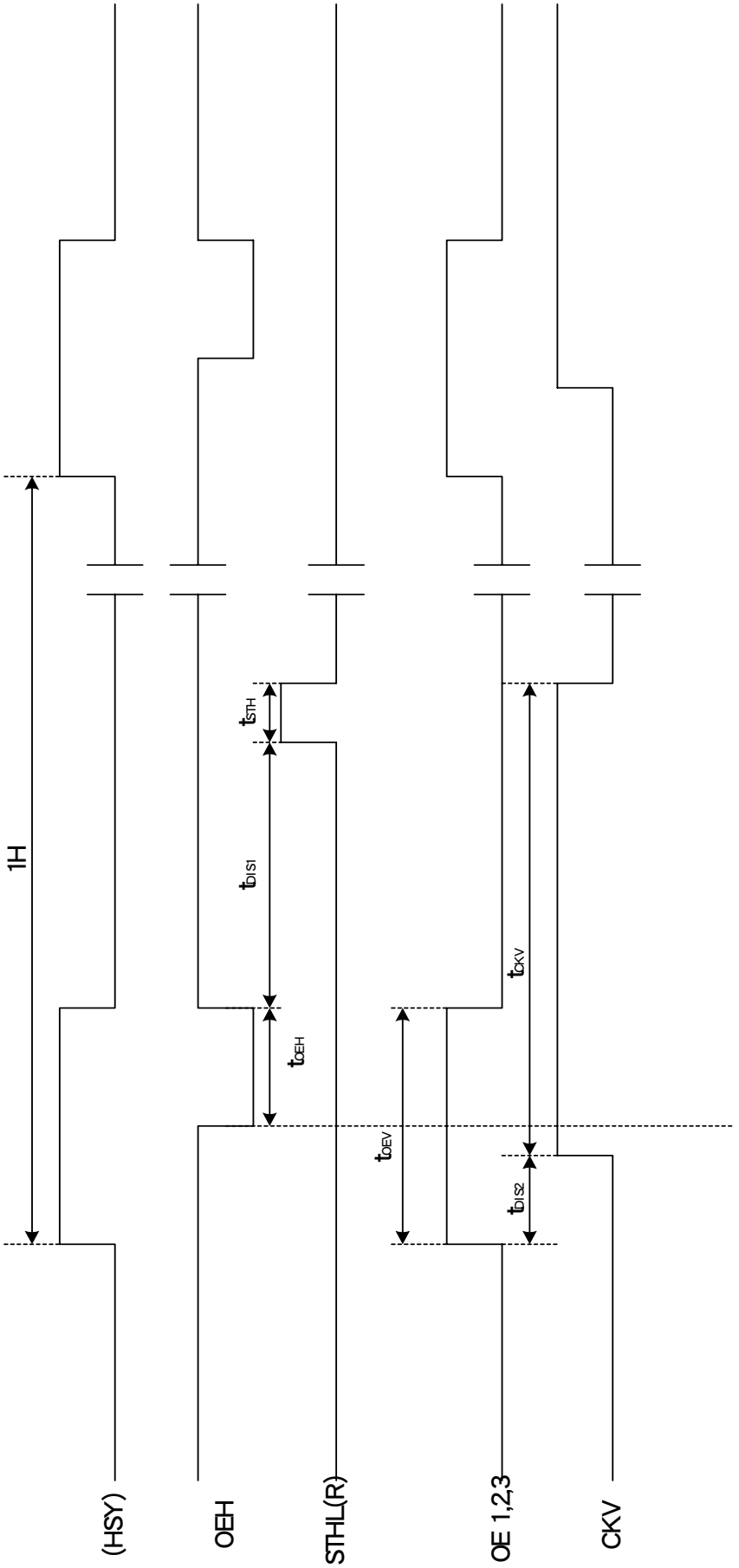

Note : The falling edge of OEV should be synchronized with the falling edge of OEH

Fig. 8-3 (b) Detail horizontal timing

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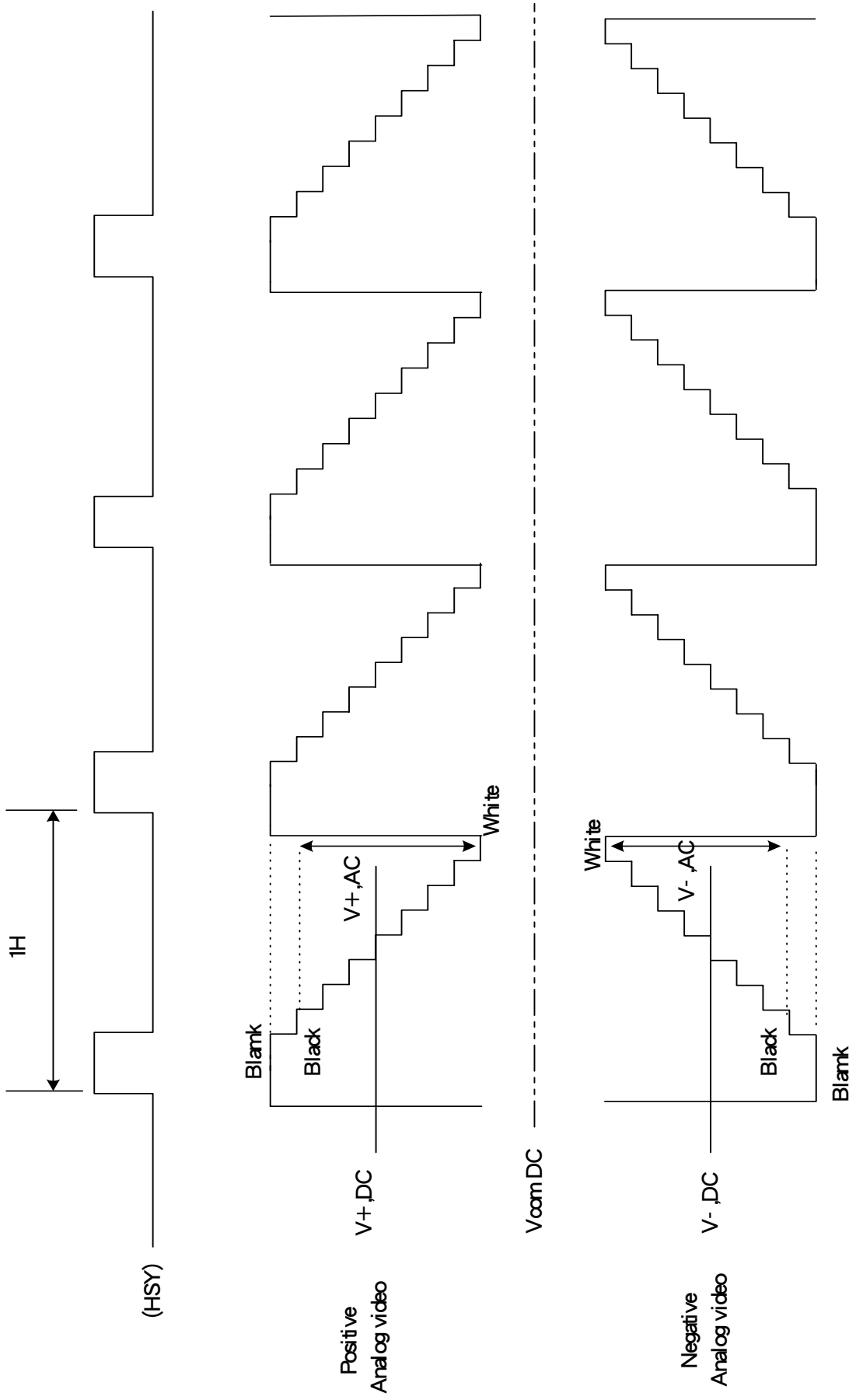

Fig 8-3(c) Vcom &Analog video timing

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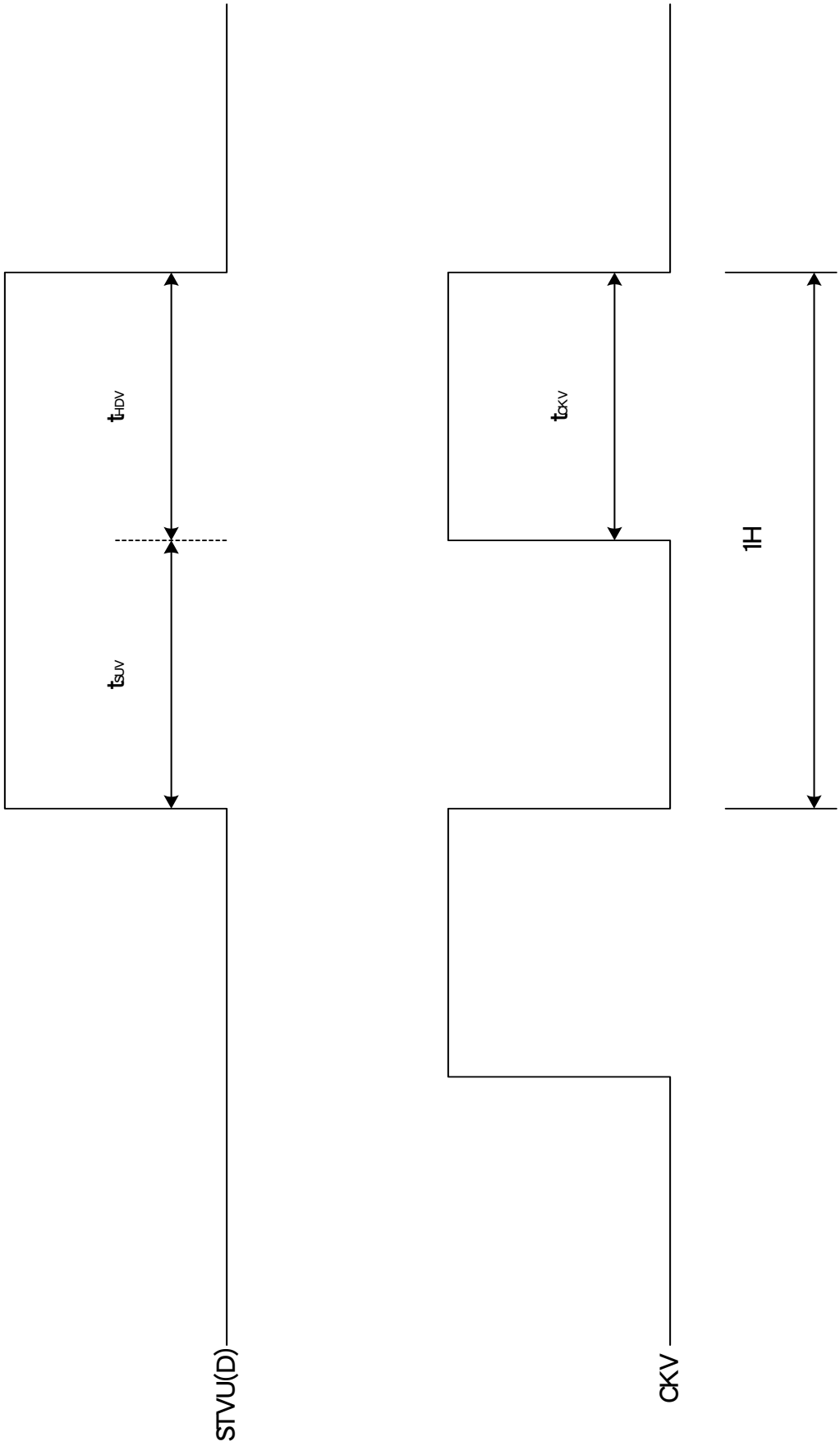

Fig. 8-4 Vertical shift clock timing

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Vertical timing

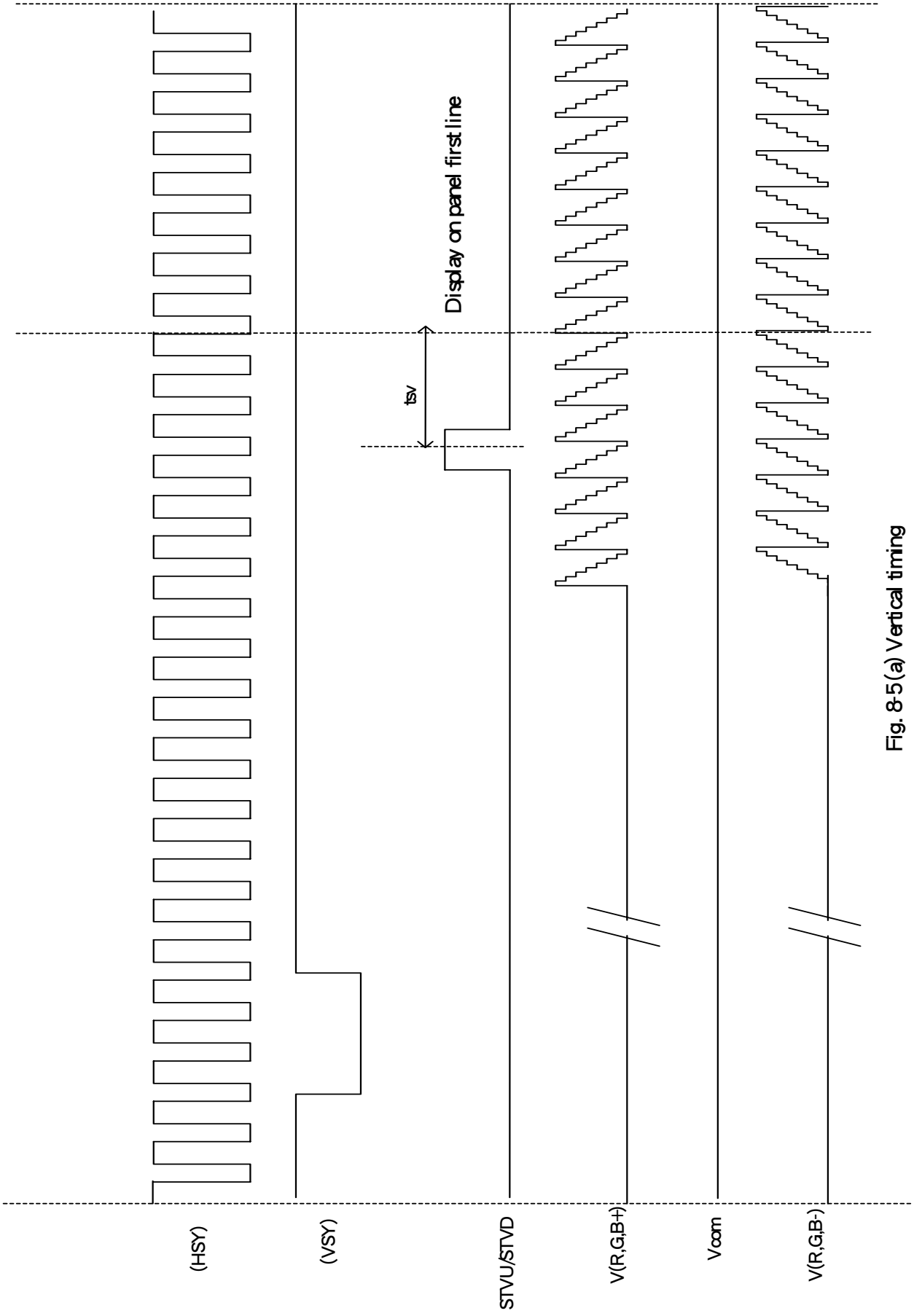

Fig. 8-5(a) Vertical timing

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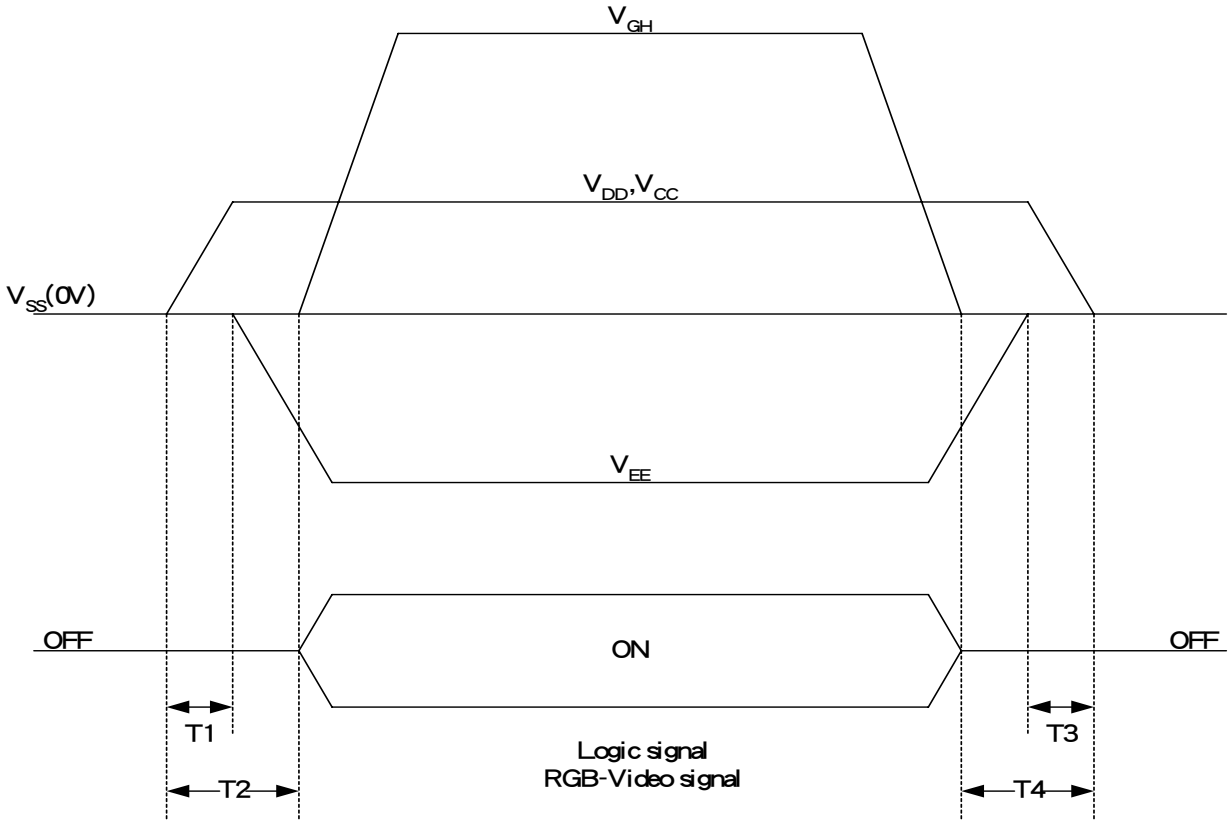

9. Power on Sequence

The Power on Sequence only effect by V_{CC}, V_{DD},V_{EE} and $V_{GH,}$ the others do not care.

1) 10ms≦T1<T2
2) 0ms<T3≦T4≦10ms

10. Optical Characteristics

10-1) Specification

Ta = 25℃

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ 21, θ 22	CR≧10	45	55		deg	Note 10-1
	Vertical	θ 12		10	15		deg	
		θ 11		30	35		deg	
Contrast Ratio		CR	At optimized Viewing angle	200	350			Note 10-2
Response time	Rise	Tr	θ =0°		15	30	ms	Note 10-4
	Fall	Tf			25	50	ms	
Brightness				300	350		cd/㎡	Note 10-3
Uniformity		U		70	75		%	Note 10-5
White Chromaticity		x	θ =0°	TBD	TBD	TBD		Note 10-3
		y		TBD	TBD	TBD		
Lamp Life Time +25℃					TBD		hrs	

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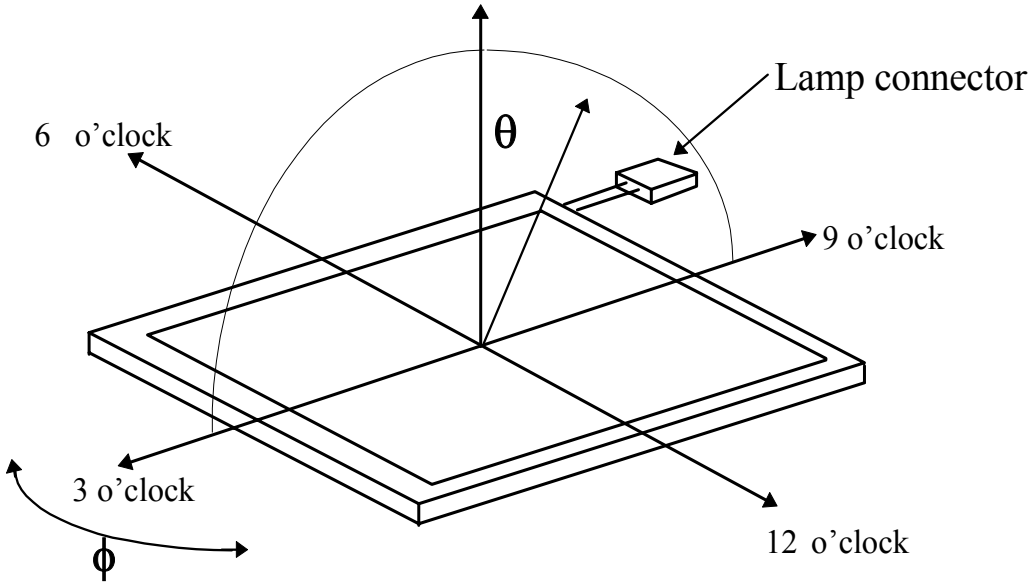
Note 10-1 : The definitions of viewing angles



Note 10-2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

(Testing configuration see 10-2)

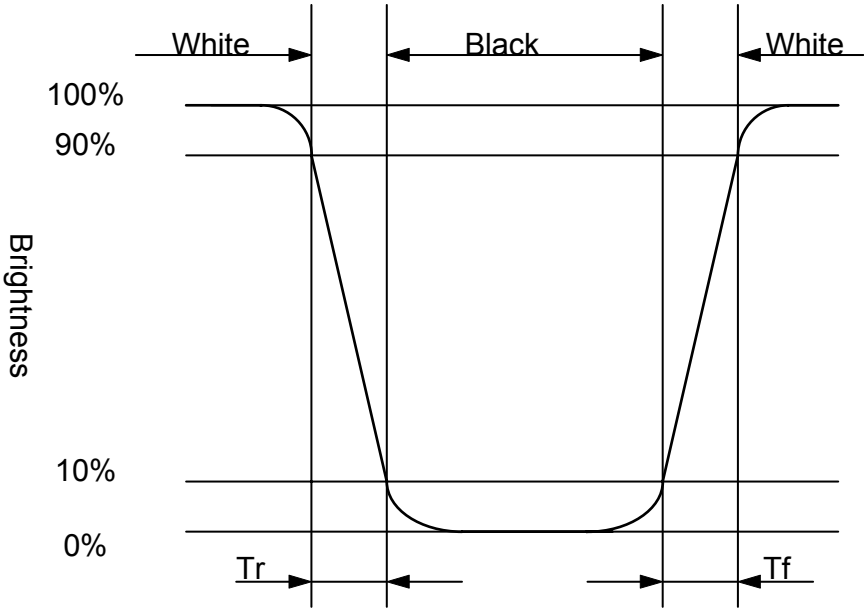
Contrast Ratio is measured in optimum common electrode voltage.

Note 10-3 : 1. Topcon BM-7(fast) luminance meter 1°field of view is used in the testing (after 20~30 minutes operation).

2.Lamp current : 6 mA

3.Inverter model : TDK-347.

Note 10-4 : The definition of response time:



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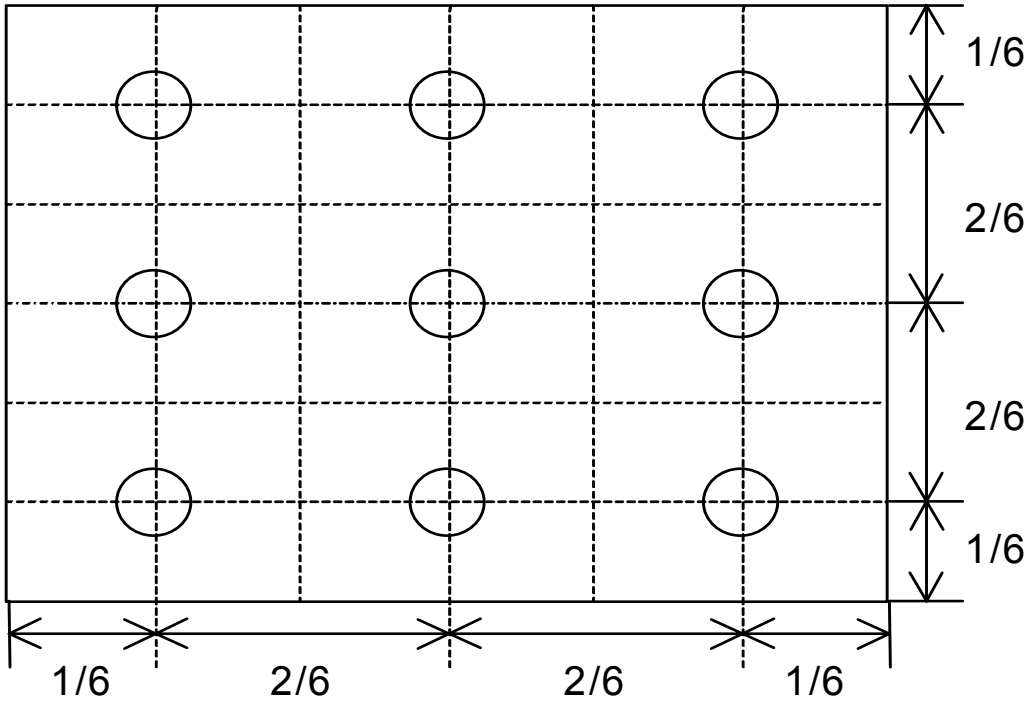
Note 10-5 : The uniformity of LCD is defined as

$$U = \frac{\text{The Minimum Brightness of the 9 testing Points}}{\text{The Maximum Brightness of the 9 testing Points}}$$

Luminance meter : BM-5A or BM-7 fast (TOPCON)
Measurement distance : 500 mm +/- 50 mm
Ambient illumination : < 1 Lux
Measuring direction : Perpendicular to the surface of module

The test pattern is white (Gray Level 63).



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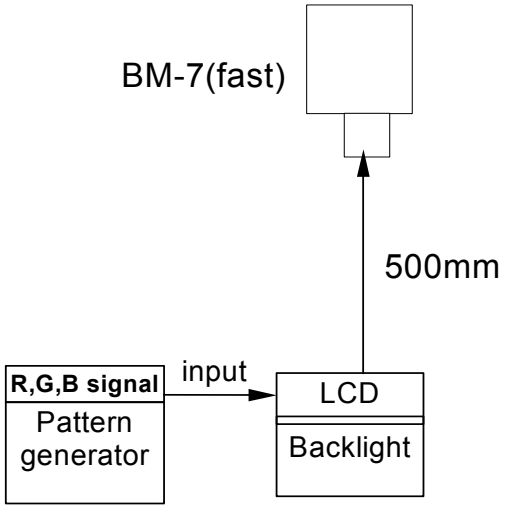
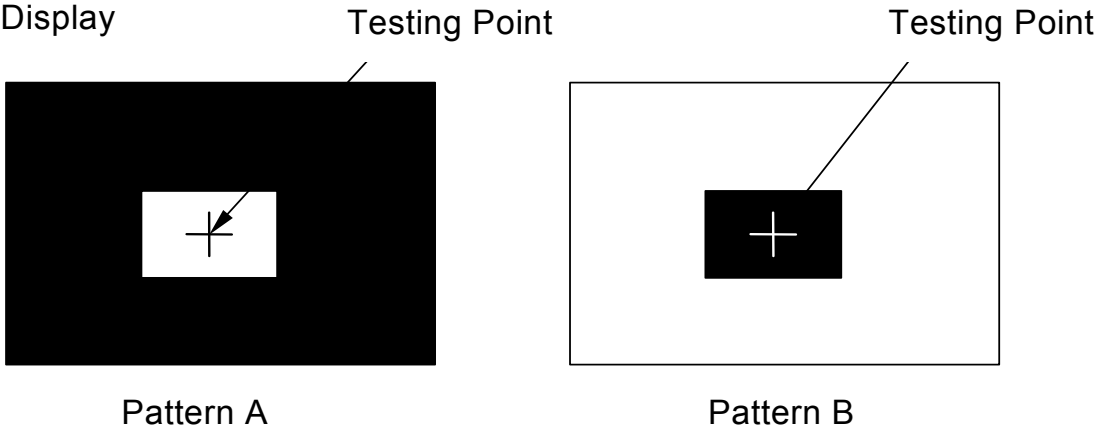
10-2) Testing configuration



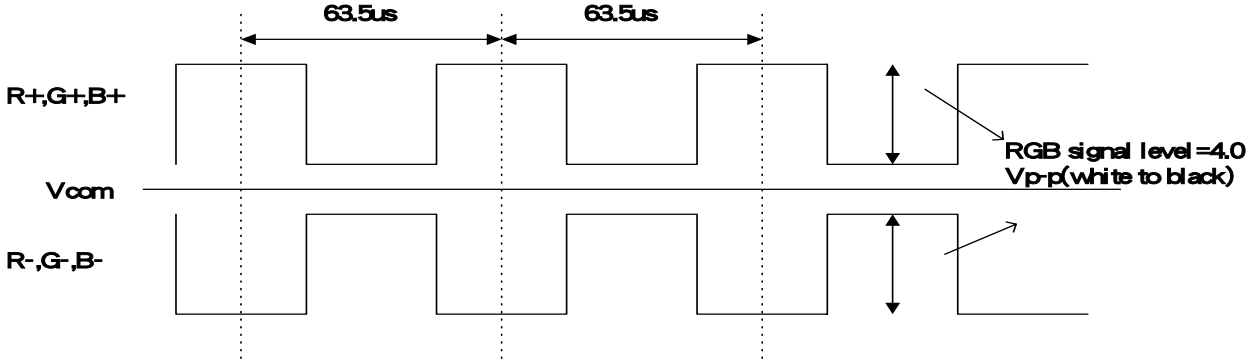
Caution: 1. Environmental illumination ≦ 1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

- LCD Display

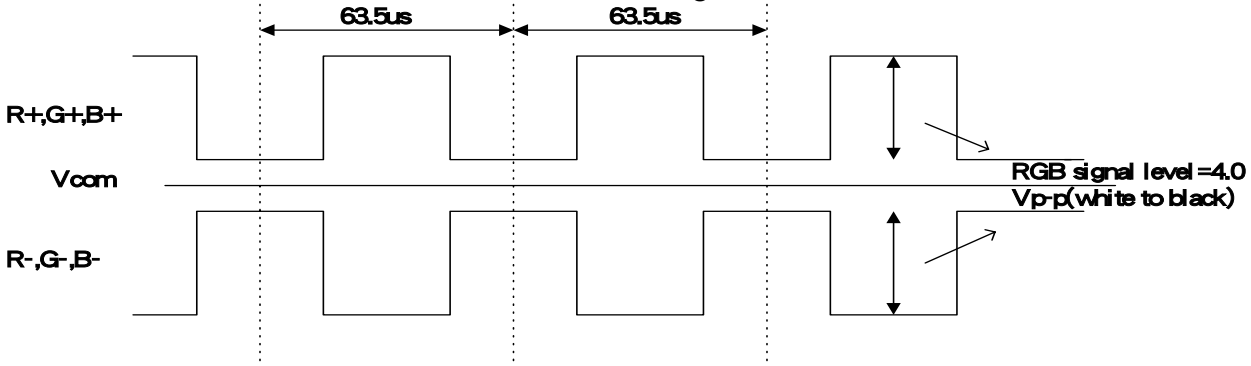


Pattern A Pattern B

- R, G, B Waveform of Pattern A at Testing Point



- R, G, B Waveform of Pattern B at Testing Point



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11. Handling Cautions

11-1) Mounting of module

a) Please power off the module when you connect the input/output connector.

b) Please connect the ground pattern of the inverter circuit surely. If the connection is not perfect, some following problems may happen possibly.
1.The noise from the backlight unit will increase.
2.The output from inverter circuit will be unstable.
3.In some cases a part of module will heat.

c) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.

d) Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

11-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.

b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.

c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.

d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

11-3) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.

b) Store the module at a room temperature place.

c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.

d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.

e) Observe all other precautionary requirements in handling general electronic components

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12. Reliability Test

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta = +80℃, 240 hrs
2	Low Temperature Storage Test	Ta = -30℃, 240 hrs
3	High Temperature Operation Test	Ta = +70℃, 240 hrs
4	Low Temperature Operation Test	Ta = -20℃, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +50℃, 80%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-20℃→+70℃, 200 Cycles 30 min 30 min
7	Vibration Test (non-operating)	Frequency：10 ~ 55 H_Z Amplitude：1 mm Sweep time: 11 mins Test Period: 6 Cycles for each direction of X, Y, Z
8	Shock Test (non-operating)	100G, 6ms Direction: ±X, ±Y, ±Z Cycle: 3 times
9	Electrostatic Discharge Test (non-operating)	200pF , 0Ω ±200V 1 time / each terminal

Ta: ambient temperature
Note: All about temperature test before must remove polarizer ’s protective film.

[Criteria]
Under the display quality test conditions with normal operation state, there should be no change which may affect practical display function.

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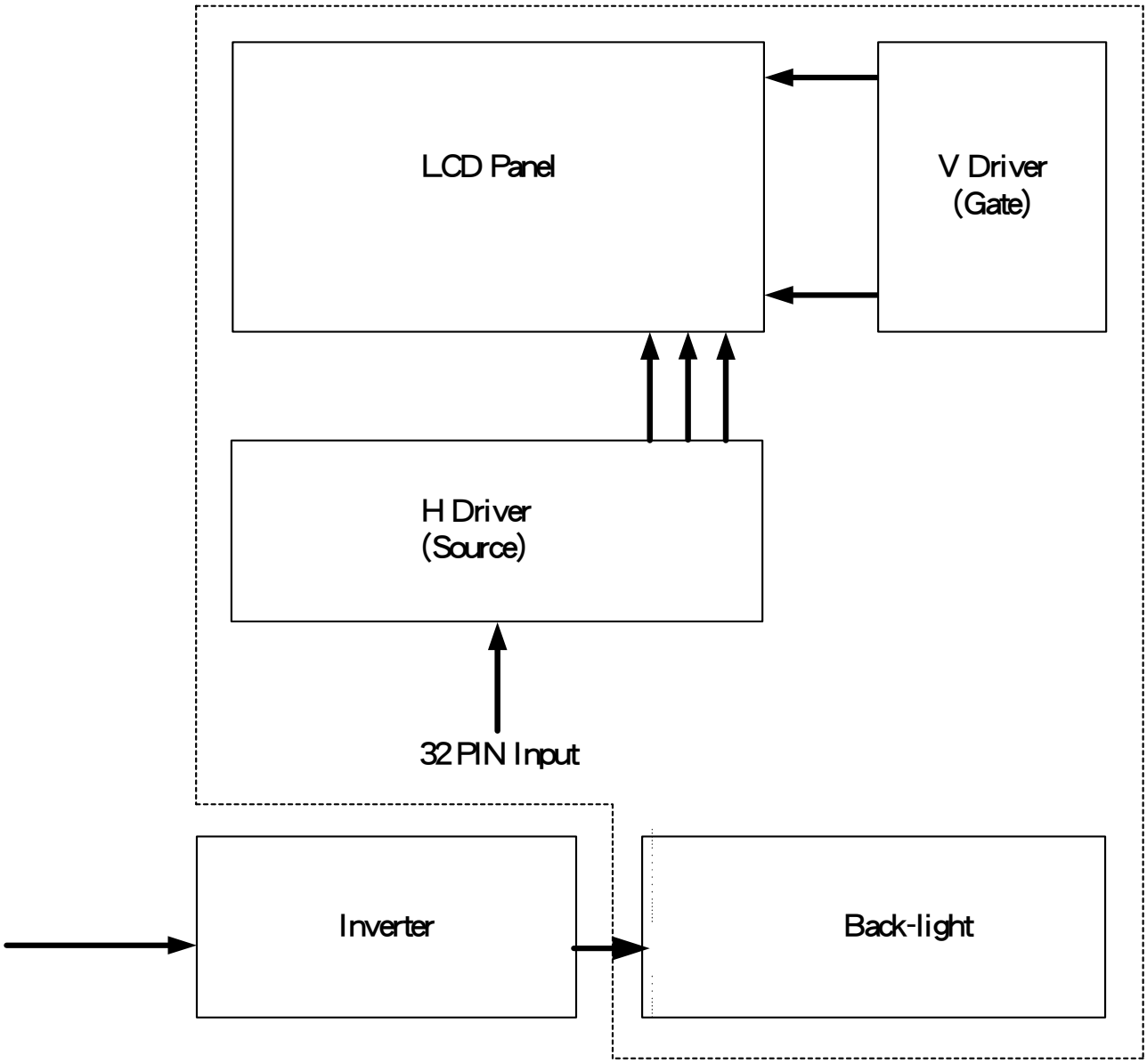
13. Block Diagram



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14. Packing

TBD

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Revision History

Rev.	Issued Date	Revised Contents
0.1	Mar.15,2005	NEW
0.2	Mar.22,2005	Modify: Page 4,5:4. Mechanical Drawing of TFT-LCD Module

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