SAMSUNG DISPLAY

Product Specification

CUSTOMER	
DATE OF ISSUE	2015.03.18

MODEL NO.	ABC097AB02
EXTENSION CODE	

Approved by	
Prepared by	
LCD Sales & Marketing Team Samsung Display Co., Ltd	

Samsung Secret

REVISION HISTORY

Date.	Rev. No.	Page	Revision Description

1. GENERAL DESCRIPTION

DESCRIPTION

The ABC097AB02 uses a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFTs as switching components. This model is composed of a TFT LCD panel, a driver circuit and BLU. This 9.7" model has a resolution of 1536 x 2048 pixels and can display up to 16,777,216 colors.

FEATURES

High contrast ratio
QXGA(1536 x 2048 pixels) resolution
PCB with rigid flex cables
Low power consumption
Fast Response
DE (Data enable) only mode
3.7V eRVDS Interface
ITO Tape
PCB Insulation Tape
12 strings, 3 dual die LEDs per string White LED Backlight
4lane(RBR) eDP Interface

APPLICATIONS

Tablet
If the intent to use this product is for other purpose, please contact Samsung Display.

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	147.451 (H) x 196.579 (V) (9.7"diagonal)	mm	
Driver Element	a-Si TFT active matrix		
Display colors	16,777,216 (24bits)		
Number of pixel	1536 * 2048 (QXGA)	Pixel	
Pixel Configuration	RGB Vertical Stripe		
Pixel pitch	3 x 0.032(H) x 0.096(V)	mm	
Display Mode	Normally Black, Transmissive, PLS		
Thickness of glass	0.2	mm	
White LED Backlight	12 strings, 3 dual die LEDs per string.		
Environmental safe regulation	Pb Free, Halogen Free		

MECHANICAL INFORMATION

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (Body)	160.01	160.31	160.61	mm	(1)
	Horizontal (HOLE-HOLE)	155.935	156.105	156.275	mm	(2)
	Vertical (Body)	208.63	208.93	209.23	mm	(1)
	Vertical (HOLE-HOLE)	212.472	212.642	212.812	mm	(2)
	Depth (Center)	1.72	1.90	2.08	mm	(3)
	Depth (with Shield-can)	4.06	4.31	4.56	mm	(4)
Weight		-	-	112.0	g	

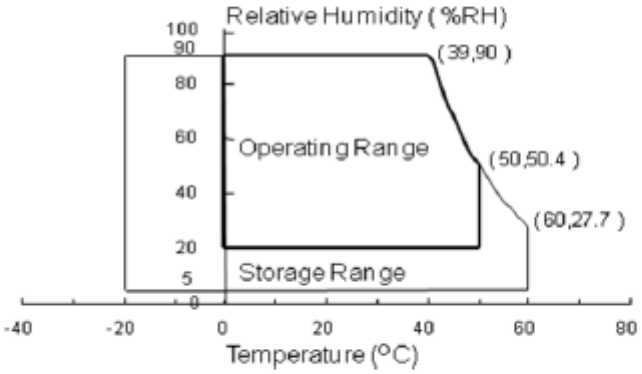
NOTE (1) without Flange and Tape
(2) Flange Hole(Upper) to Hole(Lower)
(3) TOP Polarizor to M-Chassis (without Protective Film)
Thickness Measuring Method : 100gf with Height Gauge
(4) Shield-can to Top Polarizor (without Protective Film)
Thickness Measuring Method : 100gf with Height Gauge

2. ABSOLUTE MAXIMUM RATINGS

2.1 ENVIRONMENTAL ABSOLUTE RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	60	°C	(1)
Operating temperature (Temperature of glass surface)	TOPR	0	50	°C	(1)
Shock (non-operating)	Snop		240	G	(2), (4)
Vibration (non-operating)	Vnop		2.41	G	(3), (4)

Note (1) The range of temperature and relative humidity are shown in the graph below 90% RH Max. . (39℃ ≥ Ta) If the temperature is higher than 40 ℃, the maximum temperature of wet–bulb shall be less than 39℃. No condensation



(2) Vibrate ±X, ±Y, and ± Z axis in the shape of the half sine wave one time for 2ms .
(3) Vibrate the X, Y, and Z randomly within a 5 - 500 Hz range for 30min.
(4) When testing a vibration and a shock, the fixture, which holds the module to be tested shall be hard and rigid in order for the the module not to be twisted or bent by the fixture.

2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

V_{LCD_VCC} =3.7V, V_{SS} = GND = 0V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{LCD_VCC}	V_{SS} - 0.3	4.0	V	(1),(2)
eRVDS Input Voltage	V_{LVDS}	V_{SS} - 0.3	2.0		

Note (1) Within Ta (25 ± 2 °C)
(2) Permanent damage to the device may occur if exceed maximum values.

2.2.2 BACKLIGHT UNIT

LED Manufacturer	Nichia	TG
Number of LEDs	36	<-
LED Forward Voltage Range for any LED string	MAX: 18 V at eDP flex bonding pad	<-

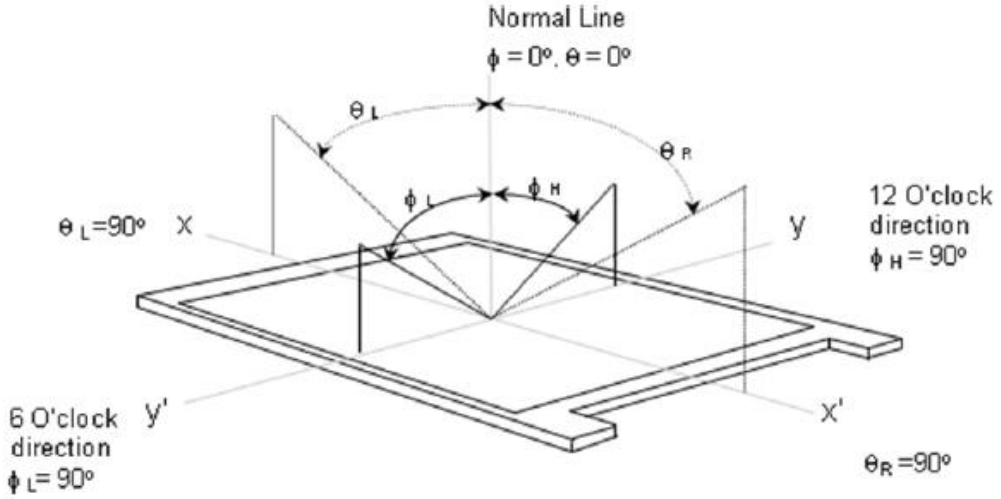
3. OPTICAL CHARACTERISTICS

The following items are measured under the stable conditions.* The optical characteristics should be measured in the dark room or the equivalent environment by the methods shown in the Note (5).
Measuring equipment : TOPCON SR-3

Ta = 25 ± 2 °C, V_{LCD_VCC} =3.7V, fv= 60Hz, fDCLK = 205.21MHz, IF = 100% duty

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	Normal Viewing Angle ϕ = 0 θ = 0	700	1000	-	-	(1)(2)(5)
Response time (Rising + Falling)		T_{RT}		-	17	24	ms	(1)(3)
White Luminance		YL		360	440	-	cd/m2	IF=100% Duty (1),(4)
Color Chromaticity (CIE)	Red	Rx		-	0.640	-		(1)(5) SR-3
		Ry			0.330			
	Green	Gx			0.300			
		Gy			0.600			
	Blue	Bx			0.150			
		By			0.060			
	White	Wx			0.3021			
		Wy			0.3150			
Viewing Angle	Hor.	θL	CR≥10 At center	-	85	-	Degrees	(1)(5)
		θH		-	85	-		
	Ver.	ϕH		-	85	-		
		ϕL		-	85	-		
White variation(13p)		δL		-	1.4	1.6	-	(6)

Note (1) The definition of viewing angle : The range of viewing angle (10 ≤ C/R)



Note (2) The definition of contrast ratio (CR) : The ratio of max. gray and min gray at 5 points (4, 5, 7, 9, and10)

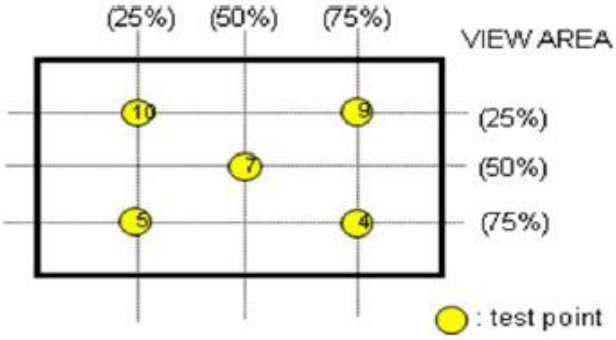
$$CR = \frac{CR(4) + CR(5) + CR(7) + CR(9) + CR(10)}{5}$$

Points = 4 5 7 9 10 at the figure of Note(6).

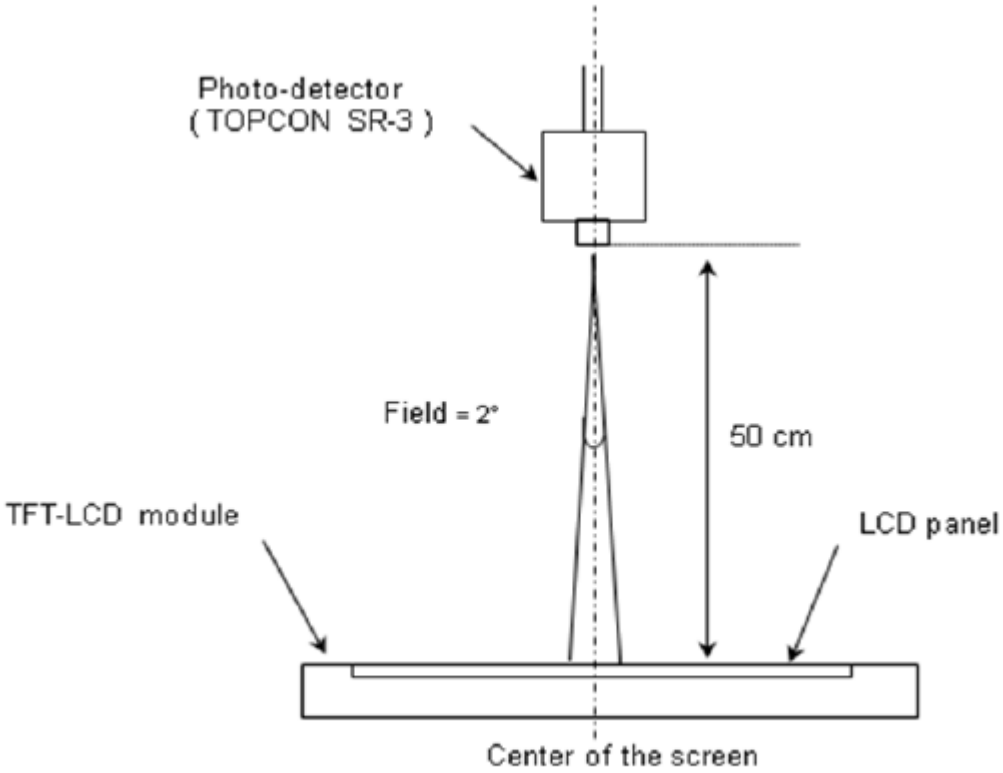
Note (4) The definition of average luminance of white : Measure the luminance of white at 5 points.

Average Luminance of White (Y_{LAVE})

$$Y_{LAVE} = \frac{Y_{L4} + Y_{L5} + Y_{L7} + Y_{L9} + Y_{L10}}{5}$$



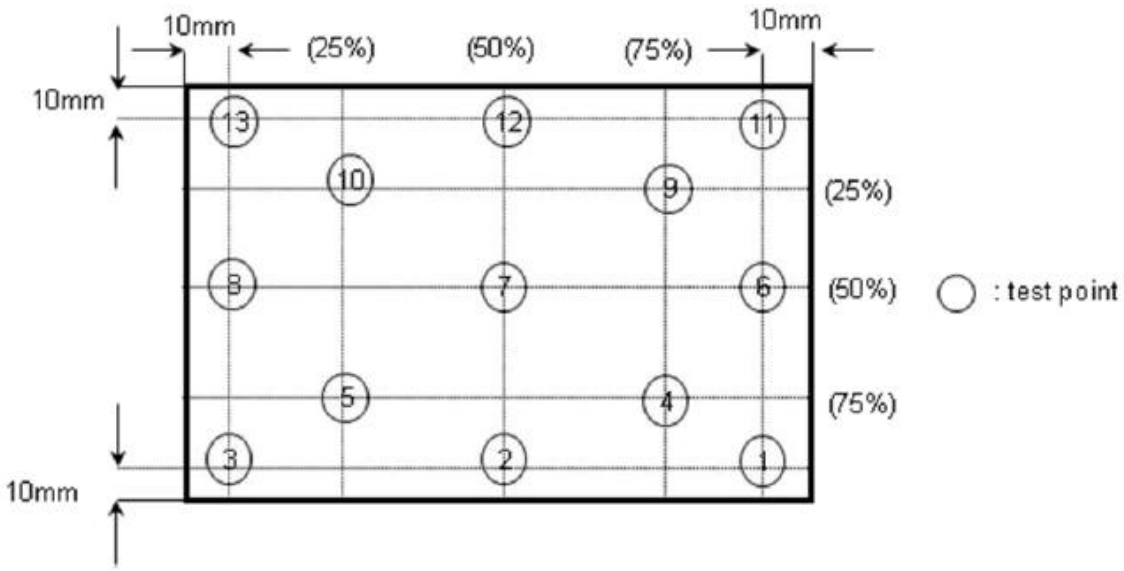
Note (5) Measure the panel, which is left for 30 min. at the normal temp. after leaving it for 30 min with turning
the back light on at the rating. The measurement should be executed under the condition including the ambient temp., 25℃±2℃, the dark room, windless(removed the direct wind), and no vibration.
Environment condition : Ta = 25 ± 2℃



[Optical characteristics measurement setup]

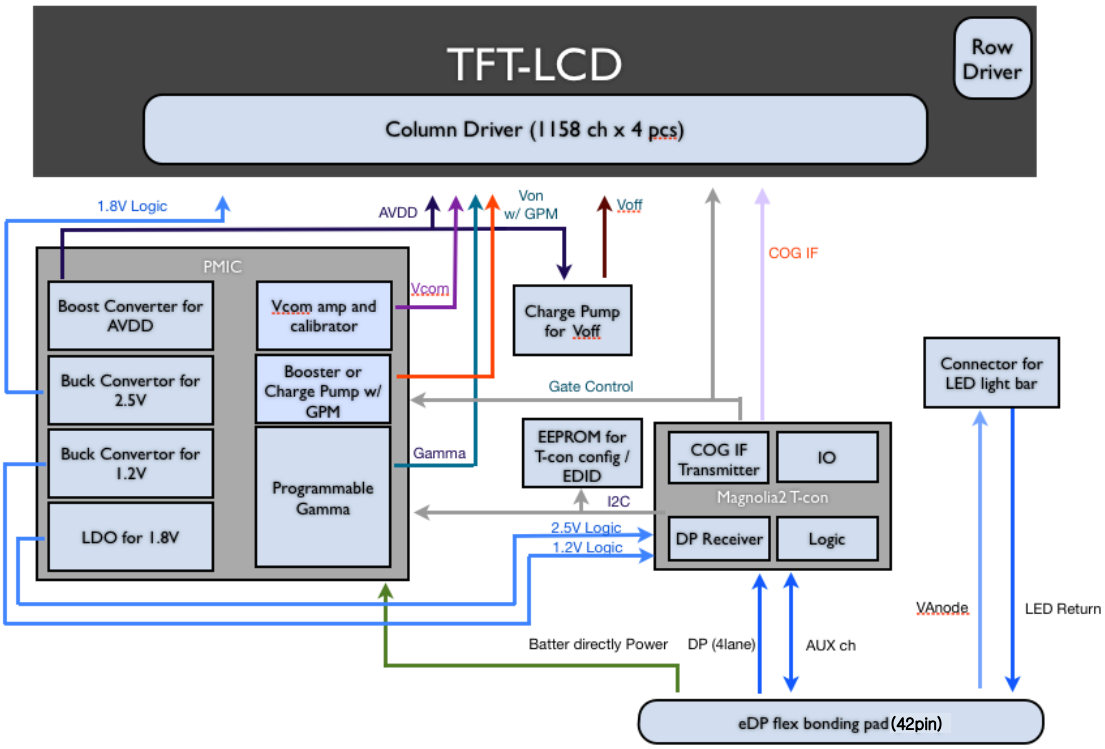
Note (6) The definition of white variation at 13 points (δ L)

$$\delta L = \frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}}$$



4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 THE STRUCTURE OF LED PLACEMENT

4.2.1 LED Connection

Table 14 LED Assignments on FPC String

String	LED1	LED2	LED3
1	1	7	13
2	2	8	14
3	3	9	15
4	4	10	16
5	5	11	17
6	6	12	18

4.2.2 LED string to string current variation

LED current variation from string to string is defined as Δ = (Imax - Imin)/Iavg, where Imax and Imin are the maximum and minimum current on any of the 6 strings, espectively. LED current variation Δ should be within ±2.0% during the complete range of PWM dimming from 17.5mA (100% duty) to0.4mA (2% duty)

4.2.3 LED Driver Requirement

16-bit dimming control through Pulse Width Modulation (PWM) scheme with consistent current on LED strings. The LED string PWM signal frequency is 8KHz or higher. Between each string a 60 degree phase delay is implemented.

5. ELECTRICAL CHARACTERISTICS

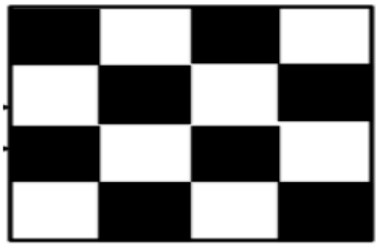
5.1 TFT LCD MODULE

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply		VDD	3.4	3.7	4.0	V	
Vsync Frequency	60 Hz	fv	-	60	-	Hz	
Rush Current	IRUSH	-	-	1.5	-	A	(5)
Current of Power Supply	White	IDD	-	215	237	mA	(2), (3)*a
	Mosaic		-	215	237	mA	(2), (3)*b
	Red		-	354	390	mA	(2), (3)*e

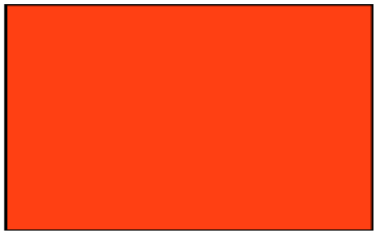
Note (1) The data pins for display and signal pins for timing should be connected.(GND= 0V)
(2) fV = 60Hz, VLCD_VCC = 3.7V , DC Current.
(3) Power dissipation pattern
Note (4) The dissipation pattern for power

(a) White screen

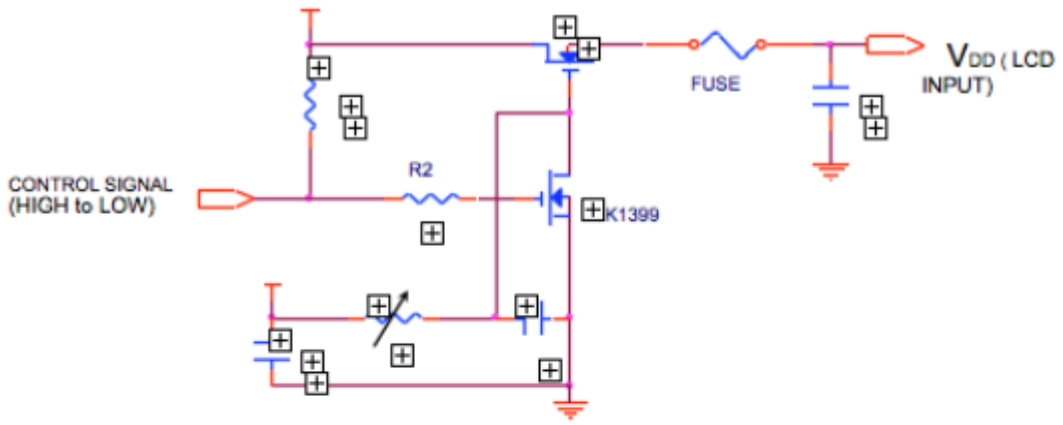
(b) Mosaic (or checker) pattern

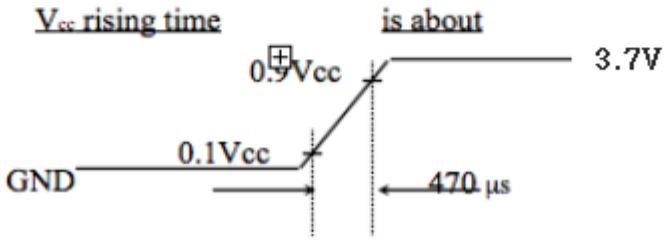


(c) Red



Note (5) The condition for measurement for rush current





5.2 Signal Timing

5.2.1 Timing Data

Signal	Parameter	Symbol	Min	Typ	Max	Unit	Note
Dclk	Clock Period	Tc		5		Ns	1
	Clock Frequency	fc		200		MHz	1/Tc
	Duty Ratio (%High)	Kdr	40	50	60	%	Tch/Tc
	Rise Time	Tr.clk		1		ns	
	Fall Time	Tf.clk		1		ns	
DE (Data Enable)	DE Setup Time	Tse		1		ns	
	Data Setup Time	Tsd		1		ns	
	Data Hold Time	Thd		1		ns	
	Horizontal Period	Th		1536		Tc	2
	Horizontal Blank Period	Tha		83		Tc	
	Vertical Period	Tv		2048		Th	Fv=60Hz, 3
	Vertical Blank Period	Twvb		11		Th	
Hsync	Hsync Back Porch	Hbp		52		Tc	
	Hsync Pulse Width	Twh		15		Tc	
	Hsync Front Porch	Hfp		16		Tc	
	H Active Period	Thd		1536		Tc	Display Period
Vsync	Vsync Back Porch	Vbp		3		Th	
	Vsync Pulse Width	Twv		1		Th	
	Vsync Front Porch	Vfp		7		Th	
	V Active Period	Tvd		2048		Th	Display Period

Notes: (1) When the timing controller sets DE only Mode, Hsync and Vsync should be set low logic level or ground. The duration of DE (DTMG) signal must be longer than 1 clock period (TC) at every horizontal sync period;

(2) Horizontal Period = One Line Scanning Time;

(3) The vertical period TV is related to the frame frequency fV, i.e., 60 Hz.

5.2.2 Video Timing Diagram

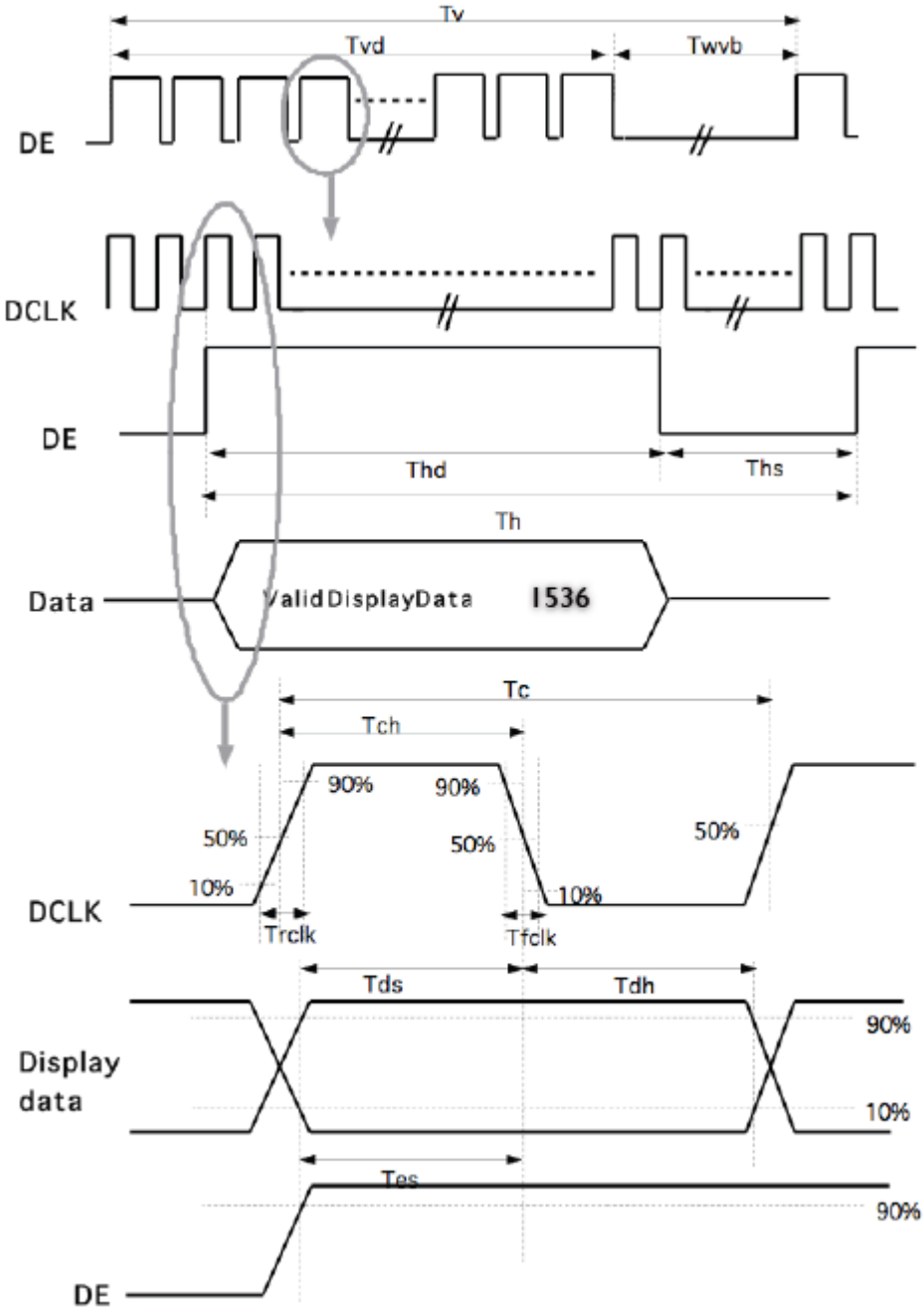


Figure 12 Display Video Timing Diagram

5.2.3 Color Input Data Reference

Color		Input Color Data																							
		Red								Green								Blue							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Dark	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(01)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(02)	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
		1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(253)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255) Bright																								
Green	Green(00)Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Green(02)	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green(255) Bright																								
Blue	Blue(00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue(02)	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Blue(255) Bright																								

Table 9 Color Data Reference

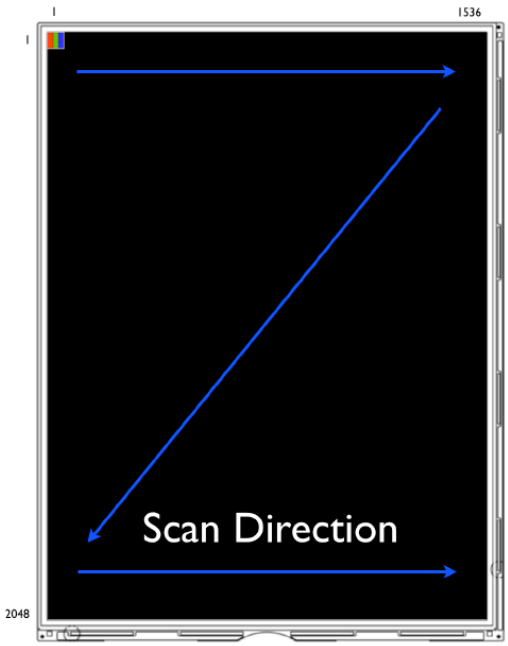
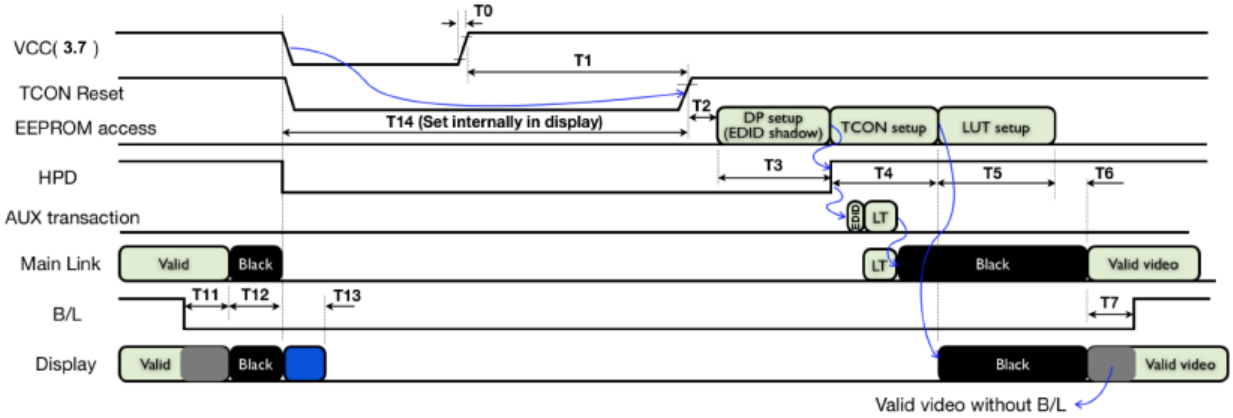


Figure 13 Pixel Format and Scanning Direction on the Display

5.2.4 Power on-off sequence



Time	Description	Min.	Typ.	Max.	Time	Description	Min.	Typ.	Max.
T0	VCC rise time (10% - 90%)	0.1	-	2	T11	One full valid frame after B/L OFF	-	-	17
T1	Reset assertion delay from VCC rising	2	-	25	T12	One full black frame after valid frame	-	-	17
T2	Internal circuit ready for EEPROM access	2	-	5	T13	Pixel discharge time	-	-	10
T3	DP Rx initialization	-	-	15	OFF Total	Total power-off delay	44		
T4	TCON initialization	-	-	25					
T5	LUT loading completion	-	-	75					
T6	One full black frame	-	-	17					
T7	One full valid frame	-	-	17					
ON Total	Total power-on delay	181			T14[1]	Preset delay for internal POR circuit	125		

1. T14 is to be set internally in display (pixel discharge, internal power supply discharge and restart, VGH pumping, etc)

Unit : ms

Figure 14. Display power On/Off Sequence Diagram

5.3 eDP INTERFACE

5.3.1 eDP DC I/O Charateristics

Parameter	Test Conditions	Min	Typ[2]	Max	Unit
I2C pins: xSCL, xSDA					
V_{OH} High-level output voltage	External 1.2kΩ pull-up to VCC		VCC		V
V_{OL} Low-level output voltage	2.5V to 2.8V I_{OL} = 8 mA			0.15VCC	V
SPI pins: IROMx					
V_{IH} LVCMOS input High-level voltage		0.7VDDIO			V
V_{IL} LVCMOS input Low-level voltage				0.25VDDIO	V
V_{OH} High-level output voltage	I_{OL} = 4 mA, I_{OH} = -4 mA	0.8VDDIO			V
V_{OL} Low-level output voltage				0.15VDDIO	V
LCD control pins:					
V_{OH} High-level output voltage	I_{OL} = 4 mA, I_{OH} = -4 mA	0.8VDDIO			V
V_{OL} Low-level output voltage				0.15VDDIO	V
General I/O pins					
V_{IH} LVCMOS input High-level voltage		0.7VDDIO			V
V_{IL} LVCMOS input Low-level voltage				0.25VDDIO	V
V_{OH} High-level output voltage	I_{OL} = 4 mA, I_{OH} = -4 mA	0.8VDDIO			V
V_{OL} Low-level output voltage				0.15VDDIO	V

5.3.2 eDP AC I/O Charateristics

Parameter	Test Conditions	Min	Typ[2]	Max	Unit
Supply ramp up time:					
$t_{2.5}$ VDDIO supply ramp up time	10% to 90% of the VDDIO supply voltage			10	ms
$t_{1.2}$ 1.2V supply ramp up time	10% to 90% of the 1.2V supply voltage			10	ms
Power ramp delay					
Δt_{POWER} Delay time from VDDIO supply to 1.2V VDD12 & VDDRX supply	90% of VDDIO supply to 90% of 1.2V supply	-10		10	ms
$\Delta t_{POWER\text{-}RST\#}$ Delay from 1.2V power ready & VDDIO power ready to RST_N pin de-assertion	90% of 1.2V supply & 90% of VDDIO supply (all power supplies ready) to 25% of the RST_N (pin D4) de-assertion (rising edge)	2			ms
CMOS output pins: GPIOx	C_L = 10 pF				
t_r Output rise time				6	ns
t_f Output fall time				6	ns
SPI pins: IROMx					
t_{hi} Clock high time		9			ns
t_{lo} Clock low time		9			ns
t_{setup} Data in setup time reference to clock rising edge		5			ns
t_{hold} Data in hold time reference to clock rising edge		5			ns
t_v Data out valid time reference to clock falling edge				9	ns
t_{ho} Data out hold time reference to clock falling edge		0			ns
t_{css} Chip select setup time reference to clock rising edge		25			ns
t_{csh} Chip select hold time reference to clock falling edge		10			ns
Master I2C pins: MSCL, MSDA					
t_{RISE} Master I2C bus 10% to 90% rise time				150	ns

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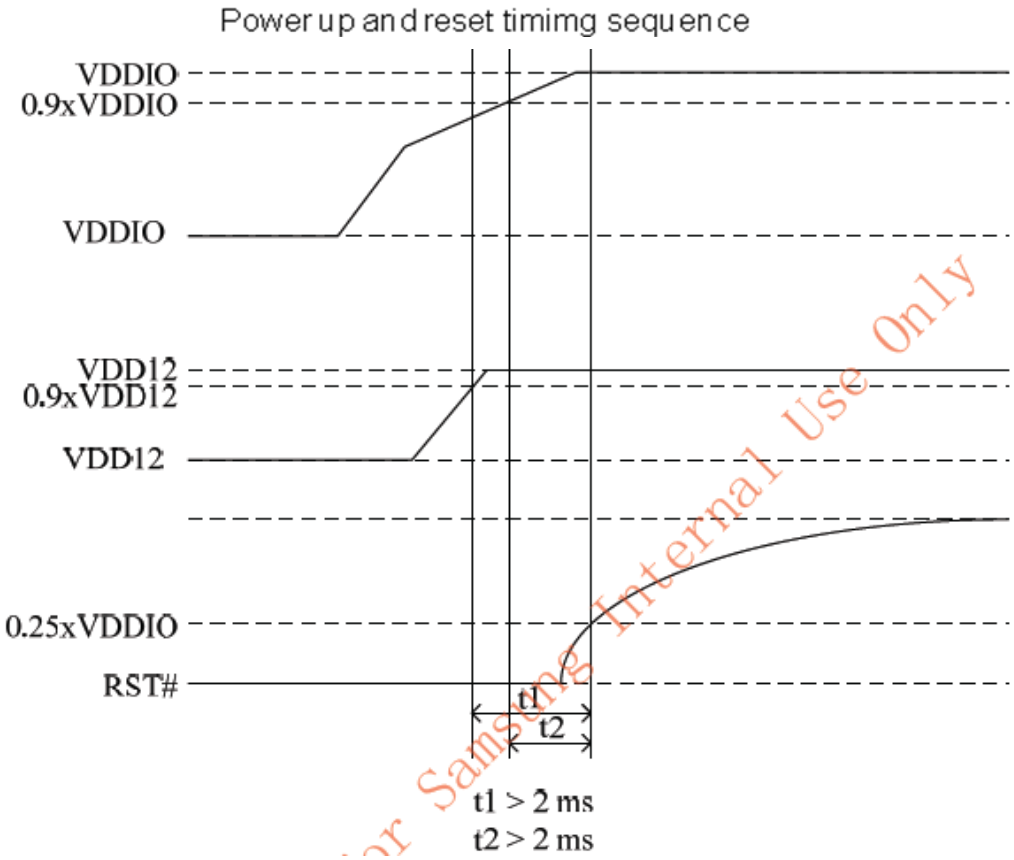

5.3.3 eRVDS transmitter characteristics

Symbol and Parameter	Test Conditions	Min	Typ[2]	Max	Unit
Transmitter Characteristics					
V_{OD}: Differential output voltage at default setting	COG LV driver test set-up as shown in the below figure Rterm=100Ω	320	400	480	mV
Minimum programmable swing (8 programmable levels)			200		mV
Maximum programmable swing (8 programmable levels)			600		mV
V_{CM}: Output common-mode voltage		500	600	700	mV
Minimum programmable V_{CM} (8 programmable steps)			500		mV
Maximum programmable V_{CM} (8 programmable steps)			700		mV
ΔV_{OD}: Variation in V_{OD} between 0 and 1				30	mV
ΔV_{CM}: Variation in V_{CM} between 0 and 1				30	mV
T_R/T_F: Rise and Fall Transition Time (20% - 80%)	V_{CM} = 600mV V_{OD} = 400mV		430		ps
R_{TX}: Transmitter Differential Output Impedance			100		Ω
Minimum programmable output impedance			70		Ω
Maximum programmable output impedance			500		Ω

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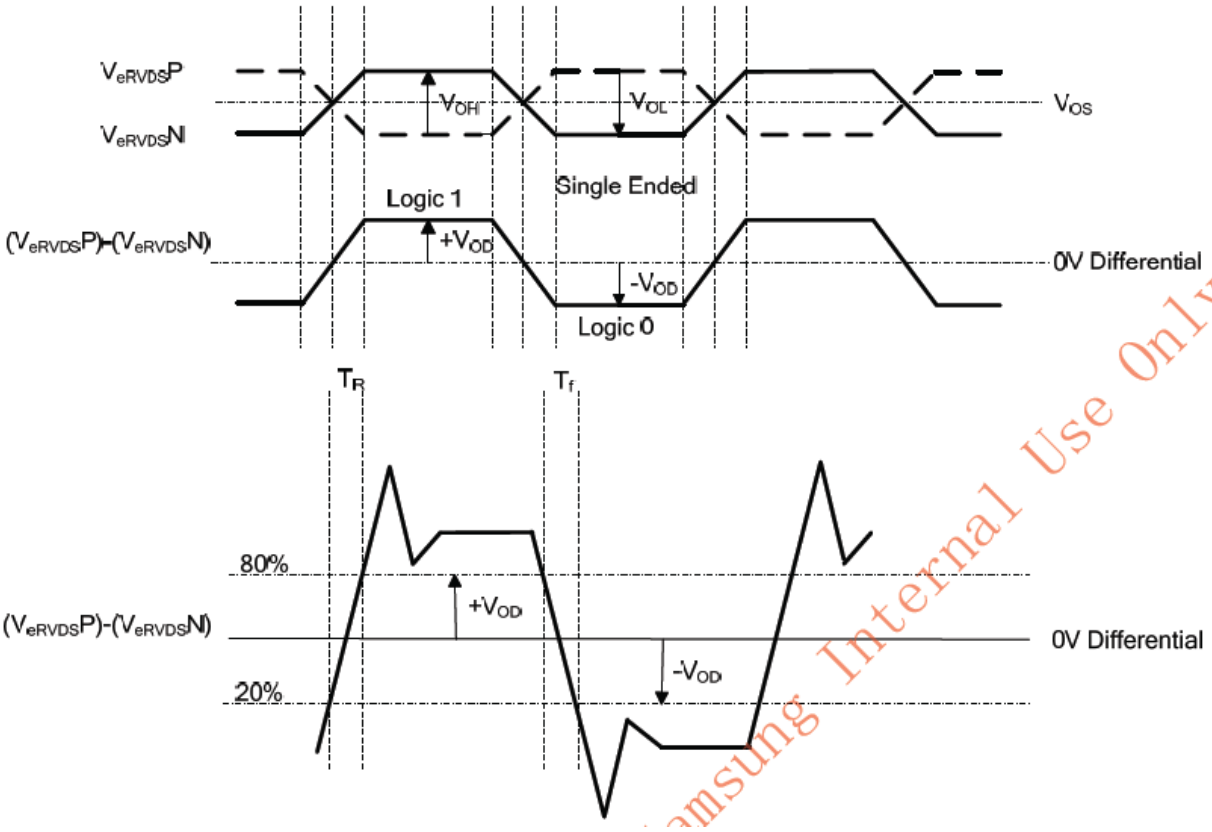
Power up and reset timimg sequence



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5.3.4 Displayport Aux channel charateristics

Symbol and Parameter		Test Conditions	Min	Typ[2]	Max	Unit
UI:	Unit Interval for AUX channel		0.4	0.5	0.6	µs
VAUX-DIFF-p-p:	AUX differential peak-to-peak voltage at TP1 when driving the bus		500		1000	mV
VAUX-DC-CM-TX:	AUX common mode voltage when receiving			GND		V
VAUX-DC-CM-RX:	AUX common mode voltage when transmitting			0.15		V
IAUX-SHORT:	AUX channel short circuit current				20	mA
RAUX-DIFF:	Differential termination resistance		80	100	120	Ω
RAUX-SE:	Single-ended termination resistance		40	50	60	Ω
CAUX:	AUX AC coupling capacitor		75		200	nF

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5.3.5 Diasplayport Main link receiver charateristics

Symbol and Parameter	Test Conditions	Min	Typ[2]	Max	Unit
Spread spectrum clock, down-spreading by SOURCE			0.5		%
Additional spread spectrum clock by SINK,					
Modulation frequency		10		40	kHz
Center spreading amplitude (programmable)		-1.0%		1.0	%
$V_{RX\text{-}DIFFp\text{-}p}$: Differential peak-to-peak input voltage at package pins		100		1320	mV
Maximum adaptive/programmable equalization level at 1.35GHz			9		dB
$V_{RX\_DC\_CM}$: Rx input DC common mode voltage			GND		V
$R_{RX\text{-}DIFF}$: Differential termination resistance		80		100	Ω
$R_{RX\text{-}SE}$: Single-ended termination resistance		40		60	Ω
I_{RX_SHORT}: Rx short circuit current limit				20	mA
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (HBR)					
RX intra-pair skew tolerance at HBR				150	ps
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (RBR)					
RX intra-pair skew tolerance at RBR				300	ps
Receiver Jitter Tolerance for High Bit Rate (HBR)					
Total jitter tolerance at 2MHz		1227			mUI
Total jitter tolerance at 10MHz		548			mUI
Total jitter tolerance at 20MHz		505			mUI
Total jitter tolerance at 100MHz		491			mUI
Receiver Jitter Tolerance for Reduced Bit Rate (RBR)					
Total jitter tolerance at 2MHz		1648			mUI
Total jitter tolerance at 10MHz		778			mUI
Total jitter tolerance at 20MHz		747			mUI
Note: Jitter Tolerance Testing follows *VESA DisplayPort™ PHY Compliance Testing Standard, Version 1.1.*					
Symbol Error Rate, normal link data transmission, HBR, 4 lane operation	1. TJ at Receiver Connector (TP3) ≦0.491UI @ Bit Error Rate (BER) = 10^{-13} 2. Eye Height at TP3 ≧ 150mVpp 3. Max lane to lane mismatch of insertion loss at TP3: 20*log |max(eye height)/min(eye height)| ≦ 2.3dB 4. Max source pre-emphasis level at level 0 (0dB) ≦ 0.25dB	10^{-13}			

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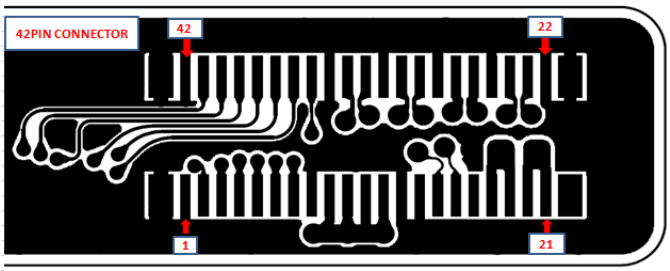
5.4 INPUT TERMINAL PIN ASSIGNMENT

eDP Connector : JAE AA03-P042VA2

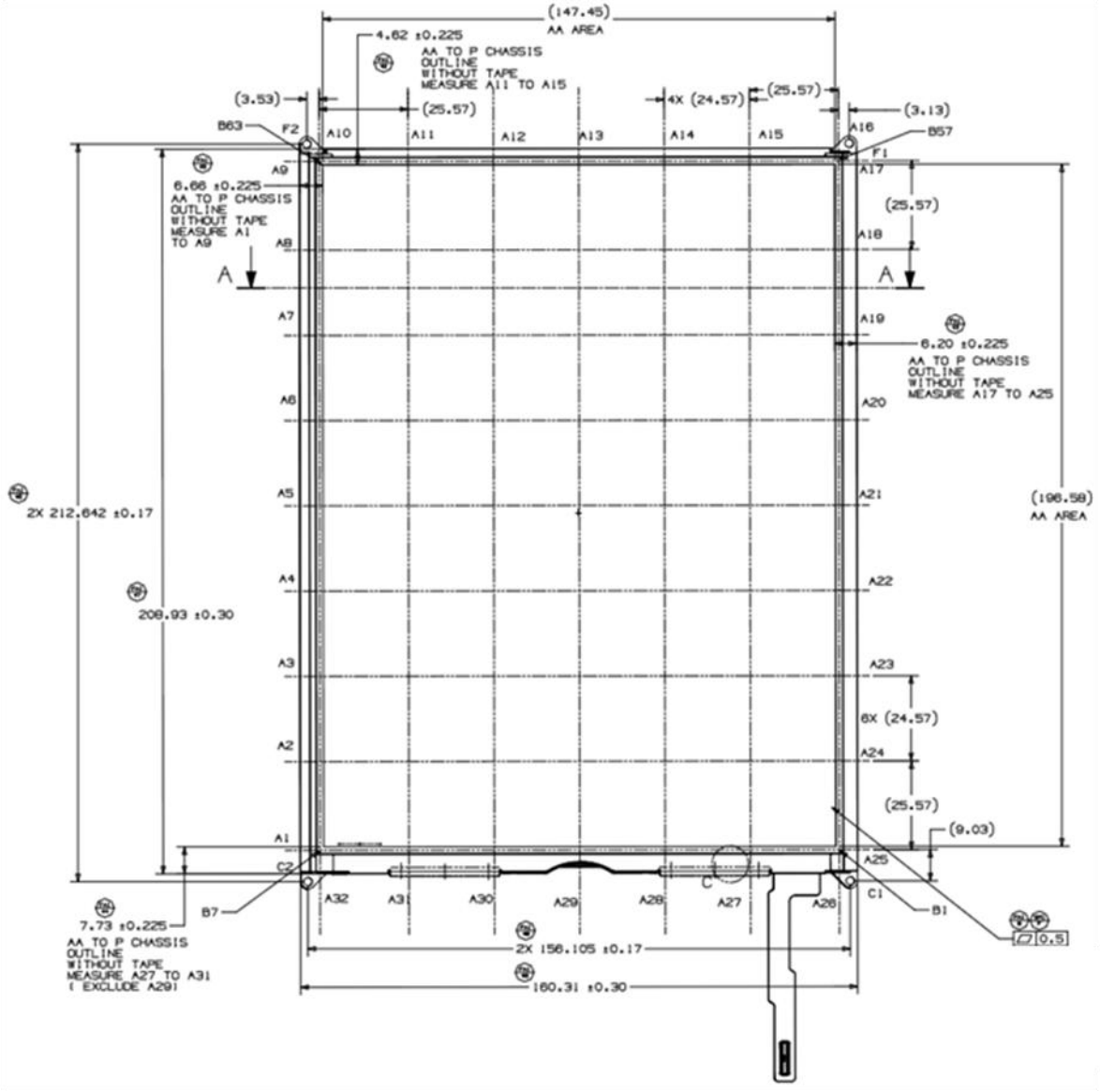
42pin (FLEX SIDE)

	Symbol
1	GND
2	LED Cathode 1B
3	LED Cathode 2B
4	LED Cathode 3B
5	LED Cathode 4B
6	LED Cathode 5B
7	LED Cathode 6B
8	GND
9	LCD_VCC
10	LCD_VCC
11	LCD_VCC
12	LCD_VCC
13	GND
14	GND
15	AUX_N
16	AUX_P
17	NC
18	LED Anode A
19	LED Anode A
20	LED Anode B
21	LED Anode B
22	GND
23	Lane 3 P
24	Lane 3 N
25	GND
26	Lane 2 P
27	Lane 2 N
28	GND
29	Lane 1 P
30	Lane 1N
31	GND
32	Lane 0 P
33	Lane 0 N
34	GND
35	HPD
36	LED Cathode 1A
37	LED Cathode 2A
38	LED Cathode 3A
39	LED Cathode 4A
40	LED Cathode 5A
41	LED Cathode 6A
42	GND

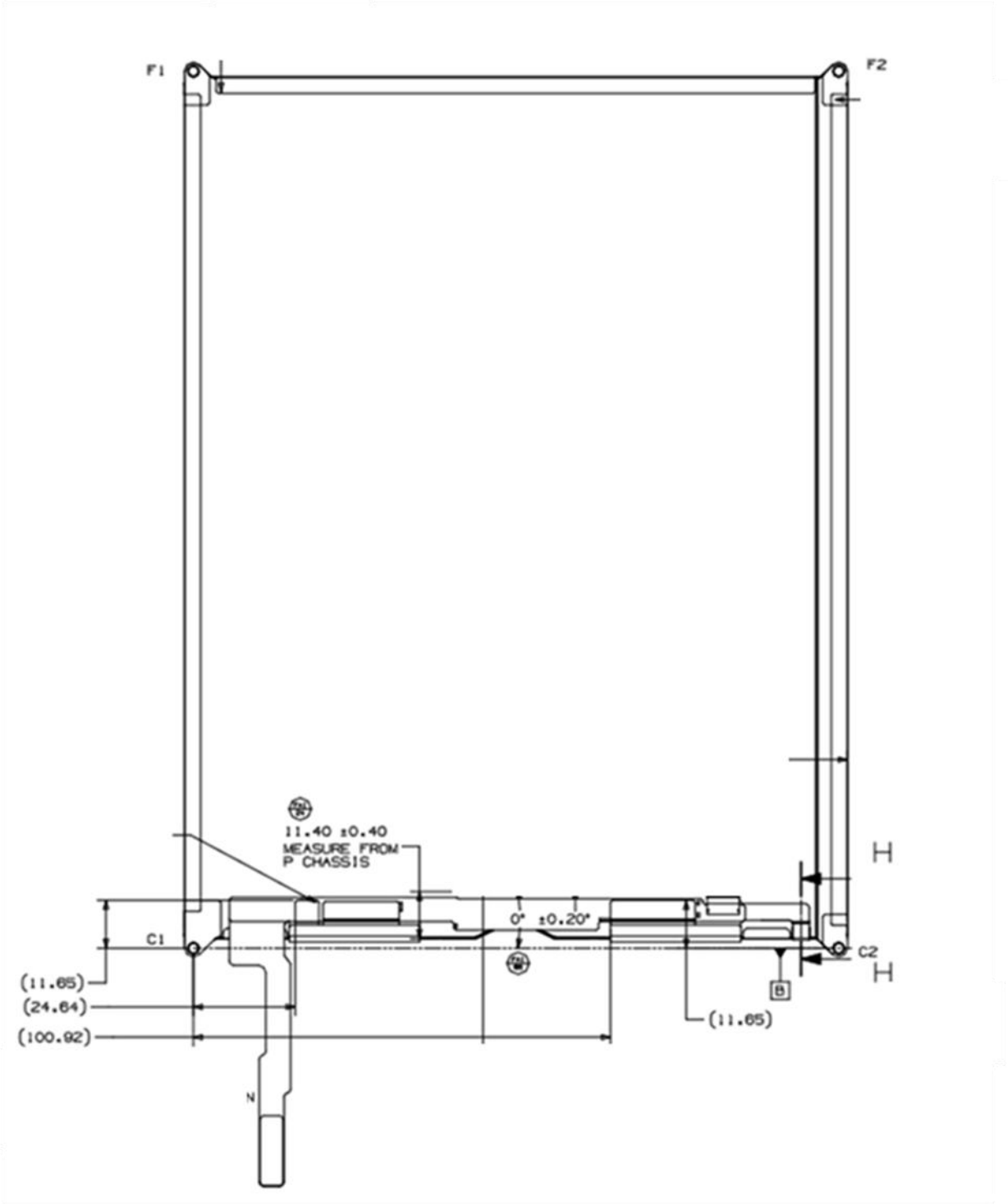


6. OUTLINE DIMENSION

6.1 TOP



6.2 Bottom


F1
F2
11.40 ±0.40
MEASURE FROM
P CHASSIS
0° ±0.20°
C1
C2
H
H
B
(11.65)
(24.64)
(100.92)
(11.65)
N

7. GENERAL PRECAUTIONS

7.1 STORAGE

We highly recommend to comply with the criteria in the table below.

ITEM	Unit	Min.	Max.
Storage Temperature	(℃)	5	40
Storage Humidity	(%rH)	35	75
Storage Life	12 months		
Storage Condition	- The storage room should be equipped with a good ventilation facility, which has a temperature controlling system. - Products should be placed on the pallet, which is away from the wall not on the floor. - Prevent products from being exposed to the direct sunlight, moisture, and water.; Be cautious not to pile the products up. - Avoid storing products in the environment, which other hazardous material is placed. - If products are delivered or kept in the storage facility more than 3 months ,we recommend you to leave products under the condition including a 20℃ temperature and a humidity of 50% for 24 hours. - If you store semi-manufactured products for more than 3 months, bake the products under the condition including the 50℃ temp. and the 10% humidity for 24hrs after being used.		