Date: April. 10th. 2015

Specification for Approval

Customer Name :

Product Name : 4.99" Diamond FHD AMOLED

Model Name : AMS499QP89-0

Description : 4.99" FHD(1080*1920) 16M Color

Proposed by			Customer's Approval
Designed	Checked	Approved	
DG LEE	JS CHAE	MH LEE	

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Also, contents in this document are subject to change after prior notice to the customer.

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Revision History

Date	REV. No.	Contents	Remark
March. 13th. '15	Preliminary	- Preliminary Product Specification (Reference AMS499QP42)	
April. 10th. '15	REV.A	- Initial Issue	

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1. Scope

This Specification defines general provisions as well as inspection standards for AMOLED module supplied by SAMSUNG Display Co., LTD.,
If the event of unforeseen problems or unspecified items occurs, we naturally shall negotiate and agree to solution with customer.

2. Warranty

Basically, warranty term is 12 months of reliability characteristics of quality level after the outgoing date in SAMSUNG Display Co., LTD., and SAMSUNG Display Co., LTD., could compensate for defectives which happens within warranty term under condition that the products should be stored or be used as specified under normal condition within the contents of specification.
Otherwise, it is impossible to compensate for defectives when they happens by customer's mistake such as careless handing or circuit change, etc.
And after 12 months of warranty term, all replacements for defectives will be charged.

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3. Features

1) Display Color : 16M_Color
2) Display Format : 4.99" FHD Diamond : 1080x1920
3) Interface : DSI 4-lane
4) Driver IC : S6E8FA0X01 (SEC)
5) Touch IC : mXT-540S (Atmel)
6) Polarizer : Hard Coating Polarizer

4. Mechanical Specification

Item	Specifications	Unit
Dimensional outline	68.28(W) x 143.26(H) x 1.666(T)	mm
Glass outline	65.2(W) x 118.49(H) x 0.61(T)	mm
Number of dots	540(W) x RG(BG) x 1920(H)	Dots
Active area	62.1(W) X 110.4(H)	mm
Diagonal Inch	4.99	inch
Pixel pitch	57.5(W) X 57.5(H)	um
Glass Thickness	0.31 (LTPS) 0.3 (Encap)	mm

5. Maximum Rating

Item		Symbol	Min.	Max.	Unit	Note
Supply voltage (Display)	Driver	VCI	-0.3	5.0	V	(1),(2)
		IOVDD	-0.3	5.0	V	(1),(2)
		VLIN	−0.3	8.8	V	(1),(2)
	DCDC	VBAT		5.5	V	(3)
		ELVDD		5.5	V	(1),(2),(3)
		ELVSS	-6.5		V	(1),(2),(3)
Supply voltage (TSP)	Logic	TSP_VDD		3.6	V	(1),(2)
	Logic	TSP_VDDIO		3.46	V	(1),(2)
	Power	TSP_AVDD		3.6	V	(1),(2)
Operating temperature		Top	-20	60	℃	-
Storage temperature		Tstg	-30	70	℃	-
Humidity		Hstg	10	90	%RH	

Note 1) Supply voltage should satisfy the below condition of
VCI, IOVDD, TSP_AVDD, TSP_VDDIO and TSP_VDD > VSS (GND).

Note 2) If the supplied voltage exceeds the maximum limitation, LSI can be damaged permanently.
Therefore, while operating, it is recommend to use LSI within the maximum electrical limitation.
If not, LSI can cause decreased reliability or operational problems.

Note 3) VBAT is input supply to DCDC IC which is mounted on SET board.
And ELVDD and ELVSS, which are supply voltage for display, are output power from DCDC IC.

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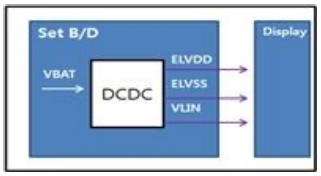
6. Electrical Characteristics

-. Test Conditions: IOVDD=1.8V, VCI=3.0V, VSS=0V, VBAT=3.8V
Temp=25℃ unless otherwise specified.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Supply voltage (Display)	Logic Voltage	IOVDD	-	1.65	1.8	3.3	V	
	Analog Voltage	VCI	-	2.9	3.0	4.8		
	Battery Supply	VBAT	-	3.42	3.8	4.18		1),2)
	Analog Voltage	VLIN	–	–	7.7	–		
Supply voltage (TSP)	Logic Voltage	TSP_VDD	-	2.7	3.0	3.3	V	
	Analog Voltage	TSP_AVDD		2.7	3.3	3.6	V	
	Interface Voltage	TSP_VDDIO		1.71	1.8	1.89	V	
Logic Input Voltage (Display)	"H" level	VIH	-	0.7*VDD3	-	VDD3	V	
	"L" level	VIL	-	0.0	-	0.3*VDD3		
Logic Output Voltage (Display)	"H" level	VOH	IOH = -1mA IOL = 1mA	0.8*VDD3	-	VDD3	V	
	"L" level	VOL		0.0	-	0.2*VDD3		
Logic Input Voltage (TSP)	"H" level	VIH	-	0.7*TSP_VDDIO	-	TSP_VDDIO+0.3	V	
	"L" level	VIL	-	-0.3	-	0.3*TSP_VDDIO		
Logic Output Voltage (TSP)	"H" level	VOH	IOL,IOH = 2.7mA	0.7*TSP_VDDIO	-	–	V	
	"L" level	VOL		–	-	0.3*TSP_VDDIO		
Logic leakage Current	"H" level	IIH	VI=VDDIO, TSP_VDDIO or VSS	–	-	10.0	uA	
	"L" level	IIL		-10.0	-	–	uA	
Current Consumption (Display)	Sleep out mode Display mode	ICI	Frame frequency=60Hz, white pattern	-	2.69	10	mA	
		IVDDIO		-	26.5	70	mA	
		IBAT		-	342	411	mA	1),2)
	Sleep in mode	ICI	sleep mode	-	-	100	uA	
Current Consumption (TSP)	Active average	IAVDD	100Hz 1 touch	–	5.08	–	mA	
		IVDD		–	5.09	–	mA	
	Idle average	IAVDD	16Hz No touch	–	0.57	–	mA	
		IVDD		–	0.78	–	mA	
Frame Frequency		f_{FRM}	-	–	(60)	–	Hz	

Note 1) VBAT is input supply to DCDC IC mounted on SET board.
Note 2) IBAT is measured at DCDC input, VBAT.



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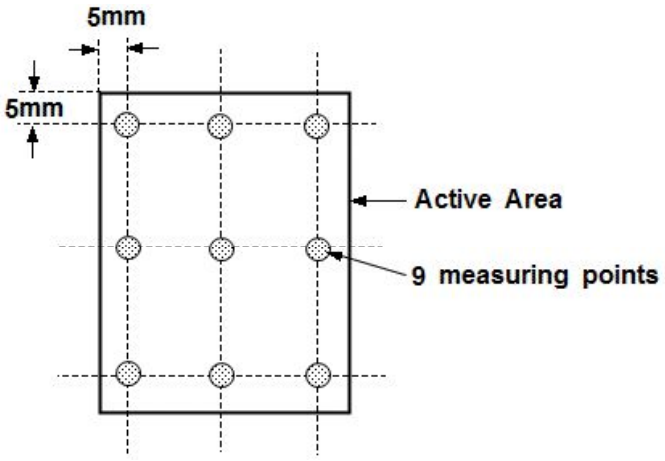
7. Electro-optical characteristics

Item		Symbol	Temp	Condition	Min.	Typ.	Max.	Unit	Note
Brightness (CTF)			25℃	Normal (White Mode)	240	300	360	cd/m^2	Center brightness
Uniformity			25℃	Normal (White Mode)	75	-	-	%	(1)
Contrast ratio		K	25℃	Φ=0°,θ=0°	3,400	-	-	-	(1),(2)
Color of CIE coordinate	White	x	25℃	Φ=0° θ=0°	0.282	0.302	0.322	-	(1),(2),(3)
		y			0.301	0.322	0.341	-	
	Red	x			0.635	0.665	0.695	-	
		y			0.304	0.334	0.364	-	
	Green	x			0.200	0.250	0.300	-	
		y			0.661	0.711	0.761	-	
	Blue	x			0.099	0.139	0.179	-	
		y			0.010	0.050	0.090	-	
Color Gamut			25℃	vs. NTSC	85	(100)	-	%	CIE1931
Viewing angle			25℃	Up/Down/Right/Left CR ratio ≥10	88	-	-	°	
Cross Talk			25℃	window: 4% white/black background: gray117	-	-	3	%	(4)
Gamma			25℃	Log(Lv-Lb)=Ylog(V)+log(a) V(Gray)= 48,72,104,132, 164,192,224,252,255 Lum(gray255)=300nit	1.9	2.2	2.5	-	

Based on the above optical spec is only 300nit(brightness)

Note 1) Uniformity Measuring Point



Uniformity = Lmin / Lmax * 100 [%]

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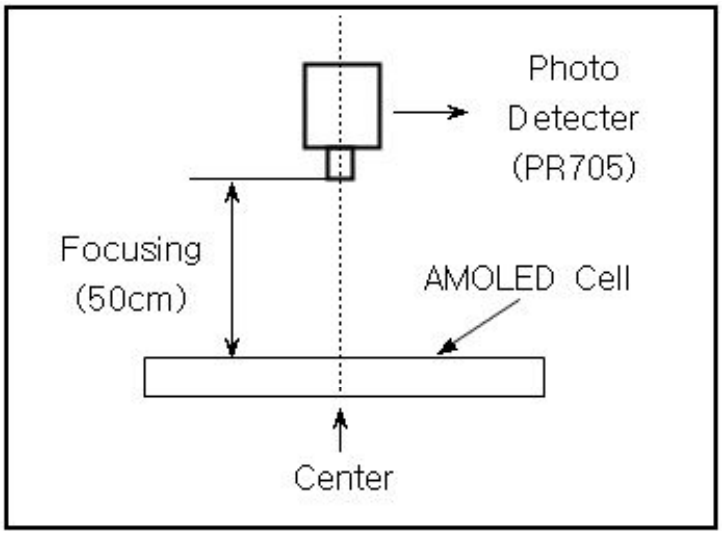
Note 2) Definition of contrast ratio (K)

$$\text{Contrast Ratio(K)} = \frac{\text{Brightness of selected dot (White patterned area) at 300cd/m}^2}{\text{Brightness of non-selected dot (Black patterned area) at 300cd/m}^2}$$

Note 3) Optical measuring system
temperature regulated chamber



Note 4) Cross Talk

a. measure luminance at the position, P_0.

b. calculate cross talk as below equation.

$$L_{W_OFF} = \frac{L_{W1} + L_{W2} + L_{W3} + L_{W4}}{4}$$

$$L_{B_OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

$$crosstlak = \frac{\left|L_{Wi_ON} - L_{W_OFF}\right|}{L_{W_OFF}} \times 100\% \quad (i = 5 \text{ to } 8)$$

$$crosstlak = \frac{\left|L_{Bi_ON} - L_{B_OFF}\right|}{L_{B_OFF}} \times 100\% \quad (i = 5 \text{ to } 8)$$

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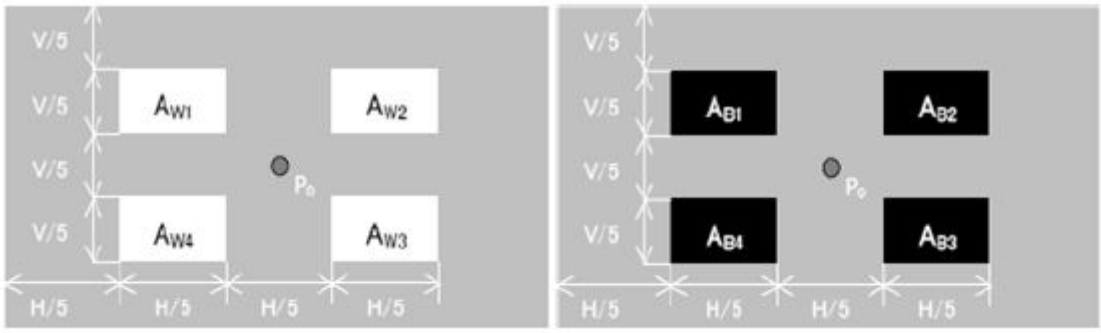
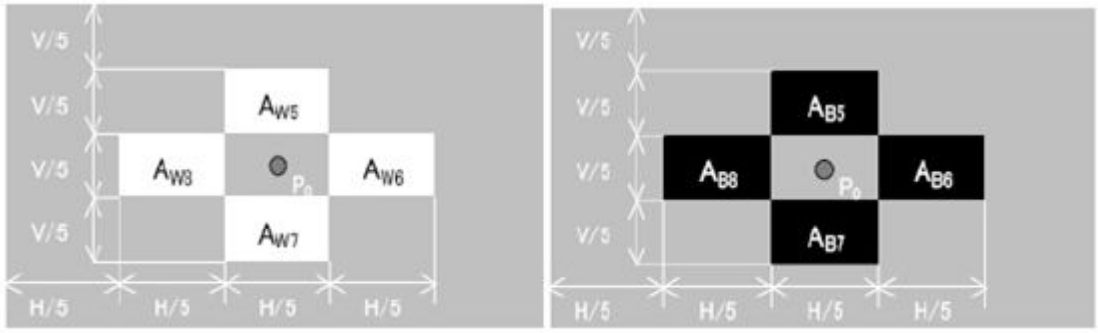


(a) L_{W_OFF}, L_{B_OFF} measuring pattern



(b) L_{W_ON}, L_{B_ON} measuring pattern

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8. I/O Connection & Block Diagram

8-1. I/O Connection

No.	Name	I/O	Description
1	TSP_AVDD_3.3V	Power	Analog voltage for touch circuits
2	GND	Ground	Ground
3	TSP_VDD_3.0V	Power	Logic voltage for touch circuits
4	D3N	I/O	Fourth differential data input/output pin
5	TSP_SDA	I	Touch I2C data
6	D3P	I/O	Fourth differential data input/output pin
7	TSP_VDDIO_3.3V	Power	Host Interface voltage for touch circuit
8	GND	Ground	Ground
9	TSP_SCL	I	Touch I2C clock
10	D0N	I	First differential data input/output pin
11	TSP_CHRG_IN	I/O	Touch charger present input
12	D0P	I/O	First differential data input/output pin
13	TSP_CHG_BAR	I	Touch State change interrupt
14	GND	Ground	Ground
15	GND	Ground	Ground
16	CKN	I	Differential clock input
17	VDDP_EN	O	Enable for VLIN of DCDC Converter
18	CKP	I	Differential clock input
19	EL_ON	O	Enable for ELVDD & ELVSS of DCDC Converter
20	GND	Ground	Ground
21	IOVDD_1.8V	Power	Power supply for display logic circuits
22	D1N	I/O	Second differential data input/output pin
23	VLIN_7.7V	Power	Power supply for display analog circuits
24	D1P	I/O	Second differential data input/output pin
25	VCI_3.0V	Power	Power supply for display analog circuits
26	GND	Ground	Ground
27	ERR_FG	O	Active high, MIPI Error monitoring pin. Not use Open
28	D2N	I/O	Third differential data input/output pin
29	RESET	I	Display reset. Active low.
30	D2P	I/O	Third differential data input/output pin
31	MTPHV	Power	Power supply for MTP Programming or Erase Open or connected to GND
32	GND	Ground	Ground
33	ELVDD_FBS	O	ELVDD Feedback, ELVDD sense input in DCDC
34	NC	-	No Connect
35	ELVDD	Power	Positive power supply for EL
36	ELVSS	Power	Negative power supply for EL

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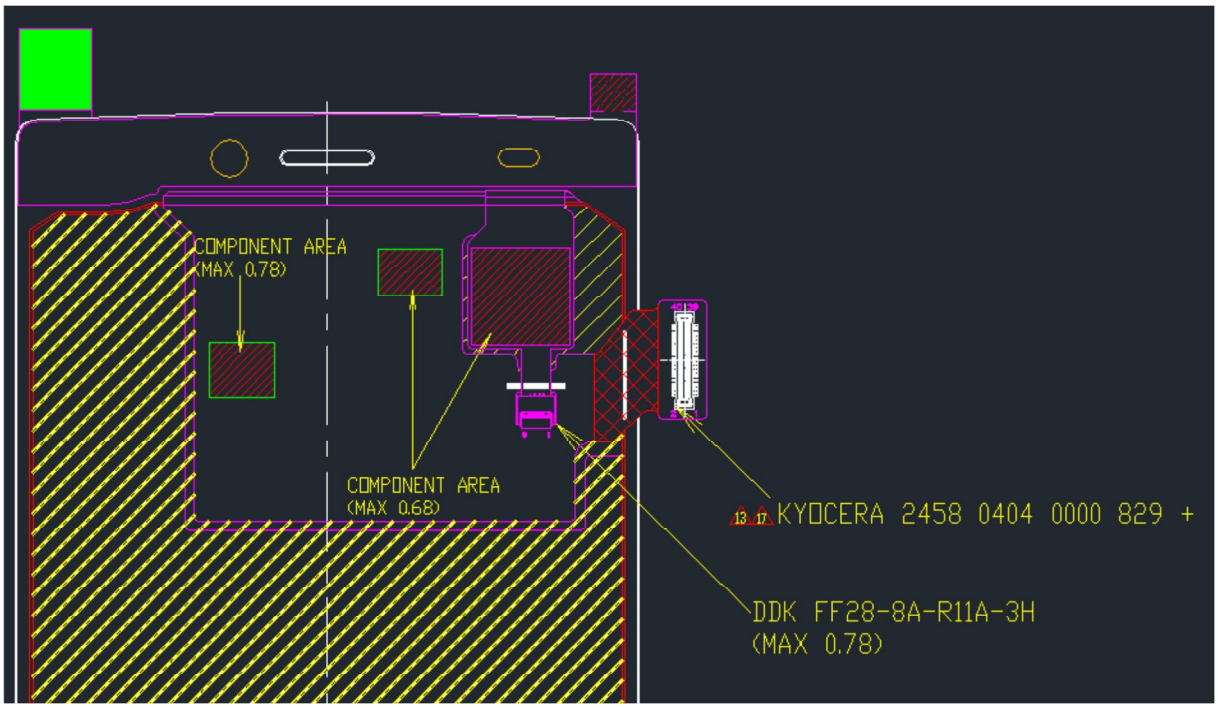
No.	Name	I/O	Description
37	ELVDD	Power	Positive power supply for EL
38	ELVSS	Power	Negative power supply for EL
39	ELVDD	Power	Positive power supply for EL
40	ELVSS	Power	Negative power supply for EL

<Pin layout of B-to-B contact pads>



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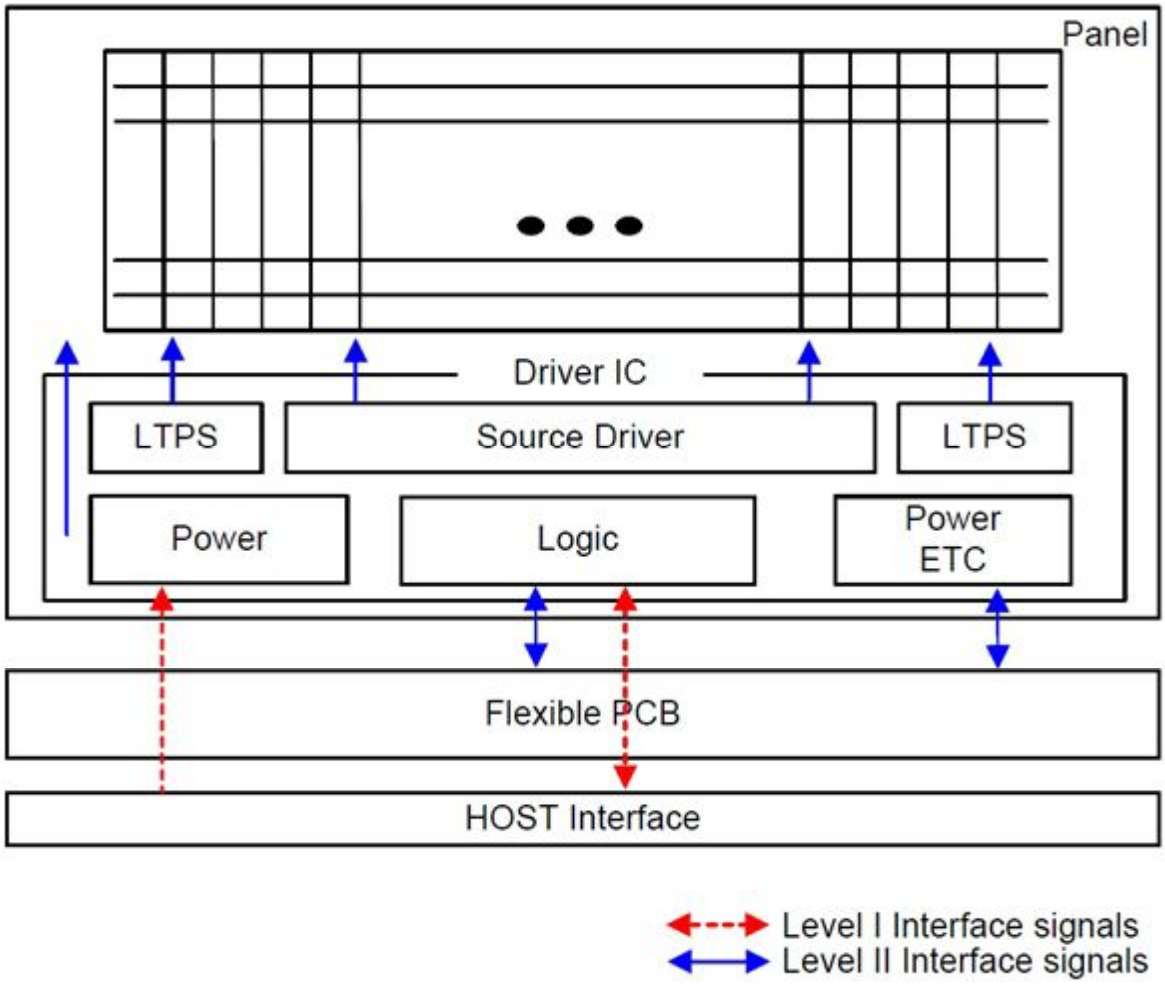
8-2. Circuit block diagram (Display)



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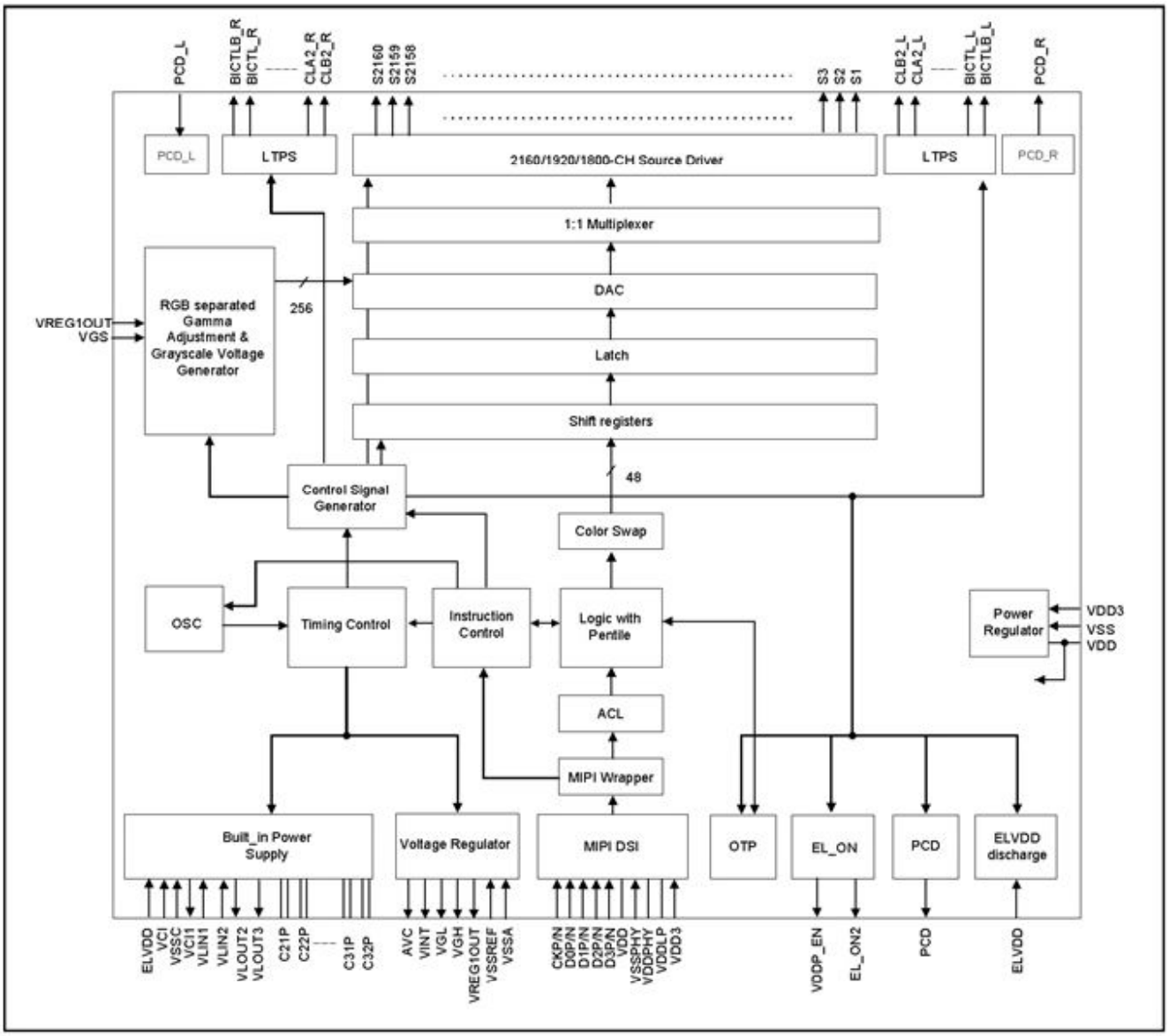
8-3. Circuit block diagram (Driver IC for display)



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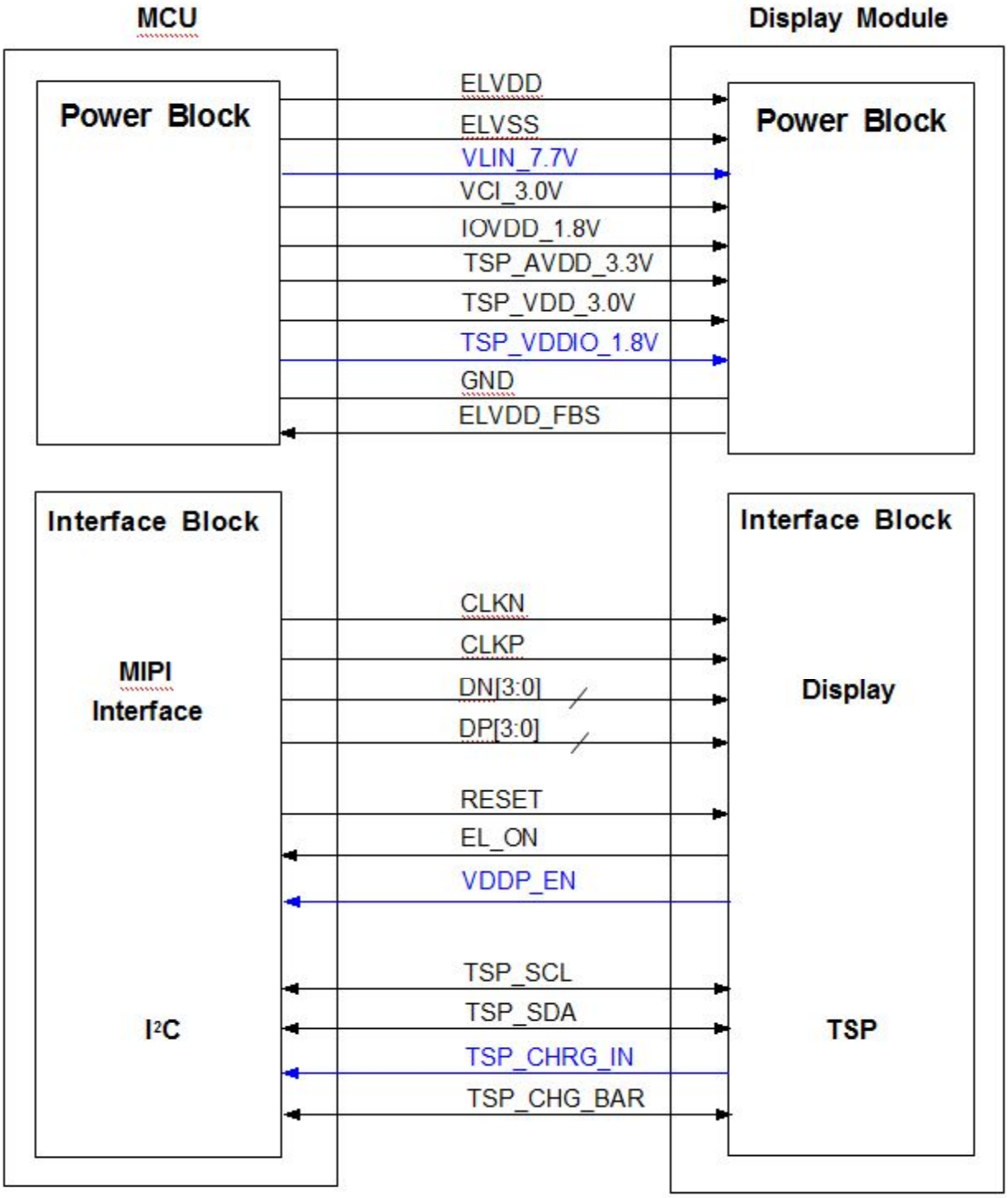
8-4. MCU and Display Module Interface Configuration



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9. Recommended Operating Sequence

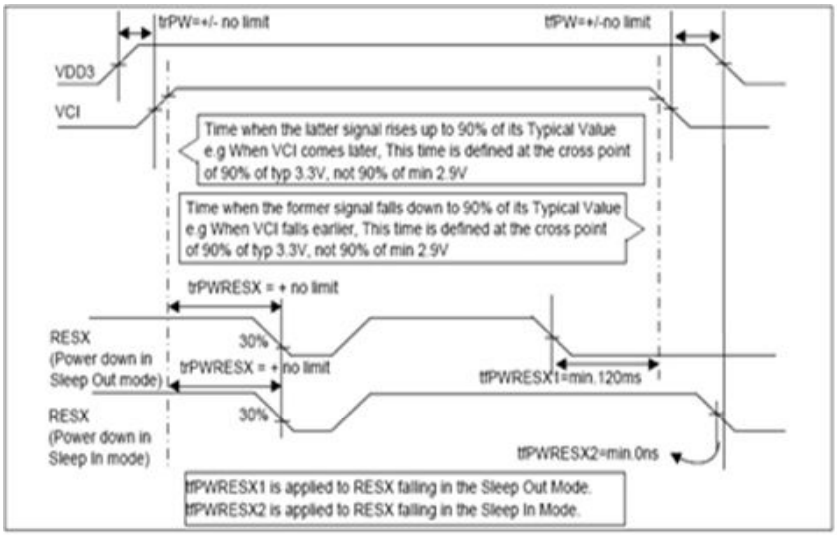
9-1. Power ON/Off, Sleep in/Out, HBM & Dimming mode

1) Power On Sequence

Order	Instruction		DATA	Remarks
1	Power Input	VBAT, VDDI, VCI on		Note1
2		wait	>10ms	
3	Data, CLK	LP00 → LP10 → LP11		Note2
4	Wait before HW reset	wait	>25ms	
5	Reset	RESX = "L"		Note1
6		wait	>10us	
7		RESX = "H"		
8		wait	>10ms	
9	Sync packet start (HS)			
10		wait	>16.7ms (1frame)	
11	Sleep Out	CMD	0x011h	
12	Wait before sending command	wait	>120ms	
13	wait for booster to be stable	wait	>100ms	
14	Frame (RGB Data)		before 1frame	
15	Display On	CMD	0x029h	

[Note1 : System Power On/Off]

Case1 - RESX Line Held High by Host at Power ON



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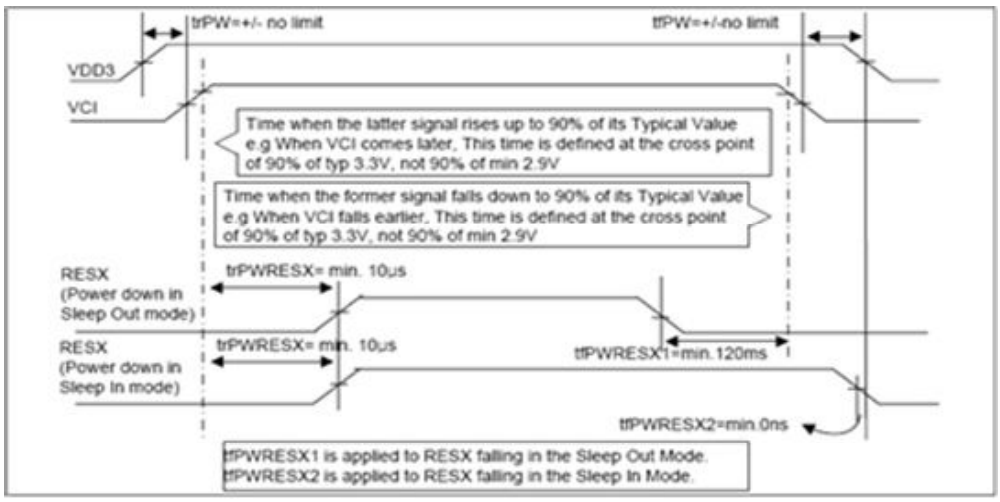
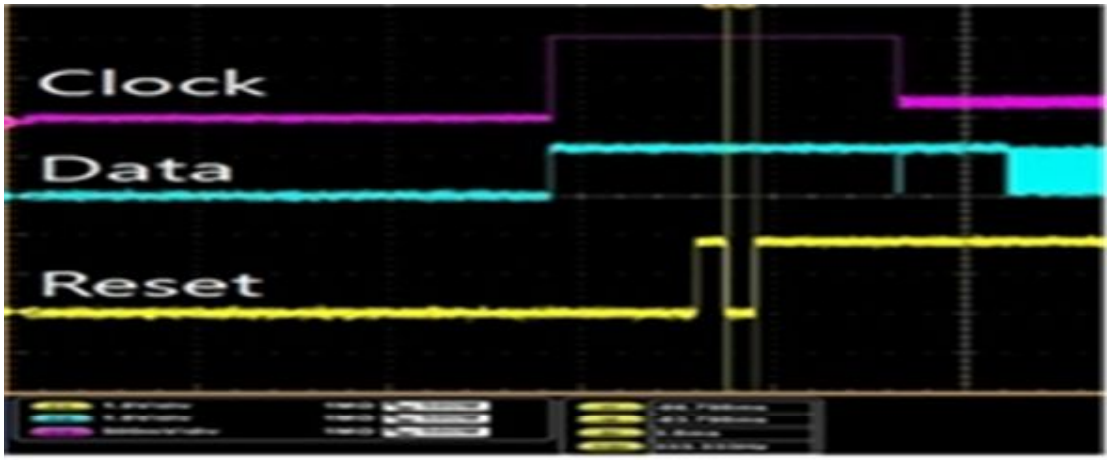
Case2 - RESX Line Held Low by Host at Power ON



[Note2 : LP Status] When it is writing Reset, Hold LP11



2) Power Off Sequence

Order	Instruction		DATA	Remarks
1	Display Off	CMD	0x028	
2		wait	>33.4ms (2frame)	
3	Sleep In	CMD	0x010	
4		wait	>120ms	
4	Sync packet stop (HS)			
5	Power Off	VCI, VDDI, VBAT off		

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3) Sleep In Sequence

Order	Instruction		DATA	Remarks
1	Display Off	CMD	0x028	
2		wait	>33.4ms (2frame)	
3	Sleep In	CMD	0x010	
4		wait	>120ms	
5	Sync packet stop (HS)			

4) Sleep Out Sequence

Order	Instruction		DATA	Remarks
1	Sync packet start (HS)			
2		wait	>16.7ms (1frame)	
3	Sleep Out	CMD	0x011h	
4	Wait before sending command	wait	>120ms	
5	wait for booster to be stable	wait	>100ms	
6	Frame (RGB Data)		before 1frame	
7	Display On	CMD	0x029h	

5) HBM Mode

Order	Instruction		DATA	Remarks
1	WRCTRLD	CMD	53H	
2		Parameter	0x28	No use HBM
			0x68	Medium brightness
			0Xe8	Max brightness

6) ACL Set

Order	Instruction		DATA	Remarks
1	WRCTRLD	CMD	55H	
2		Parameter	0x00	ACL Off
			0x01	ACL 33%
			0x02	ACL 40%
			0x03	ACL 50%

7) Dimming Mode

Case1) Brightness is Over 60nit

Order	Instruction		DATA	Remarks
1	WRCTRLD	CMD	51H	
2		parameter	0xXXh	

Ex) ffh = 255/255 * 300 = 300nit, d9h=217/255 * 300 = 255nit, 5eh=94/255 * 300 = 110nit
34h= 34/255 * 300 = 61nit

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Case2) Brightness is under 60nit ~ 32nit

WRDISBV=33h~1Bh					
Order	Instruction		DATA	previous	Remarks
1		CMD	0xF0		LEVEL 2 key Command unlock(F0h)
2		P1	0x5A		
3		P2	0x5A		
4		CMD	0xB0		Global parameter (B0h)
5		P1	0x21		
6		CMD	0xC9		Write Gamma value (C9h)
7		P1	0xXX		
8		P2	0xXX		
9		P3	0xXX		
10		P4	0xXX		
11		P5	0xXX		
12		P6	0xXX		
13		P7	0xXX		
14		P8	0xXX		
15		P9	0xXX		
16		P10	0xXX		
17		P11	0xXX		
18		P12	0xXX		
19		P13	0xXX		
20		P14	0xXX		
21		P15	0xXX		
22		P16	0xXX		
23		P17	0xXX		
24		P18	0xXX		
25		P19	0xXX		
26		P20	0xXX		
27		P21	0xXX		
28		P22	0xXX		
29		P23	0xXX		
30		P24	0xXX		
31		P25	0xXX		
32		P26	0xXX		
33		P27	0xXX		
34		P28	0xXX		
35		P29	0xXX		
36		P30	0xXX		
37		P31	0xXX		
38		P32	0xXX		
39		P33	0xXX		
40		CMD	0xF7		LTPS Timming/Gamma Update (F7h)
41		P1	0x03		
42		CMD	0xF0		LEVEL 2 key lock
43		P1	0xA5		
44		P2	0XA5		
45		wait	>10ms		
46	WRDISBV	CMD	51h		
		Parameter	0x33h~1Bh		

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Ex) 33h=51/255 *300=60nit ~ 1Bh=27/255 * 300 = 32nit

if Case is WRDISBV = 33h~1Bh(60nit ~ 32nit)

1) Level 2 Command unlock

ex) F0h → 5A, 5A (Level 2 Command unlock)

2) Read Level 3 Gamma Data (C9h 67th~99th)

3) Update Gamma Value for Level3 at Level5 Gamma value para

ex) B0h → 21h

C9h → P1~P33 **(the Value of Level 3 Gamma Data)**

4) Gamma Update

ex) F7h → 03h

5) Level 2 Command lock

ex) F0h → A5, A5 (Level 2 Command lock)

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Case3) Brightness is under 31nit ~ 0nit

(5) WRDISBV= 1Ah~00h					
Order	**Instruction**		**DATA**	**previous**	**Remarks**
1		CMD	0xF0		LEVEL 2 key Command unlock (F0h)
2		P1	0x5A		
3		P2	0x5A		
4		CMD	0xB0		Global parameter (B0h)
5		P1	0x21		
6		CMD	0xC9		Write Gamma value (C9h)
7		P1	0xXX		
8		P2	0xXX		
9		P3	0xXX		
10		P4	0xXX		
11		P5	0xXX		
12		P6	0xXX		
13		P7	0xXX		
14		P8	0xXX		
15		P9	0xXX		
16		P10	0xXX		
17		P11	0xXX		
18		P12	0xXX		
19		P13	0xXX		
20		P14	0xXX		
21		P15	0xXX		
22		P16	0xXX		
23		P17	0xXX		
24		P18	0xXX		
25		P19	0xXX		
26		P20	0xXX		
27		P21	0xXX		
28		P22	0xXX		
29		P23	0xXX		
30		P24	0xXX		
31		P25	0xXX		
32		P26	0xXX		
33		P27	0xXX		
34		P28	0xXX		
35		P29	0xXX		
36		P30	0xXX		
37		P31	0xXX		
38		P32	0xXX		
39		P33	0xXX		
40		CMD	0xF7		LTPS Timming/Gamma Update (F7h)
41		P1	0x03		
42		CMD	0xF0		LEVEL 2 key unlock
43		P1	0xA5		
44		P2	0XA5		
45		wait	>10ms		
46	WRDISBV	**CMD**	**51h**		
			0x1Ah~00h		

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if Case is WRDISBV = 1Ah~00h(31nit ~ 0nit)

1) Level 2 Command unlock

ex) F0h → 5A, 5A (Level 2 Command unlock)

2) Read Level 1 Gamma Data (C9h 100th~132th)

3) Update Gamma Value for Level1 at Level5 Gamma value para

ex) B0h → 21h

C9h → P1~P33 (the Value of Level 1 Gamma Data)

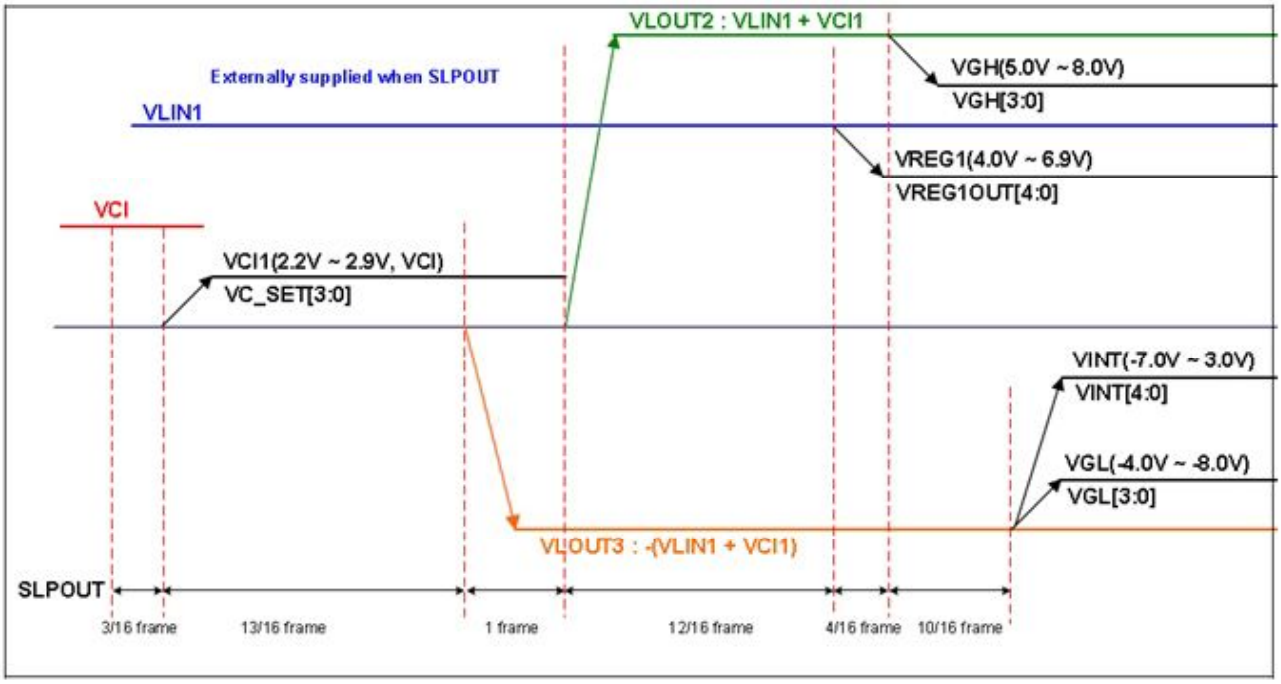
4) Gamma Update

ex) F7h → 03h

5) Level 2 Command lock

ex) F0h → A5, A5 (Level 2 Command lock)

9-2. Internal Power Supply Pattern Diagram



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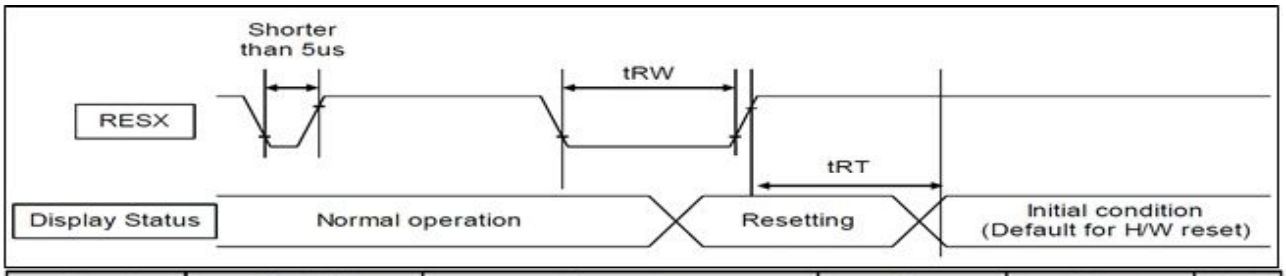
10. AC characteristics

10-1. Reset Timing



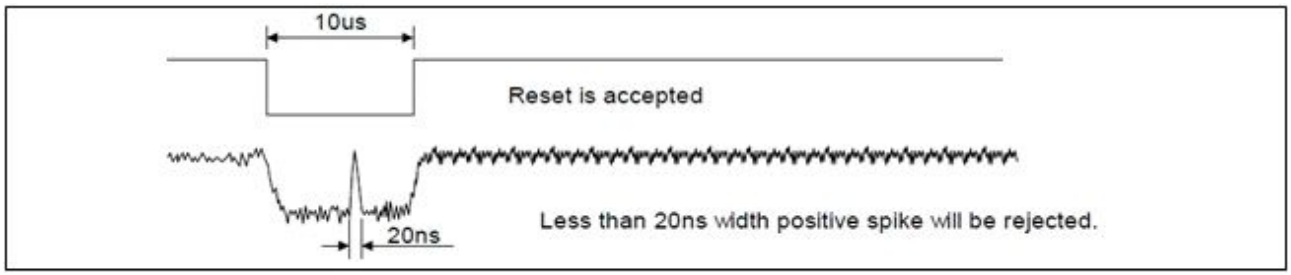
Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	tRW	Reset pulse duration	10	–	μs
	tRT	Reset cancel	–	5(5)	ms
			–	120(6, 7)	

NOTE:

1. The reset cancel includes also required time for loading ID bytes (or similar) from EEPROM (or similar) to ID (or similar) registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table below

RESX Pulse	Action
Shorter than 5us	Reset rejected
Longer than 10μs	Reset
Between 5μs and 9μs	Reset starts

3. During the Resetting period, the display will be blanked (The display enters blanking sequence, in which maximum time is 120ms, when Reset Starts in Sleep Outmode. The display remains in the blank state at Sleep-In mode) and then return to default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset is applied during sleep In Mode.
6. When Reset is applied during Sleep out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also sleep out command cannot be sent out for 120msec.
8. HW reset cannot cause any spike/glitch on control or data lines or spike/glitch/noise on power (VCI and VDD3) lines.
9. The display module can also initialize and calibrate DSI-CLK± DSI-D0± and DSI-D1± lanes within 5ms if it is needed when DSI has been selected to use.

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11. MIPI characteristics

11-1. DC Characteristics

Items		Parameter	Min.	Nom.	Max.	Unit	Note
LP_TX	Thevenin output high level	VOH	1.1	1.2	1.3	V	
	Thevenin output low level	VOL	-50		50	mV	
	Output impedance of LP transmitter	ZOLP	110			Ω	(1)
HS_RX	Common-mode voltage HS receive mode	VCMRX (DC)	70		330	mV	(2, 3)
	Differential input high threshold	VIDTH			70		
	Differential input low threshold	VIDTL	-70				
	Single-ended input high voltage	VIHHS			460		(2)
	Single-ended input low voltage	VILHS	-40				
	Single-ended threshold for HS termination enable	VTERM-EN			450		
	Differential input impedance	ZID	80	100	125	Ω	
LP_RX	Logic1 input voltage	VIH	880			mV	
	Logic0 input voltage, not in ULP State	VIL			550		
	Input hysteresis	VHYST	25				(4)
LP_CD	Logic1 contention threshold	VIHCD	450				
	Logic0 contention threshold	VIOLED			200		

NOTE:

1. Even though a maximum value for ZOLP is not specified, the output impedance of the LP transmitter ensures that the TRLP/TFLP specification is met
2. Excluding additional RF interference of 100mV peak sine wave beyond 450MHz.
3. This *table* value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz
4. Temperature condition = 25°C

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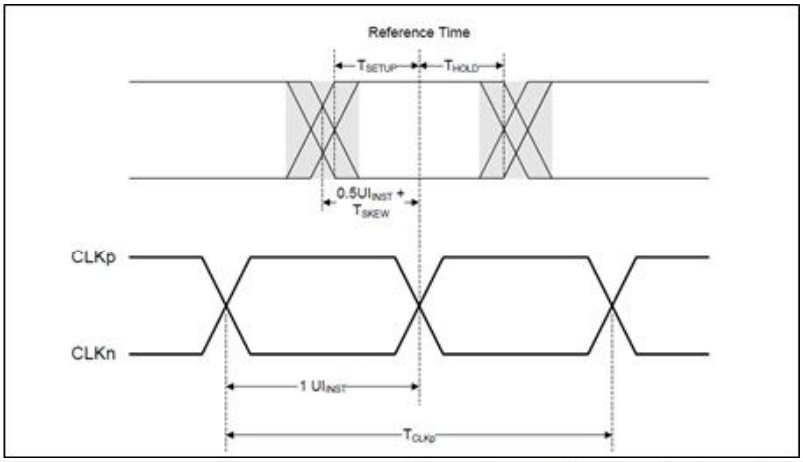
11-2. High Speed Data-clock Timing

Host sends a differential clock signal to the S6E8AA0 to be used for data sampling. This signal is a DDR (Half-rate) clock and has one transition per data bit time. The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure below.



Clock Parameter	Symbol	# of d-lane	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UIINST	4	2		12.5	ns	(1, 2)

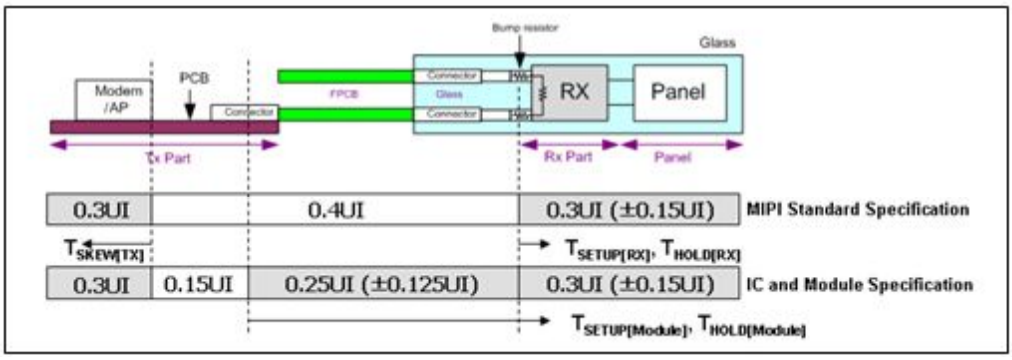
NOTE:

1. This value corresponds to a minimum 80Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to clock skew (Measured at transmitter)	TSKEW[TX]	-0.15		0.15	UIINST	(1)
Data to clock setup time (Receiver)	TSETUP[RX]	0.15			UIINST	(2)
Clock to data hold time (Receiver)	THOLD[RX]	0.15			UIINST	(2)

NOTE:

1. Total silicon and package delay budget of 0.3 × UIINST
2. Total setup and hold window for receiver of 0.3 × UIINST
3. TSETUP[RX] and THOLD[RX] are only for RX without FPCB and connector and guaranteed by design. For module test, TSETUP[Module] and THOLD[Module] specification including FPCB and connector is 0.275UIINST. Refer to Figure below.



MIPI data-clock timing specifications on Module

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12. Interface

12-1. Feature

□ 2/4 data lanes

□ HS (High speed) transmission (Unidirectional)

□ LP (Low power) transmission (Bidirectional)

□ Both video and command modes are supported

□ Diagnostic function-checksum and ECC error monitoring

□ Functionality supported by Escape mode

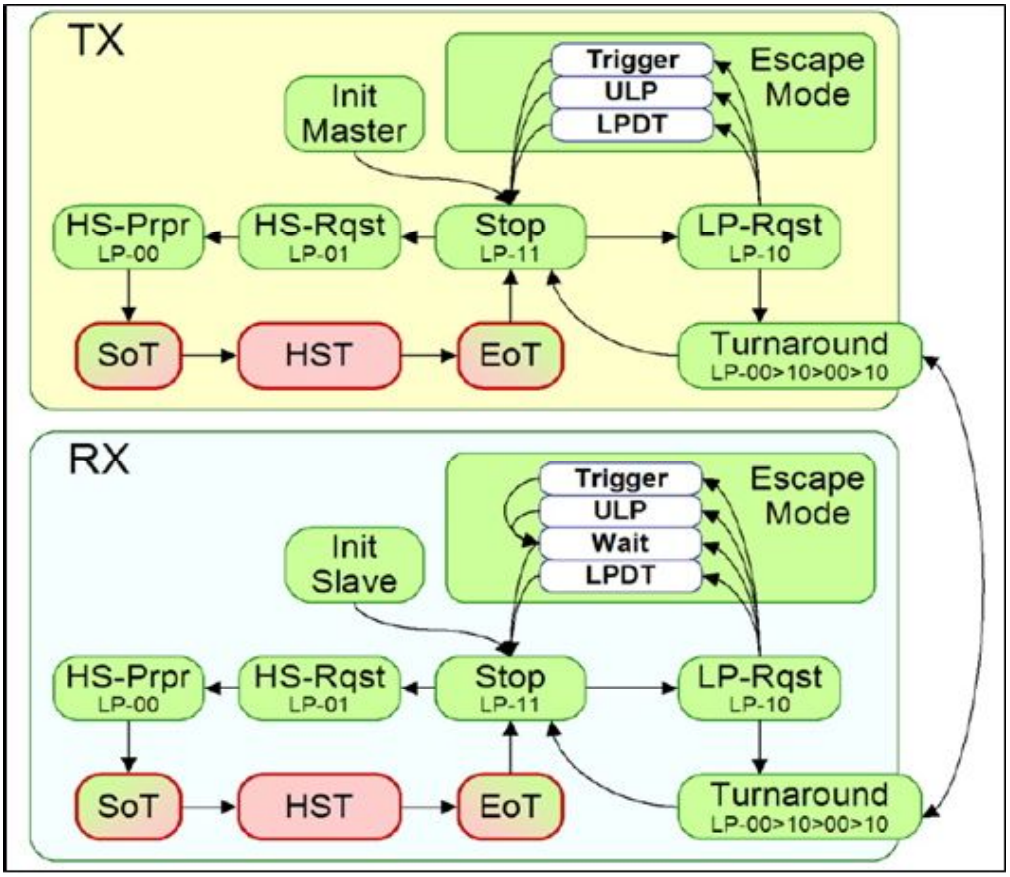
□ Clock lane supports ULPS

□ Packet-based protocol

12-2 MIPI D-PHY

12-2-1. Global Operation

Figure below shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround and Initialization



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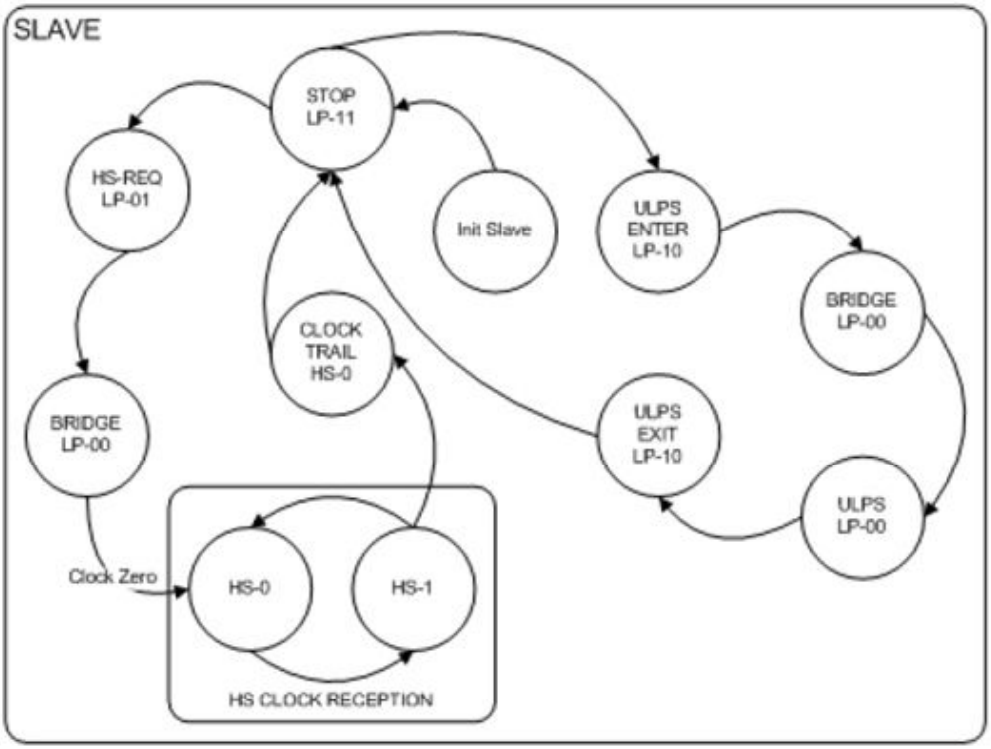
12-2-2. Lane state

State Code	Line Voltage Levels		High-speed	Low-power	
	DP-line	DN-line	Burst Mode	Control Mode	Escape Mode
HS-0	HS low	HS high	Differential-0	N/A	N/A
HS-1	HS high	HS low	Differential-1	N/A	N/A
LP-00	LP low	LP low	N/A	Bridge	Space
LP-01	LP low	LP high	N/A	HS-Rqst	Mark-0
LP-10	LP high	LP low	N/A	LP-Rqst	Mark-1
LP-11	LP high	LP high	N/A	Stop	N/A

12-2-3. Clock Lane Flow Diagram



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12-2-4. High Speed Data Transmission

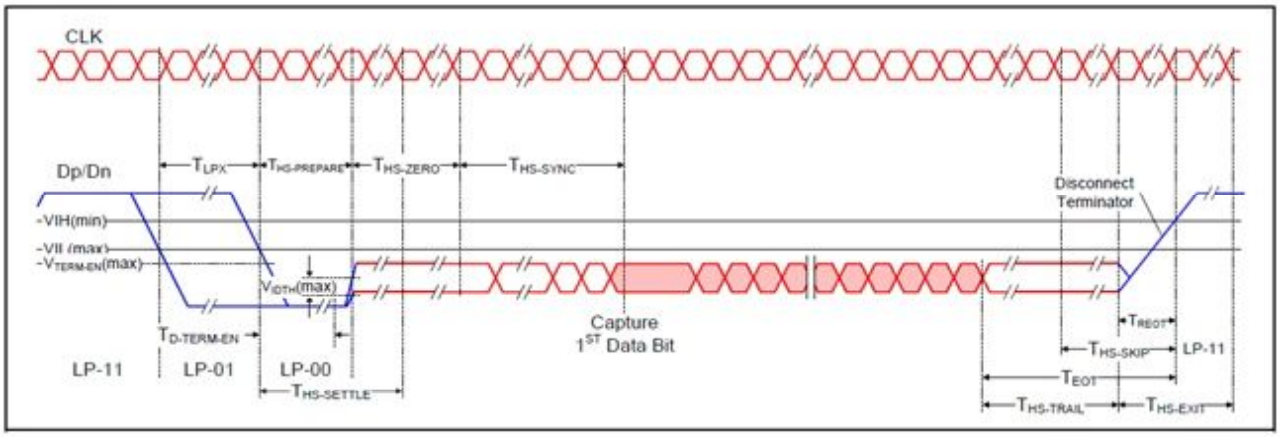
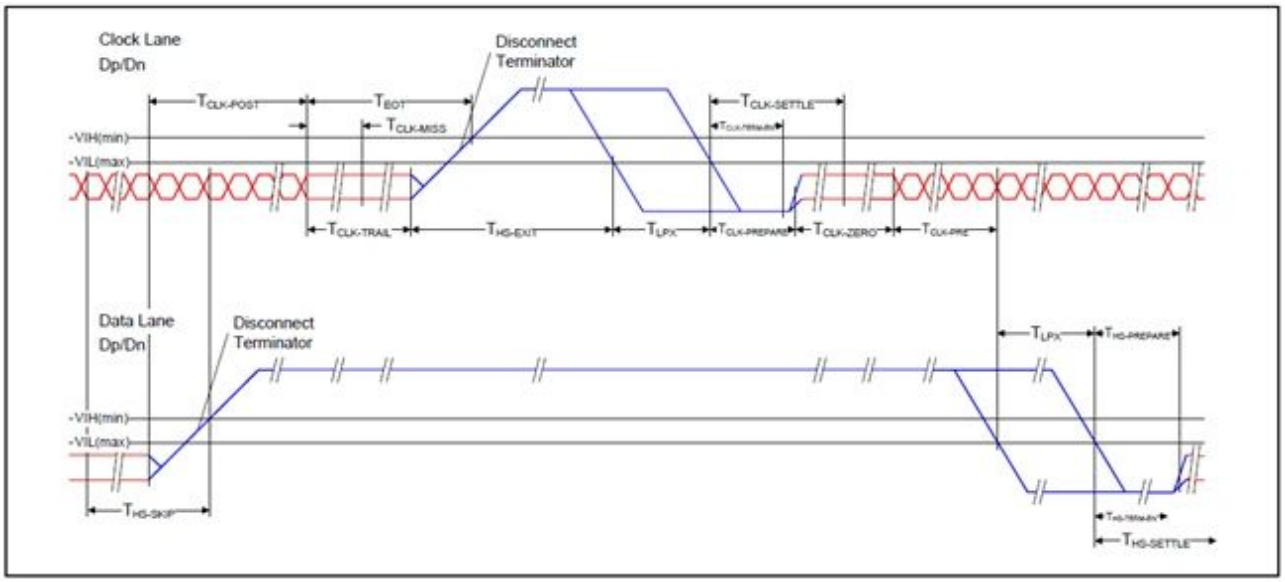


Figure shows the sequence of the high speed data transmission including SoT data.

12-2-5. High Speed Clock Transmission



This Figure shows the sequence of the high speed clock transmission. In high speed mode the clock lane provides a low-swing differential DDR clock signal from Master to Slave for high speed data transmission.

12-2-6. Escape Mode

Escape Mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Though Escape Mode operation is optional in D-PHY, the host processor and peripheral in which Command Mode operation is supported shall implement reverse-direction Escape Mode as well as forward direction Escape Mode.

A Data Lane shall enter Escape Mode via an Escape Mode Entry procedure (LP-11,LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape Mode in Space state (LP-00). If an LP-10 is detected after the first Bridge state or an LP-11 is detected at any time

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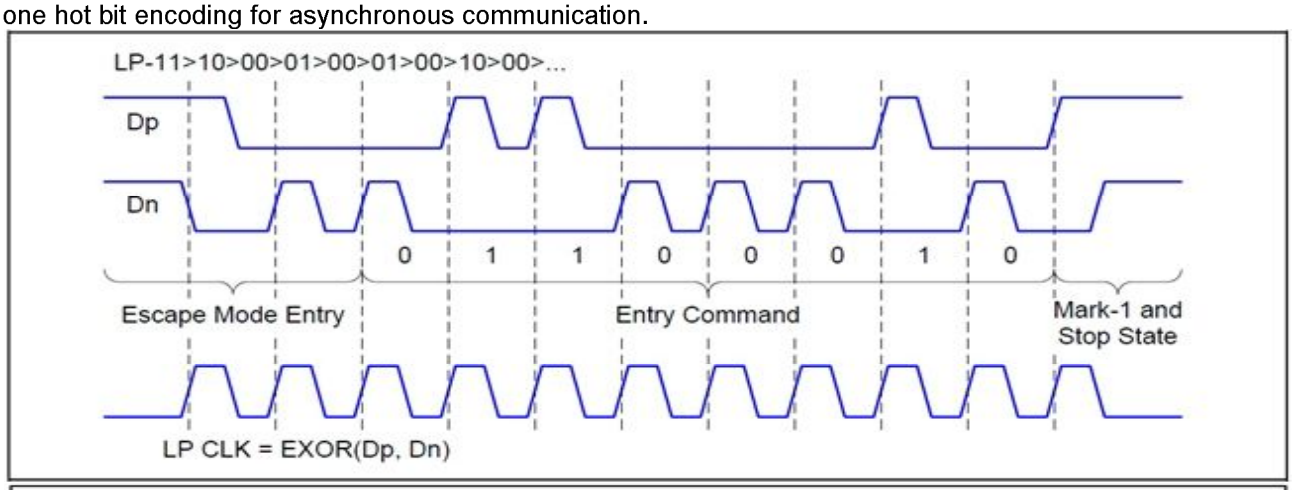
before the final Bridge state (LP-00), the Escape Mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

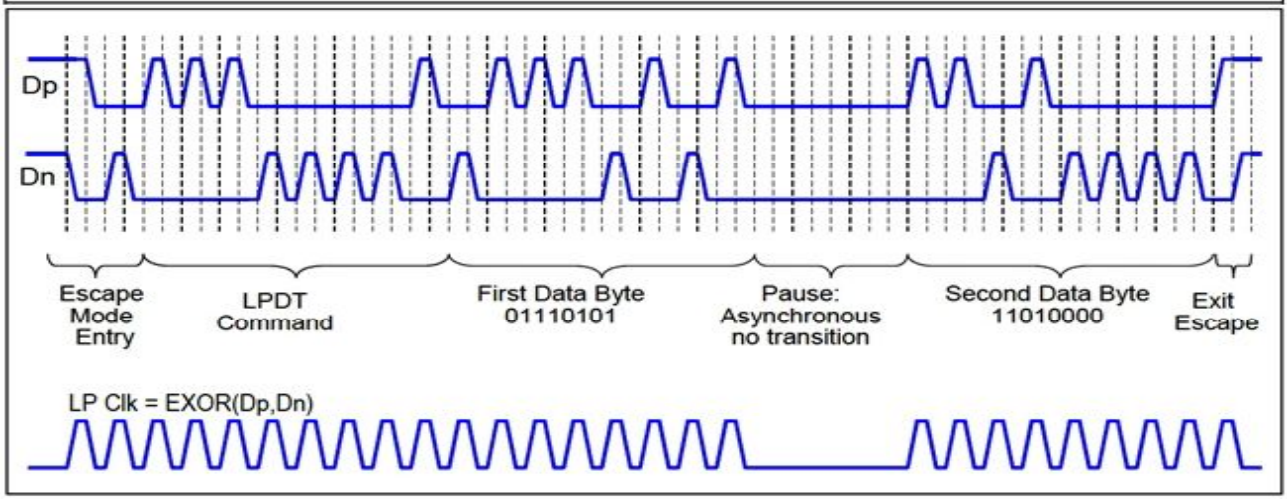
Once Escape Mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. Table below (MIPI Escape Mode Entry Code) lists all currently available Escape Mode commands and actions. All unassigned commands are reserved for future expansion

Escape Mode Action	Command Type	Entry Command Pattern (First Bit Transmitted to Last Bit Transmitted)	S6E8AA0	
			LP-RX	LP-TX
Low-power data transmission	Mode	11100001	O	O
Ultra-low power state	Mode	00011110	O	–
Undefined-1	Mode	10011111	–	–
Undefined-2	Mode	11011110	–	–
Reset-trigger (Remote application)	Trigger	01100010	O	–
Unknown-3	Trigger	01011101	–	-
Unknown-4 (Acknowledge trigger)	Trigger	00100001	–	O
Unknown-5	Trigger	10100000	–	–

12-2-7. Low Power Data Lane Operation

The Figure below shows the sequence of the low power data transmission. The Escape mode uses the spaced one hot bit encoding for asynchronous communication.





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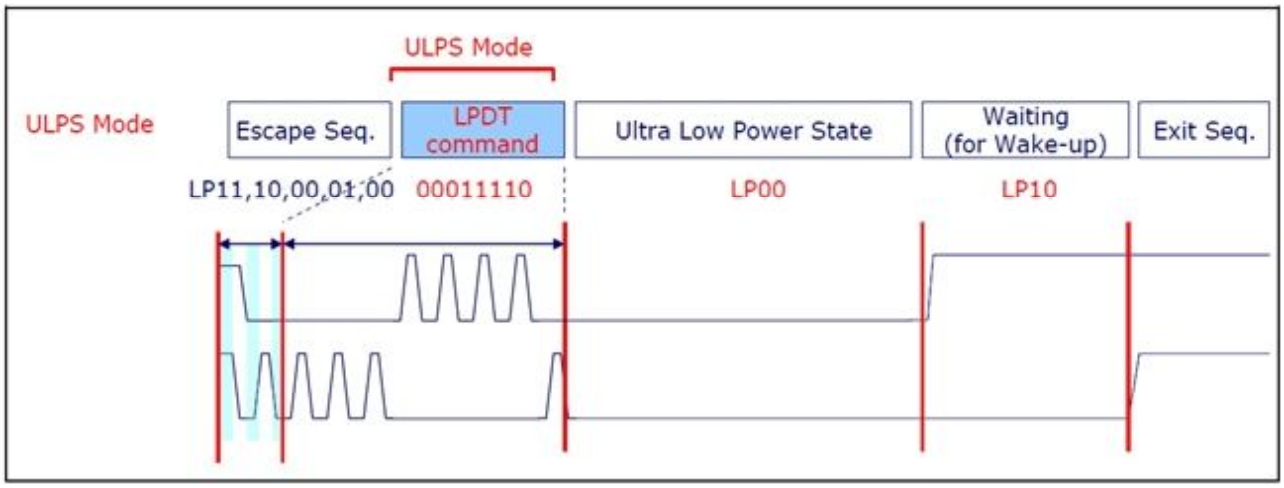
12-2-8. Ultra-low Power State

If the Ultra Low Power Entry Command is sent after an Escape Mode Entry command, the Lane shall enter the Ultra Low Power State (ULP). This Command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop State. Figure below shows an Ultra Low Power Entry and Exit example.



The Host processor provides LP10 state before Exit to wait for the MIPI SLAVE's stabilization. ULPS packet turn off the PHY_IO HS_RX. The ULPS turn off the bias current of HS_RX. The LP10 wakeup state is a trigger to turn on the HS_RX before normal STOP state.

12-2-9. Remote Application Reset

Remote Application Reset Command is used in case of transmission from the host processor to the peripheral. If the Entry Command Pattern matches the Remote Application Reset Command a Trigger is flagged to the protocol at the peripheral side via the logical PPI.
Figure below shows MIPI remote application reset packet using LP mode.
The host processor can send software reset trigger by Remote Application Reset Packet.

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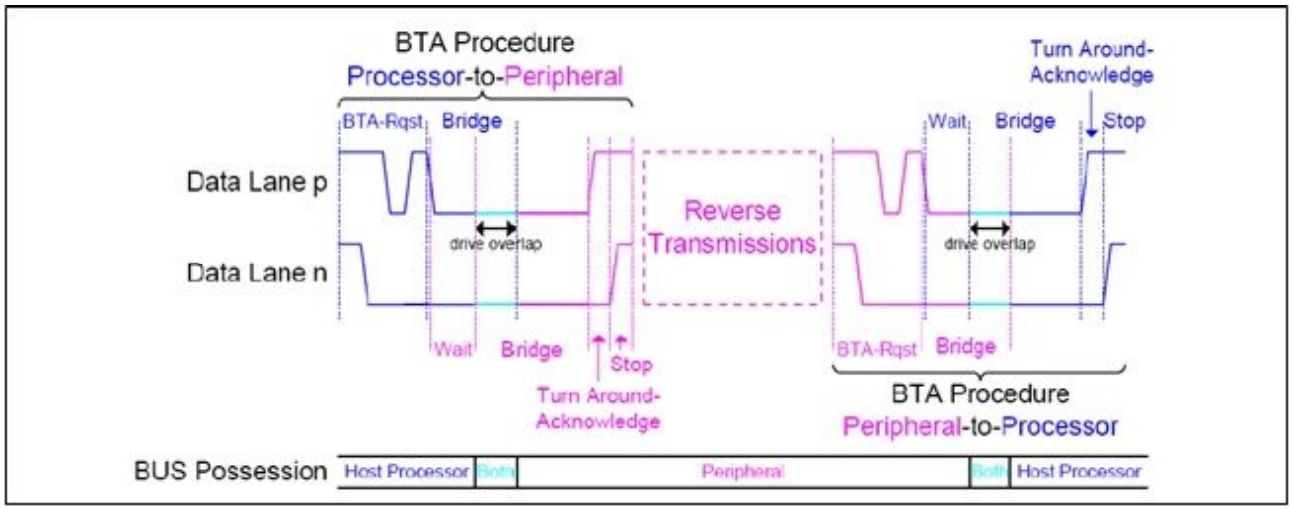
12-2-10. Bi-directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Figure below shows the BTA procedure graphically.



The low power clock timing for both sides of the Link does not have to be the same, but may differ. However, the ratio between the Low Power State Periods, T_{LPX} is constrained to ensure proper Turnaround behavior. The T_{LPX} (Master)/ T_{LPX} (Slave) shall be between 2/3 (0.667) and 3/2 (1.50). The handshake process for BTA allows only limited mismatch of Escape Mode clock frequencies between a host processor and a peripheral.

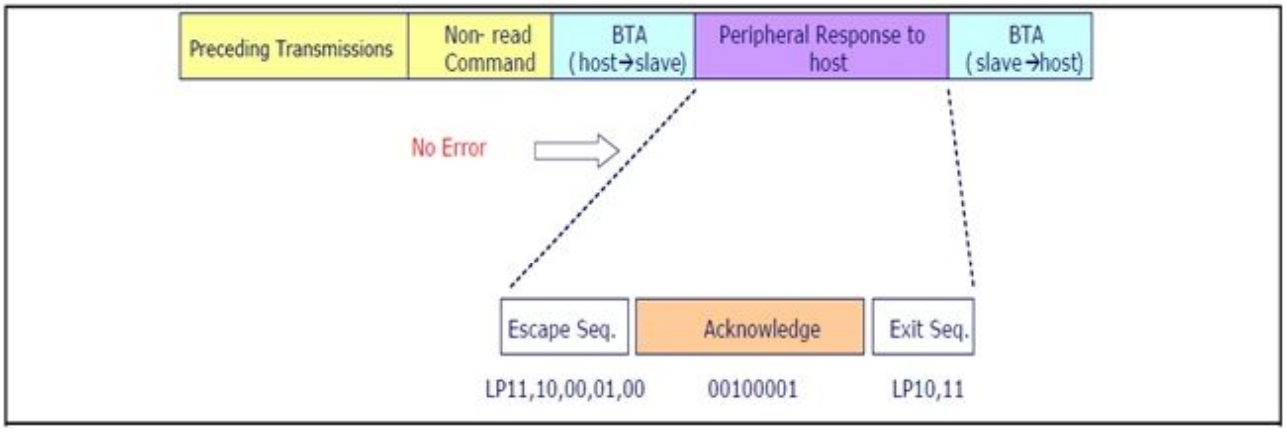


Figure shows an example of BTA after non-read command. The SLAVE get the lane controllability by BTA procedure to send the acknowledge packet on the successful data reception.

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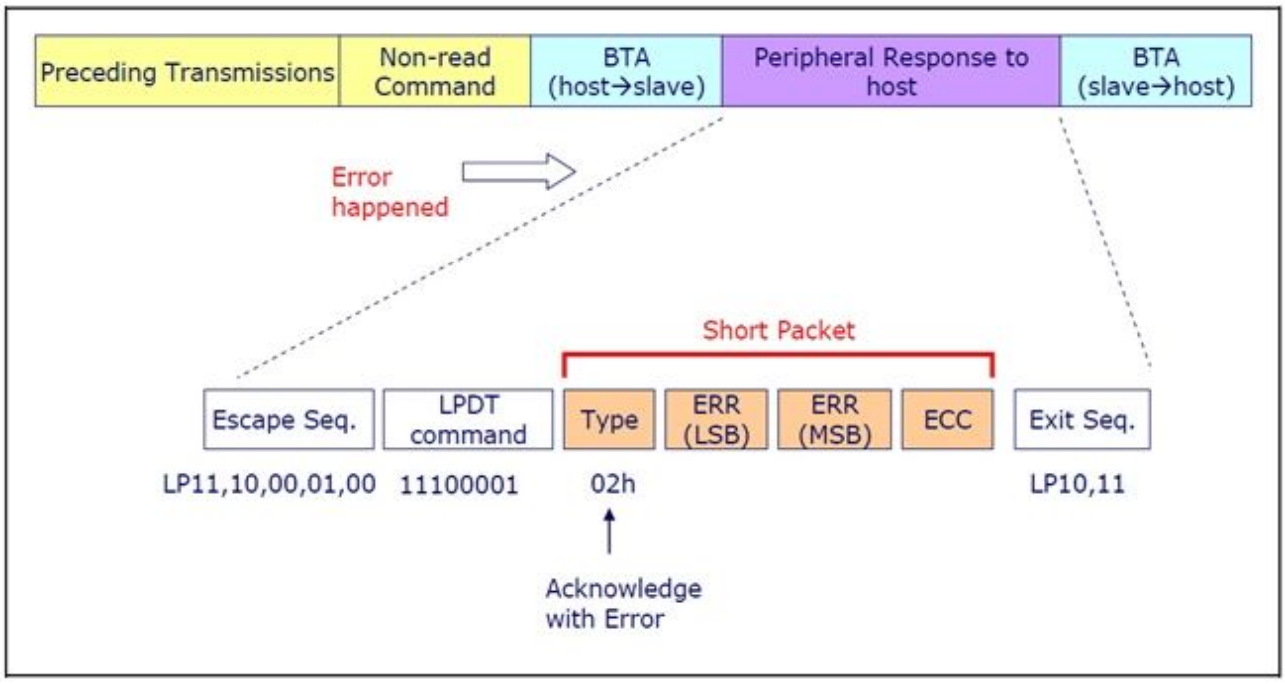

Figure shows an example of BTA after non-read command. The SLAVE gets the lane controllability by BTA procedure to send the acknowledge with error packet on the data reception error.

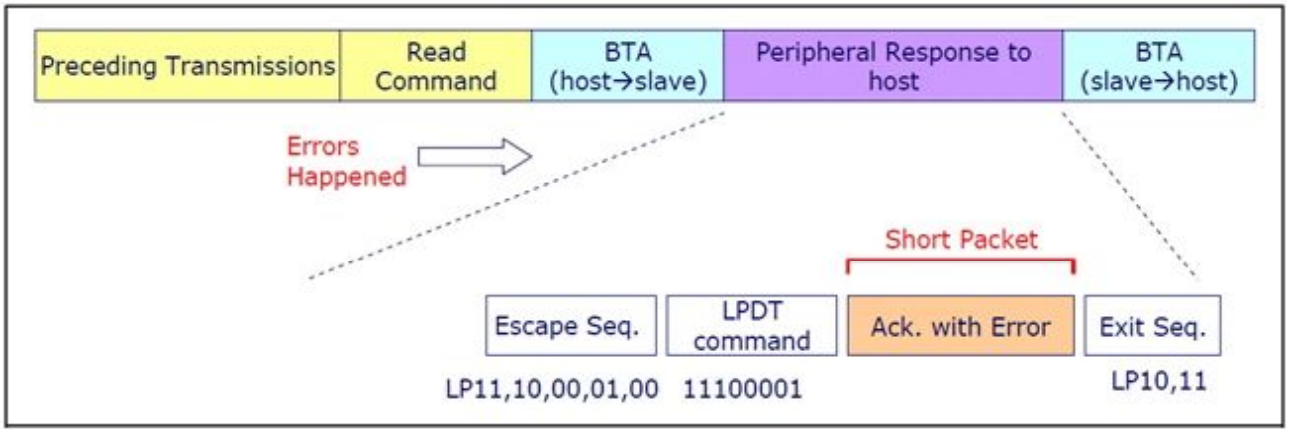

Figure shows an example of BTA after-read command. The SLAVE gets the lane controllability by BTA procedure to send the acknowledge with error packet on the data reception error.

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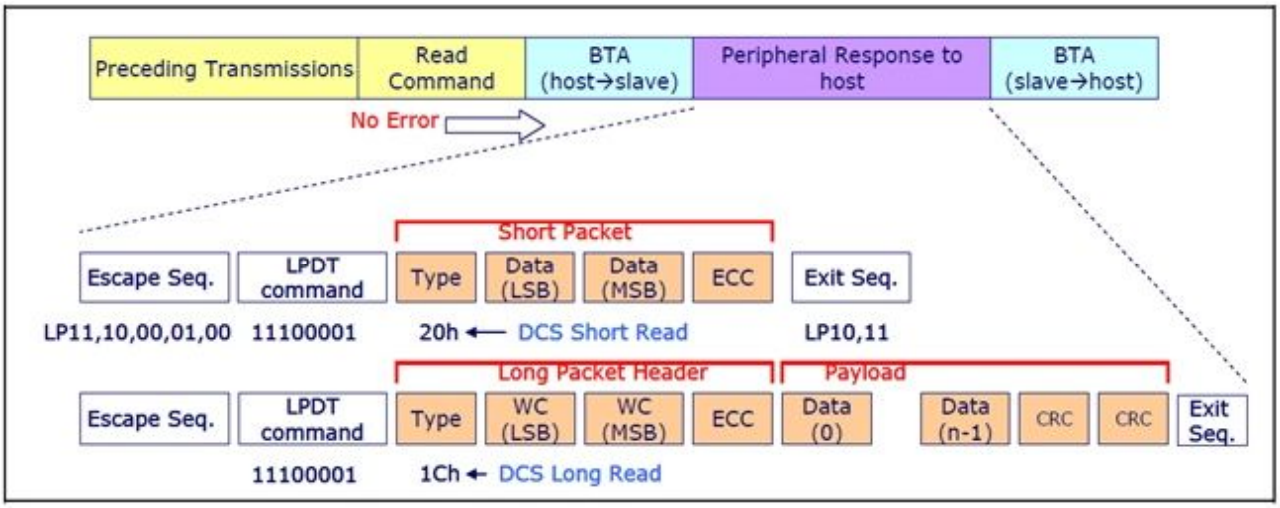

Figure shows an example of BTA after read command. The SLAVE gets the lane controllability by BTA procedure to send readed data packet on the successful data reception.

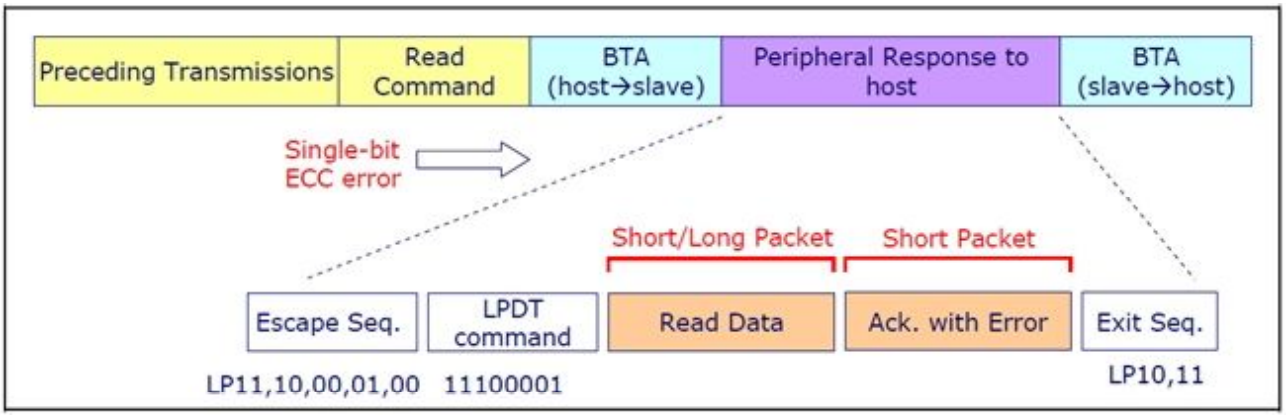

Figure shows an example of BTA after read command. The SLAVE gets the lane controllability by BTA procedure to send readed data packet and acknowledge with error on the one bit error.

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12-2-11. Global Operation Timings

The values in the table require a clock tolerance no worse than ± 10% for implementation.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns	(1, 6)
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52 × UI				(5)
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI	
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns	
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.	95		300		(6)
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38		
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60				(5)
$TC_{LK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300				
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35ns + 4 × UI		(6)
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAI}$L or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.			105ns + n × 12 × UI		(3, 5)
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns	(5)
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4 × UI		85ns + 6 × UI		

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Parameter	Description	Min.	Typ.	Max.	Unit	Note
$T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$	$T_{HS\text{-}PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10 × UI				
$T_{HS\text{-}SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS\text{-}PREPARE}$.	85ns + 6 × UI		145ns + 10 × UI		
$T_{HS\text{-}SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55ns + 4 × UI		(6)
$T_{HS\text{-}TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max (n × 8 × UI, 60ns + n × 4 × UI)				(2, 3, 5)
T_{INIT}						
T_{LPX}	Transmitted length of any Low-Power state period	56.25	62.5	68.75	ns	(4, 5)
Ratio T_{LPX}	Ratio of T_{LPX}(MASTER)/T_{LPX}(SLAVE) between Master and Slave side	2/3		3/2		
$T_{TA\text{-}GET}$	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5 × T_{LPX}			ns	(5)
$T_{TA\text{-}GO}$	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	4 × T_{LPX}				
$T_{TA\text{-}SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		2 × T_{LPX}		
T_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	

NOTE:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. If a > b then max (a, b) = a otherwise max (a, b) = b
3. Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode
4. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
5. Transmitter-specific parameter
6. Receiver-specific parameter

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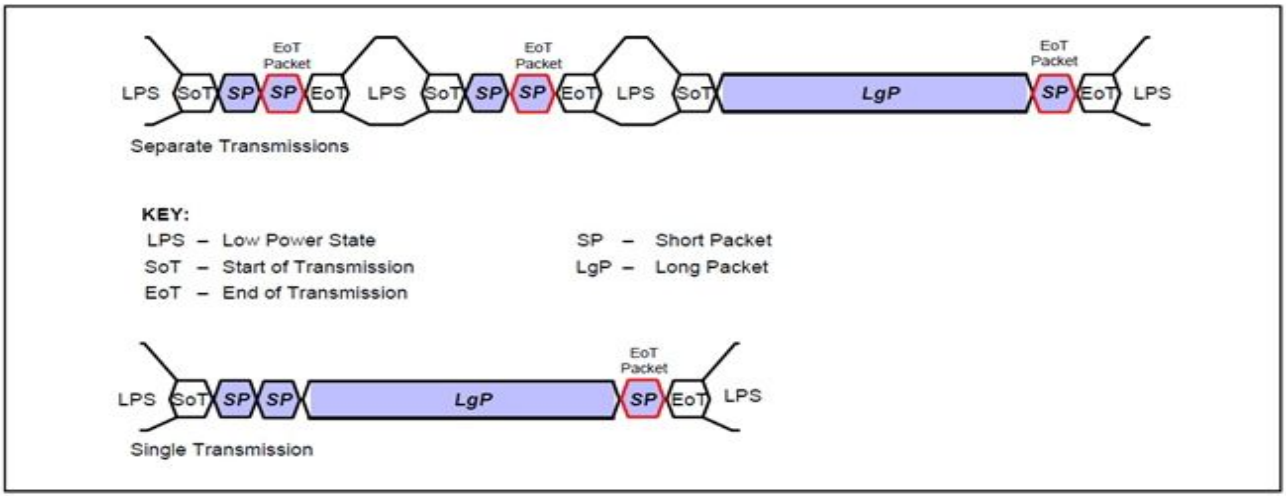
12-3 MIPI DSI

12-3-1. Multiple Packets Per Transmission

The MIPI CORE of S6E8AA0 supports four data transmission defined in MIPI DSI specification.
And in order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp packet can be enabled or disabled with register.



12-3-2. General Packet Structure

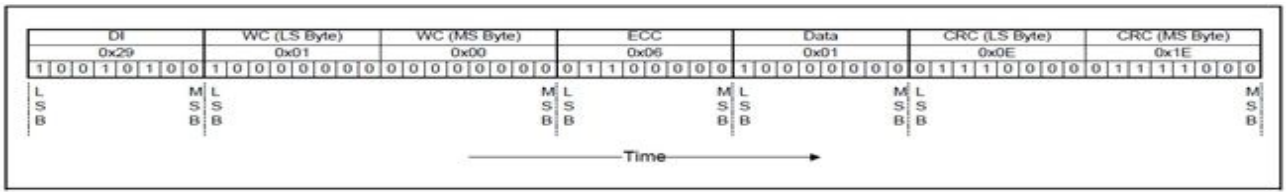
Two packet structures are defined for low-level protocol communication: Long packets and Short packets. For both packet structures, the Data Identifier is always the first byte of the packet.

12-3-3. Common Packet Element

Long and Short packets have several common elements

12-3-4. Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.
Figure below shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.



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12-3-5. Data Type Command Table

Data Type,		Description	Packet Size	(VD_PKT,GN_PKT)			
(hex)	(binary)			LL	HL	LH	HH
01h	00 0001	Sync event, V sync start	Short		O		O
11h	01 0001	Sync event, V sync end	Short		O		O
21h	10 0001	Sync event, H sync start	Short		O		O
31h	11 0001	Sync event, H sync end	Short		O		O
08h	00 1000	End of transmission packet	Short	O	O	O	O
02h	00 0010	Color mode (CM) off command	Short		O		O
12h	01 0010	Color mode (CM) on command	Short		O		O
22h	10 0010	Shut down peripheral command	Short		O		O
32h	11 0010	Turn on peripheral command	Short		O		O
03h	00 0011	Generic short WRITE, no parameters	Short			-	-
13h	01 0011	Generic short WRITE, 1parameter	Short			O	O
23h	10 0011	Generic short WRITE, 2parameters	Short			-	-
04h	00 0100	Generic READ, no parameters	Short			-	-
14h	01 0100	Generic READ, 1parameter	Short			O	O
24h	10 0100	Generic READ, 2parameters	Short			-	-
05h	00 0101	DCS WRITE, no parameters	Short	O	O	O	O
15h	01 0101	DCS WRITE, 1parameter	Short	O	O	O	O
06h	00 0110	DCS READ, no parameters	Short	O	O	O	O
37h	11 0111	Set maximum return packet size	Short	O	O	O	O
09h	00 1001	Null packet, no data	Long	O	O	O	O
19h	01 1001	Blanking packet, no data	Long		O		O
29h	10 1001	Generic long write	Long			O	O
39h	11 1001	DCS long write/write_LUT command packet	Long	O	O	O	O
0Eh	00_1110	Packet pixel stream, 16bit RGB 565 format	Long		O		O
1Eh	01_1110	Packet pixel stream, 18bit RGB 666 format	Long		O		O
2Eh	10_1110	Packet pixel stream, 18bit RGB loosely 666 format	Long		O		O
3Eh	11 1110	Packed pixel stream, 24-bit RGB, 888 format	Long		O		O
x0h&Fh	xx 0000	DO NOT USE					
	xx 1111	All unspecified codes are reserved					

Note that VDT_PKT(H=Video & Command mode supported, L=Only Command mode) and GN_PKT(H=DCS & Generic supported, L=Only DCS).

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Data Types for Peripheral-sourced Packets

Data Type (hex)	Data Type (binary)	Description	Packet Size	GN PKT	
				L	H
00h ~ 01h	00 000x	Reserved	Short	–	–
02h	00 0010	Acknowledge with error report	Short	O	O
03h ~ 07h	00 0011 ~ 00 0111	Reserved		–	–
08h	00 1000	End of transmission Packet	Short		
09h ~ 10h	00 1001 ~ 01 0000	Reserved			
11h	01 0001	Generic short READ response, 1-byte returned	Short		O
12h	01 0010	Generic short READ response, 2-bytes returned	Short		O
13h ~ 18h	01 0011 ~ 01 1000	Reserved		–	–
1Ah	01 1010	Generic long READ response	Long		O
1Bh	01 1011	Reserved		–	–
1Ch	01 1100	DCS long READ response	Long	O	O
1Dh ~ 20h	01 1101 ~ 10 0000	Reserved		–	–
21h	10 0001	DCS short READ response, 1-byte returned	Short	O	O
22h	10 0010	DCS short READ response, 2-bytes returned	Short	O	O
23h ~ 28h	10 0011 ~ 10 1000	Reserved		–	–
29h ~ 3Fh	10 1001 ~ 11 1111	Reserved		–	–

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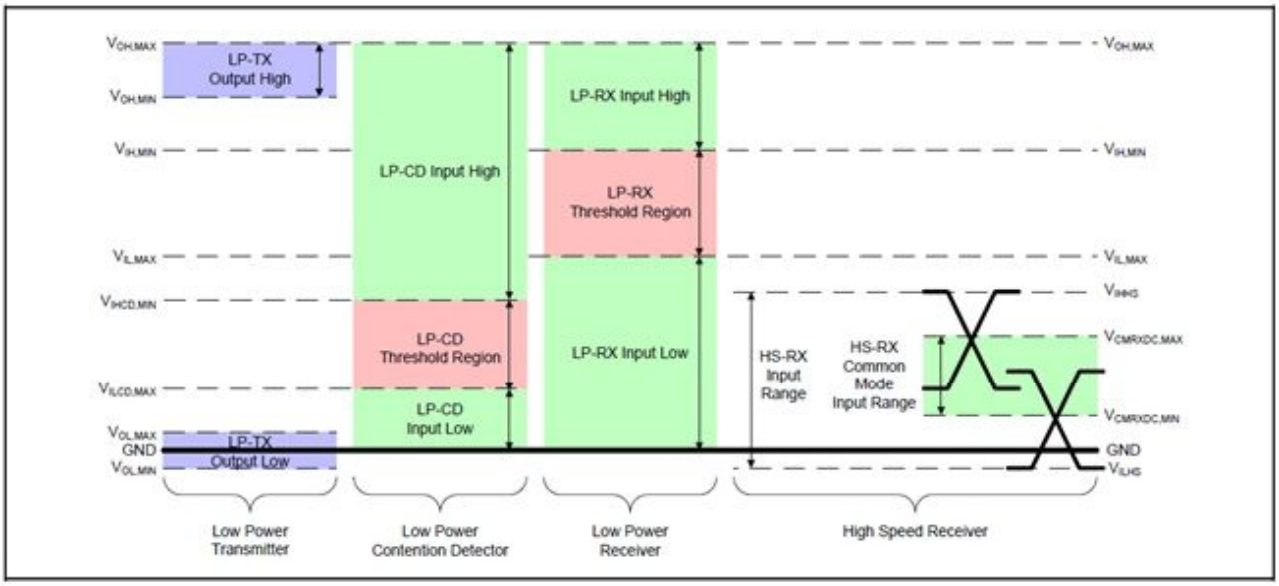
12-3-6. Error Report Packet

Bit	Description	Implementation
0	SoT error	O
1	SoT sync error	O
2	EoT sync error	O
3	Escape mode entry command error	O
4	Low-power transmit sync error	O
5	HS receive timeout error (Timeout error)	O
6	False control error	O
7	Contention Detection error	O
8	ECC Error, single-bit (Detected and corrected)	O
9	ECC Error, multi-bit (Detected, not corrected)	O
10	Checksum error (Long packet only)	O
11	DSI data type not recognized	O
12	DSI VC ID invalid	O
13	Invalid transmission length	O
14	Reserved	–
15	DSI protocol violation	O

12-3-7. Lane Connection Detection



The Low-power receiver and a separate contention detector shall be used in a bi-directional Data Lane to monitor the line voltage on each Low-power signal. The Low-power receiver shall be used to detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL. The contention detector shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than VIHCD. An LP low fault shall not be detected when the pin voltage is less than VILCD.

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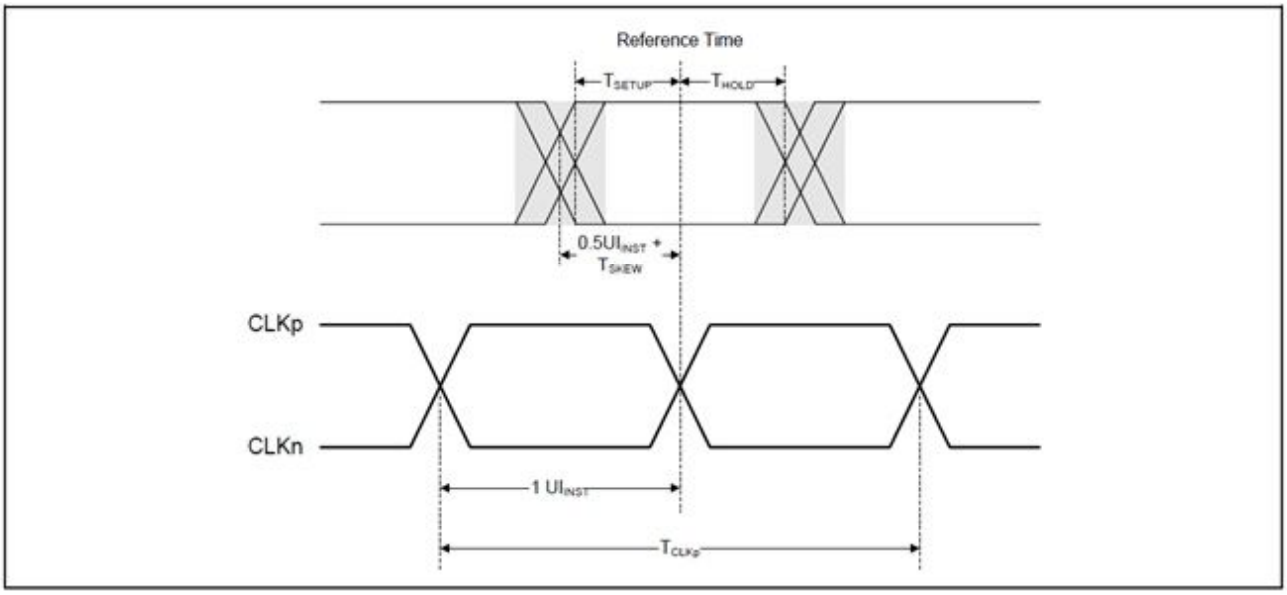
12-4 MIPI Characteristics

12-4-1. High Speed Data-clock Timing

Host sends a differential clock signal to the S6E8AA0 to be used for data sampling. This signal is a DDR (Half-rate) clock and has one transition per data bit time. The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in figure below.



Clock Parameter	Symbol	# of d-lane	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UII_{NST}	4	2		12.5	ns	(1,2)

NOTE:

1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Skew (Measured at transmitter)	$T_{SKEW[TX]}$	-0.15		0.15	UIINST	(1)
Data to Clock Setup Time (Receiver)	$T_{SETUP[RX]}$	0.15			UIINST	(2)
Clock to Data Hold Time (Receiver)	$T_{HOLD[RX]}$	0.15			UIINST	

NOTE:

1. Total silicon and package delay budget of 0.3 × UIINST
2. Total setup and hold window for receiver of 0.3 × UIINST
3. TSETUP[RX] and THOLD[RX] are only for RX without FPCB and connector and guaranteed by design. For module test, TSETUP[Module] and THOLD[Module] specification including FPCB and connector is 0.275UIINST. Refer to figure below

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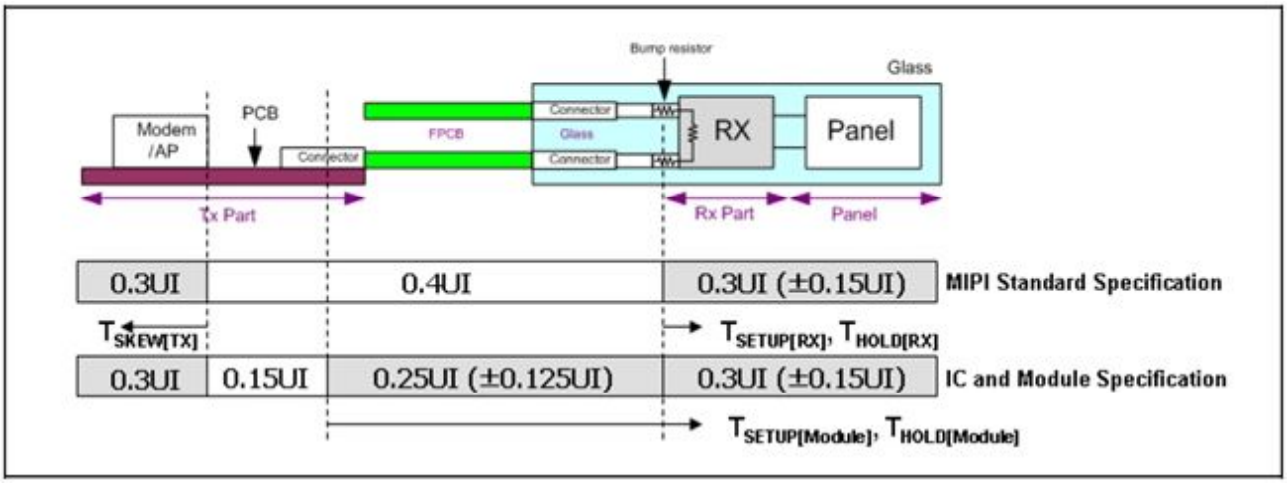

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13. Quality Level

13-1. AMOLED Module of Characteristic Inspection

13-1-1. The environmental conditions

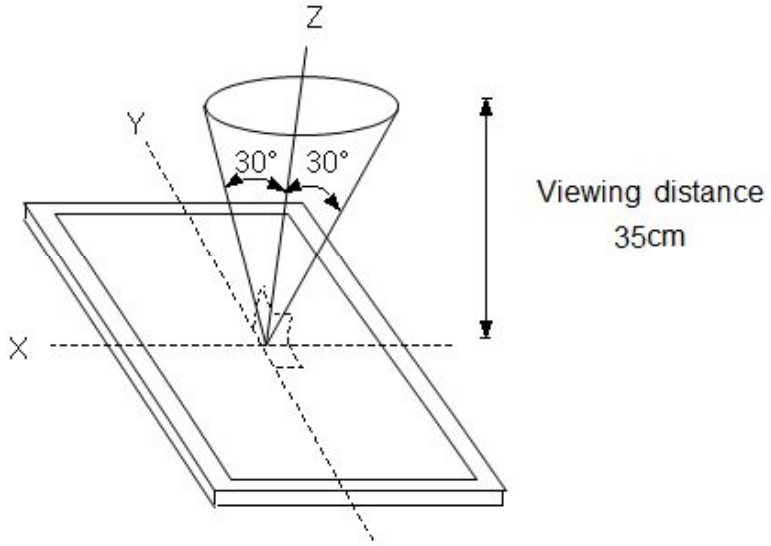
① Temperature & Humidity

Room temperature : 22 ± 3℃

Humidity : 65 ± 20%RH

② Viewing distance : 35cm ± 5cm

Viewing angle(tolerance) : ± 30°



③ Ambient light intensity : 800 ~ 1200 lux

13-1-2. Window

The environmental conditions for inspection shall be as follows.

① Light source : D65, Bar type 1 Lamp

② Ambient light intensity : 800 ~ 1200 lux

③ Viewing Distance : 35 ± 5cm

④ Viewing angle (tolerance) : the front side 90°(Z) ± 5°

⑤ Viewing Time : 10 ± 2 sec

⑥ Inspection Background : Only Black

⑦ Inspection Mode : Only Reflection inspection

⑧ Color variation(Icon,IR) : Transmitted inspection by backlight source (Light intensity :600Lux)

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13-2. Sampling Procedures for each item's acceptance table

Defect type	Sampling Procedures	AQL
Major Defect	MIL-STD-105D Inspection level Ⅰ normal inspection single sample inspection	0.65
Minor Defect	MIL-STD-105D Inspection level Ⅰ normal inspection single sample inspection	1.5

① Major defect

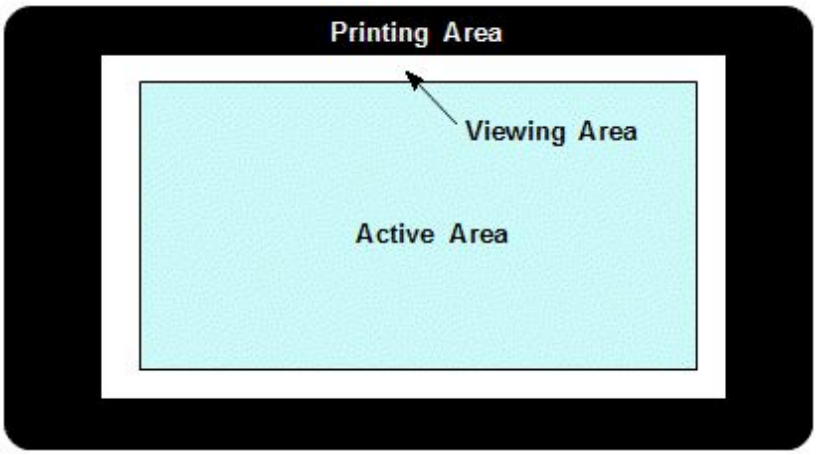
: A major defect refers to a defect which may substantially degrade usability for product applications.

② Minor defect

: A minor defects refers to a defect which is not considered to substantially degrade product application,or a defect which deviates from existing standards almost unrelated to the effective use of the product or its operation.

③ Determination of inspection area : Active Area + Viewing Area

Defect in "Out of Viewing Area" Zone should not be judged.



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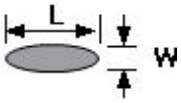
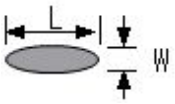
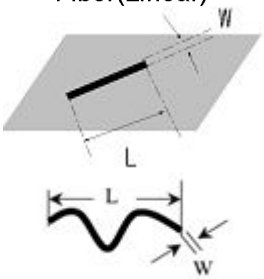
13-3. Inspection Item

13-3-1. Panel

No.	Item	Criterion of Defect	Type
1	No Display	Not allowance	Major
2	Irregular operating	Not allowance	Major
3	Dot Defect	Defect / Acceptable number Bright Dot / 0 **Dark Dot / 4 (regardless of color)** - Dark Dot Distance ≥ 20mm (Acceptable)	Minor
4	Polarizer Dent / Bubble  Ø=(L+W)/2	Size Ø (mm) / Acceptable number Ø ≦ 0.20 / Ignore 0.20 < Ø ≦ 0.50 / 3 0.50 < Ø ≦ 0.80 / 2 0.80 < Ø / 0	Minor
5	Dark / Bright Spots (Foreign Material)  Ø=(L+W)/2	Size Ø (mm) / Acceptable number Ø ≦ 0.15 / Ignore **0.15 < Ø ≦ 0.20 / 2** **0.20 < Ø / 0**	Major
6	Polarizer Scratch / Fiber(Linear) 	Width (㎜) / Length (㎜) / Acceptable number W ≦ 0.03 / Ignore / Ignore 0.03 < W ≦ 0.05 / L ≦ 2.0 / Ignore 0.03 < W ≦ 0.05 / 2.0 < L ≦ 5.0 / 2 0.05 < W ≦ 0.08 / L ≦ 1.0 / Ignore 0.05 < W ≦ 0.08 / 1.0 < L ≦ 5.0 / 2 0.08 < W / - / 0	Major
7	Discoloration / Panel Stain	Ignore If its limit sample is needed, it can be fixed mutually with a customer.	Major
8	WAD (White angular dependency)	Ignore If its limit sample is needed, it can be fixed mutually with a customer.	Major

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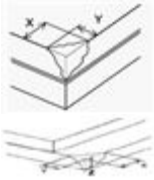
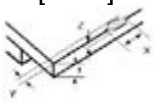
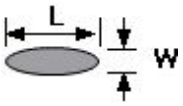
<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td rowspan="3">9</td><td>Glass Chipping
 
[Pad area]</td><td>These criteria are applied to all corners of panel glass (unit : mm)
<table>
<tr><th></th><th>Z</th><th>X</th><th>Y</th></tr>
<tr><td>Non-pad area</td><td>≦ t</td><td>≦ 1.0</td><td>≦ 1.0</td></tr>
<tr><td>Pad area</td><td>≦ t</td><td>≦ 2.0</td><td>≦ 1.2</td></tr>
</table>
* Pad means the contact edge, overhung single glass part</td><td>Major</td></tr>
<tr><td> </td><td>These criteria are applied to all side edges of panel glass (unit : mm)
<table>
<tr><th>Z</th><th>X</th><th>Y</th></tr>
<tr><td>≦ t</td><td>≦ 2.0</td><td>≦ 0.5</td></tr>
</table></td><td>Major</td></tr>
<tr><td>
[Front]
 
[Opposite]</td><td>These criteria are applied to only sides of pad area of panel glass (unit : mm)
<table>
<tr><th></th><th></th><th>Z</th><th>X</th><th>Y</th></tr>
<tr><td rowspan="2">Pad front side</td><td>Near Pattern</td><td>≦ t</td><td>≦ 5.0</td><td>≦ 0.4</td></tr>
<tr><td>No Pattern</td><td>≦ t</td><td>≦ 5.0</td><td>≦ 0.5</td></tr>
<tr><td colspan="2">Pad opposite side</td><td>≦ t</td><td>≦ 5.0</td><td>≦ 0.6</td></tr>
</table></td><td>Major</td></tr>
</table>

13-3-2. Window

<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>1</td><td>Window Black/White Spots (Circular Foreign Material)
 

Ø=(L+W)/2</td><td>
<table>
<tr><th rowspan="2">Size Ø (mm)</th><th colspan="2">Acceptable number</th></tr>
<tr><th>V/A</th><th>Out of V/A (BM area)</th></tr>
<tr><td>Ø ≦ 0.15</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.15 ＜ Ø ≦ 0.25</td><td>2</td><td>2</td></tr>
<tr><td>0.25 ＜ Ø</td><td>0</td><td>0</td></tr>
</table>
Note : In case a foreign material is removed with a soft cloth, it is ignored.</td><td>Major</td></tr>
<tr><td>2</td><td>Window Dent / Bubble</td><td>
<table>
<tr><th rowspan="2">Size Ø (mm)</th><th colspan="2">Acceptable number</th></tr>
<tr><th>V/A</th><th>Out of V/A (BM area)</th></tr>
<tr><td>Ø ≦ 0.15</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.15 ＜ Ø ≦ 0.25</td><td>2</td><td>2</td></tr>
<tr><td>0.25 ＜ Ø</td><td>0</td><td>0</td></tr>
</table></td><td>Major</td></tr>
</table>

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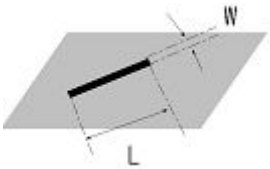
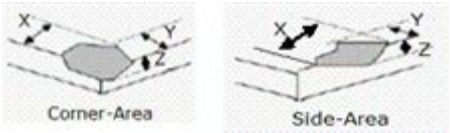
No.	Item	Criterion of Defect	Type
3	Window Scratch 		Major

Width (㎜)	Length (㎜)	Acceptable number
W ≦ 0.03	Ignore	Ignore
0.03 ＜ W ≦ 0.05	L ≦ 2.0	Ignore
	2.0 < L ≦ 5.0	1
0.05 ＜ W ≦ 0.08	L ≦ 1.0	Ignore
	1.0 < L ≦ 4.0	1
0.08＜ W	Apply to Dent/Bubble	-

No.	Item	Criterion of Defect	Type
4	Window (Line-shaped Foreign Material)		Major

Width (㎜)	Length (㎜)	Acceptable number
W ≦ 0.03	Ignore	Ignore
0.03 ＜ W ≦ 0.05	L ≦ 2.0	Ignore
	2.0 < L ≦ 5.0	1
0.05 ＜ W ≦ 0.08	L ≦ 1.0	Ignore
	1.0 < L ≦ 4.0	1
0.08＜ W	Apply to Spots (Circular Foreign Material)	-

No.	Item	Criterion of Defect	Type
5	Window Chipping		Major



	X	Y	Z	Acceptable number
Front	X≦1.0	Y≦0.35		Total 2
Side/Corner/Back	X≦1.0	Y≦0.16	Z≦1/2t	

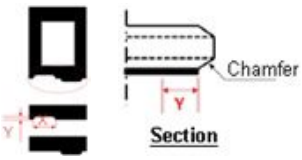
No.	Item	Criterion of Defect	Type
6	Window Printing Defect		Major

Location	Size	Acceptable Number
Printing Inside	D ≦ 0.1	Ignore
	0.1 < D ≦ 0.2	2
	D ＞ 0.2	0
Printing Outside	Y ≦ 0.1	Ignore
	X≦1.5, 0.1<Y≦0.15	1
	X>1.5, or Y>0.15	0

[Inside]

D=(X+Y)/2

[Outside]



Note : These criteria are applied to each side

Note : Pinhole of the BM area follow the inside criteria

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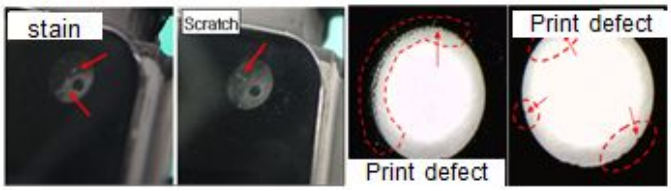
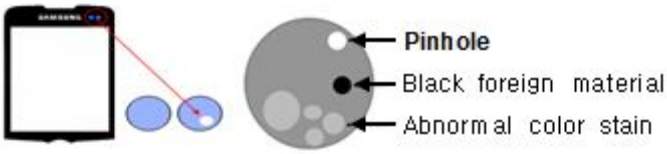
<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>7</td><td>Window ICON Printing Defect</td><td>Not allowed printing disconnection</td><td>Major</td></tr>
<tr><td>8</td><td>Window Icon Foreign Material</td><td>
<table>
<tr><th>Size (mm)</th><th>Acceptable Number</th></tr>
<tr><td>Φ≦0.2</td><td>1</td></tr>
<tr><td>0.2<Φ</td><td>0</td></tr>
</table>
Note) Light intensity : 600Lux
Apply to each icon at transmitted inspection mode</td><td rowspan="2">Major</td></tr>
<tr><td>9</td><td>Printing Pinhole In BM Area</td><td>1) Distance 15cm & 400lux & Transmitted inspection mode
2) Area: LED key around area(A/A bottom area)
3) If it is not found in front visual : OK

</td></tr>
<tr><td>10</td><td>Window Camera Hole</td><td>Foreign material/Stain/Scratch/Printing defects
1) Not allowed at Camera Hole center area
2) Allowed at Edge Area Printing Face : within 0.15mm

</td><td>Major</td></tr>
<tr><td>11</td><td>Window IR Sensor / LED Hole Area</td><td>
<table>
<tr><th></th><th>Defect Mode</th><th>Size (mm)</th><th>Acceptable Number</th></tr>
<tr><td>1</td><td>Pinhole</td><td>Φ≦0.15</td><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">Black Foreign Material</td><td>Φ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1<Φ≦0.15</td><td>1</td></tr>
<tr><td>3</td><td>Abnormal Color Stain</td><td>Φ≦0.3</td><td>Ignore</td></tr>
</table>

</td><td>Major</td></tr>
<tr><td>12</td><td>Surface Contamination</td><td>There should be no surface contamination which cannot be removed when being cleaned with a soft cloth.</td><td>Major</td></tr>
<tr><td>13</td><td>Icon Color Variation (Transparency)</td><td>If it is limited sample to need, it can be fixed mutually with with a customer
Inspection mode : Transmittance (Light intensity : 600Lux)</td><td>Major</td></tr>
<tr><td>14</td><td>IR Color Variation (Transparency)</td><td>If Transparency is satisfied : allowed
Inspection mode : Transmittance (Light intensity : 600Lux)</td><td>Major</td></tr>
</table>

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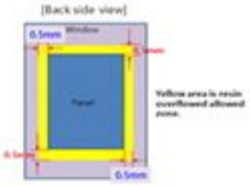
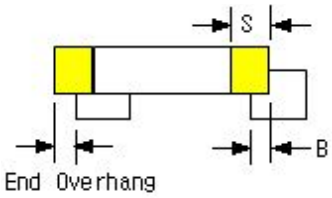
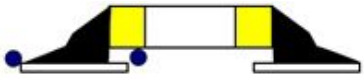
13-3-3. Other

No.	Item	Criterion of Defect		Type
1	Lamination	Resin cleaning marks (no height difference)	Allowed	Major
		Resin overflow /residues	0.5mm allowed from each edge of a panel 	
		Resin bubble	Not allowed. (If its limit sample is needed, it can be fixed mutually.)	
		Resin non-application (under viewing/active area)	Not allowed	
		Resin Vertical Pit	Not allowed	
2	FPCA SMT (Soldering)	(1) No polarity opposition (2) No wrong insertion		Major
3	FPCA Solder Short	Short of proximity pattern and land is defect		Major
4	FPCA Solder Crack	There should be no crack which gives an effect to quality of the display		Major
5	FPCA End Overhang	The size above 1/2 of soldering electrode of the parts overhang to the LAND is prohibited (but, contacting near other components is prohibited.) 		Major
6	FPCA Solder Ball	Not allowed if (Φ> 150um) 		Major

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<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>7</td><td>FPCB
(Dent/Scratch)</td><td>(1) Open Area : Not allowed if Cu layer exposed.
(2) Solder mask Area : Not allowed if Cu layer exposed.
(3) Pattern Area : Not allowed if Cu layer exposed.
(4) Black shield Area :
<table>
<tr><th>Defect Mode</th><th>Size</th><th>Acceptable Number</th></tr>
<tr><td>Line shaped</td><td>L ≦ 5mm</td><td>Ignore</td></tr>
<tr><td rowspan="2">Spot / Face Shaped</td><td>S(Area) ≦0.6mm^2</td><td>Ignore</td></tr>
<tr><td>0.6mm^2 < S(Area) < 1.0mm^2</td><td>2 Point</td></tr>
</table></td><td>Major</td></tr>
<tr><td>8</td><td>FPC Tilt Defect</td><td>Not allowed</td><td>Major</td></tr>
<tr><td>9</td><td>TSP Function NG</td><td>Not allowed</td><td>Major</td></tr>
<tr><td>10</td><td>Black Tape Bubble</td><td>If it's not seen at the front side : allowed.</td><td>Major</td></tr>
<tr><td>11</td><td>Black Tape Dent</td><td>If it's not seen at the front side : allowed.</td><td>Major</td></tr>
<tr><td>12</td><td>window cover film
(protect film)</td><td>Cover film shall not be located out of the window area.
Cover film shall not be torn, made a hole.</td><td>Major</td></tr>
</table>

※ Other cosmetic items which are not defined above are allowed,

if they are not seen at the front side after assembling phone set.

But, they follow the SDC's criteria, if SDC has one.

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14. Reliability

14-1. Environmental test

No	Item	Condition	qnty	Result	Judgment Criterion
1	High Temperature Storage	60℃/ 120hours	5	OK	1. No clearly visible defects or remarkable deterioration of display quality.However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted. 2. No function-related abnormalities 3. Optical criteria : .White △u'v' ≤0.02
2	Low Temperature Storage	-20℃/ 120hours	5	OK	
3	High Temperature Humidity Storage	60℃/90%RH/ 120hours	10	OK	
4	Thermal Shock	85℃ 1hr, -40℃ 1hr / 30 Cycles	10	OK	
5	Temperature Humidity Bias	60℃/93%RH/ 120hours	10	OK	

Note) The results must be measured after 2 hours later under room temperature keeping.

14-2. Other test

No.	Item	Condition	qnty	Result	Judgment Criterion
1	ESD	- Air discharge : ±8kV, 5POINT, Each 2times - Contact discharge : ±4kV, 5POINT, Each 2times	5	OK	1. No visible defects .(optical / mechanical) 2. No function-related abnormalities

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15. Handling Precautions

15-1. Mounting Method

The AMOLED panel of SAMSUNG Display CO.,LTD. module consists of two slim glasses with polarizer which can easily get damaged. Since the module is constructed as to be fixed by utilizing fitting holes in the printed circuit board. Extreme care should be used when handling the AMOLED modules.

15-2. Caution of AMOLED Handling and Cleaning

When cleaning the display surface, use soft cloth solvent as recommended below and wipe gently.

◎ Isopropyl alcohol
◎ Ethyl alcohol
◎ Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.
Do not use the following solvent.

◎ Water
◎ Ketone
◎ Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns.
Do not use the following solvent on the pad and prevent it from being contaminated.

◎ HCFC (Other area except ITO pad can use the HCFC for cleaning process)
◎ Soldering flux
◎ Chlorine(Cl), Sulfur(S)
◎ Spittle, Fingerprint

If the product is not wrapped with a desiccant added pad, ITO pattern can be damaged by corrosion. SAMSUNG Display CO,.LDT. suggests wrapping a product with a desiccant unless customers particularly indicate that they do not want it. In case ITO pattern corrodes due to the usage of chlorine, sulfur or customer's mishandling of the product, the responsibility lies with the customer.

15-3. Caution Against Static Charge

For AMOLED module, use C-MOS LSI drivers, therefore we recommend that you ;
Connect any unused input terminal to VCI or VSS, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.
It could occur static electricity when taping off the film which protects AMOLED.
Against static charge, you should make sure that the product is safe or not by experiment in advance.

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15-4. Packing

◎ The packing principle is that AMOLED module should keep its packing condition at the time of delivery.
◎ For safety & avoiding the module damage, Carton box must stack the below 4 boxes. When storing the AMOLED after unpacking, note the followings.
◎ AMOLED module is consisted of GLASS and assemblies. It should avoid pressure, strong impact, and being dropped from a height.
◎ To prevent modules from degradation, do not operate or store them in a place where they are directly exposed to sunlight or high temperature/humidity.

15-5. Caution for Operation

◎ If you do not follow normal POWER ON , OFF sequence or abnormal operating, then AMOLED module can be damaged electro-optically and does not recover.
Do not change software without SDC confirmation.
◎ Response time may extremely delay at a temperature lower than operating range, AMOLED does not normally operate at a high temperature. But this may recover at a proper temperature.
◎ When you set optimal operating voltage to AMOLED module, you can see the optimal contrast of AMOLED. So, add voltage controllable function at SET Module.
◎ AMOLED module may not display normally when twisting power or pressing power is added. Therefore you should secure AMOLED module maximum thickness at set assembly not to have any pressure affect AMOLED module.
◎ Electro-chemical reaction may occur when there is humidity on pad, therefore, you should use AMOLED Module below maximum operating humidity.
◎ AMOLED Module Power Vdd should be designed to protect surge current at SET Module.
◎ You should not damage connector and cable for AMOLED module assembly by force folding or by applying extreme power.
◎ AMOLED may not display normally when it is interfered by surrounding elements, therefore you should consider setting design not to damage AMOLED module by surrounding elements.
◎ To satisfy EMI standards, you should plan your design after considering emitting energy.
◎ We can not guarantee display characteristics outside viewing area, therefore your set window should be fixed into viewing area.
◎ Image-sticking may occur if AMOLED displays same image for a long time, so you need to make a change for AMOLED.

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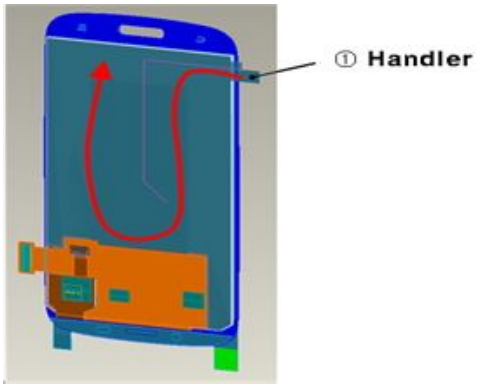

◎ When remove the window protective film, Necessarily need to apply as a way to prevent Cushion and conductive tape Delamination.
- As a upper Figure,the handler take off the direction of the arrow to remove the protective film.

15-6. Storage

◎ Place in a dark place where neither exposure to direct sunlight or any fluorescent light is permitted and keep at room temperature & room humidity.
◎ Store with no contact with polarizer surface.
[It is recommended to store them as they have been contained in the inner container when we delivered them.]

15-7. Safety Precautions

◎ Disassembly or modification may cause electric shock, damages to sensitive part inside of the AMOLED module, dust adhesion, or scratches on the display part.
◎ In the event that the contents of AMOLED module are on skin, wipe them with a paper towel or gauge and wash the part well, and receive medical attention if necessary.
◎ Do not use the AMOLED module for the special purpose besides display units.
◎ Be careful of the glass chips that may cause injury to fingers of skin, when the display part is broken.
◎ For keeping safe quality from outer exposure or contamination, modules should be consumed within 2 months after unpacking.

15-8. Precautions before Use

You should discuss the following case with SAMSUNG Display CO., LTD.
◎ in case of any questions about contents of this "Specification For Approval".
◎ in case of occurring new problems not mentioned at this "Specification For Approval".
◎ in case of your request about income inspection specification change.
◎ in case of occurring new problem at your driving test.

※ If SAMSUNG Display CO., LTD has to change the conditions specified in the specification, previously the negotiation shall be held and decided.

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16. Drawing

16-1. Product Drawing

Next Page

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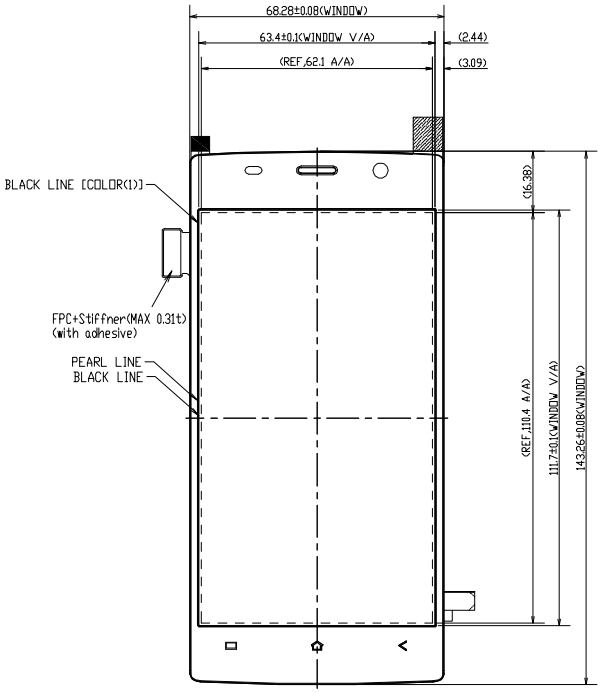
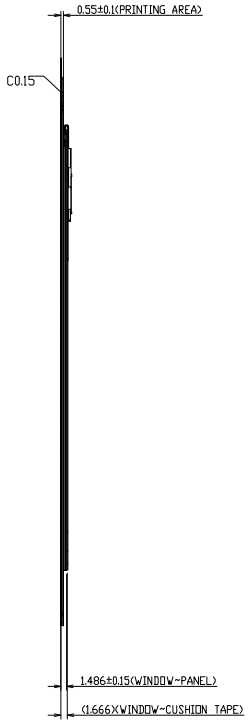
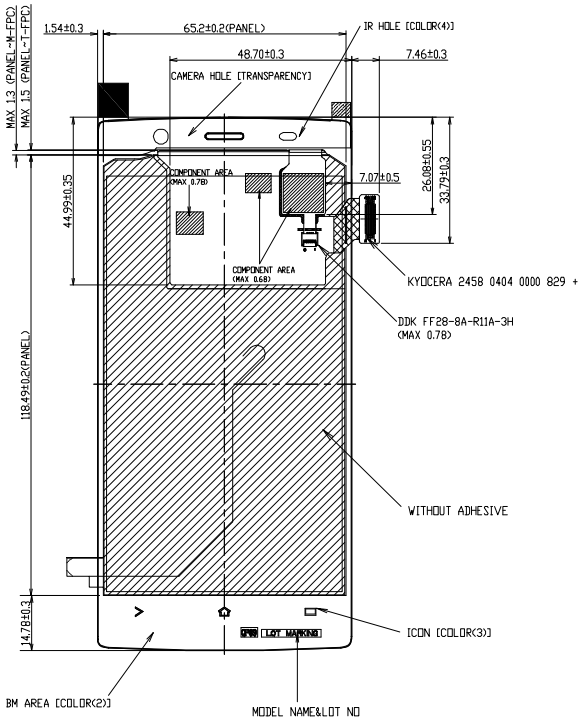
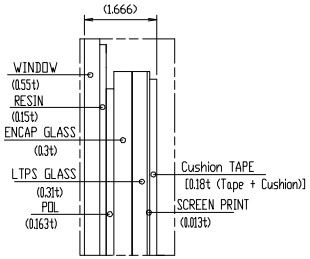
[PIN MAP]

Pin number	Pin name
1	TSP_AVDD_3.3V
2	GND
3	TSP_VDD_3.0V
4	DSN
5	TSP_SDA
6	DSP
7	TSP_VDDIO_1.8V
8	GND
9	TSP_SCL
10	DON
11	TSP_CHRG_IN
12	DOP
13	TSP_CHG_BAR
14	GND
15	GND
16	CKN
17	VDDP_EN
18	CKP
19	EL_ON
20	GND
21	IOVDD_1.8V
22	DIN
23	VLIN_7.7V
24	DIP
25	VCI_3.0V
26	GND
27	ERR_FG
28	BSN
29	RESET
30	BSP
31	WTPHV
32	GND
33	ELVDD_FBS
34	NC
35	ELVDD
36	ELVSS
37	ELVDD
38	ELVSS
39	ELVDD
40	ELVSS









STACK UP(S=NS)

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NOTE

1. DESCRIPTION : AMOLED DISPLAY, 4.99", FHD(1080X1920)
2. UNIT : mm
3. THIS MODULE IS ACCORDING TO ENVIRONMENTAL REQUIREMENTS(ROHS).
4. GLASS MATERIAL : NEG T2X-1
5. WINDOW COATING : AF
6. LOT MARK MUST BE REAR OF WINDOW

REV	DATE	DESCRIPTION OF REVISION	REASON	CHK'D BY	REV	DATE	DESCRIPTION OF REVISION	REASON	CHK'D BY

GENERAL TOLERANCE			
STEP	LEV.1	LEV.2	LEV.3
0 < X ≤ 4	±0.05	±0.10	±0.2
4 < X ≤ 16	±0.08	±0.15	±0.3
16 < X ≤ 64	±0.12	±0.25	±0.5
64 < X ≤ 256	±0.25	±0.40	±0.8

UNIT	mm	DES'D BY	CHK'D BY	APP'D BY	MODEL NAME	AMS499QP89	
SCALE	1:1	C.D.LIM	D.C.KIM	J.S.OH	PART NAME	OUTLINE DIMENSION	
TOLERANCE							
-		'15.03.13	'15.03.13	'15.03.13			
SAMSUNG DISPLAY		PROJECTION	STD.TOL	SIZE	CODE NO.	-	SHEET 1/1
			±0.3	A2	SPEC NO.	TDS00441-000	VER 000

2015.02.13 / Rigid Module Development 3 Group / C.D.LIM

301/014285/6819
이동규/124107066/국내 본사제품개발1그룹(OLED)/1196721 64/20150409165032

16-2. Main FPCB Drawing

16-2-1. Main FPC Schematic Diagram

Next Page

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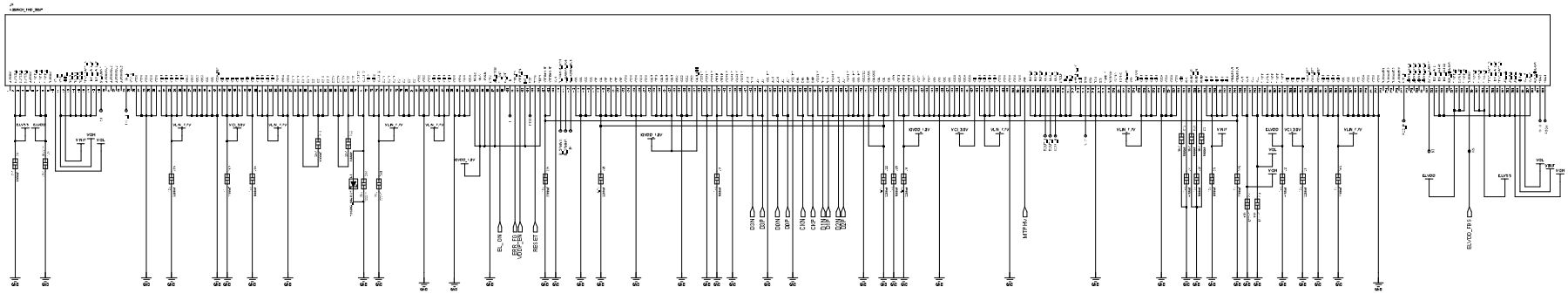
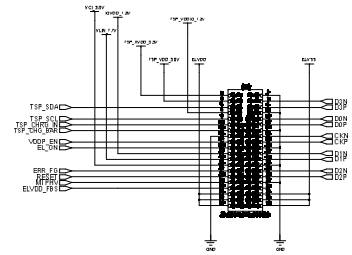
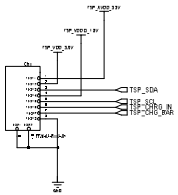
301701428564851







Changed by	SHAUEDAL	Date	2013/07/09	Title	13.3in-2K
Engineer	SHAUEDAL	Drawn By	SHAUEDAL	Size	A3 0.5X
Spec No.	0.0122561-000				
Part Name	ASSY FPC-MAIN				
PRA Code	LJ5-317-KA				
Sheet	1/1	P.11			

Samsung Display

SPECIFICATION

AMS490GP42 MAIN REV0.1_GIDNEE

Samsung Confidential

김민영/12425738/Rigid제품개발그룹/1193102141/20140515101007

16-2-2. Main FPC Electronic Part List

NO	CATEGORY	REFERENCE	Q'ty	SPECIFICATION	SDC CODE	MAKER
1	C-CER,CHIP	C9,C13,C14, C23,C26,C27	6	1000nF,10%,10V,X5R,TP,1005	2203-006562	Note 4
2	C-CER,CHIP	C5,C6,C11	3	1000nF,10%,16V,X5R,TP,1005	2203-006841	Note 3
3	C-CER,CHIP	C15,C16,C24,C25	4	2200nF,10%,16V,X5R,TP,1005	2203-007392	Note 5
4	C-CER,CHIP	C1,C12	2	2200nF,10%,10V,X5R,TP,1005	2203-007271	Note 1
5	C-CER,CHIP	C2,C4,C7, C10	4	4700nF,20%,10V,X5R,TP,1005	2203-007393	Note 2
6	C-CER,CHIP	C17~C20	4	1000nF,10%,25V,X5R,TP,1005	2203-007456	Note 6
7	C-CER,CHIP	C8,C21,C22	3	2200nF,10%,6.3V,X5R,TP,1005	2203-006838	Note 7
8	C-CER,CHIP	C3	1	4700nF,16V,X5R,TP,1005	2203-008573	Note 8
9	CONNECTOR-FPC/FFC/PIC	CN1	1	FF28-8A-R11A-3H 8P,0.25mm,SDC-A,AU,Y,FLIP,TOP	3708-003074	DDK
10	SOCKET-BOARD TO BOARD	CN2	1	24 5804 040 000 829+ 40P,2R,0.4MM,SDC-S,AU,BLK	3710-003885	Kyocera ELCO
11	DIODE	D1	1	RB520G-30GT2R,30V,100mA,	0404-001378	ROHM
12	FPC	FPC	1	AMS499QP42 Main FPC	-	BH-Flex

1) FPCB ASS'Y IS PB & Halogen FREE
2) NOTE 1 : AVX, MURATA, MURATB, SEM, TAIYO, TDK, TJSEM
2) NOTE 2 : AVX, MURATA, SEM, TAIYO, TDK, TJSEM, WALSIN
2) NOTE 3 : AVX, KYOCE, MURATA, MURATB, SEM, TAIYK, TAIYO, TDK, TJSEM, YOUNYI
2) NOTE 4 : AVX, DARFON, JMTELE, KEMET, KYOCE, SAMC, SAMHC, SEM, TAIYO, TDK, TJSEM, WALSIN, YAGEO
2) NOTE 5 : AVX, MURATA, SEM, YAIYO, TJSEM
2) NOTE 6 : MURATA, SEM, TAIYO, TJSEM, WALSIN
2) NOTE 7 : AVX, MURATA, MURATB, PHYCOM, SAMC, SEM, TAIYK, TAIYO, TDK, TJSEM, WALSIN, YAGEO
2) NOTE 8 : MURATA, SEM

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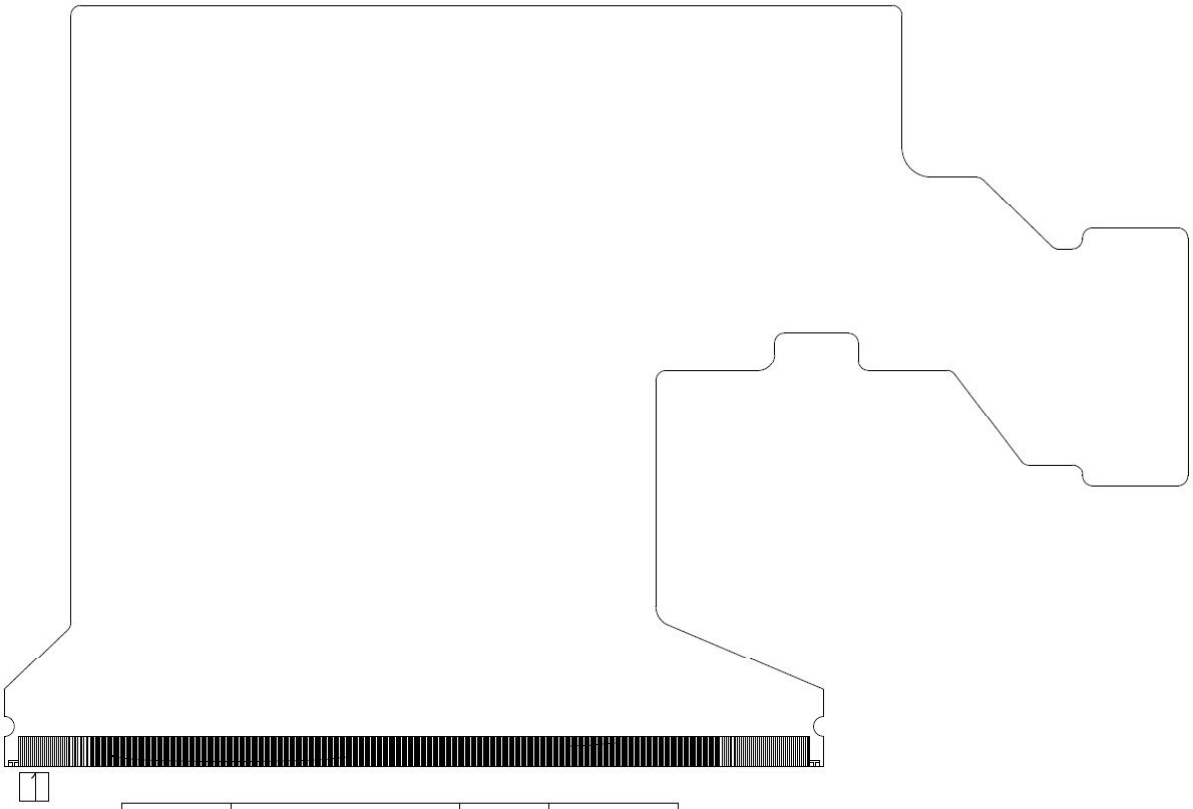
301701428564851

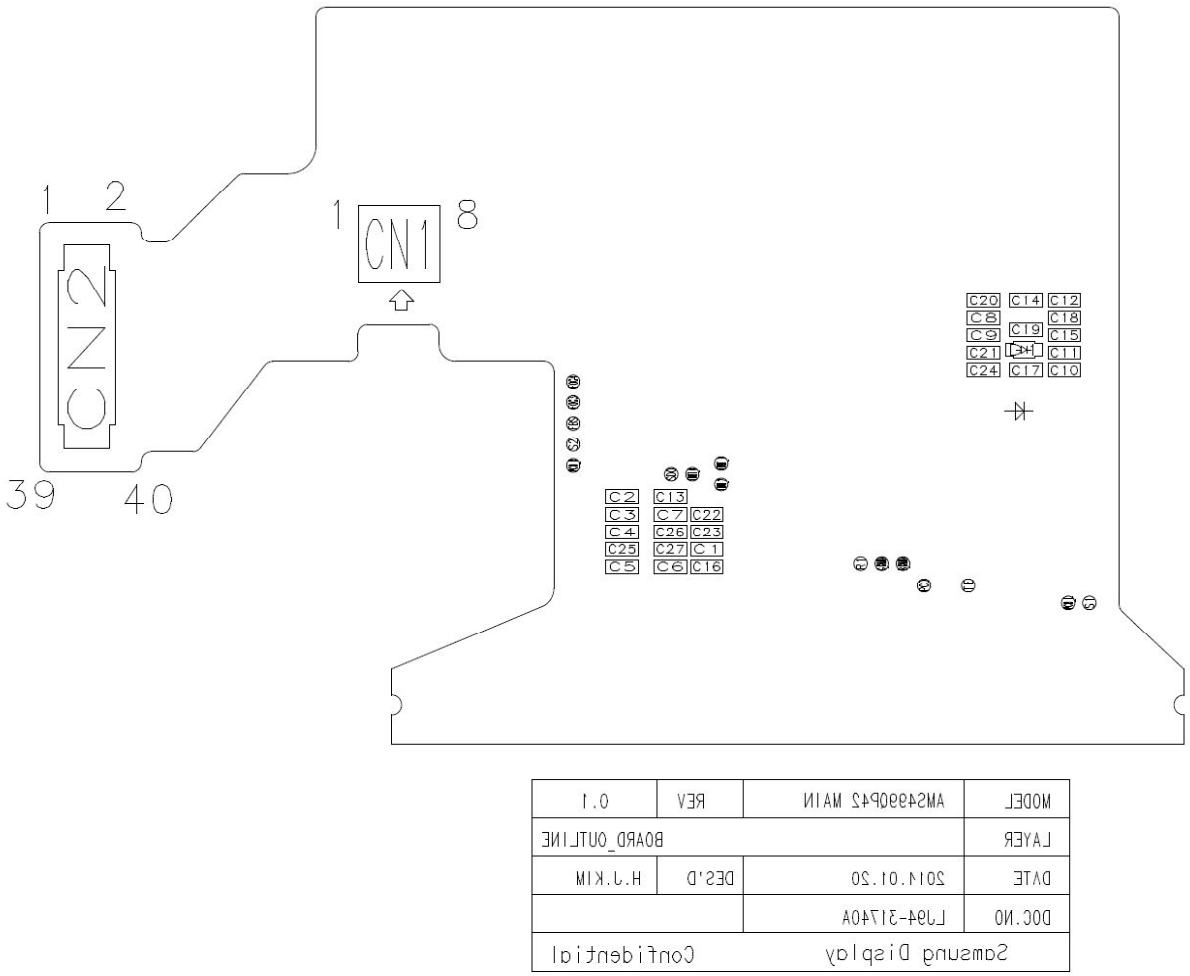
16-2-3. Main FPC Placement (Front)



MODEL	AMS499QP42 MAIN	REV	0.1
LAYER	TOP		BOARD_OUTLINE
DATE	2014.01.20	DES'D	H.J.KIM
DOC.NO	LJ94-31740A		
Samsung Display		Confidential	

이동규/12410706/국내 본사|제품개발1그룹(OLED)/119672164/20150409163744
301701428564851

16-2-4. Main FPC Placement (Rear)



MODEL	AMS499QP42 MAIN	REV	0.1
LAYER	BOARD_OUTLINE		
DATE	2014.01.20	DES'D	H.J.KIM
DOC.NO	LJ94-31740A		
Samsung Display		Confidentiol	

이동규/12410706/국내 본사|제품개발1그룹(OLED)/119672164/20150409163744
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16-3. TSP FPCB Drawing

16-3-1. TFPC Schematic Diagram

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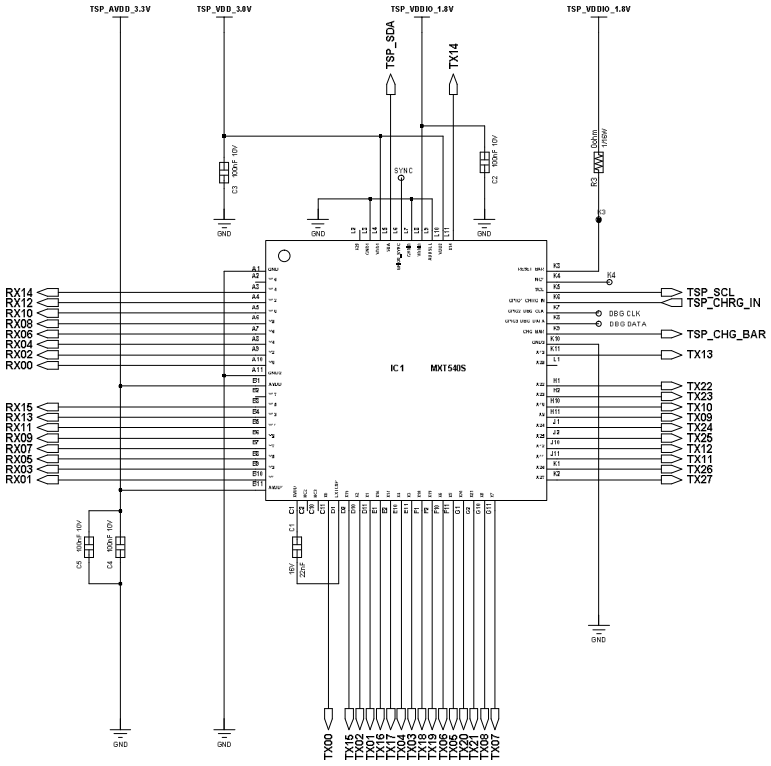
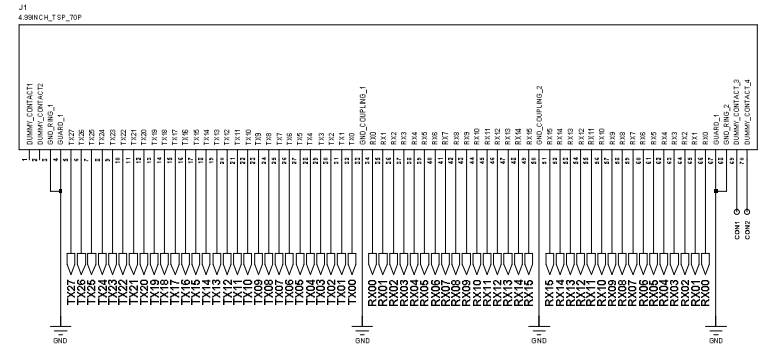
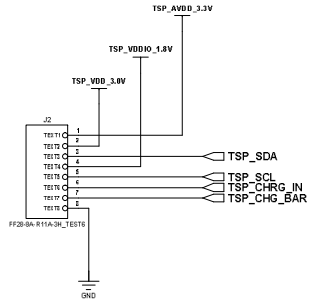
301701428564851







Changed by H.J.KIM	Date 2012.08.20	Time	Spec No.	ODS02952-000	Samsung Display
Engineer I.W.JUNG	Drawn By I.W.JUNG	R&D CHK	Part Name	ASSY FPC-TSP	
			PBA Code	LJ94-31739A	SPECIFICATION AMS499QP42_TSP_REV0.2
			Sheet	1/1 [A3]	

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김민영/12425738/Rigid제품개발그룹/1193102141/20140515094525

260751400113655

16-3-2. TSP FPC Electronic Part List

NO	CATEGORY	REFERENCE	Q'ty	SPECIFICATION	SDC CODE	MAKER
1	IC-MICROCONTROLLER	IC1	1	mXT540S,UFBGA,72Z30,6x6x0.6mm,400KHz,3.0V,-40to+85C	0903-001968	ATMEL
(대체)	IC-MICROCONTROLLER	IC1	1	mXT540S,UFBGA,72Z30,6x6x0.6mm,400KHz,3.0V,-40to+85C, FAB_MAGNACHIP	0903-001993	ATMEL
2	C-CER,CHIP	C1	1	22nF,10%,16V,X7R,TP,1005	2203-006137	NOTE 1
3	R-CHIP	R3	1	0ohm,5%,1/16W,TP,1005	2007-000171	NOTE 3
4	C-CER,CHIP	C2~C5	4	100nF,10%,10V,X5R,TP,1005	2203-005482	NOTE 2
5	FPC	FPC	1	ASM499QP42 Touch FPC	LJ41-11903A	BH-Flex

1) FPCB ASS'Y IS PB & Halogen FREE
2) NOTE 1 : DARFON, MURATA, SAMHC, SEM, SHEC, TAIYK, TAIYO, TJSEM, YAGEO
2) NOTE 2 : AVX, DARFON, DONGU, JOHNM, MURATA, MURATAB, PHYCOM, SEM, TAIYK, TAIYO, TDK,TJSEM,YAGEO
2) NOTE 3 : ABCO, ASJPTE, KOA, KOATA, KYOCE, MATSUSE, OEDQD, PSIND, ROHM, SEM, SHTEM, TAITEC, UNIROY, V0091, YAGEO

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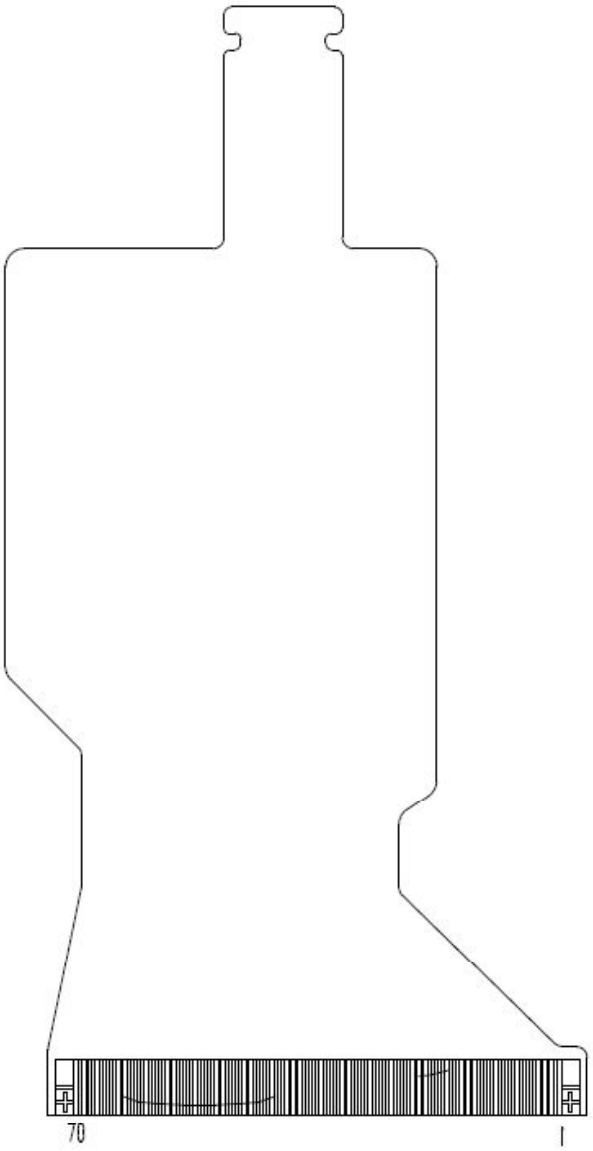
301701428564851

16-3-3. TSP FPC Placement (Front)



MODEL	AMS499QP42 TSP	REV	0.2
LAYER	TOP		BOARD_OUTLINE
DATE	2013.10.23	DES'D	M.H.KWON
DOC.NO	LJ94-31739A		
Samsung Display		Confidential	

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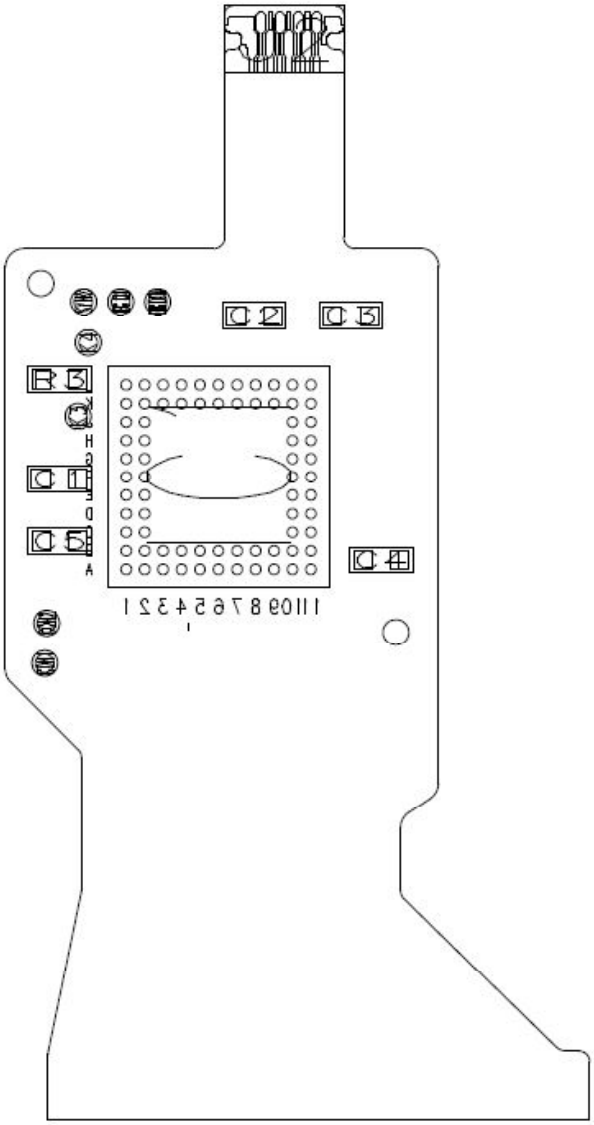
301701428564851

16-3-4. TSP FPC Placement (Rear)



MODEL	AMS499QP42 TSP	REV	0.2
LAYER	BOTTOM		BOARD_OUTLINE
DATE	2013.10.23	DES'D	M.H.KWON
DOC.NO	LJ94-31739A		
Samsung Display			Confidential

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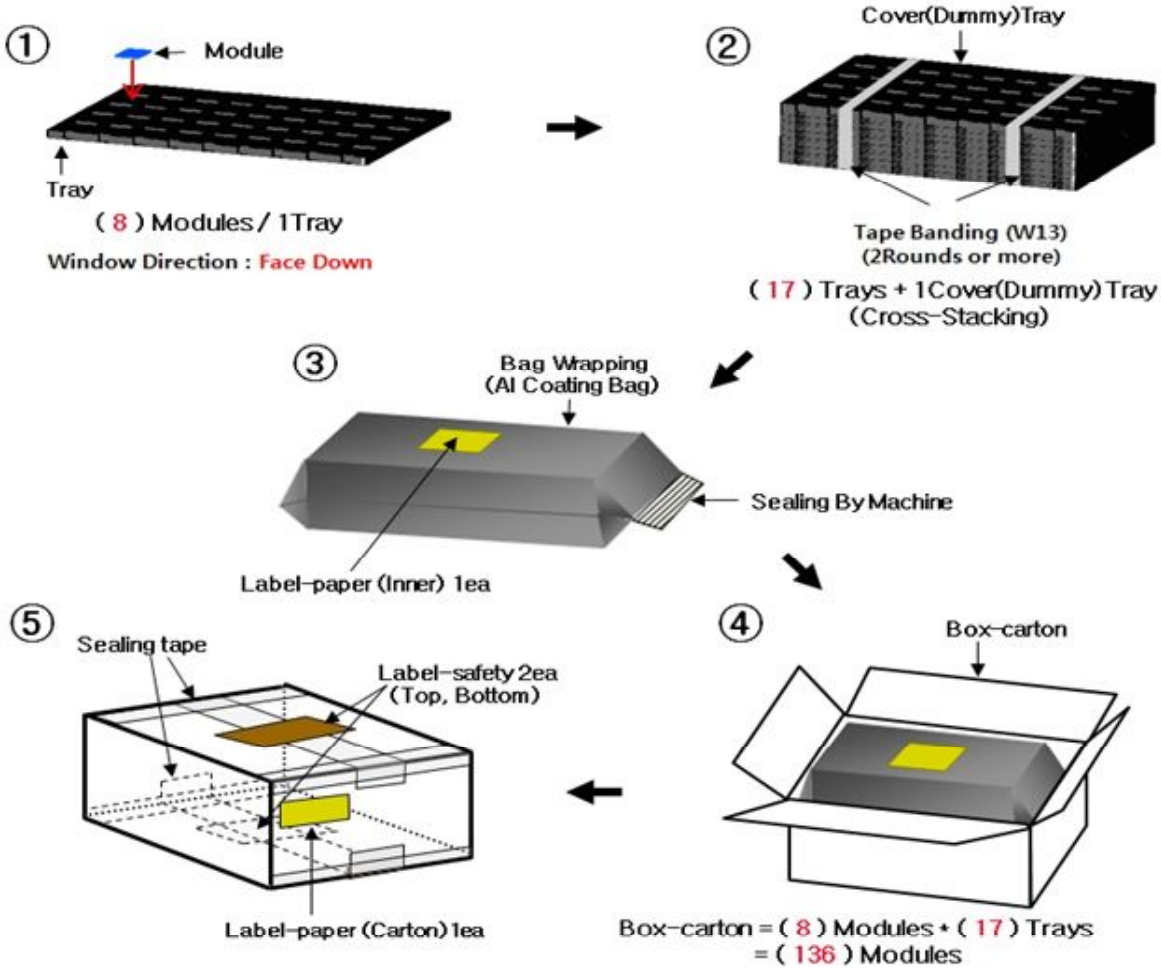
17. Packing Specification

17.1 Box Pack



Note

(1) Total :Box-carton approx. : (10)kg

(2) Size : 583(L) x 388(W) x 210(H)

(3) Place the Module in the tray facing the active area direction.

(4) Stack the trays and cover (dummy) tray.

(5) Resistance of tray surface : 106~109Ω

(6) Wrap the Al coating bag by Packing machine and affix the Label-Paper on Bag

(7) Put the bag in the Box-carton .

(8) Seal the Box-carton and affix the Label-safety & Label-paper.

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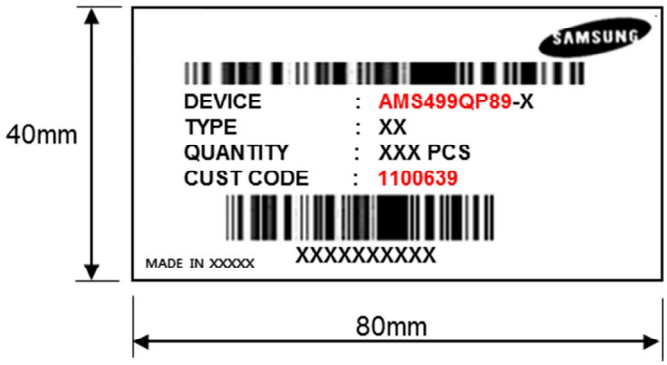
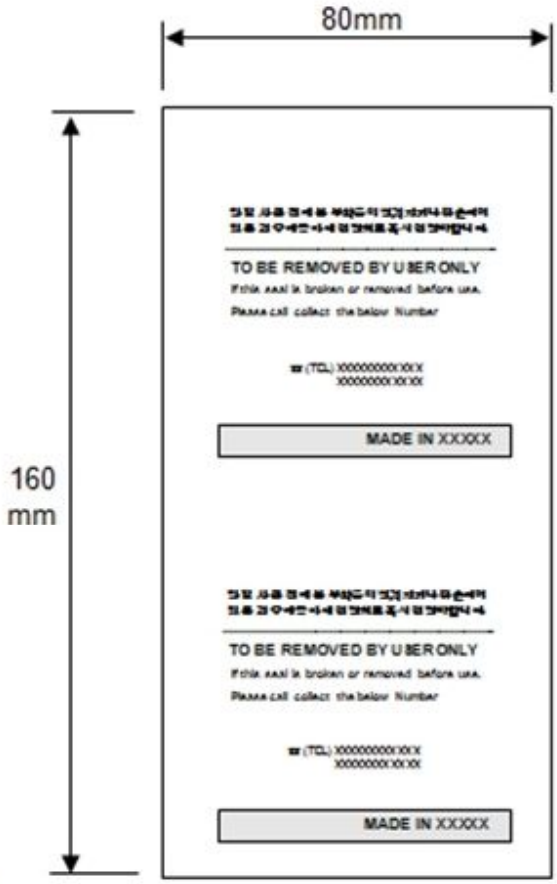
17.2 Label

* Label-paper (Inner)



* Label-paper (Carton)

* Label-safety



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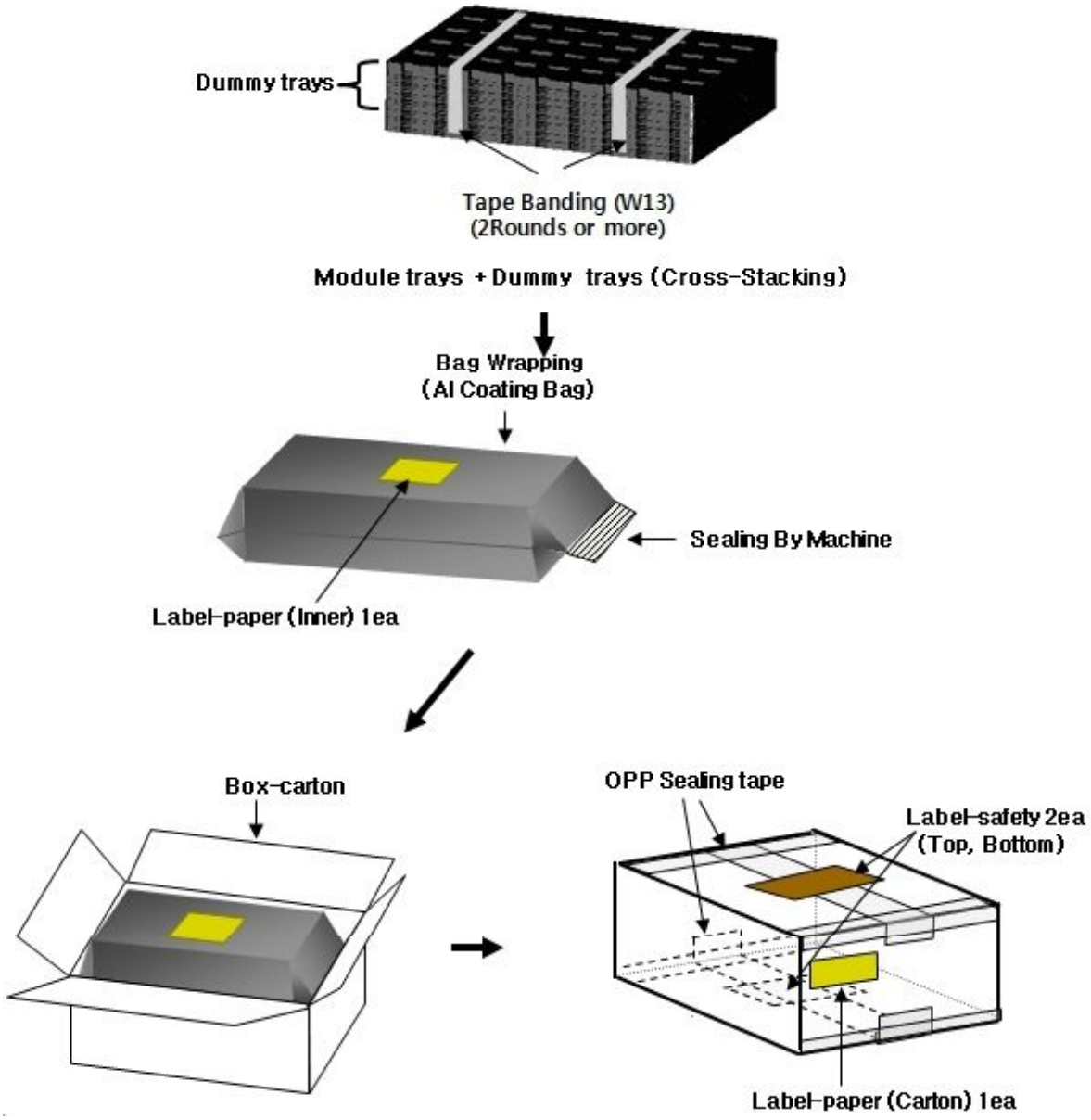
301701428564851

17.3 Packing for Small Quantities



Note

When package quantity is small, Modules containing trays are stacked the bottom, and dummy trays are stacked at the top of package,
then wrap the Al coating bag by Packing machine and affix the Label-Paper on Bag.
Put the Bag in the Box-carton
Seal the Box-carton and affix the Label-safety & Label-Paper.

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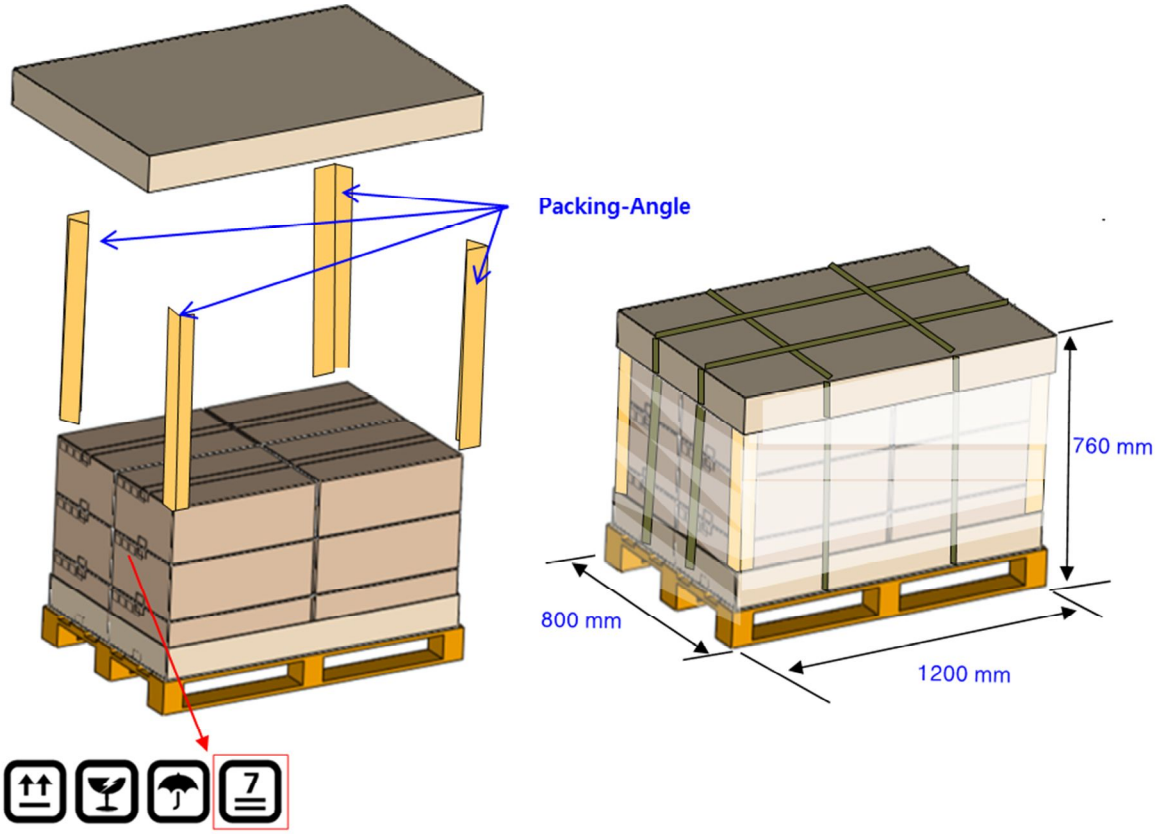
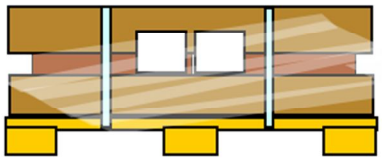
301701428564851

17.4 Over Pack

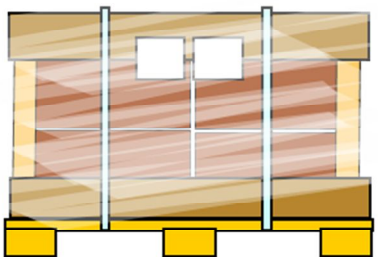


[Carton-box level : 최대 7단 적재]

17.5 Packing for Small Quantities



1 step
[Carton Box : 1~4 Box]



2 step
[Carton Box : 5~8 Box]

-. Small Quantities (1step ,2 step) must stack on the Top.

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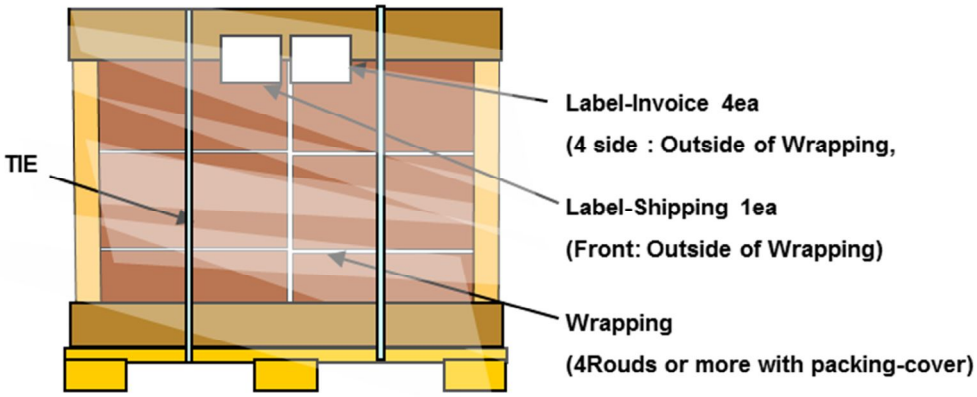
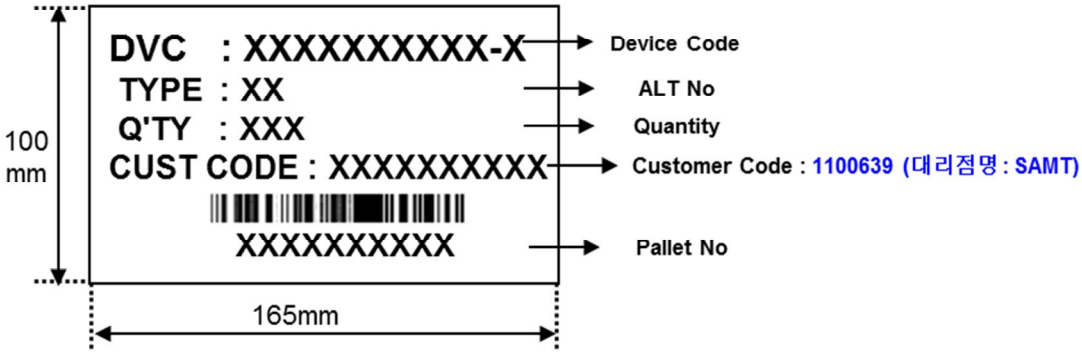
301701428564851

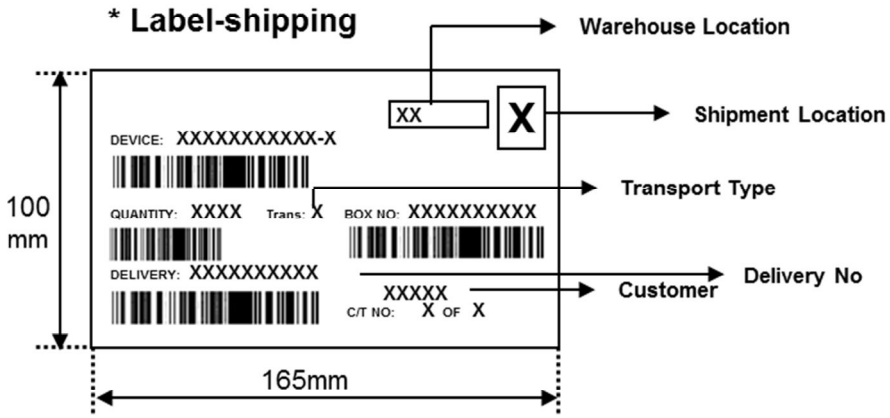
17.6 Over Pack Attach



* Label-invoice



* Label-shipping



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301701428564851

* Reference Image (Except Label and Wrap)

Carton Box		
Pallet		

Caution

For keeping Safe quality from outer exposure or contamination, modules should be consumed with in 2 months after unpacking.

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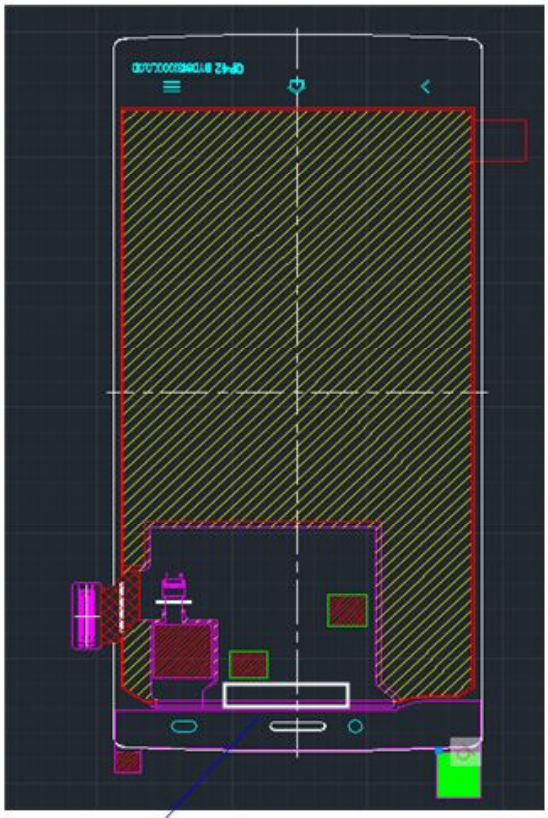
301701428564851

18. Module Marking



$S_1 \ldots S_n$
L_S L_D YYMMDD L_1L_2 V

Digit code	Description	Example
$S_1 \ldots S_n$	supplier's material code in n digits.	AMS499QP89-0
L_S	assembled site where sample was made. K: Korea, D: Dongkwan in China, T: Tenjin in China	D
L_D	assembled shift when sample was made. A: A-shift(day), B: B-shift(night), C: C-shift	A
YYMMDD	the year, month and date when sample was made. YY: year, MM: month, DD: date	150410
L_1L_2	assembled line where sample was made. 01: 1-line, 02: 2-line, ... , 99: 99-line	01
V	sample version W: W/S, E: E/S O: C/S or MP, P: PCN	O

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301701428564851