



**ISSUED DATE : 2008-08-28**

**SAMSUNG TFT-LCD PRODUCT INFORMATION**  
**MODEL : LTM230HT01**

Note : This is Product Information is subject to change after 3 months of issuing date.

Application Engineering Part 1, HD LCD Business

Samsung Electronics Co . , LTD.



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## General Description

### Description

LTM230HT01 is a color active matrix liquid crystal display (LCD) that uses amorphous silicon TFT (Thin Film Transistor) as switching components. This model is composed of a TFT LCD panel, a driver circuit and a back light unit. The resolution of a 23" is 1920 x 1080 and this model can display up to 16.7 millions colors.

### Features

- High contrast ratio, high aperture structure
- TN (Twisted Nematic) mode
- Wide Viewing Angle
- High speed response
- FHD (1920 x 1080 pixels) resolution
- Low power consumption
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface (2pixel/clock)
- Compact Size Design
- RoHS, TCO 03' compliance

### Applications

- Workstation & desktop monitors
  - Display terminals for AV application products
  - Monitors for industrial machine
- \* If the module is used to other applications besides the above, please contact SEC in advance.

## General Information

Items	Specification	Unit	Note
Pixel Pitch	0.2655(H) x 0.2655(W)	mm	
Active Display Area	509.76(H) x 286.74(V)	mm	
Surface Treatment	Haze 25% , Hard coating (3H)		
Display Colors	16.7M (Hi-FRC)	colors	
Number of Pixels	1,920 x 1,080	pixel	
Pixel Arrangement	RGB vertical stripe		
Display Mode	Normally White		
Power Consumption	TBD		
Luminance of White	300(Typ.)	cd/m <sup>2</sup>	

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**Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal (H)	533.5	534.0	534.5	mm	w/o inverter ass'y
	Vertical (V)	311.2	311.7	312.2	mm	
	Depth (D)	-	-	18.9	mm	
Weight		-	-	3,000	g	LCD module only

Note (1) Mechanical tolerance is  $\pm 0.5\text{mm}$  unless there is a special comment.

**1. Absolute Maximum Ratings**

If the condition exceeds maximum ratings, it can cause malfunction or unrecoverable damage to the device.

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	$V_{DD}$	GND-0.5	6.5	V	(1)
Data Signal	$V_{sig}$	-	5	V	
Storage temperature	$T_{STG}$	-25	60	°C	(2)
Center of Glass surface temperature (Operation)	$T_{OPR}$	0	50	°C	(2)
Shock ( non - operating )	$S_{nop}$	-	50	G	(3)(5)
Vibration ( non - operating )	$V_{nop}$	-	1.5	G	(4)(5)

Note (1)  $T_a = 25 \pm 2 \text{ }^\circ\text{C}$

- (2) Temperature and relative humidity range are shown in the figure below.
  - a. 90 % RH Max. ( $T_a \leq 39\text{ }^\circ\text{C}$ )
  - b. Maximum wet-bulb temperature at  $39\text{ }^\circ\text{C}$  or less. ( $T_a \leq 39\text{ }^\circ\text{C}$ )
  - c. No condensation
- (3) 11ms, sine wave, one time for  $\pm X, \pm Y, \pm Z$  axis
- (4) 10-300 Hz, Sweep rate 10min, 30min for X,Y,Z axis
- (5) At vibration and shock test, the fixture which holds the module to be tested has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

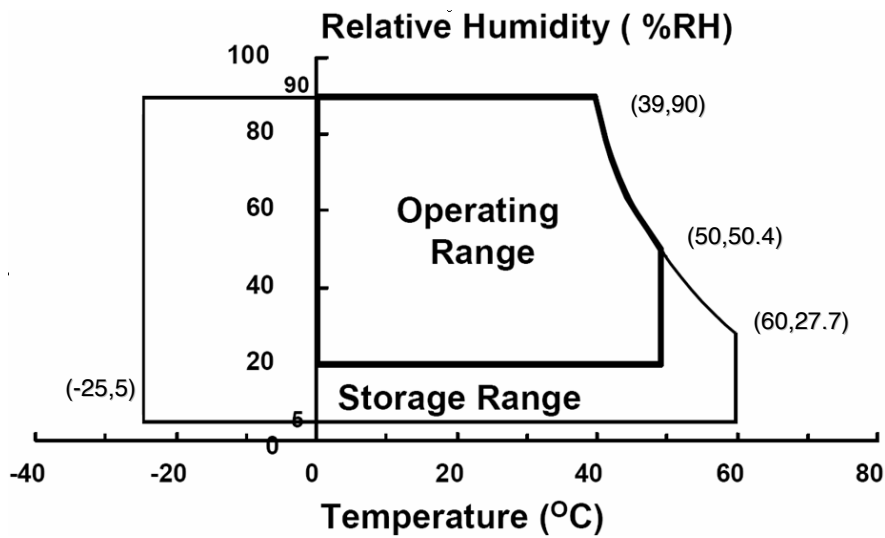


Fig. Temperature and Relative humidity range

## 2. Optical Characteristics

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The optical characteristics should be measured in a dark room or equivalent.

Measuring equipment : SR-3, RD-80S (TOPCON), EZ-Contrast (Eldim)

(Ta = 25 ± 2°C, VDD=5V, fv= 60Hz, fDCLK= 67.3 MHz, IL = 7.5mArms)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio (Center of screen)	C/R		600	1000	-		(3) SR-3	
Response Time(On/Off)	On/Off	Tr + Tf	-	5	8	msec	(5) RD-80S	
Luminance of White (Center of screen)	Y <sub>L</sub>		250	300	-	cd/m <sup>2</sup>	(6) SR-3	
Color Chromaticity (CIE 1931)	Red	Rx	0.610	0.640	0.670		(7),(8) SR-3	
		Ry	0.300	0.330	0.360			
	Green	Gx	0.270	0.300	0.330			
		Gy	0.570	0.600	0.630			
	Blue	Bx	0.120	0.150	0.180			
		By	0.030	0.060	0.090			
	White	Wx	0.283	0.313	0.343			
		Wy	0.299	0.329	0.359			
	Color Chromaticity (CIE 1976)	Red	Ru'	-	0.451	-		
			Rv'	-	0.523	-		
Green		Gu'	-	0.125	-			
		Gv'	-	0.564	-			
Blue		Bu'	-	0.175	-			
		Bv'	-	0.158	-			
White		Wu'	-	0.198	-			
		Wv'	-	0.468	-			
C.G.L (ACC ONLY)	White	Δu'v'	-	-	0.02		(9)	

\* C.G.L : Color Grayscale Linearity

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Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Temperature	-		-	6500	-	K	
Viewing Angle	Hor.	$\theta_L$	70	80	-	Degrees	(8) SR-3
		$\theta_R$	70	80	-		
	Ver.	$\theta_U$	70	80	-		
		$\theta_D$	70	80	-		
Brightness Uniformity (9 Points)	$B_{uni}$		-	-	25	%	(4) SR-3

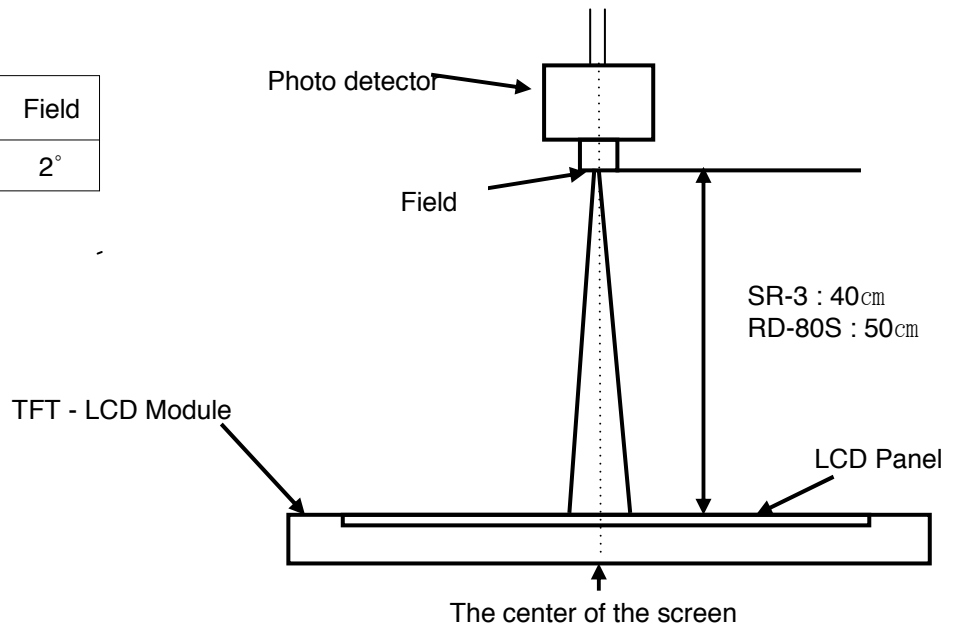
Note (1) Test Equipment Setup

The measurement should be executed in a stable, windless and dark room between 30min after lighting the back light at the given temperature for stabilization of the back light. This should be measured in the center of screen.

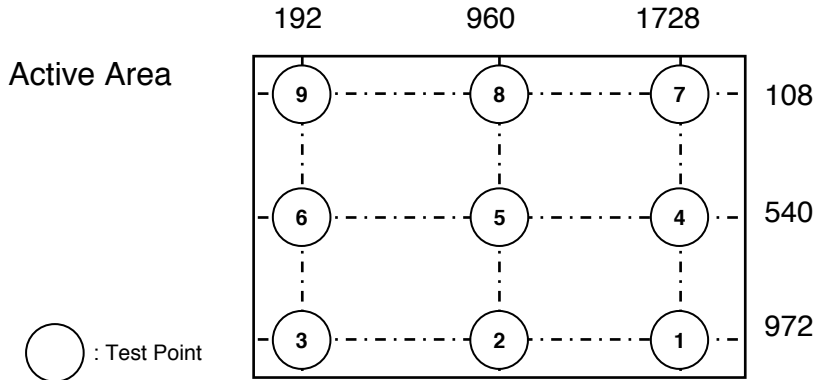
Single lamp current : 7.5mA

Environment condition :  $T_a = 25 \pm 2 \text{ }^\circ\text{C}$

Photo detector	Field
SR-3	2°



Note (2) Definition of test point



Note (3) Definition of Contrast Ratio (C/R)

: Ratio of gray max (Gmax) & gray min (Gmin) at the center point⑤ of the panel

$$CR = \frac{G_{max}}{G_{min}}$$

Gmax : Luminance with all pixels white

Gmin : Luminance with all pixels black

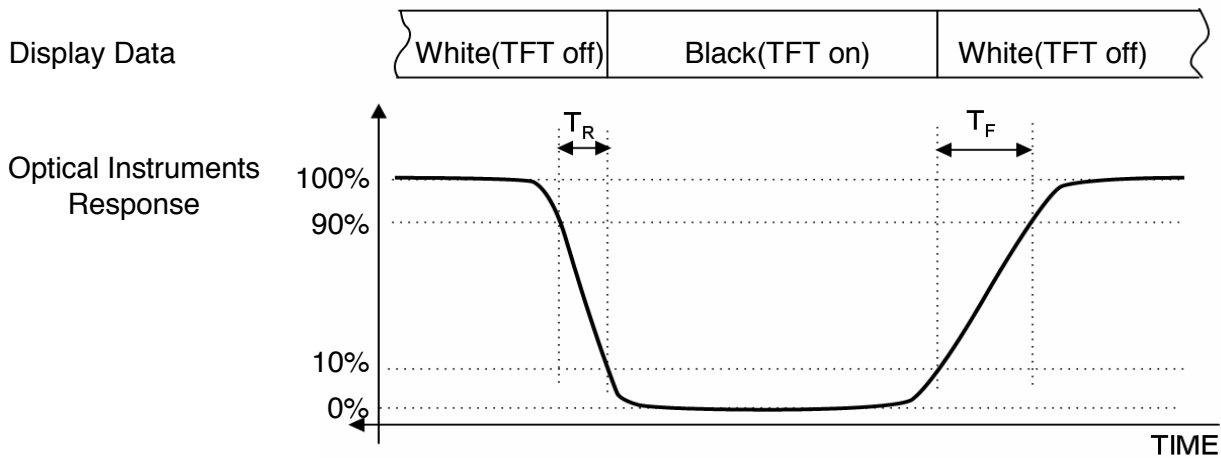
Note (4) Definition of 9 points brightness uniformity

$$Buni = 100 \times \frac{(B_{max} - B_{min})}{B_{max}}$$

Bmax : Maximum brightness

Bmin : Minimum brightness

Note (5) Definition of Response time : Sum of Tr, Tf

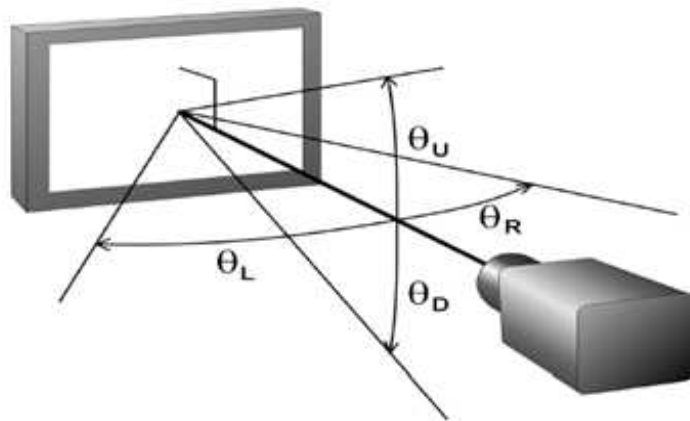




Note (6) Definition of Luminance of White : Luminance of white at center point⑤

Note (7) Definition of Color Chromaticity (CIE 1931, CIE1976)  
 Color coordinate of Red, Green, Blue & White at center point⑤

Note (8) Definition of Viewing Angle  
 : Viewing angle range ( $CR \geq 10$ )



Note (9) Color Grayscale Linearity

a. Test image : 100% full white pattern with a test pattern as below

b. Test pattern : Squares, 40mm by 40mm in size, filled with 255, 225, 195, 165, 135 and 105 grays steps should be arranged at the center⑤ of the screen.



c. Test method

-1<sup>st</sup> gray step : move a square of 255 gray level should be moved into the center of the screen and measure luminance and  $u'$  and  $v'$  coordinates.

- Next gray step : Move a 225 gray square into the center and measure both luminance and coordinates, too.

d. Test evaluation

$$\Delta u' v' = \sqrt{(u'_A - u'_B)^2 + (v'_A - v'_B)^2}$$

Where A, B : 2 gray levels found to have the largest color differences between them

i.e. get the largest  $\Delta u'$  and  $\Delta v'$  of each 6 pair of  $u'$  and  $v'$  and calculate the  $\Delta u'v'$ .

### 3. Electrical Characteristics

#### 3.1 TFT LCD Module

The connector for display data & timing signal should be connected.

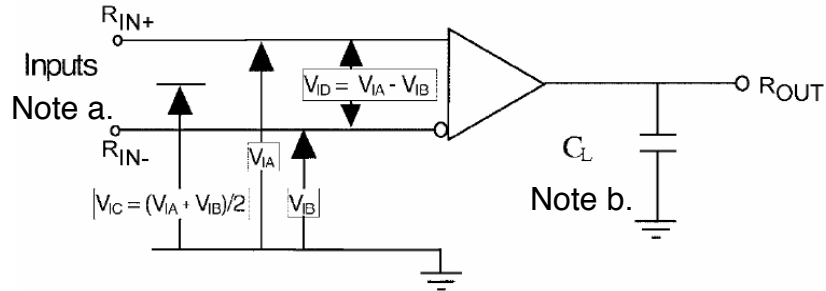
Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Voltage of Power Supply	V <sub>DD</sub>	4.5	5.0	5.5	V	(1)	
LVDS Input Characteristics	Differential Input Voltage for LVDS Receiver Threshold	High	-	-	+100	mV	(2)
		Low	-100	-	-	mV	
	LVDS skew	t <sub>SKEW</sub>	-300		300	ps	(3)
	Differential input voltage	V <sub>ID</sub>	200		600	mV	(4)
	Input voltage range (single-ended)	V <sub>IN</sub>	0		2.4	V	(4)
	Common mode voltage	V <sub>CM</sub>	0+  V <sub>ID</sub>  /2	1.2	2.4-  V <sub>ID</sub>  /2	V	(4)
Current of Power Supply	(a) Black	I <sub>DD</sub>	-	1,600	-	mA	(5),(6)
	(b) White		-	1,100	-	mA	
	(c) Dot		-	1,800	2,200	mA	
Vsync Frequency	f <sub>V</sub>	49.0	59.9	75.1	Hz		
Hsync Frequency	f <sub>H</sub>	54.2	66.0	83.8	kHz		
Main Frequency	f <sub>DCLK</sub>	56.4	67.3	83.0	MHz		
Rush Current	I <sub>RUSH</sub>	-	-	5.0	A	(7)	

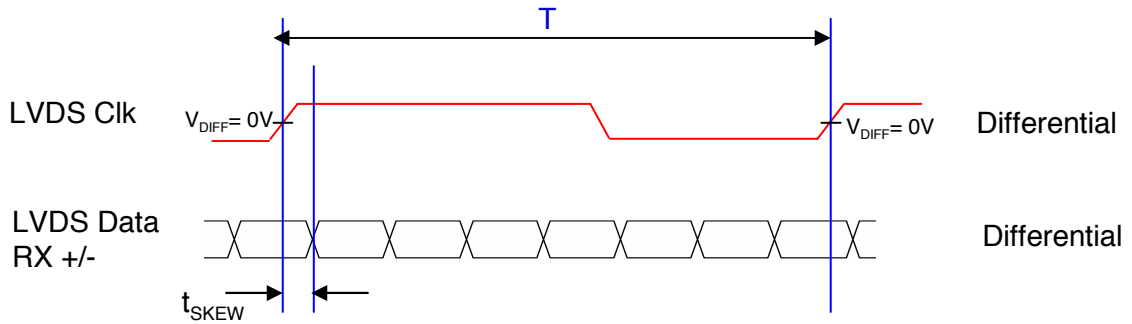
Note (1) The ripple voltage should be controlled under 10% of V<sub>DD</sub>.

(2) Differential receiver voltage definitions and propagation delay and transition time test circuit

- a. All input pulses have frequency = 10MHz,  $t_R$  or  $t_F=1ns$
- b.  $C_L$  includes all probe and fixture capacitance



(3) LVDS Receiver DC parameters are measured under static and steady conditions which may not be reflective of its performance in the end application.

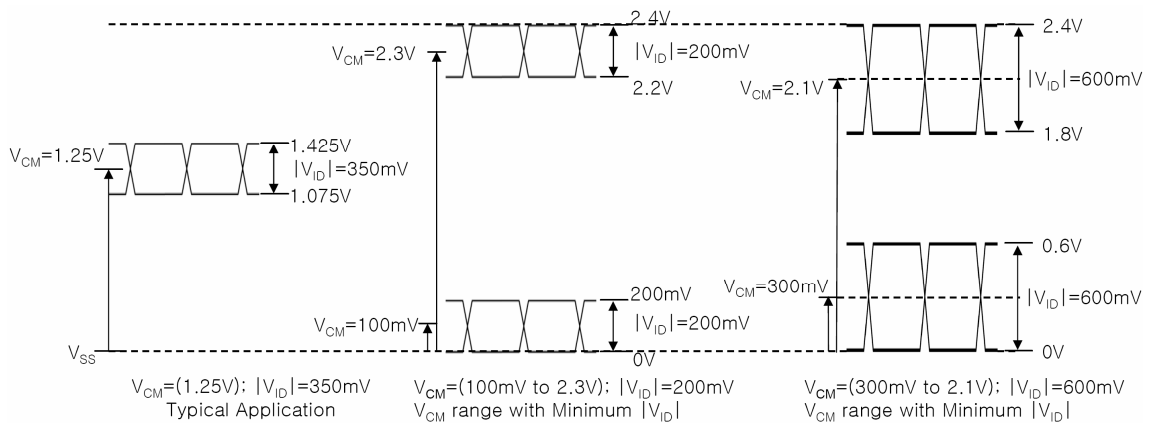


where  $t_{skew}$  : skew between LVDS clock & LVDS data,

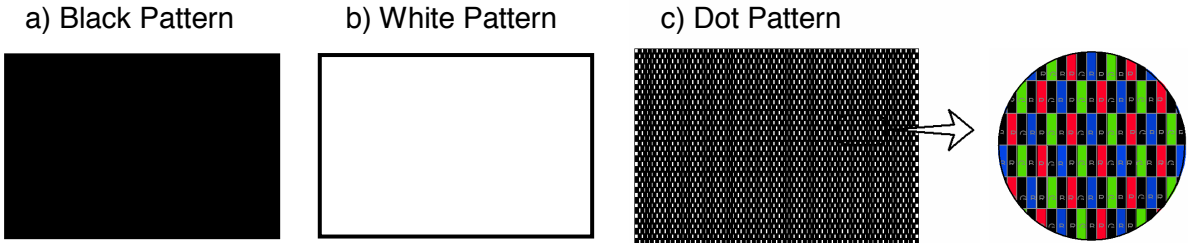
$T$  : 1 period time of LVDS clock

cf) (-/+) of 300psec means LVDS data goes before or after LVDS clock.

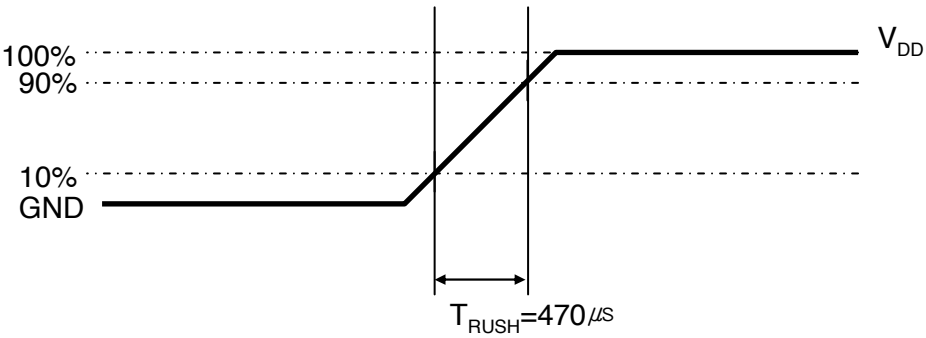
(4) Definition of  $V_{ID}$  and  $V_{CM}$  using single-end signals



(5)  $f_V=60\text{Hz}$ ,  $f_{\text{DCLK}} = 67.3 \text{ MHz}$ ,  $V_{\text{DD}} = 5.0\text{V}$ , DC Current.  
(6) Power dissipation check pattern (LCD Module only)



(7) Measurement Condition



Rush Current  $I_{\text{RUSH}}$  can be measured when  $T_{\text{RUSH}}$  is  $470\mu\text{s}$ .

### 3.2 Back Light Unit

The back light unit is an edge - lighting type with 2 dual CCFTs ( Cold Cathode Fluorescent Tube ) The characteristics of two dual lamps are shown in the following tables.

Ta=25 ± 2°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Lamp Current	I <sub>L</sub>	4.0	7.5	8.0	mArms	(1)	
Lamp Voltage	V <sub>L</sub>	-	850	-	Vrms		
Lamp Frequency	f <sub>L</sub>	40	-	80	kHz	(2)	
Operating Life Time	Hr	50,000	-	-	Hour	(3)	
Inverter waveform	Asymmetry rate	Wasy	-	-	10	%	(4)
	Distortion rate	Wdis	1.2726	1.414	1.5554		
Startup Voltage	Vs	-	-	0°C : 1,840	Vrms	(5)	
				25°C : 1,450			

Note (1) Specified values are for a single lamp.

Lamp current is measured with current meter for high frequency as shown below.  
Refer to the following block diagram of the back light unit for more information.

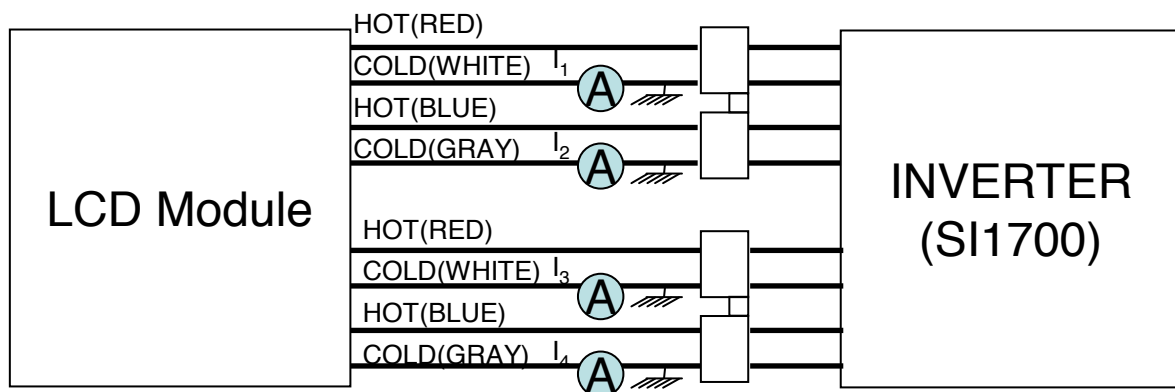


Fig. Measurement point of Lamp Current

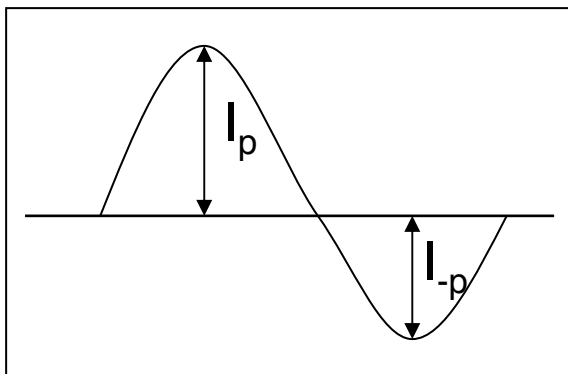
(2) Lamp frequency which may produce interference with horizontal synchronous frequency may cause line flow on the display. Therefore lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.

(3) Life time (Hr) is defined as the time when brightness of a lamp unit itself becomes 50% or less than its original value at the condition of  $T_a = 25 \pm 2^\circ\text{C}$  and  $I_L = 7.5\text{mA}_{rms}$

(4) Designing a system inverter intended to have better display performance, power efficiency and lamp reliability.

They would help increase the lamp lifetime and reduce leakage current.

- a. The measurement should be done at typical lamp current.
- b. The asymmetry rate of the inverter waveform should be less than 10%.
- c. The distortion rate of the waveform should be  $\sqrt{2}$  with  $\pm 10\%$  tolerance.
  - Inverter output waveform had better be more similar to ideal sine wave.



**Fig. Wave form of the inverter**

- Asymmetry rate

$$\frac{|I_p - I_{-p}|}{I_{rms}} \times 100$$

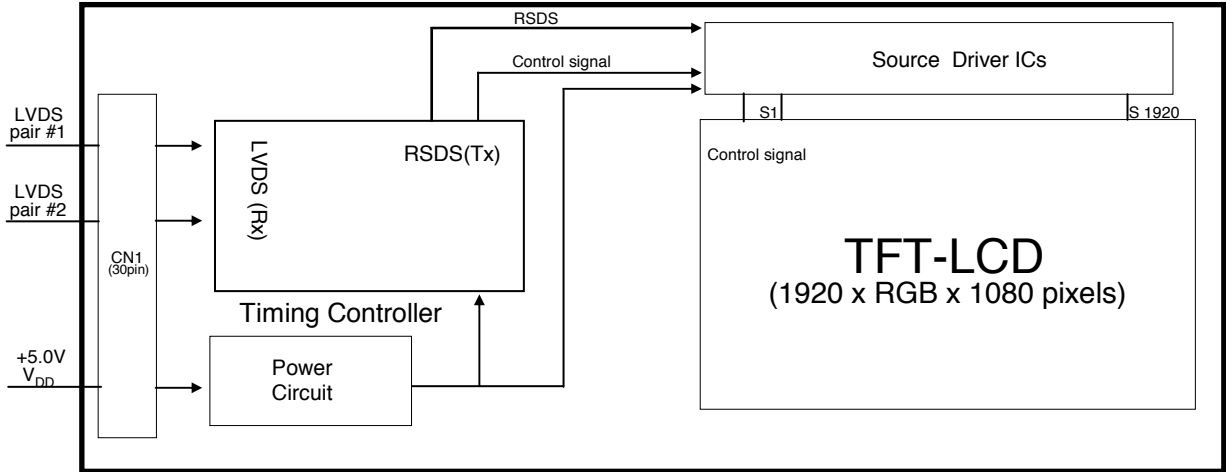
- Distortion rate

$$\left| \frac{I_p}{I_{rms}} \right| \text{ or } \left| \frac{I_{-p}}{I_{rms}} \right|$$

(5) If an inverter has shutdown function, it should keep its output for over 1 second even if the lamp connector is open. Otherwise the lamps may not be turned on.

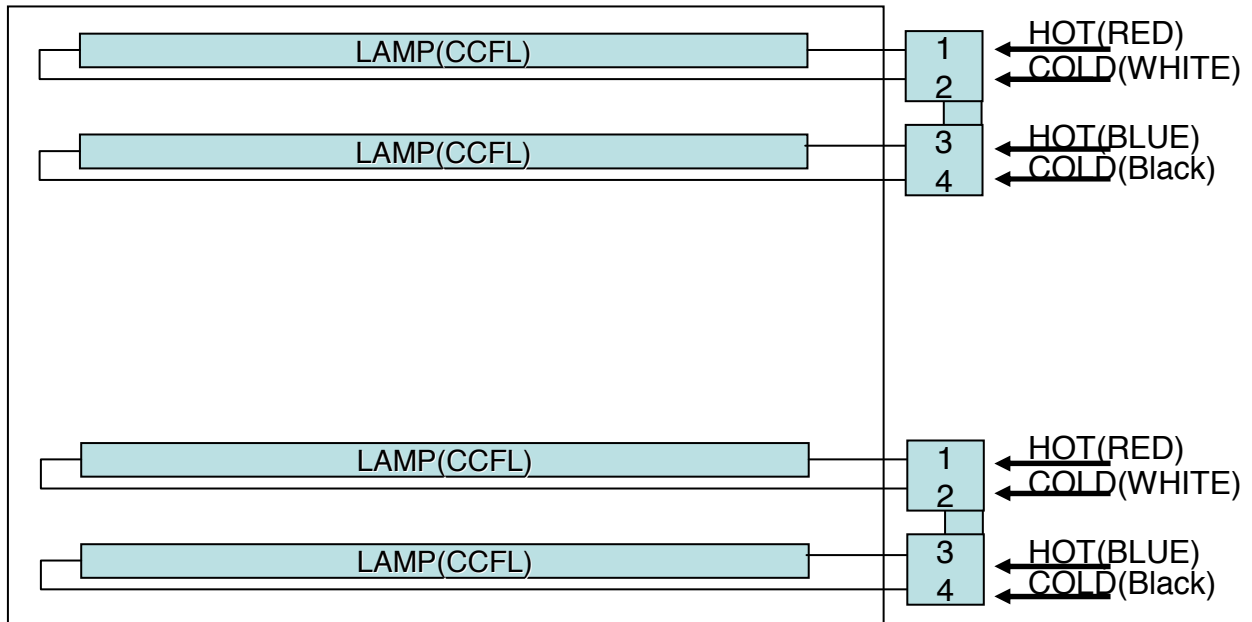
## 4. BLOCK DIAGRAM

### 4.1 TFT LCD Module



### 4.2 Back Light Unit

Connector : YEON-HO 35001HS-04L





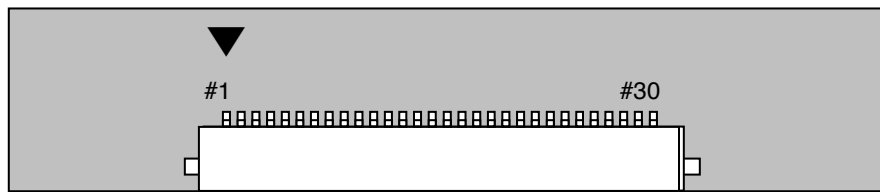
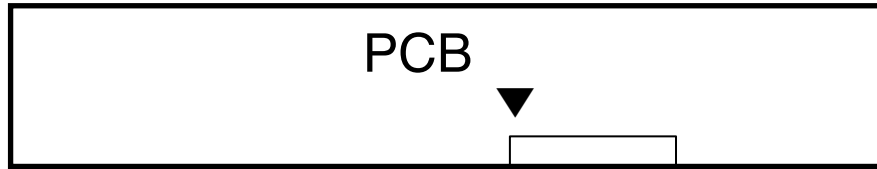
## 5. Input Terminal Pin Assignment

### 5.1. Input Signal & Power ( Connector : UJU IS100-L300-C23 or Compatible )

PIN NO	SYMBOL	FUNCTION
1	RXO0N	Negative LVDS differential data output
2	RXO0P	Positive LVDS differential data output
3	RXO1N	Negative LVDS differential data output
4	RXO1P	Positive LVDS differential data output
5	RXO2N	Negative LVDS differential data output
6	RXO2P	Positive LVDS differential data output
7	GND	Ground
8	RXOC-	Negative Sampling Clock (ODD data)
9	RXOC+	Positive Sampling Clock (ODD data)
10	RXO3N	Negative LVDS differential data output
11	RXO3P	Positive LVDS differential data output
12	RXE0N	Negative LVDS differential data output
13	RXE0P	Positive LVDS differential data output
14	GND	Ground
15	RXE1N	Negative LVDS differential data output
16	RXE1P	Positive LVDS differential data output
17	GND	Ground
18	RXE2N	Negative LVDS differential data output
19	RXE2P	Positive LVDS differential data output
20	RXEC-	Negative Sampling Clock (EVEN data)
21	RXEC+	Positive Sampling Clock (EVEN data)
22	RXE3N	Negative LVDS differential data output
23	RXE3P	Positive LVDS differential data output
24	GND	Ground
25	NC	* CE (For LCD internal use only. Do not connect)
26	NC	* CTL (For LCD internal use only. Do not connect)
27	NC	No Connection
28	VDD	Power Supply : +5V
29	VDD	
30	VDD	

\* If the system already uses the 25, 26pins, it should keep under GND level  
The voltage applied to those pins should not exceed -200mV.

Note) Pin number starts from Left side



UJU IS100-L300-C23 or Compatible



**Fig. Connector diagram**

- a. All GND pins should be connected together and also be connected to the LCD's metal chassis.
- b. All power input pins should be connected together.
- c. All NC pins should be separated from other signal or power.

## 5.2 LVDS Interface (1)

### 5.2.1 Odd Pixel Data (1st pixel data)

LVDS Transmitter ( <b>DS90C383</b> , <b>DS90C385</b> ) Signal Interface						
Device Input Pin		Device Input Signal		Output Signal	To LTM230HT01 Interface ( CN101 )	
No	Symbol	Symbol	Function		Terminal	Symbol
51	TXIN0	RO0	Red Odd Pixel Data (LSB)	TXOUT0- TXOUT0+	No. 1 No. 2	RXO0- RXO0+
52	TXIN1	RO1	Red Odd Pixel Data			
54	TXIN2	RO2	Red Odd Pixel Data			
55	TXIN3	RO3	Red Odd Pixel Data			
56	TXIN4	RO4	Red Odd Pixel Data			
2	TXIN5	RO7	Red Odd Pixel Data (MSB)	TXOUT3- TXOUT3+	No. 10 No. 11	RXO3- RXO3+
3	TXIN6	RO5	Red Odd Pixel Data	TXOUT0- TXOUT0+	No. 1 No. 2	RXO0- RXO0+
4	TXIN7	GO0	Green Odd Pixel Data (LSB)			
6	TXIN8	GO1	Green Odd Pixel Data	TXOUT1- TXOUT1+	No. 3 No. 4	RXO1- RXO1+
7	TXIN9	GO2	Green Odd Pixel Data			
8	TXIN10	GO6	Green Odd Pixel Data	TXOUT3- TXOUT3+	No. 10 No. 11	RXO3- RXO3+
10	TXIN11	GO7	Green Odd Pixel Data (MSB)			
11	TXIN12	GO3	Green Odd Pixel Data	TXOUT1- TXOUT1+	No. 3 No. 4	RXO1- RXO1+
12	TXIN13	GO4	Green Odd Pixel Data			
14	TXIN14	GO5	Green Odd Pixel Data			
15	TXIN15	BO0	Blue Odd Pixel Data (LSB)			
16	TXIN16	BO6	Blue Odd Pixel Data	TXOUT3- TXOUT3+	No. 10 No. 11	RXO3- RXO3+
18	TXIN17	BO7	Blue Odd Pixel Data (MSB)			
19	TXIN18	BO1	Blue Odd Pixel Data	TXOUT1- TXOUT1+	No. 3 No. 4	RXO1- RXO1+
20	TXIN19	BO2	Blue Odd Pixel Data	TXOUT2- TXOUT2+	No. 5 No. 6	RXO2- RXO2+
22	TXIN20	BO3	Blue Odd Pixel Data			
23	TXIN21	BO4	Blue Odd Pixel Data			
24	TXIN22	BO5	Blue Odd Pixel Data			
50	TXIN27	RO6	Red Odd Pixel Data	TXOUT3- TXOUT3+	No. 10 No. 11	RXO3- RXO3+

5.2.2 Even Pixel Data (2nd pixel data)

LVDS Transmitter ( DS90C383, DS90C385 ) Signal Interface						
Device Input Pin		Device Input Signal		Output Signal	To LTM230HT01 Interface ( CN101 )	
No	Symbol	Symbol	Function		Terminal	Symbol
51	TXIN0	RE0	Red Even Pixel Data (LSB)	TXOUT0- TXOUT0+	No. 12 No. 13	RXE0- RXE0+
52	TXIN1	RE1	Red Even Pixel Data			
54	TXIN2	RE2	Red Even Pixel Data			
55	TXIN3	RE3	Red Even Pixel Data			
56	TXIN4	RE4	Red Even Pixel Data			
2	TXIN5	RE7	Red Even Pixel Data (MSB)	TXOUT3- TXOUT3+	No. 22 No. 23	RXE3- RXE3+
3	TXIN6	RE5	Red Even Pixel Data	TXOUT0- TXOUT0+	No. 12 No. 13	RXE0- RXE0+
4	TXIN7	GE0	Green Even Pixel Data (LSB)			
6	TXIN8	GE1	Green Even Pixel Data	TXOUT1- TXOUT1+	No. 15 No. 16	RXE1- RXE1+
7	TXIN9	GE2	Green Even Pixel Data			
8	TXIN10	GE6	Green Even Pixel Data	TXOUT3- TXOUT3+	No. 22 No. 23	RXE3- RXE3+
10	TXIN11	GE7	Green Even Pixel Data (MSB)			
11	TXIN12	GE3	Green Even Pixel Data	TXOUT1- TXOUT1+	No. 15 No. 16	RXE1- RXE1+
12	TXIN13	GE4	Green Even Pixel Data			
14	TXIN14	GE5	Green Even Pixel Data			
15	TXIN15	BE0	Blue Even Pixel Data (LSB)	TXOUT3- TXOUT3+	No. 22 No. 23	RXE3- RXE3+
16	TXIN16	BE6	Blue Even Pixel Data			
18	TXIN17	BE7	Blue Even Pixel Data (MSB)			
19	TXIN18	BE1	Blue Even Pixel Data	TXOUT1- TXOUT1+	No. 15 No. 16	RXE1- RXE1+
20	TXIN19	BE2	Blue Even Pixel Data	TXOUT2- TXOUT2+	No. 18 No. 19	RXE2- RXE2+
22	TXIN20	BE3	Blue Even Pixel Data			
23	TXIN21	BE4	Blue Even Pixel Data			
24	TXIN22	BE5	Blue Even Pixel Data			
50	TXIN27	RE6	Red Even Pixel Data	TXOUT3- TXOUT3+	No. 22 No. 23	RXE3- RXE3+

5.2 LVDS Interface (2)

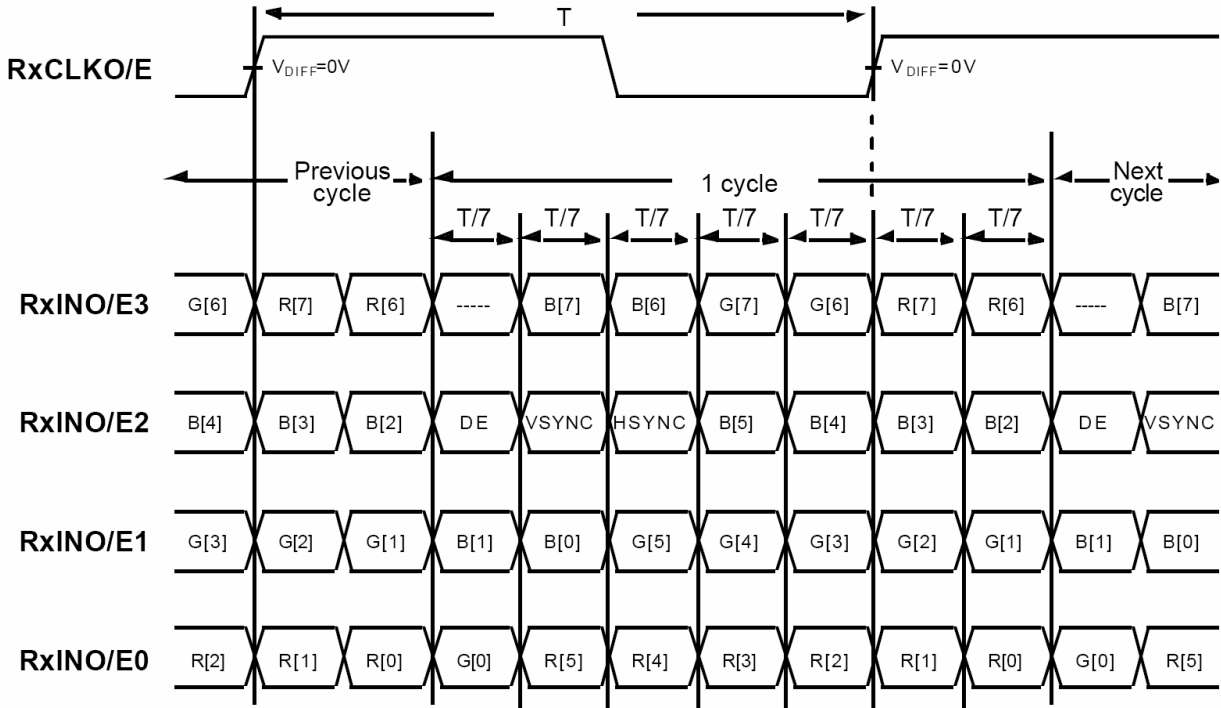
5.2.3 Odd Pixel Data (1st pixel data)

LVDS Transmitter ( <b>DS90C387</b> ) Signal Interface						
Device Input Pin		Device Input Signal		Output Signal	To LTM230HT01 Interface ( CN101 )	
No	Symbol	Symbol	Function		Terminal	Symbol
10	R10	RO0	Red Odd Pixel Data (LSB)	A0M A0P	No. 1 No. 2	RXO0- RXO0+
9	R11	RO1	Red Odd Pixel Data			
8	R12	RO2	Red Odd Pixel Data			
7	R13	RO3	Red Odd Pixel Data			
6	R14	RO4	Red Odd Pixel Data			
3	R17	RO7	Red Odd Pixel Data (MSB)	A3M A3P	No. 10 No. 11	RXO3- RXO3+
5	R15	RO5	Red Odd Pixel Data	A0M A0P	No. 1 No. 2	RXO0- RXO0+
2	G10	GO0	Green Odd Pixel Data (LSB)			
1	G11	GO1	Green Odd Pixel Data	A1M A1P	No. 3 No. 4	RXO1- RXO1+
100	G12	GO2	Green Odd Pixel Data			
94	G16	GO6	Green Odd Pixel Data	A3M A3P	No. 10 No. 11	RXO3- RXO3+
93	G17	GO7	Green Odd Pixel Data (MSB)			
99	G13	GO3	Green Odd Pixel Data	A1M A1P	No. 3 No. 4	RXO1- RXO1+
96	G14	GO4	Green Odd Pixel Data			
95	G15	GO5	Green Odd Pixel Data			
92	B10	BO0	Blue Odd Pixel Data (LSB)	A3M A3P	No. 10 No. 11	RXO3- RXO3+
86	B16	BO6	Blue Odd Pixel Data			
85	B17	BO7	Blue Odd Pixel Data (MSB)			
91	B11	BO1	Blue Odd Pixel Data	A1M A1P	No. 3 No. 4	RXO1- RXO1+
90	B12	BO2	Blue Odd Pixel Data	A2M A2P	No. 5 No. 6	RXO2- RXO2+
89	B13	BO3	Blue Odd Pixel Data			
88	B14	BO4	Blue Odd Pixel Data			
87	B15	BO5	Blue Odd Pixel Data	A3M A3P	No. 10 No. 11	RXO3- RXO3+
4	R16	RO6	Red Odd Pixel Data			

5.2.4 Even Pixel Data (2nd pixel data)

LVDS Transmitter ( <b>DS90C387</b> ) Signal Interface						
Device Input Pin		Device Input Signal		Output Signal	To LTM230HT01 Interface ( CN101 )	
No	Symbol	Symbol	Function		Terminal	Symbol
84	R20	RE0	Red Even Pixel Data (LSB)	A4M A4P	No. 12 No. 13	RXE0- RXE0+
81	R21	RE1	Red Even Pixel Data			
80	R22	RE2	Red Even Pixel Data			
79	R23	RE3	Red Even Pixel Data			
78	R24	RE4	Red Even Pixel Data			
75	R27	RE7	Red Even Pixel Data (MSB)	A7M A7P	No. 22 No. 23	RXE3- RXE3+
77	R25	RE5	Red Even Pixel Data	A4M A4P	No. 12 No. 13	RXE0- RXE0+
74	G20	GE0	Green Even Pixel Data (LSB)			
73	G21	GE1	Green Even Pixel Data	A5M A5P	No. 15 No. 16	RXE1- RXE1+
72	G22	GE2	Green Even Pixel Data			
66	G26	GE6	Green Even Pixel Data	A7M A7P	No. 22 No. 23	RXE3- RXE3+
65	G27	GE7	Green Even Pixel Data (MSB)			
71	G23	GE3	Green Even Pixel Data	A5M A5P	No. 15 No. 16	RXE1- RXE1+
70	G24	GE4	Green Even Pixel Data			
69	G25	GE5	Green Even Pixel Data			
64	B20	BE0	Blue Even Pixel Data (LSB)	A7M A7P	No. 22 No. 23	RXE3- RXE3+
58	B26	BE6	Blue Even Pixel Data			
57	B27	BE7	Blue Even Pixel Data (MSB)			
63	B21	BE1	Blue Even Pixel Data	A5M A5P	No. 15 No. 16	RXE1- RXE1+
62	B22	BE2	Blue Even Pixel Data	A6M A6P	No. 18 No. 19	RXE2- RXE2+
61	B23	BE3	Blue Even Pixel Data			
60	B24	BE4	Blue Even Pixel Data			
59	B25	BE5	Blue Even Pixel Data			
76	R26	RE6	Red Even Pixel Data	A7M A7P	No. 22 No. 23	RXE3- RXE3+

5.2.5 Timing Diagrams of LVDS For Transmitting  
 LVDS Receiver : Integrated T-CON



5.3 Back Light Unit

	Pin No.	Input	Color	Function
Upper	1	Hot1	RED	High Voltage
	2	Cold1	White	Ground
	-			
	3	Hot2	Blue	High Voltage
	4	Cold2	Gray	Ground
Lower	1	Hot1	RED	High Voltage
	2	Cold1	White	Ground
	-			
	3	Hot2	Blue	High Voltage
	4	Cold2	Gray	Ground
	Connect or Part No.	YEON-HO 35001HS-04L		



5.3 Input Signals, Basic Display Colors and Gray Scale of Each Color

COLOR	DISPLAY (8bit)	DATA SIGNAL																												GRAY SCALE LEVEL
		RED								GREEN								BLUE												
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7					
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	-		
	GREEN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	-		
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-		
	RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	-		
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	-		
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-		
GRAY SCALE OF RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0		
	DARK ↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1		
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2		
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~R252		
	LIGHT ↓	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:			
		1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R253		
	RED	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R254		
RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R255			
GRAY SCALE OF GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0		
	DARK ↑	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G1		
		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G2		
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G252		
	LIGHT ↓	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:			
		0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	G253		
	GREEN	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	G254		
GREEN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	G255			
GRAY SCALE OF BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0		
	DARK ↑	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	B1		
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	B2		
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B252		
	LIGHT ↓	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:			
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	B253		
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	B254		
BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	B255			

Note (1) Definition of Gray :  
 Rn : Red Gray, Gn : Green Gray, Bn : Blue Gray (n = Gray level)  
 Input Signal : 0 = Low level voltage, 1 = High level voltage

## 6. Interface Timing

### 6.1 Timing Parameters ( DE only mode )

SIGNAL	ITEM	SYMBOL	MIN.	TYP.	MAX.	Unit	NOTE
Clock	Frequency	$1/T_C$	56.4	67.3	83.0	MHz	-
Hsync		$F_H$	54.2	66	83.8	kHz	-
Vsync		$F_V$	49	59.9	75.1	Hz	-
Vertical Display Term	Active Display Period	$T_{VD}$	1080	1080	1080	Lines	-
	Vertical Total	$T_V$	1105	1111	1118	Lines	-
Horizontal Display Term	Active Display Period	$T_{HD}$	960	960	960	Clocks	2pixel/clock
	Horizontal Total	$T_H$	990	1010	1040	clocks	2pixel/clock

Note (1) This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

(2) Test Point : TTL control signal and CLK at LVDS Tx input terminal in system

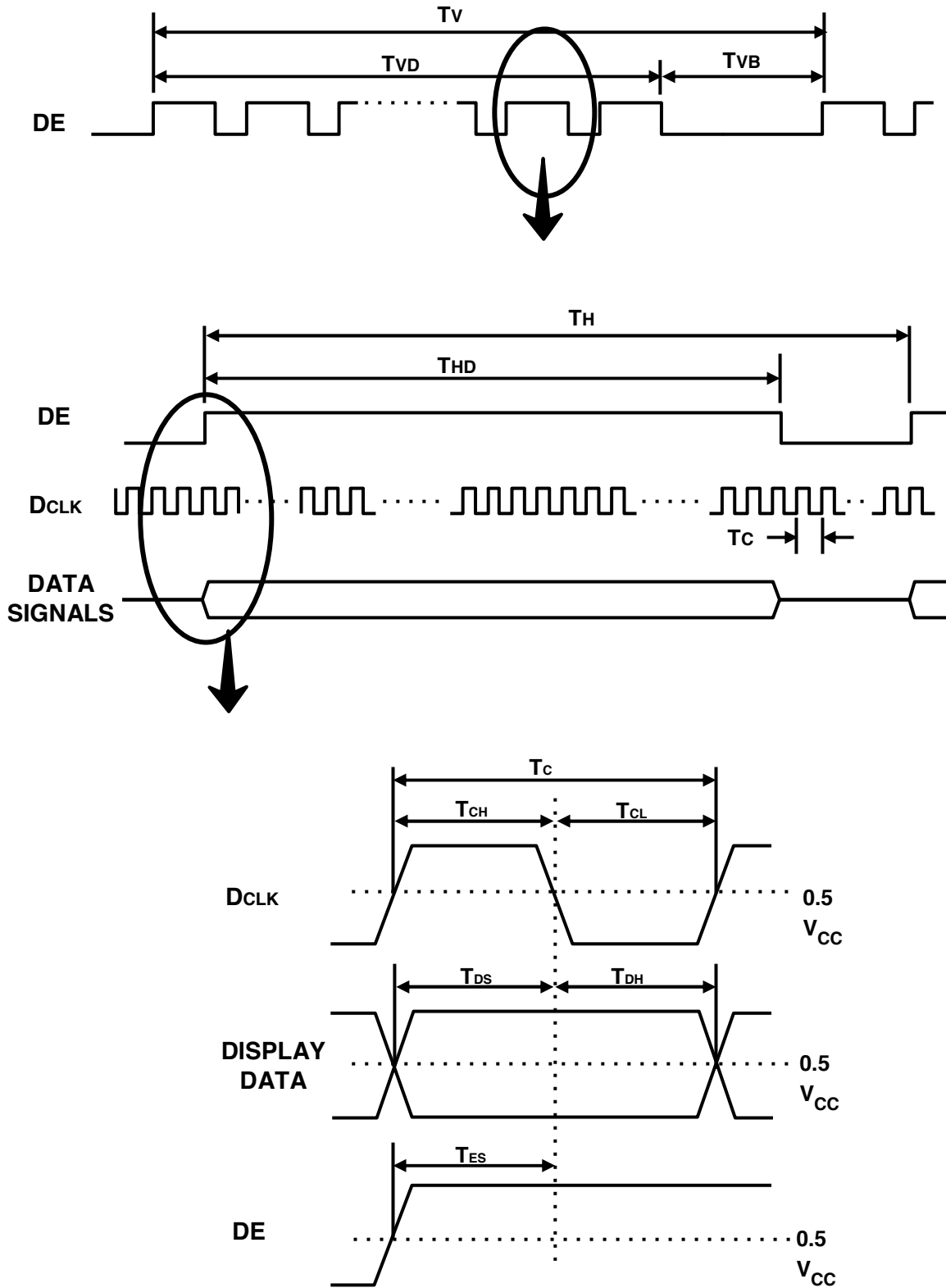
(3) Internal Vcc = 3.3V

(4) Best operation clock frequency is 67.3 MHz (60Hz)

(5) Clock frequency = Frame frequency x  $T_V(\text{Typ})$  x  $T_H(\text{Typ})$

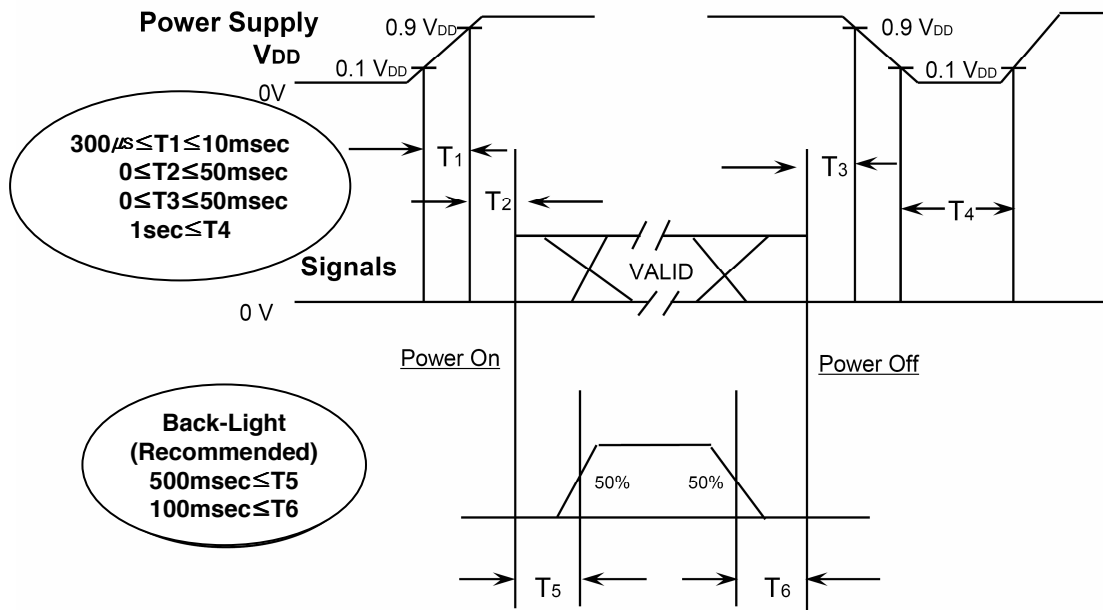
(6) Max, Min variation range is at main clock Typ value (69.3 MHz).

6.2 Timing diagrams of interface signal ( DE only mode )



### 6.3 Power ON/OFF Sequence

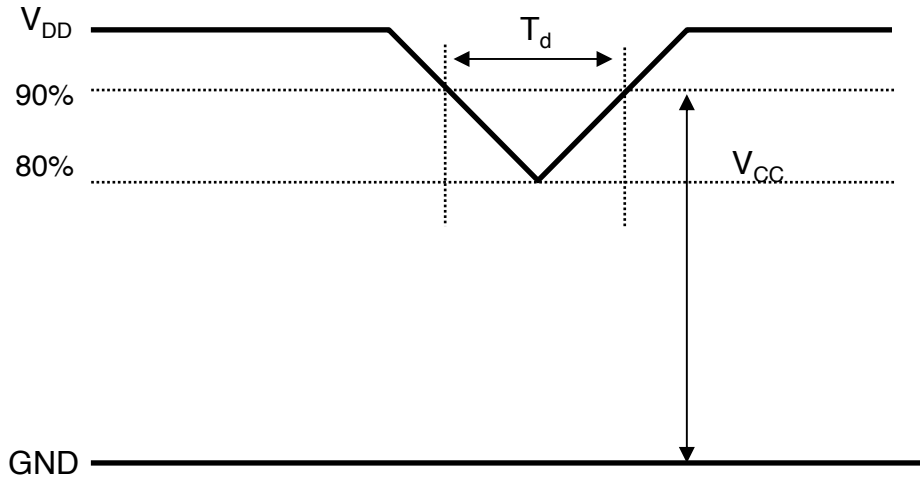
To prevent a latch-up or DC operation of the LCD Module, the power on/off sequence should be as the diagram below.



- T1 : V<sub>DD</sub> rising time from 10% to 90%
- T2 : The time from V<sub>DD</sub> to valid data at power ON.
- T3 : The time from valid data off to V<sub>DD</sub> off at power Off.
- T4 : V<sub>DD</sub> off time for Windows restart
- T5 : The time from valid data to B/L enable at power ON.
- T6 : The time from valid data off to B/L disable at power Off.

- The supply voltage of the external system for the Module input should be the same as the definition of V<sub>DD</sub>.
- Apply the lamp voltage within the LCD operation range. When the back light turns on before the LCD operation or the LCD turns off before the back light turns off, the display may momentarily show abnormal screen.
- In case of V<sub>DD</sub> = off level, please keep the level of input signals low or keep a high impedance.
- T4 should be measured after the Module has been fully discharged between power off and on period.
- Interface signal should not be kept at high impedance when the power is on.

### 6.4 VDD Power Dip Condition



$$4.5V \leq V_{DD} \leq 5.5V$$

$$\text{If } V_{DD}(\text{typ.}) \times 80\% \leq V_{CC} \leq V_{DD}(\text{typ.}) \times 90\%$$

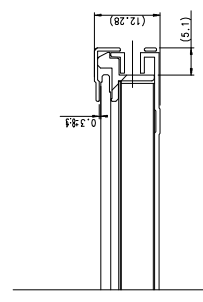
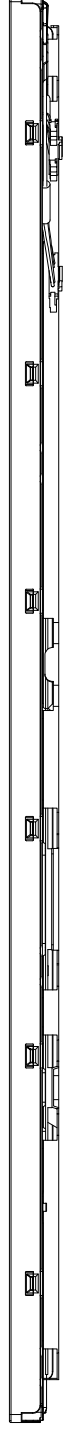
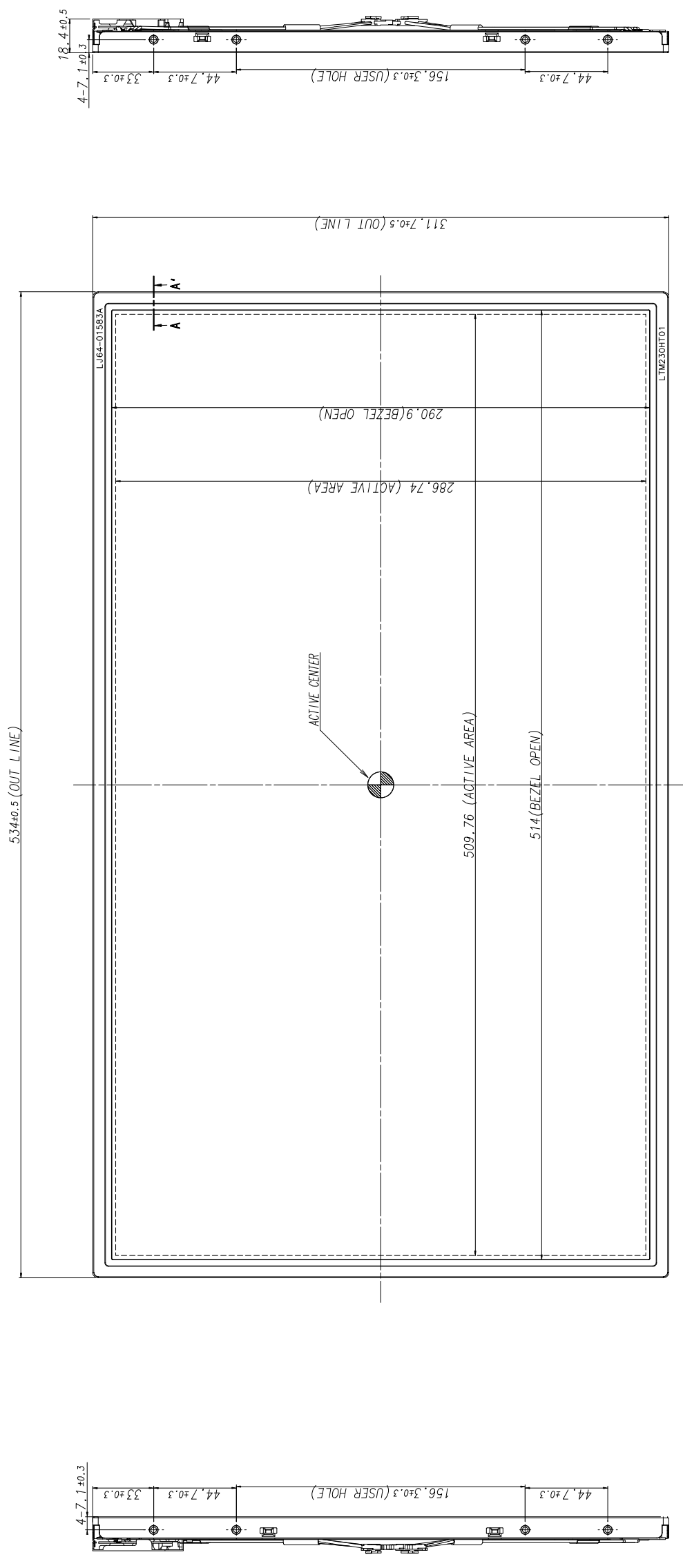
$$\text{Then, } 0 < T_d \leq 20\text{msec}$$

- Note (1) The above conditions are for the glitch of the input voltage.  
 (2) For stable operation of an LCD Module power, please follow them.  
 i.e., if  $\text{typ VDD} \times 80\% \leq V_{cc} \leq \text{typ VDD} \times 90\%$ , then  $T_d$  should be less than 20ms.

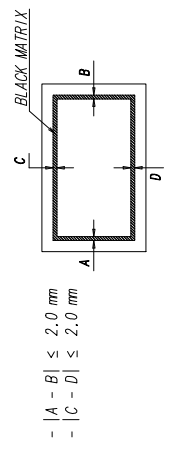
**7. Outline Dimension**

[ Refer to the next page ]

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SECTION A-A' (2:1)



- NOTES
1. BACKLIGHT : 4 COLD CATHODE FLUORESCENT LAMPS
  2. I/F CONNECTOR SPEC.
    - MAKER: UJU
    - PART NO.: IS100-L300-C23 OR EQUIVALENT
  3. LAMP CONNECTOR SPEC.
    - MAKER: YEON HO
    - PART NO.: 35001HS-04L OR EQUIVALENT
  4. USER MOUNTING TORQUE SPEC : 4 ~ 6 kgf-cm
  5. BLACK MATRIX SPEC (When set up at standing)

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## 8. General Precautions

### 8.1 Handling

- (a) When the module is assembled, it should be attached to the system firmly using all mounting holes. Be careful not to twist and bend the module.
- (b) Because the inverter uses high voltages, it should be disconnected from power source before it is assembled or disassembled.
- (c) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, it may cause improper operation or damage to the module and CCFT back light.
- (d) Note that polarizer films are very fragile and could be damaged easily. Do not press or scratch the surface harder than a HB pencil lead.
- (e) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, staining or discoloration may occur.
- (f) If the surface of the polarizer is dirty, clean it using absorbent cotton or soft cloth.
- (g) Desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might cause permanent damage to the polarizer due to chemical reaction.
- (h) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth . In case of contact with hands, legs or clothes, it must be washed away with soap thoroughly.
- (i) Protect the Module from static, or the CMOS Gate Array IC would be damaged.
- (j) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (k) Do not disassemble the Module.
- (l) Do not pull or fold the lamp wire.
- (m) Do not adjust the variable resistor located on the Module.
- (n) Protection film for polarizer on the Module should be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (o) Pins of I/F connector should not be touched directly with bare hands.

## 8.2 Storage

- (a) Do not leave the Module in high temperature, and high humidity for a long time. It is highly recommended to store the Module with temperature from 0 to 35 °C and relative humidity of less than 70%.
- (b) Do not store the TFT-LCD Module in direct sunlight.
- (c) The Module should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light in storing.

## 8.3 Operation

- (a) Do not connect or disconnect the Module in the "Power On" condition.
- (b) Power supply should always be turned on/off by the item 6.3 "Power on/off sequence"
- (c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (d) The cable between the back light connector and its inverter power supply should be connected directly with a minimized length. A longer cable between the back light and the inverter may cause lower luminance of lamp(CCFT) and may require higher startup voltage(Vs).

## 8.4 Operation Condition Guide

- (a) The LCD product should be operated under normal conditions.  
Normal condition is defined as below;
  - Temperature :  $20 \pm 15$  °C
  - Humidity :  $65 \pm 20$  %
  - Display pattern : continually changing pattern (Not stationary)
- (b) If the product will be used in extreme conditions such as high temperature, humidity, display patterns or operation time etc., It is strongly recommended to contact SEC for Application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at Airports, Transit Stations, Banks, Stock market, and Controlling systems.

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## 8.5 Others

- (a) Ultra-violet ray filter is necessary for outdoor operation.
- (b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (c) Do not exceed the absolute maximum rating value. ( supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on)  
Otherwise the Module may be damaged.
- (d) If the Module keeps displaying the same pattern for a long period of time, the image may be "sticked" to the screen.  
To avoid image sticking, it is recommended to use a screen saver.
- (e) This Module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.
- (f) Please contact SEC in advance when you display the same pattern for a long time.