SAMSUNG ELECTRONICS

Approval

TO : Dell / Compal

DATE : Set. 19. 2003

SAMSUNG TFT-LCD

MODEL NO.: LTN150PG-L02

Any Modification of Spec is not allowed without SEC permission

APPROVED BY : K. H. Shin

PREPARED BY : **Technical Customer Service Team**

SAMSUNG ELECTRONICS CO., LTD.

wise view™

Approval

CONTENTS

Revision History ----------(3)

General Description ----------(4)

1. Absolute Maximum Ratings ----------(5)
   1.1 Absolute Ratings of environment
   1.2 Electrical Absolute Ratings

2. Optical Characteristics ----------(7)

3. Electrical Characteristics ----------(10)
   3.1 TFT LCD Module
   3.2 Backlight Unit

4. Block Diagram ----------(14)
   4.1 TFT LCD Module
   4.2 Backlight Unit

5. Input Terminal Pin Assignment ----------(16)
   5.1 Input Signal & Power
   5.2 LVDS Interface
   5.3 Backlight Unit
   5.4 Timing Diagrams of LVDS For Transmitting
   5.5 Input Signals, Basic Display Colors and Gray Scale of Each Color.
   5.6 Pixel format

6. Interface Timing ----------(22)
   6.1 Timing Parameters(DE Mode)
   6.2 Timing Diagrams of interface Signal (DE Mode)
   6.3 Power ON/OFF Sequence

7. Outline Dimension ----------(24)

8. Packing ----------(25)

9.Markings and Others ----------(26)

10. GENERAL PRECAUTIONS ----------(28)

Appendix 1.EDID

Appendix 2.Inverter spec.

REVISION HISTORY

Approval

Date	Rev.No.	Page	Summary
Apr. 16, 2003	P00	All	LTN150PG-L02 model rev.P00 specification was First issued.
Set. 01, 2003	A00	All	To correct typos
		16	To correct the input connector (JAE, FI-XB30SRL-HF11)
		24	To change the length of lamp wire tape (52mm→60mm)
		Appendix	To update EDID

GENERAL DESCRIPTION

DESCRIPTION

LTN150PG-L01 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight system. The resolution of a 15.0" contains 1400 x 1050 pixels and can display up to 262,144 colors. 6 O'clock direction is the Optimum viewing angle.

FEATURES

- Thin and light weight
- High contrast ratio
- SXGA-Plus (1400x1050 pixels) resolution
- Low power consumption
- DE (Data enable) only mode.
- LVDS Interface with 2 pixel / clock (2 channel)

APPLICATIONS

- Notebook PC and desktop monitors
- Display terminals for AV application products
- Monitors for Industrial machine
- If the usage of this product is not for PC application, but for others, please contact SEC

GENERAL INFORMATION

ITEM	SPECIFICATION	UNIT	NOTE
Display area	304.1(H)X228.1(V) (15.0” diagonal)	mm	
Driver element	a-si TFT active matrix		
Display colors	262,144		
Number of pixel	1400 x 1050 (SXGA-Plus)	pixel	
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.2175(H) x 0.2175(V)	mm	
Display Mode	Normally white		
Surface treatment	HAZE 25, HARD-COATING 3H		

Mechanical Information

ITEM		MIN.	TYP.	MAX.	NOTE
Module Size	Horizontal (H)	316.8	317.3	317.8	
	Vertical (V)	241.6	242.1	242.6	
	Depth (D)	-	-	6.0	
Weight			550g	565g	Without Inverter

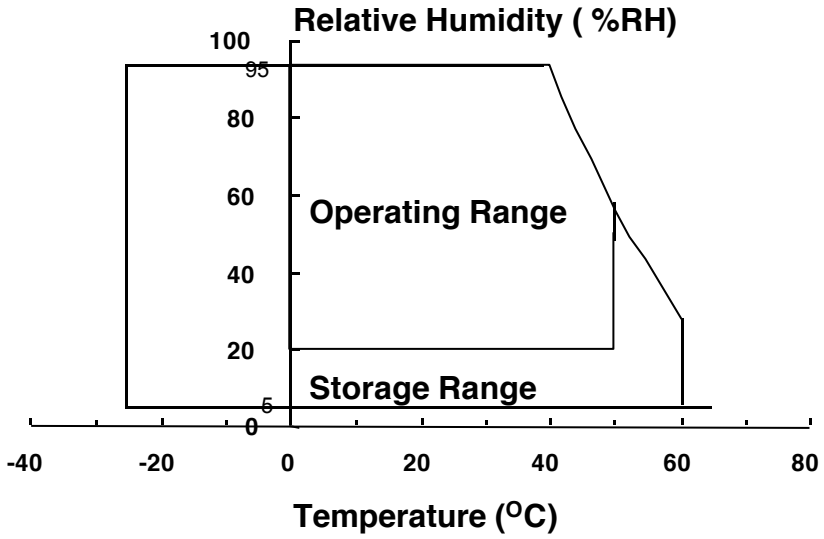
Note (1) Depth of signal interface connector part.

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Storage temperate	T_{STG}	-25	60	^{O}C	(1)
Operating temperate (Temperature of glass surface)	T_{OPR}	0	50	^{O}C	(1)
Shock (non-operating)	Snop	-	220	G	(2), (4)
Vibration (non-operating)	Vnop	-	1. 5	G	(3), (4)

Note (1) Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 $^{O}C \geq$ Ta)
Maximum wet - bulb temperature at 39 ^{O}C or less. (Ta > 40 ^{O}C) No condensation.
(2) 2ms, half sine wave, one time for $\pm X, \pm Y, \pm Z$.
(3) 10 ∽ 300 ∽ 10 Hz, Sweep rate 10 min, 30 min for X,Y,Z.
(4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.



1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

(Vss = GND = 0 V)

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
Power Supply Voltage	Vcc	Vss-0.3	4.0	V	(1)
Logic Input Voltage	V_{IN}	Vss-0.3	Vcc + 0.3	V	(1)

NOTE (1) Within Ta (25 ± 2 ^{O}C)

(2) BACK-LIGHT UNIT

Ta = 25 ± 2 ^{O}C

ITEM	SYMBOL	MIN.	MAX.	UNIT.	NOTE
Lamp current	I_L	3.0	7.0	mA_{rms}	(1)
Lamp frequency	F_L	50	80	KHz	(1)

NOTE (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

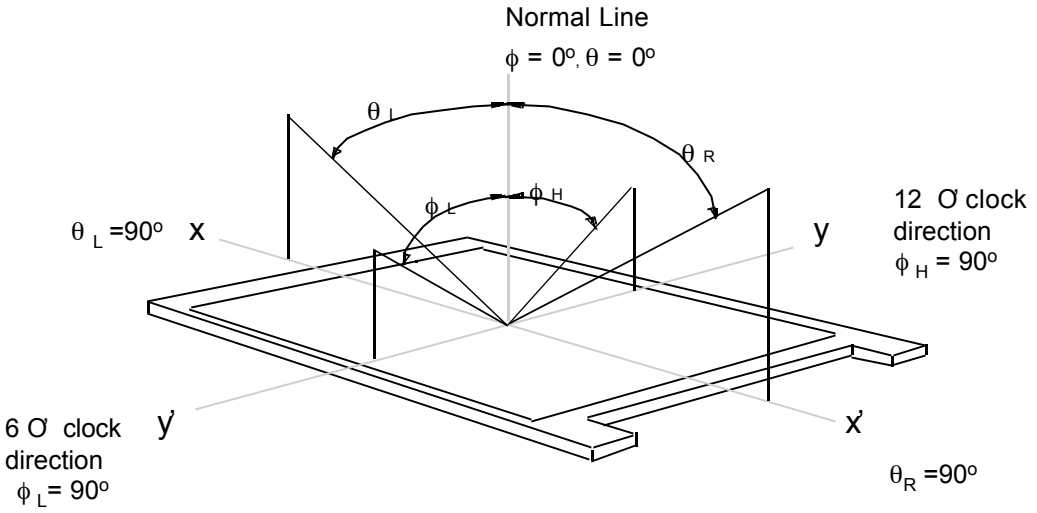
2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5).
Measuring equipment : TOPCON BM-5A

* Ta = 25 ± 2°C , V_{DD}=3.3V, fv= 60Hz, f_{DCLK}=54MHz, I_L = 6.3 mA

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Contrast Ratio (5 Points)		CR	ϕ = 0, θ = 0 Normal Viewing Angle	300	-	-		
Response Time at 25℃	Rising	T_R		-	10	15	msec	(1), (3)
	Falling	T_F		-	15	20		
Luminance of White		Y_L		180	200	-	cd/m^2	(1), (4) @6.3mm
Color Chromaticity (CIE)	Red	R_X		0.560	0.580	0.600		(1), (5) PR650
		R_Y		0.320	0.340	0.360		
	Green	G_X		0.290	0.310	0.330		
		G_Y		0.530	0.550	0. 570		
	Blue			0.135	0.155	0.175		
		B		0.135	0.155	0.175		
	White	W_X		0.293	0.313	0.333		
		W_Y		0.309	0.329	0.349		
Viewing Angle	Hor.	θ_L	CR ≥10 (at center point)	60	-	-	Degrees	
		θ_R		60	-	-		
	Ver.	ϕ_H		45	-	-		
		ϕ_L		45	-	-		
13 Points White Variation					-	2.0		(6)

Note 1) Definition of Viewing Angle :

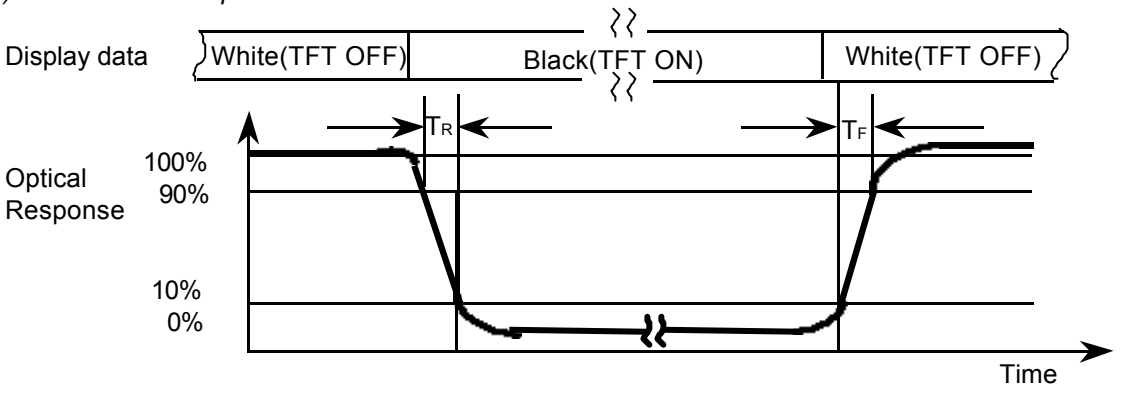


Note 2) Definition of Contrast Ratio (CR) :

$$CR = \frac{CR1 + CR2 + CR3 + CR4 + CR5}{5}$$

POINTS : ④ , ⑤ , ⑦ , ⑨ , ⑩ at FIGURE OF NOTE 6)

Note 3) Definition of Response time :



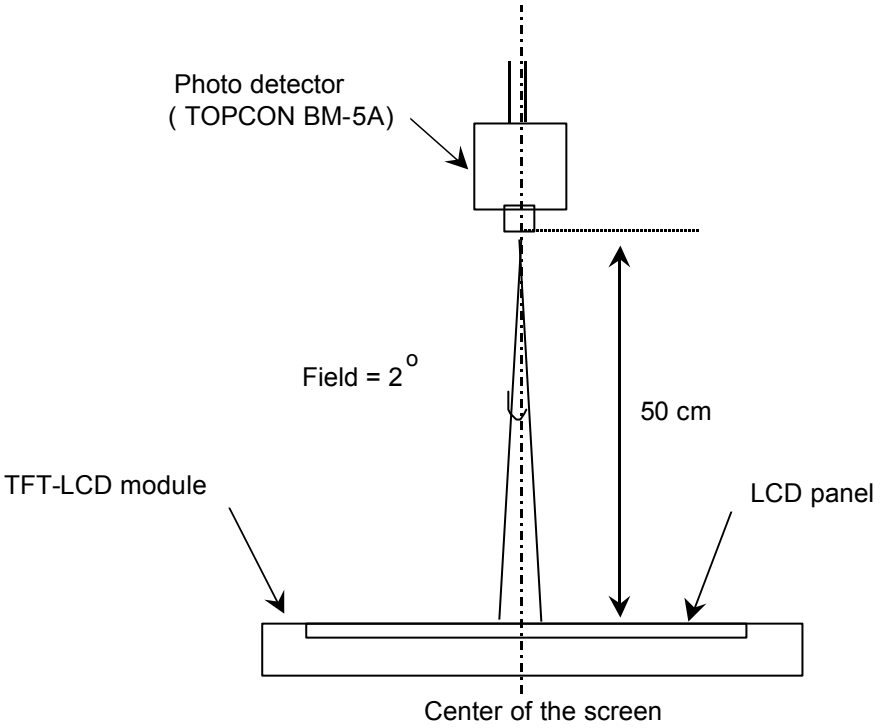
Note 4) Definition of Average Luminance of White : measure the luminance of white at 5 points.

Average Luminance of White ($Y_{L,AVE}$)

$$Y_{L,AVE} = \frac{Y_{L4} + Y_{L5} + Y_{L7} + Y_{L9} + Y_{L10}}{5}$$

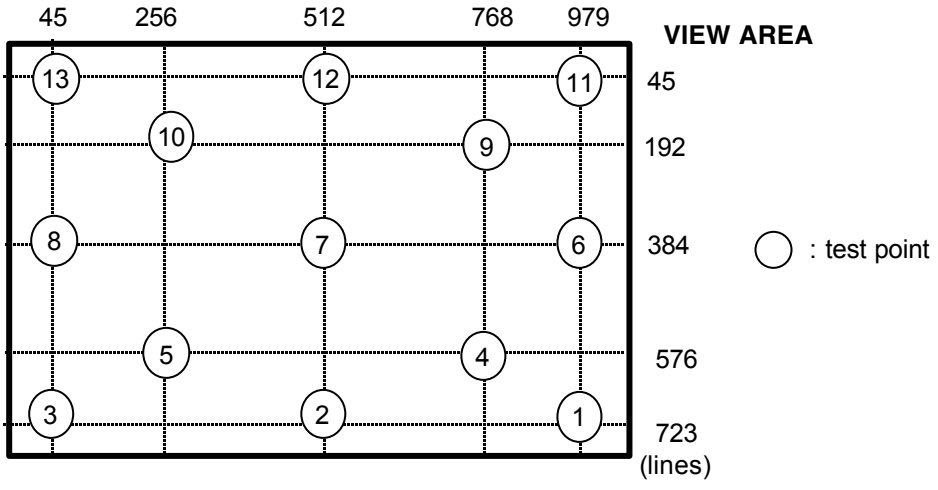
POINTS : ④ , ⑤ , ⑦ , ⑨ , ⑩ at FIGURE OF NOTE 6)

Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 minutes, the measurement should be executed. Measurement should be executed in a stable, windless,and dark room.
30 minutes after lighting the back-light. This should be measured in the center of screen.
Lamp current : 6.0 mA
Environment condition : Ta = 25 ± 2 °C



Note 6) Definition of 13 points white variation (δ_W), CR variation(C_{VER}) [① ~ ⑬]

$$\delta L = \frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}} \qquad \delta C_R = \frac{\text{Maximum CR of 13 points}}{\text{Minimum CR of 13 points}}$$



3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta=25 ± 2 °C

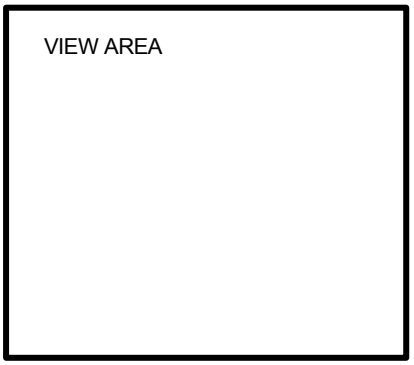
ITEM		SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Voltage of Power Supply		V_{DD}	3.0	3.3	3.6	V	
Differential Input Voltage for LVDS Receiver Threshold	High	V_{IH}	-	-	+100	mV	V_{CM}=+1.2V
	Low	V_{IL}	-100	-	-	mV	
Vsync Frequency		fv	-	60	-	Hz	
Hsync Frequency		f_H	-	63.98	-	KHz	
Main Frequency		f_{DCLK}	42.7	54	85	MHz	
Rush Current		I_{RUSH}	-	-	1.5	A	(4)
Current of Power Supply	White	I_{DD}	-	430	-	mA	(2),(3)*a
	Mosaic		-	450	-	mA	(2),(3)*b
	Max Pattern		-	550	600	mA	(2),(3)*c

Note (1) Display data pins and timing signal pins should be connected.(GND=0V)

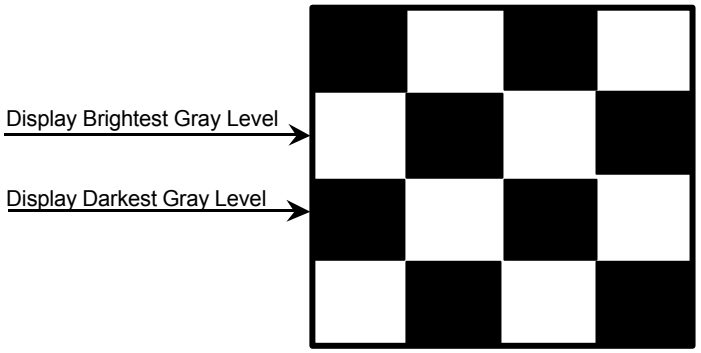
(2) f_V=60Hz, f_{DCLK} =54MHZ, Vdd = 3.3V , DC Current.

(3) Power dissipation pattern

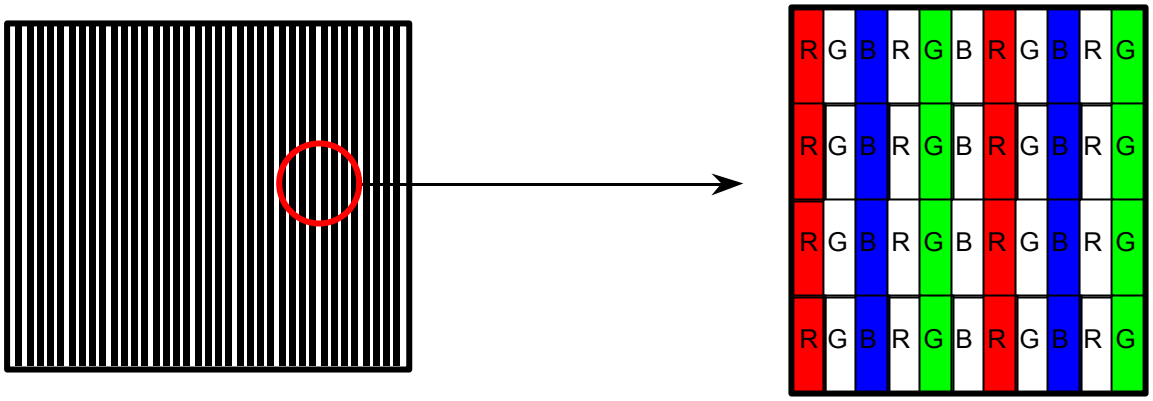
*a) White Pattern



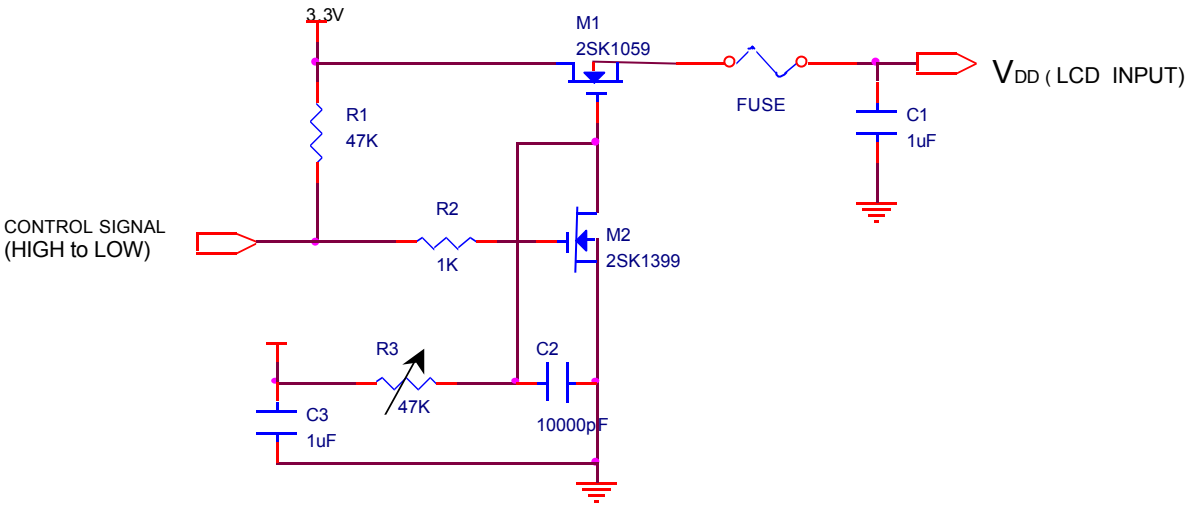
*b) Mosaic Pattern



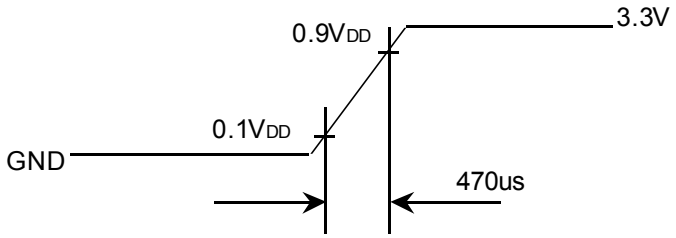
*c) Maximum Power pattern : 1dot vertical stripe



4) Rush current measurement condition



VDD rising time is 470us



3.2 BACK-LIGHT UNIT

The backlight system is an edge - lighting type with a single CCFT (Cold Cathode Fluorescent Tube).
The characteristics of a single lamp are shown in the following tables.

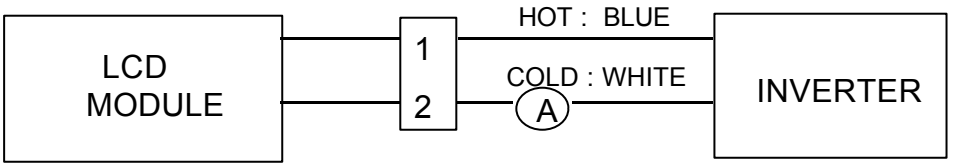
INVERTER : Ambit / Sumida

Ta=25 ± 2 °C

ITEM	SYMB	MIN	TYP	MAX	UNIT	NOTE
Lamp Current	I_L	2.0	6.0	7.0	mArms	(1)
Lamp Voltage	V_L		655		Vrms	I_L=6.0mA
Frequency	f_L	45	60	80	kHz	(2)
Power Consumption	P_L	-	4.0	-	W	(3)
Operating Life Time	Hr	15,000	-	-	Hour	(4)
Startup Voltage	V_S	-	-	1150	Vrms	25°C
				1380	Vrms	0 °C
Lamp Startup Time	V_S	-	-	1	sec	(5)

Note) The waveform of the inverter output voltage must be area symmetric and the design of the inverter must have specifications for the modularized lamp.
The performance of the backlight, for example life time or brightness, is much influenced by the characteristics of the DC-AC inverter for the lamp. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.
When you design or order the inverter, please make sure that a poor lighting caused by the mismatch of the backlight and the inverter(miss lighting, flicker, etc.) never occur. When you confirm it, the module should be operated in the same condition as it is installed in your instrument.

Note (1) Lamp current is measured with a high frequency current meter as shown below.



No 2 Pin is V_{LOW}.

Ambit / Sumida

(2) Lamp frequency may produce interference with horizontal synchronous frequency and this may cause line flow on the display. Therefore lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.

(3) refer to I_L x V_L to calculate.

(4) Life time (Hr) of a lamp can be defined as the time in which it continues to operate under the condition Ta = 25 ±2 °C and I_L = 6.0 mArms until one of the following event occurs.
1. When the brightness becomes 50% or lower than the original.

(5) The voltage above this value should be applied to the lamp for more than 1 second to startup Otherwise the lamp may not be turned on.

3.3 INVERTER

Inverter : AMBIT/SUMIDA

Ta = 25 ± 2°C

ITEM		MIN	TYP	MAX	UNIT	NOTE
Input Voltage(Vin)		7.5	14.4	21.0	mArms	
Open Circuit Voltage		1400		1800	Vrms	IL =6.0 mArms
PWM duty cycle		10 ±2 @SMB_DAT FFH	-	100 @SMB_DAT 00H	%	Vin=14.4V
Efficiency	Optical	20	-	-	Nit/W	After 30min turn on at the center of LCD Vin=14.4V @6.0mA(3)
	Electrical	-	80	-	%	
Operating Frequency		45	55	65	kHz	SMB_DAT=00H
PWM Frequency		200	210	220	Hz	Vin=14.4V
Input Voltage Ripple		-	-	0.5	Vpp	Peak to peak value
Input Power Consumption		-	5.0	5.7	W	(1) Iout=6.0mArms
In-rush current		-	-	1.5	A	
Shutdown time		-	1.0	1.4	sec	
Start-up time		-	-	0.1	sec	(2)

Note

(1) Vin=14.4V, IL=6.0mA

(2) Inverter start-up time

(3) Efficiency should be calculated as below formulation.

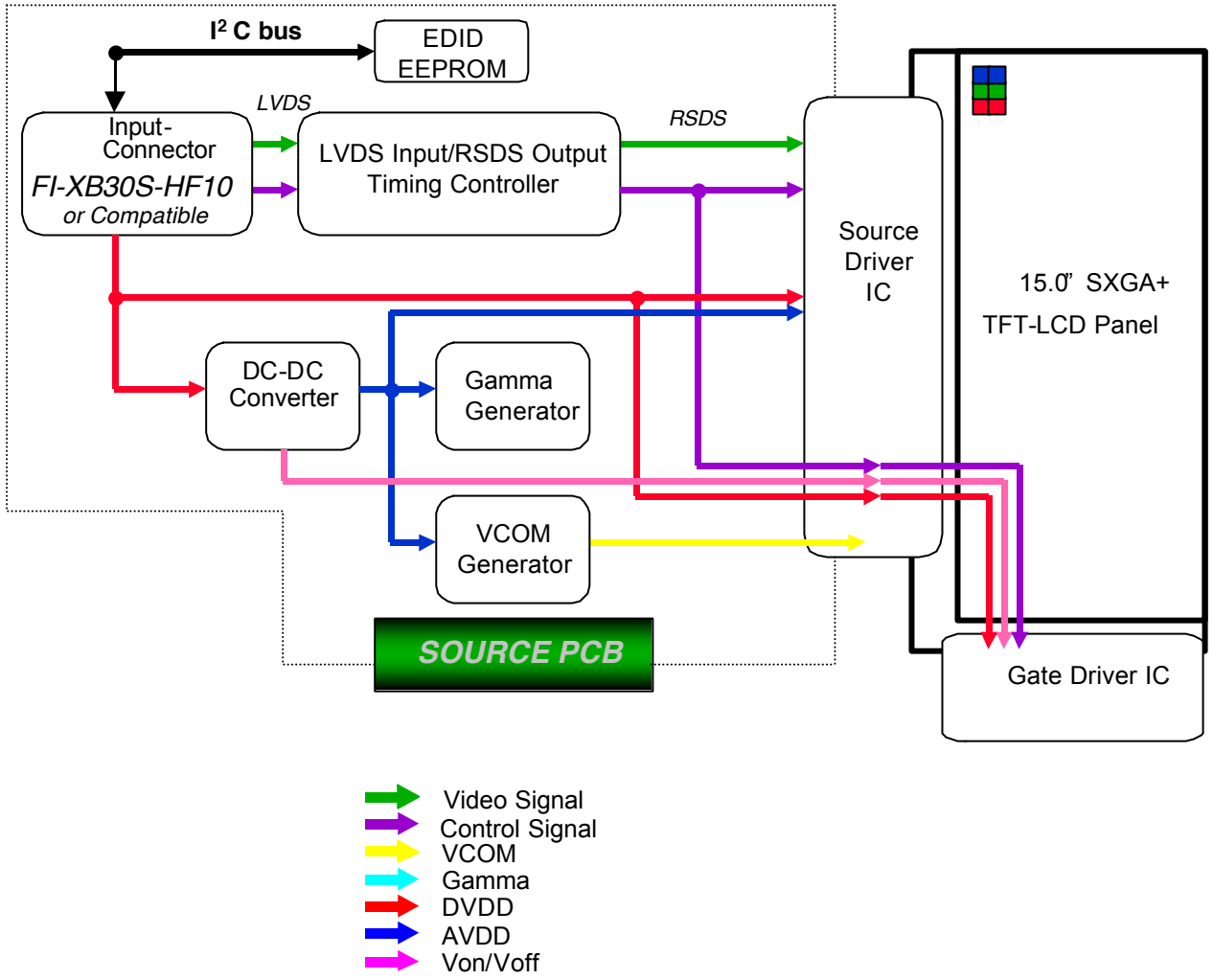
Optical efficiency = output Brightness(nits) / Input power(watt)

Electrical efficiency = output power / input power

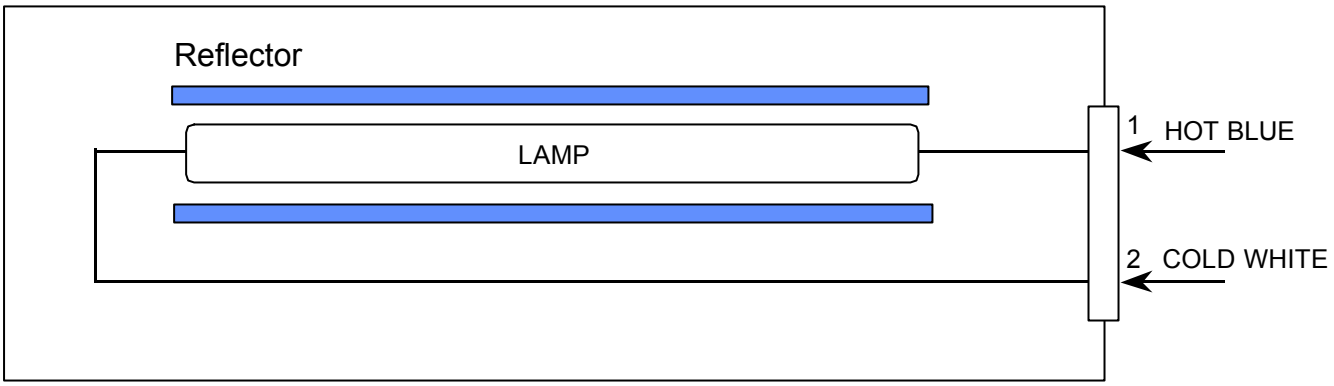
Approval

4. BLOCK DIAGRAM

4.1 TFT LCD Module



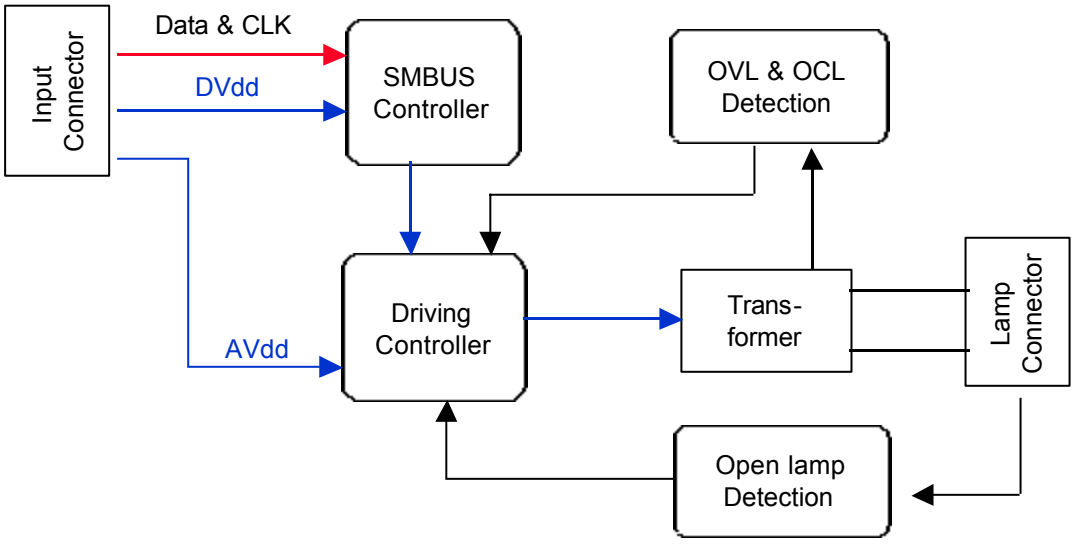
4.2 BACKLIGHT UNIT



Note) The output of the inverter may change according to the material of the reflector.

4.3 Inverter UNIT

- Input Connector : HONDA, LVC-D20SFYG



5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power LVDS, Connector : (JAE, FI-XB30SRL-HF11)

PIN NO	SYMBOL	FUNCTION	POLARITY	REMARK
1	Vss	Ground		
2	VDD	POWER SUPPLY +3.3V		
3	VDD	POWER SUPPLY +3.3V		
4	VEEDID	N/A (DDC 3.3V Power)		
5	BIST	Panel BIST control		
6	CLKEDID	N/A (DDC Clock)		
7	DATAEDID	N/A (DDC data)		
8	O_RxIN0-	LVDS Differential Data INPUT (Odd R0-R5,G0)	Negative	
9	O_RxIN0+	LVDS Differential Data INPUT (Odd R0-R5,G0)	Positive	
10	Vss	Ground		
11	O_RxIN1-	LVDS Differential Data INPUT (Odd G1-G5,B0-B1)	Negative	
12	O_RxIN1+	LVDS Differential Data INPUT (Odd G1-G5,B0-B1)	Positive	
13	Vss	Ground		
14	O_RxIN2-	LVDS Differential Data INPUT (Odd B1-B5,Sync,DE)	Negative	
15	O_RxIN2+	LVDS Differential Data INPUT (Odd B1-B5,Sync,DE)	Positive	
16	Vss	Ground		
17	O_RxCLK-	LVDS Differential Data INPUT (Odd Clock)	Negative	
18	O_RxCLK+	LVDS Differential Data INPUT (Odd Clock)	Positive	
19	Vss	Ground		
20	E_RxIN0-	LVDS Differential Data INPUT (Even R0-R5,G0)	Negative	
21	E_RxIN0+	LVDS Differential Data INPUT (Even R0-R5,G0)	Positive	
22	Vss	Ground		
23	E_RxIN1-	LVDS Differential Data INPUT (Even G1-G5,B0-B1)	Negative	
24	E_RxIN1+	LVDS Differential Data INPUT (Even G1-G5,B0-B1)	Positive	
25	Vss	Ground		
26	E_RxIN2-	LVDS Differential Data INPUT (Even B1-B5,Sync,DE)	Negative	
27	E_RxIN2+	LVDS Differential Data INPUT (Even B1-B5,Sync,DE)	Positive	
28	Vss	Ground		
29	E_RxCLK-	LVDS Differential Data INPUT (Even Clock)	Negative	
30	E_RxCLK+	LVDS Differential Data INPUT (Even Clock)	Positive	

5.2 LVDS Interface : Transmitter DS90CF363 or Compatible

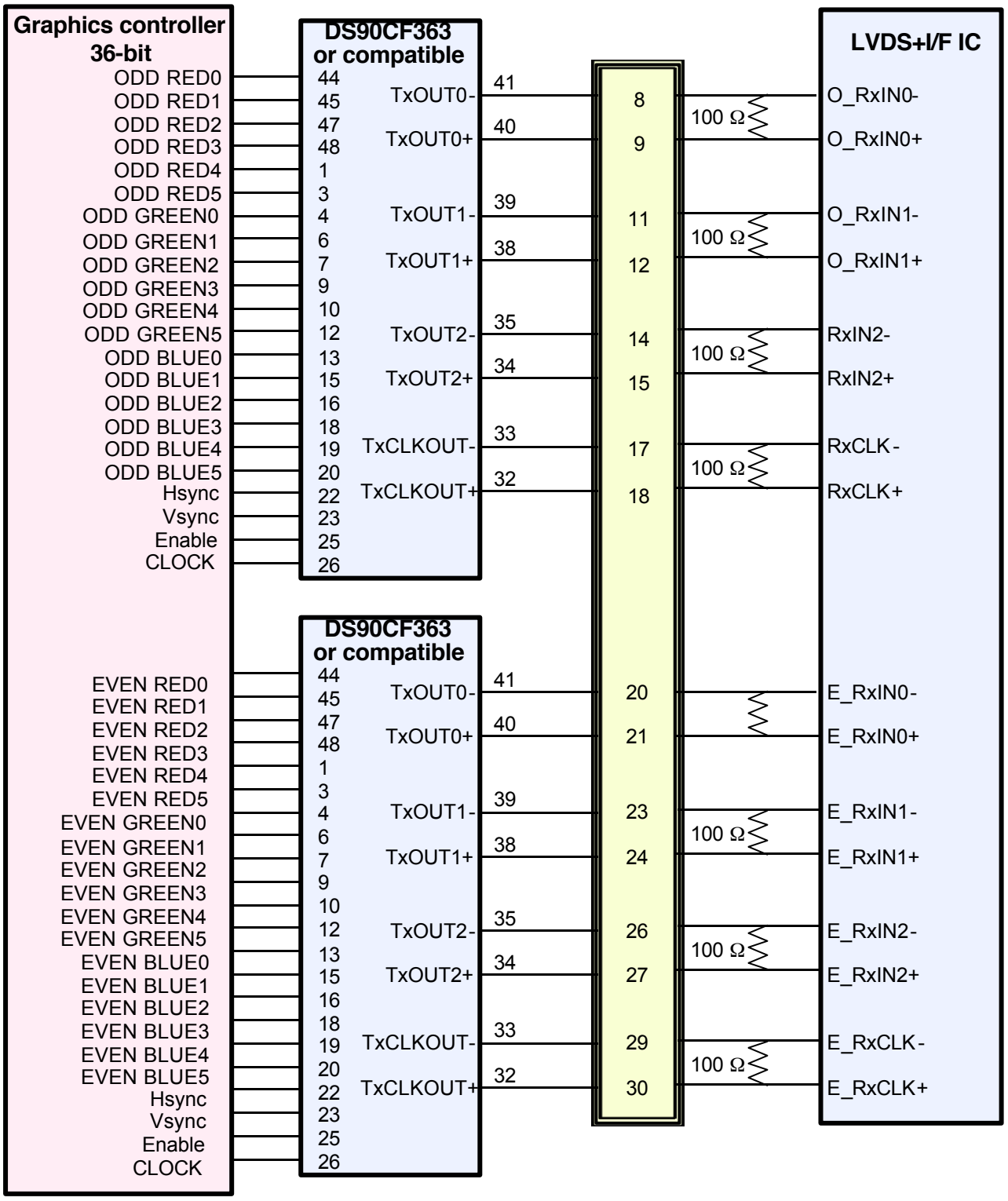
LVDS for Odd pixel

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
44	TxIN0	RO0	12	TxIN11	GO5
45	TxIN1	RO1	13	TxIN12	BO0
47	TxIN2	RO2	15	TxIN13	BO1
48	TxIN3	RO3	16	TxIN14	BO2
1	TxIN4	RO4	18	TxIN15	BO3
3	TxIN5	RO5	19	TxIN16	BO4
4	TxIN6	GO0	20	TxIN17	BO5
6	TxIN7	GO1	22	TxIN18	Hsync
7	TxIN8	GO2	23	TxIN19	Vsync
9	TxIN9	GO3	25	TxIN20	DE
10	TxIN10	GO4	26	TxCLK IN	Clock

LVDS

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
44	TxIN0	RE0	12	TxIN11	GE5
45	TxIN1	RE1	13	TxIN12	BE0
47	TxIN2	RE2	15	TxIN13	BE1
48	TxIN3	RE3	16	TxIN14	BE2
1	TxIN4	RE4	18	TxIN15	BE3
3	TxIN5	RE5	19	TxIN16	BE4
4	TxIN6	GE0	20	TxIN17	BE5
6	TxIN7	GE1	22	TxIN18	Hsync
7	TxIN8	GE2	23	TxIN19	Vsync
9	TxIN9	GE3	25	TxIN20	DE
10	TxIN10	GE4	26	TxCLK IN	Clock

Flat Link Interface



Note : The LCD Module uses a 100ohm resistor between positive and negative lines of each receiver input.

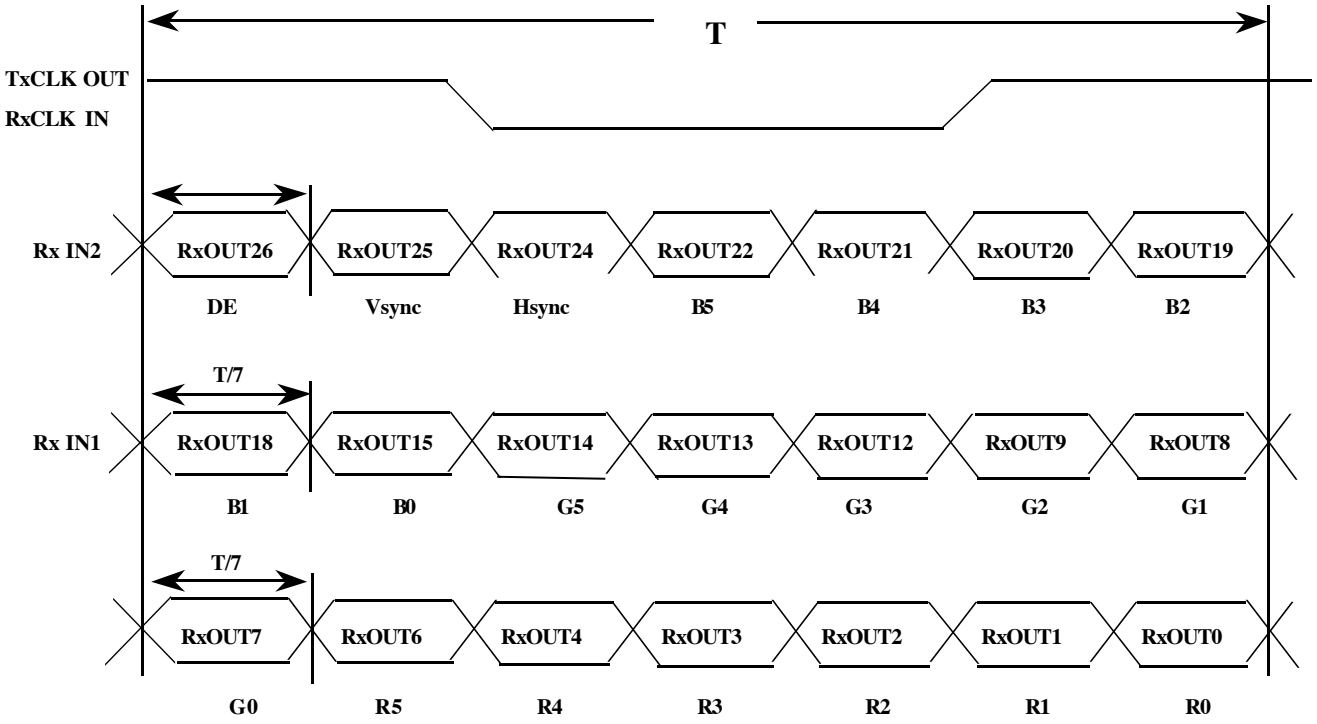
5.3 BACK LIGHT UNIT

Connector : JST BHSR - 02VS -1

Pin NO.	Symbol	Color	Function
1	HOT	Blue	High Voltage
2	COLD	White	Ground

T/7

5.4 Timing Diagrams of LVDS For Transmission

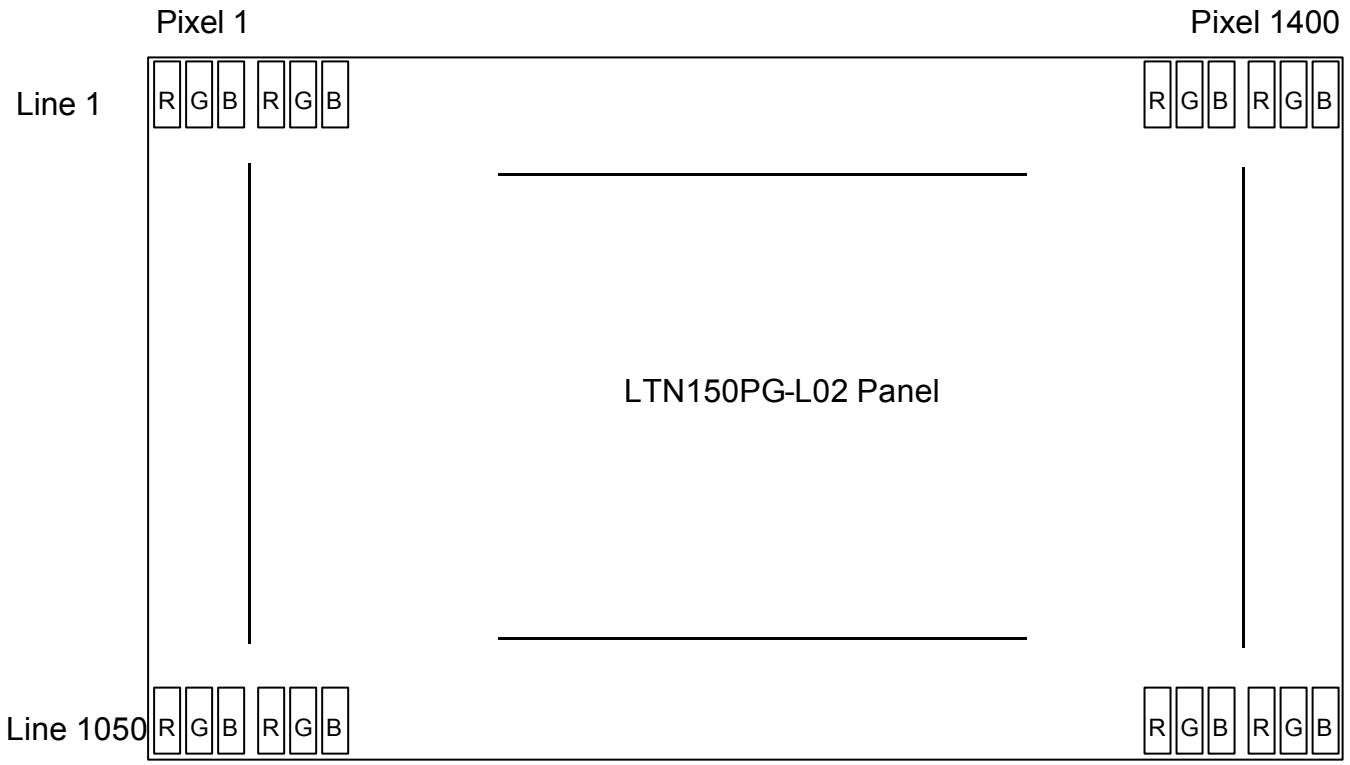


5.5 Input Signals, Basic Display Colors and Gray Scale of Each Color

COLOR	DISPLAY	DATA SIGNAL																		GRAY SCALE LEVEL
		RED						GREEN						BLUE						
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5	
COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	GREEN	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
	CYAN	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
	RED	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	MAGENTA	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	-
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
GRAY SCALE OF **RED**	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	DARK ↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~R60
	↓ LIGHT	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
		1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
		0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	RED	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
GRAY SCALE OF **GREEN**	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	DARK ↑	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G60
	↓ LIGHT	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
		0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
		0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	GREEN	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
GRAY SCALE OF **BLUE**	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	DARK ↑	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B60
	↓ LIGHT	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	GREEN	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

Note 1) Definition of gray :
Rn: Red gray, Gn: Green gray, Bn: Blue gray (n=gray level)
Note 2)Input signal: 0 =Low level voltage, 1=High level voltage

5.6 Pixel Format in the display

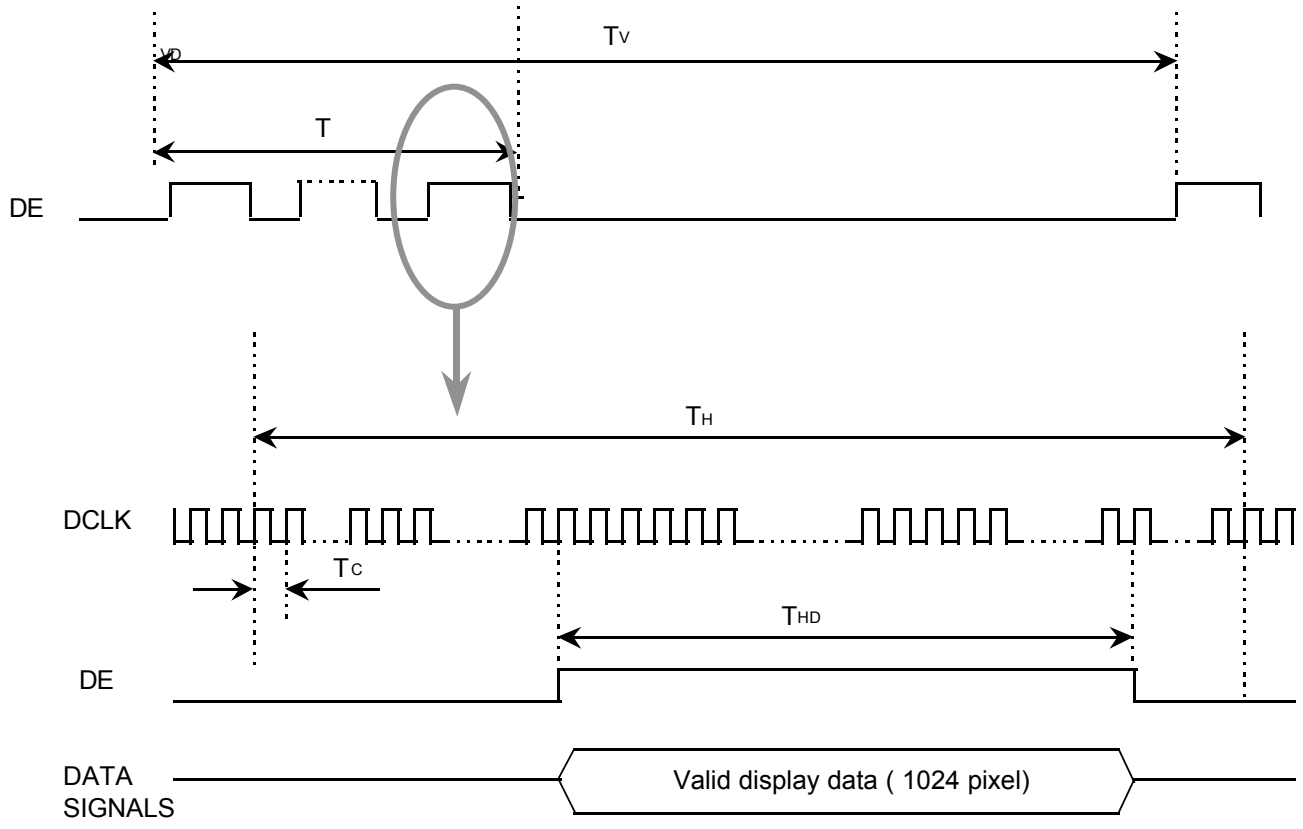


6. INTERFACE TIMING

6.1 Timing Parameters

Signal	Item	Symbol	MIN	TYP	MAX	Unit	Note
Frame Frequency	Cycle	T_V	-	1066	-	lines	
Vertical Active Display Term	Display Period	T_{VD}	-	1050	-	lines	
One Line Scanning Time	Cycle	T_H	-	844	-	clocks	(1)
Horizontal Active Display Term	Display Period	T_{HD}	-	700	-	clocks	

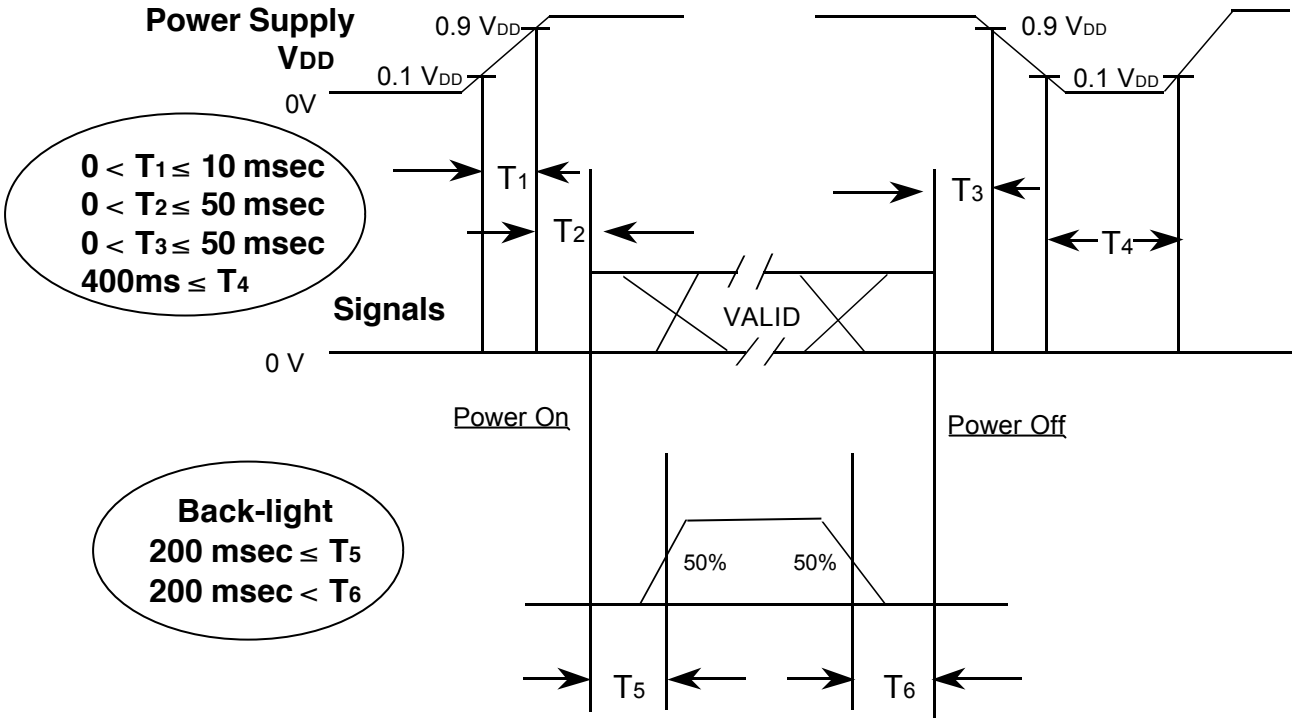
6.2 Timing diagrams of interface signal



Note : All input condition(level&timing) for SN75LVDS88 are the same with those of LPD11826 or compatible.

6.3 Power ON/OFF Sequence

: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown below.



Power ON/OFF Sequence

T1 : Vdd rising time from 10% to 90%
T2 : The time from Vdd to valid data at power ON.
T3 : The time from valid data off to Vdd off at power Off.
T4 : Vdd off time for Windows restart
T5 : The time from valid data to B/L enable at power ON.
T6 : The time from valid data off to B/L disable at power Off.

NOTE.

(1) The supply voltage of the external system for the module input should be the same as the definition of V_{DD}.

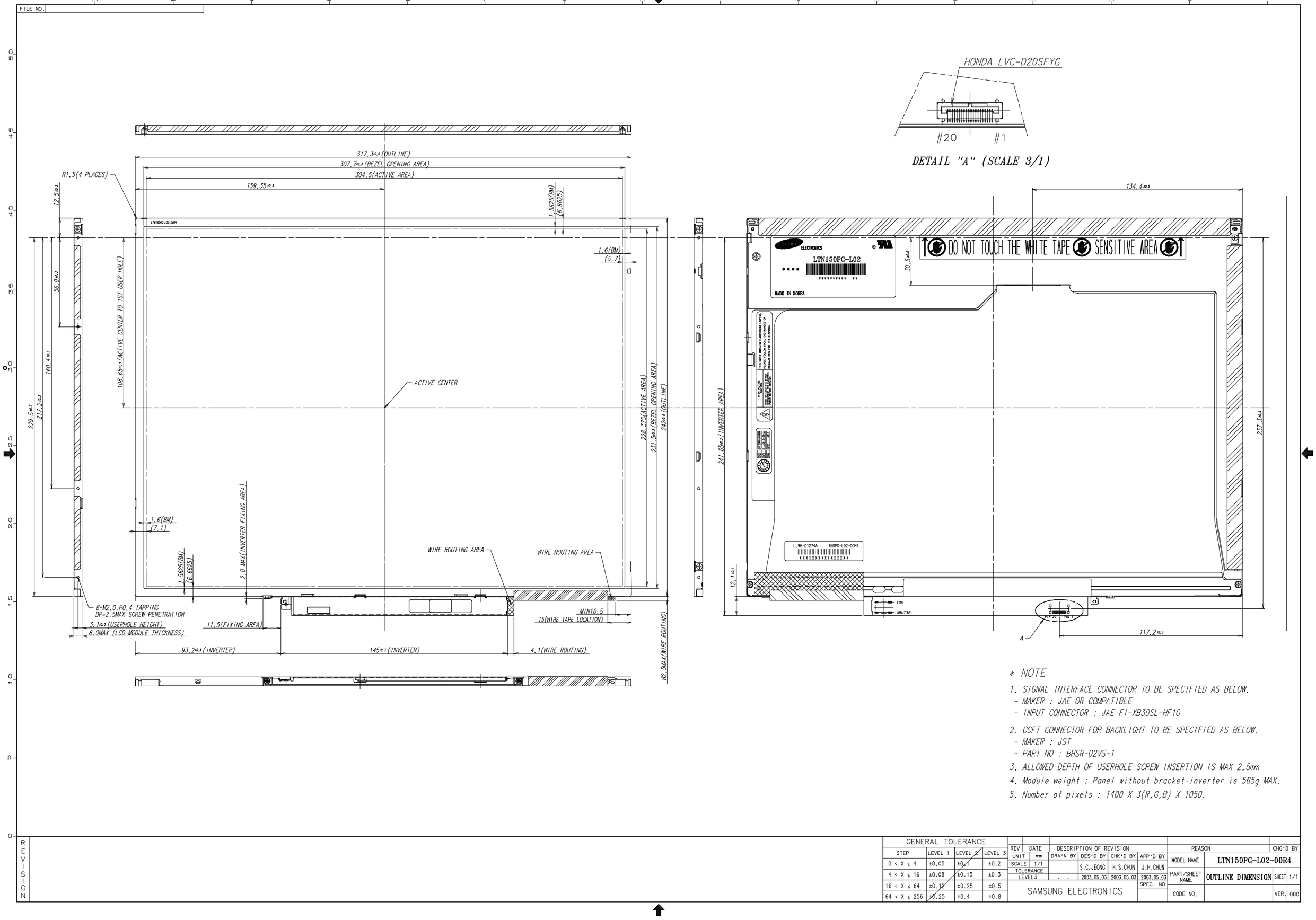
(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become white.

(3) In case of V_{DD} = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

FILE NO.



* NOTE

1. SIGNAL INTERFACE CONNECTOR TO BE SPECIFIED AS BELOW.
   - MAKER : JAE OR COMPATIBLE
   - INPUT CONNECTOR : JAE FI-XB30SL-HF10
2. CCFT CONNECTOR FOR BACKLIGHT TO BE SPECIFIED AS BELOW.
   - MAKER : JST
   - PART NO : BHSR-02VS-1
3. ALLOWED DEPTH OF USERHOLE SCREW INSERTION IS MAX 2.5mm
4. Module weight : Panel without bracket-inverter is 565g MAX.
5. Number of pixels : 1400 X 3(R,G,B) X 1050.

REVISION

GENERAL TOLERANCE			
STEP	LEVEL 1	LEVEL 2	LEVEL 3
0 < X ≤ 4	±0.05	±0.1	±0.2
4 < X ≤ 16	±0.08	±0.15	±0.3
16 < X ≤ 64	±0.12	±0.25	±0.5
64 < X ≤ 256	±0.25	±0.4	±0.8

REV	DATE	DESCRIPTION OF REVISION				REASON	CHG'D BY
UNIT	mm	DRA'N BY	DES'D BY	CHK'D BY	APP'D BY		
SCALE	1/1		S.C.JEONG	H.S.CHUN	J.H.CHUN	MODEL NAME	LTN150PG-L02-00R4
TOLERANCE LEVEL3		. .	2003.05.03	2003.05.03	2003.05.03	PART/SHEET NAME	OUTLINE DIMENSION SHEET 1/1
SAMSUNG ELECTRONICS					SPEC. NO	CODE NO.	VER. 000

Approval

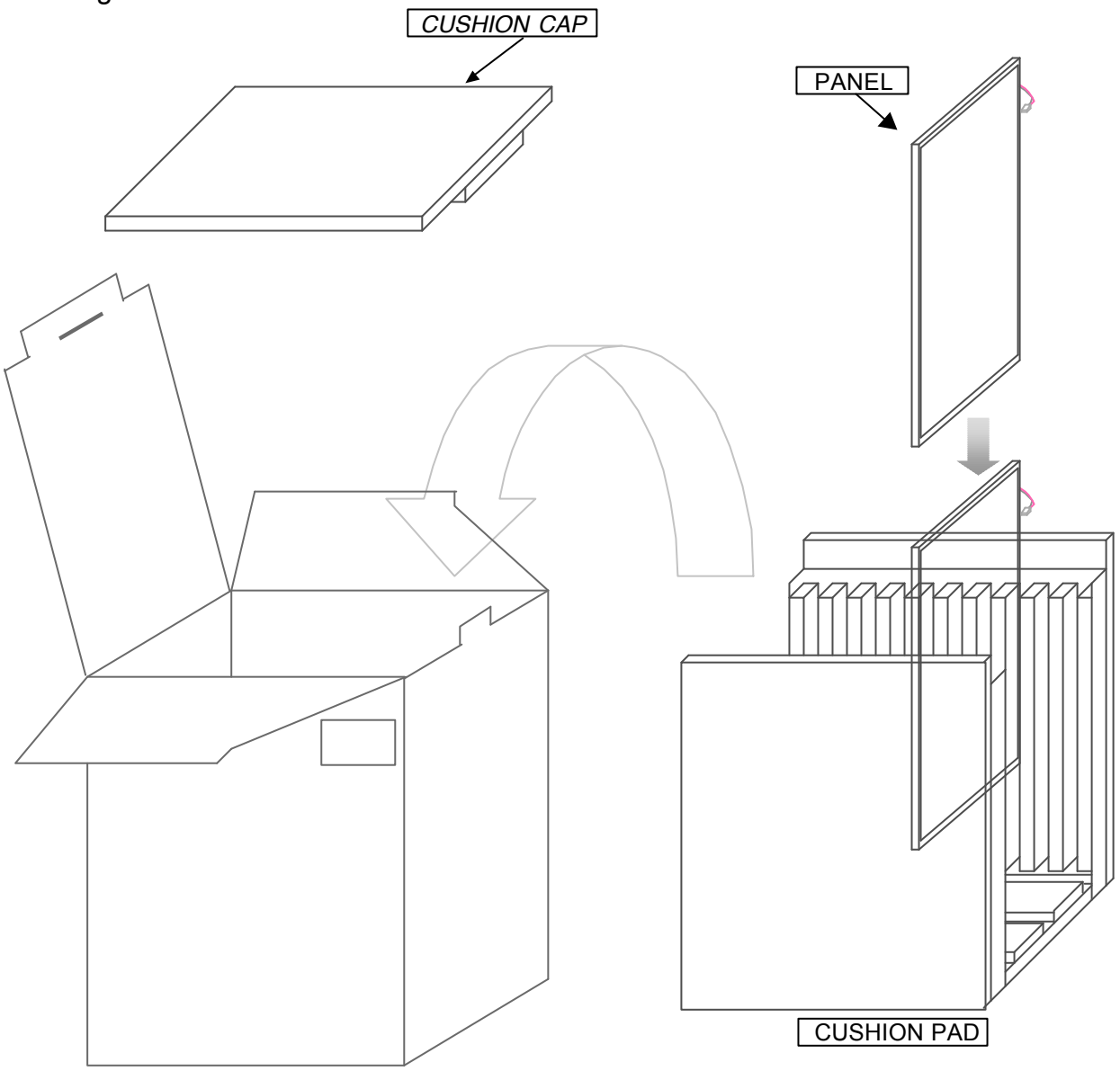
8. PACKING

1. CARTON(Internal Package)

(1) Packing Form

Corrugated Cardboard box and Corrupad form as shock absorber

(2) Packing Method



PACKING CASE

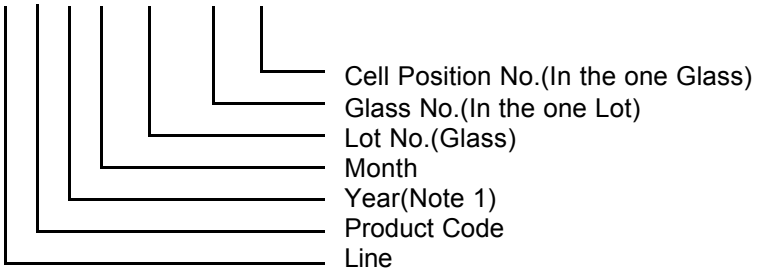
Note 1)Total Weight : Approximately 9.0 kg
2) Acceptance number of piling : 10 sets
3) Carton size : 317(W)×286(D)×355(H)
4) MAX accumulation quantity : 5 cartons

No	Part name	Quantity
1	Static electric protective sack	10
2	Packing case(Inner box) included shock absorber	1 set
3	Pictorial marking	2 pics
4	Carton	1 set

9. MARKINGS & OTHERS

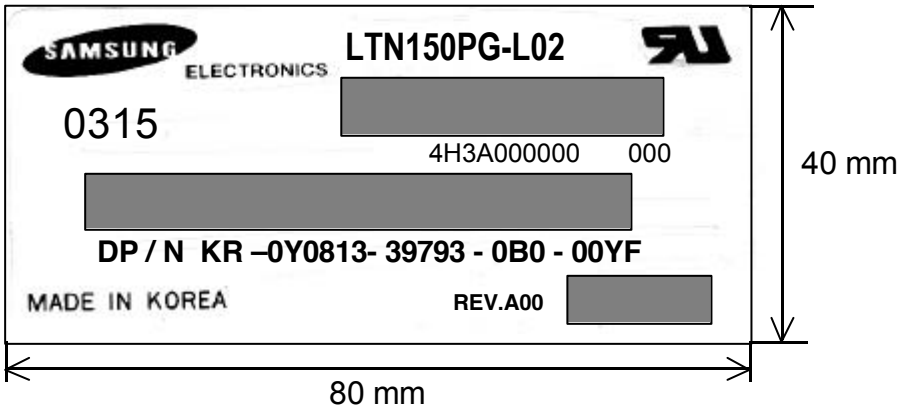
A nameplate bearing followed by is affixed to a shipped product at the specified location on each product.

(1)Parts number : LTN150PG-L02
(2)Revision : One letter
(3)Control code : One letter
(4)Lot number : 4 H 3 A XXX XX X



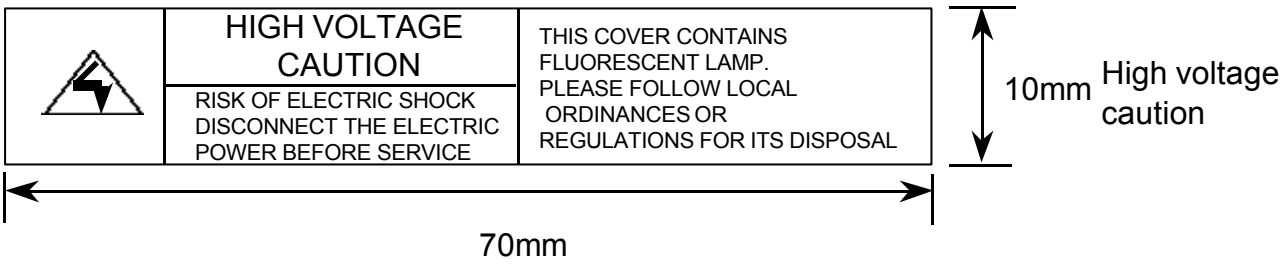
NOTE 1). This code indicating year is omitted in the products of KIHENG site.

(5) Nameplate Indication

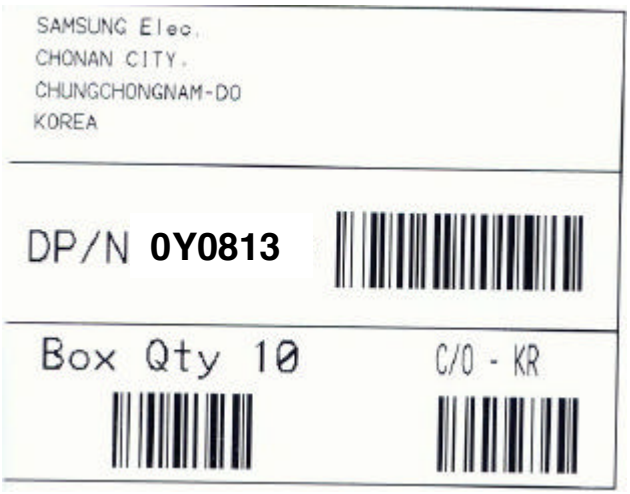


Parts name : LTN150PG - L02
Lot number : 4H3A000000
Inspected work week : 0315
DP/N : Dell Part Number (“**0Y0813**” is for 150PG-L02)
REV.A00 : Product Revision Code

This HIGH VOLTAGE CAUTION is carved in mold frame



(6) Packing box attach



(7) Packing box Marking : Samsung TFT-LCD Brand Name

10. GENERAL PRECAUTIONS

1. Handling

(a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.

(b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and CCFT backlight.

(c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.

(d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(f) The desirable cleaners are water, IPA(Isoprophyl Alcohol) or Hexane.
Do not use Keptone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth . In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(h) Protect the module from static , it may cause damage to the C-MOS Gate Array IC.

(i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(j) Do not disassemble the module.

(k) Do not pull or fold the lamp wire.

(l) Do not adjust the variable resistor which is located on the back side.

(m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(n) Pins of I/F connector shall not be touched directly with bare hands.

2. STORAGE

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C and relative humidity of less than 70%.

(b) Do not store the TFT-LCD module in direct sunlight.

(c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

3. OPERATION

(a) Do not connect,disconnect the module in the " Power On" condition.

(b) Power supply should always be turned on/off by following item 6.3 " Power on/off sequence ".

(c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(d) The cable between the backlight connector and its inverter power supply shall be a minimized length and be connected directly . The longer cable between the backlight and the inverter may cause lower luminance of lamp(CCFT) and may require higher startup voltage(Vs).

4. OTHERS

(a) Ultra-violet ray filter is necessary for outdoor operation.

(b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.

(d) If the module displays the same pattern continuously for a long period of time,it can be the situation when the image " sticks" to the screen.

(e) This module has its circuitry PCB' s on the rear side and should be handled carefully in order not to be stressed.

Appendix 1. EDID

Approval

Address (HEX)	FUNCTION	Value HEX	BIN	DEC	ASCII or Data	Notes
00	Header	00	00000000	0		EDID Header
01		FF	11111111	255		
02		FF	11111111	255		
03		FF	11111111	255		
04		FF	11111111	255		
05		FF	11111111	255		
06		FF	11111111	255		
07		00	00000000	0		
08	ID Manufacturer Name	4C	01001100	76	S	3 character ID
					E	
09		A3	10100011	163	C	"SEC"
0A	ID Product Code	50	01010000	80	P	"P"
0B		47	01000111	71	G	"G"
0C	32-bit serial no.	00	00000000	0		
0D		00	00000000	0		
0E		00	00000000	0		
0F		00	00000000	0		
10	Week of manufacture	00	00000000	0		
11	Year of manufacture	0D	00001101	13	2003	2003
12	EDID Structure Ver.	01	00000001	1	1	EDID Ver. 1.0
13	EDID revision #	03	00000011	3	3	EDID Rev. 3
14	Video input definition	80	10000000	128		
15	Max H image size	1E	00011110	30	30	30.45cm
16	Max V image size	17	00010111	23	23	22.8375cm
17	Display Gamma	78	01111000	120	2.2	Gamma 2.2
18	Feature support		00001010	10		
19	Red/green low bits	87	10000111	135		10000111
1A	Blue/white low bits	F5	11110101	245		11110101
1B	Red x/ high bits	94	10010100	148	0.580	Red x 0.580=
						1001010010
1C	Red y	57	01010111	87	0.340	Red y 0.340=
						0101011100
1D	Green x	4F	01001111	79	0.310	Green x 0.310=
						0100111101
1E	Green y	8C	10001100	140	0.550	Green y 0.550=
						1000110011
1F	Blue x	27	00100111	39	0.155	Blue x 0.155=
						0010011111
20	Blue y	27	00100111	39	0.155	Blue y 0.155=
						0010011111
21	White x	50	01010000	80	0.313	White x 0.315=
						0101000001
22	White y	54	01010100	84	0.329	White y 0.329=
						0101010001
23	Established timing 1	00	00000000	0		
24	Established timing 2	00	00000000	0		
25	Established timing 3	00	00000000	0		

Address (HEX)	FUNCTION	Value HEX	BIN	DEC	ASCII or Data	Notes
26	Standard timing #1	01	00000001	1		not used
27		01	00000001	1		
28	Standard timing #2	01	00000001	1		not used
29		01	00000001	1		
2A	Standard timing #3	01	00000001	1		not used
2B		01	00000001	1		
2C	Standard timing #4	01	00000001	1		not used
2D		01	00000001	1		
2E	Standard timing #5	01	00000001	1		not used
2F		01	00000001	1		
30	Standard timing #6	01	00000001	1		not used
31		01	00000001	1		
32	Standard timing #7	01	00000001	1		not used
33		01	00000001	1		
34	Standard timing #8	01	00000001	1		not used
35		01	00000001	1		
36	Detailed timing/monitor descriptor #1	30	00110000	48	108	Main clock= 108 MHz
37		2A	00101010	42		
38		78	01111000	120	1400	Hor active=700*2 pixels
39		20	00100000	32	288	Hor blanking=288 pixels
3A		51	01010001	81		4bit : 4bit
3B		1A	00011010	26	1050	Vertcal active=1050 lines
3C		10	00010000	16	16	Vertical blanking=16 lines
3D		40	01000000	64		4bit : 4bit
3E		30	00110000	48	48	Hor sync. Offset=24 pixels
3F		70	01110000	112	112	H sync. Width=56 pixels
40		14	00010100	20	1 4	V sync. Offset=1 lines V sync. Width=4 lines
41		00	00000000	0		2bit : 2bit :2bit :2bit
42		30	00110000	48	304	H image size= 304.5 mm(approx)
43		E4	11100100	228	228	V image size = 228.375 mm(approx)
44		10	00010000	16		
45		00	00000000	0		No Horizontal Border
46		00	00000000	0		No Vertical Border
47		19	00011001	25		
48	Detailed timing/monitor	00	00000000	0		Manufacturer Specified (Timing)
49		00	00000000	0		
4A		00	00000000	0		
4B		0F	00001111	15		
4C		00	00000000	0		
4D		00	00000000	0		**Value** =HSPWmin / 2
4E		00	00000000	0		**Value** =HSPWmax / 2
4F		00	00000000	0		**Value** =Thbpmin /2

Approval

Address (HEX)	FUNCTION	Value HEX	BIN	DEC	ASCII or Data	Notes
50	descriptor #2	00	00000000	0		**Value** =Thbpmax /2
51		00	00000000	0		**Value** =VSPWmin /2
52		00	00000000	0		**Value** =VSPWmax /2
53		00	00000000	0		**Value** =Tvbpmin / 2
54		00	00000000	0		**Value** =Tvbpmax / 2
55		0F	00001111	15		Thpmin= **value** *2 + HA pixelclks
56		F2	11110010	242		Thpmax= **value** *2 + HA pixelclks
57		02	00000010	2		Tvpmin= **value** *2 + VA lines
58		4B	01001011	75		Tvpmax= **value** *2 + VA lines
59		00	00000000	0		Module revision
5A		00	00000000	0		
5B		00	00000000	0		
5C		00	00000000	0		ASCII Data String Tag
5D		FE	11111110	254		
5E		00	00000000	0		
5F		59	01011001	89	[Y]	
60		30	00110000	48	[0]	
61	Detailed timing/monitor	38	00111000	56	[8]	
62	descriptor #3	31	00110001	49	[1]	
63		33	00110011	51	[3]	
64		03	00000011	3	3	
65		31	00110001	49	[1]	
66		35	00110101	53	[5]	
67		30	00110000	48	[0]	
68		50	01010000	80	[P]	
69		47	01000111	71	[G]	
6A		0A	00001010	10	[^]	
6B		20	00100000	32	[ ]	
6C		00	00000000	0		
6D		00	00000000	0		
6E		00	00000000	0		Monitor Name Tag (ASCII)
6F		FE	11111110	254		
70		00	00000000	0		
71		CE	11001110	206		
72		C6	11000110	198		
73	Detailed timing/monitor	BA	10111010	186		
74	descriptor #4	AB	10101011	171		
75		95	10010101	149		
76		77	01110111	119		
77		4D	01001101	77		
78		12	00010010	18		
79		01	00000001	1		
7A		0A	00001010	10		
7B		20	00100000	32		
7C		20	00100000	32		
7D		20	00100000	32		
7E	Extension Flag	00	00000000	0		
7F	Checksum	**AF**	10101111	175		

Approval Inverter Specification for P2

SEC : LTN150XC-L01 / LTN150PG-L02

2003. 03. 25

REV. 0.0

- Inverter Input Voltage Range : 7.5 ~ 21V

2003. 04. 24

REV. 0.1

- Lamp Current

Max : 6.0(± 0.3)mA → **2.0**(± 0.3)mA

6.3(± 0.3)mA

Min : 1.8(± 0.3)mA →

1. General

This specification should be used as a guideline for designing the inverter used in P2 Program.

Brightness control method of inverter should be PWM(Burst) mode control.

1.1 Model

Type	Samsung Part Number	Supplier Part Number	Remark
TFT_LCD	LTN150XC-L01 LTN150PG-L02		

2. Specification

2.1 General electrical specification

Referenced Panels: Samsung TFT-LCD

Item		Minimum	Typical	Maximum	Remarks
Input voltage(Vin)		7.5 V	14.4V	21.0 V	
Open Circuit Voltage		1.4kVrms	-	1.8kVrms	
Lamp voltage		-	655Vrms	-	
Lamp Current		2.0 ± 0.3 mArms @ SMB_DAT FFH	-	6.3± 0.3 mArms @SMB_DAT 00H	Vin = 7.5 ~ 21.0V
Dimming Duty Cycle		10(± 2%)		100%	
Efficiency	**Optical**	20nits/W	-	-	After 30min turn on at the center of the LCD. Vin = 14.4V, Iout=6.0mArms
	Electrical	-	80%	-	
Operating Frequency		45 kHz	55kHz	65kHz	
PWM Frequency			210 ± 10Hz		
Input Power Consumption		-	-	5.7W	Vin = 14.4V, Iout = 6.0mArms SMB_DAT=00H
In-rush current		-	-	1.5A	
Shutdown time		0.6sec	1.0sec	1.4sec	
Start-up time				0.1sec	

2.2 Connectors

2.2.1 Backlight connector (CN1)

2.2.1.1 Backlight connector CN1 must be same as table 1.

Connector Maker	Connector Part No.	Remark
JST	**SM02B-BHSS-1-TB**	

2.2.1.2 Pin assignment

2.2.1.2.1 SM02B-BHSS-1-TB

Pin No	Symbol	Description	Remark
1	**HV**	**Power supply for CCFL**	
2	**RTN**	**Return**	

2.2.2 Input connector(CN2)

It must be a **HONDA, LVC-D20SFYG** 20pin connector, and the pin assignment is ;

Input connector		Voltage	Comments
HONDA	**LVC-D20SFYG**		
Pin	**Function**		
1	INV_SRC	7.5V to 7.5V to 21V	This power rail should be used as a power rail to drive the backlight DC-AC converter
2			This power rail should be used as a power rail to drive the backlight DC-AC converter
3	INV_SRC	7.5V to 21V	This power rail should be used as a power rail to drive the backlight DC-AC converter
4	NC	-	No Connection
5	GND		Ground
6	5VSUS	5V	This should be used as power source for the control circuitry on the inverter
7	5VALW	5V	This should be used as power source that stores the brightness/contrast values & the circuit that interfaces with SMB_CLK & SMB_DAT
8	GND		Ground
9	SMB_DAT		SMBus interface for sending brightness & contrast information to the inverter/panel
10	SMB_CLK		SMBus interface for sending brightness & contrast information to the inverter/panel
11	GND		Ground
12	FPBACK		Control signal input into the inverter to turn the backlight ON & OFF (1 - ON, 0 – OFF)
13	GND		Ground

14	LAMP_STAT		Lamp Status, on(High)/off(Low), from control chip
15 ~ 20	NC		No Connection

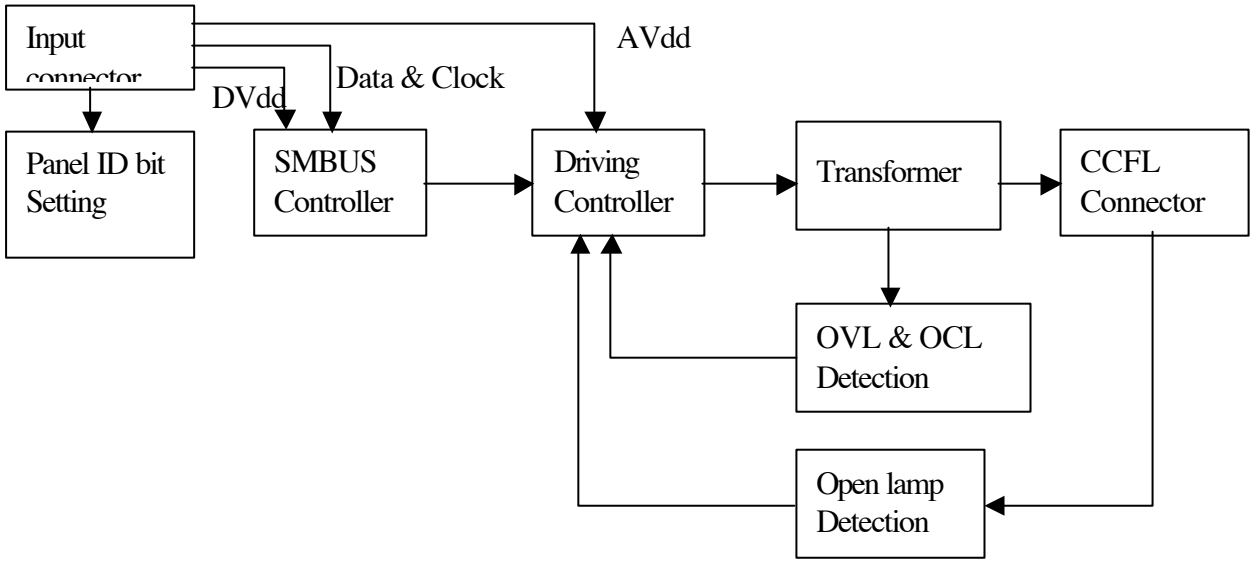
2.2.3 SMBUS Address Definition

Table 9.8 SMBus address definition for brightness & contrast

Device Identifier				Device Address			Read/Write Bit
0	1	0	1	A2	A1	A0	R/W=0

Inverter SMBUS Address	**A2**	**A1**	**A0**
Address = 58H	1	0	0
Recommend using Dallas Semiconductor DS1803 (Dual digital potentiometer) or equivalent function IC. Use Wiper 0 for contrast control & Wiper 1 for brightness (Backlight) control in case DS1803.			

2.2.4. Circuit Block Diagram



3.0 Safety Requirement

Inverter must comply with UL1950 3rd edition, CSA22.2 No. 950-95, EN60950-1992 + A1 & A2 and other applicable regulations.

The inverter has several safety critical components due to high voltage. See list and associated comments:

PWB : The PWB must be UL Recognized and have a 94V-1 or V-0 rating.

Transformer : Bobbin and other plastic parts must be UL Recognized and have appropriate temperature ratings for the application. Plastic must have 94V-1 or V-0 Flame Rating.

High Voltage Capacitors : Must have adequate ratings for the application.

Fuse : Must be UL Listed with appropriate ratings for application.

Output Connector(s) : Must be UL Recognized. Must provide adequate spacing from pin to pin for high voltage.

Note) It is preferable that the inverter be a UL Recognized assembly. If assembly is not UL Approved, then a CFM (Confirmation List of Material) must be provided with each shipment of inverters providing manufacturer identification and material/part identification for each critical part.

4.0 Emissions Requirements

Inverter design must be such that is does not prevent host product from complying with CFR47-Part 15 Class B Limits, CISPR-22 Class B Limits, and EN55022 Class B Limits. Consideration should be given to high frequency signals, ringing on signals, filtering of ground and voltage lines, and use of good high frequency grounding techniques.

5.0 Immunity Requirements

Inverter Design must be such that it does not prevent host product from complying with EN50082-1 Generic Immunity Requirements for European Union. This includes ESD, EFT, FRI, Surge, Harmonics, and Flicker.

6.0 Reliability

Minimum MTBF: 10,000 Hrs min @ 25C +/- 1C, 60% RH.

7.0 Mechanical Spec.

7.1 Drawing - Refer to separate drawing.

Inverter Layout Drawing

Please see attached drawing

Appendix A. Inverter Design Features (Inverter design – checklist)

Following table outlines the desired features and design checklist of the inverter.

Item	Feature	Description
1	Soft-start	Lamp should soft start.
2	Short/Open detection	Lamp out (mechanical broken) detection should be provided.
3	Over current protection	Over current protection : Must be checked at all temperature/voltage extremes
4	Over voltage Protection	Over voltage protection : Must be checked at all temperature/voltage extremes And have a stable cut off point.
5	Start-up time Control	Good start-up transient response
6		If dual conversion stage is used both stages shall synchronize
7		There is no indication that the inverter design must be tuned to the bulb.
8		Verify that Strike time and Strike voltage meet the Panel specification
9		The inverter board is designed with test nodes and an ICT fixture is in place to Verify that all components are within the design tolerances.
10		Four corner testing (Voltage vs. Temperature) has been performed on several Inverters using a lamp with components (i.e. BJT & Zener Diodes from different build lots
11		Four corner testing (min. & max.Voltage vs. Temperature) has been performed on several Inverters not using a lamp with components (i.e. BJT & Zener Diodes) from different build lots.
12		Efficiency should be measured – in side the panel and outside of the panel. Results should be analyzed and circuit modified, if the difference between efficiencies is too great.
13		Test inverter over the operating temperature inside the panel. (Notebook operating temperature ambient of 0 to 40 °C
14		Check stress factors on critical components (i.e. voltage and power ratings).
15 16		Panel should be observed in all display modes to ensure that pattern interference is not present. Look for this in the area of the panel that is closest to the bulb. This is sometimes termed as beat frequencies problem. Abnormal what if analysis must be performed. For e.g. what happens if a component opens, shorts? The goal here is to make sure that failures do not result in safety issues.
17		Obtain drawings of key components, Transformer, inductor, ballast cap, valves, resonant cap etc. Verify that none of the aforementioned is over stressed.
18		Check thermals, to ensure that hotspots are not present, such that the customer can feel heat through the plastics, or display discoloration results.
19		Ensure that the inverter can not be heard (humming or clicking noises) and that control loop is stable
20		EMI recommendation: 1.The GND on the inverter board should be connected to the display metal which should be connected to the notebook system GND. This should be achieved through a secure mechanism such as a screw, copper washer etc. and NOT using conducting foam or copper tape. 2.The ground of the inverter should also be positively connected to the GND on the source PCBs on the panel. The GND point should be physically close to the input connector of the inverter.

Appendix B. CCFL Specification

Our Backlight system is an edge-lighting type with single CCFT(Cold Cathode Fluorescent Tube)Lamp . The characteristics of single lamp are shown in following table.

1. LTN150XC-L01/LTN150PG-L02

Items	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp current	I_L	2.0	6.0	7.0	mArms	Note1, 2
Lamp Voltage	V_L	-	655	-	Vrms	+/-5% @ I_L=6.0mA
Lamp power	Pcfl	-	3.93	-	Watt	@ I_L=6.0mA
Lamp frequency	Fcfl	45	60	80	kHz	Note 3
Kick-off Voltage	Vs	-	-	1150	Vrms	Ta=25°C
		-	-	1380		Ta=0°C
Life time	Hlife				Hour	Note4, @ I_L=6.0mA
CCFL turn on time	Ton	-	-	0.5	msec	

Note1. If CCFT lamp was flowed below minimum current, lamp become unstable for ignition.
And if the CCFT lamp was flowed over maximum current, lamp life time should be shorter than normal condition.

Note2. At the condition of luminance YL=TBD cd/m2 on TFT-LCD Panel output.

Note3. Lamp frequency may produce interference with Horizontal synchronous frequency and this may cause beat on the display. Therefore lamp driving frequency shall be detached as much as possible from the horizontal synchronous frequency and its harmonics to avoid interference.

Note4. Lamp life time is defined as the time when either A or B occur in the continuous operation under the condition of Ta=25°C and at maximum current.

A) Brightness becomes 50% of the original value.
B) Kick-off voltage at Ta=0°C exceeds maximum value.

Appendix C. P2 Inverter Test Plan.

1. Functional Test Items

Check Items	Split Condition	Sample Quantity	Test Condition	Remark
Output current (Min, Max) & Output deviation	Input voltage Vin=7.5V, 14.4V, 21V Temperature Ta=0°C, Ta=25°C, Ta=50°C	5	SMB_DAT=00H SMB_DAT=FFH	
Output Voltage	Output current SMBUS_DAT=FFH and 00H Temperature Ta=0°C, Ta=25°C, Ta=50°C	5	Input voltage Vin=7.5V, 14.4V, 21V	
Input Power	Output current SMBUS_DAT=FFH and 00H Temperature Ta=0°C, Ta=25°C, Ta=50°C	5	Input voltage Vin=7.5V, 14.4V, 21V	
Kick-off Voltage & Operating freq.	Temperature Ta=0°C , Ta=25°C Ta=50°C	5	Vin=14.4V, SMB_DAT=00H No load condition	
Shutdown time	Temperature Ta=0°C , Ta=25°C, Ta=50°C	5	Vin=14.4V, SMB_DAT=00H Open voltage detection & shutdown time check	
Turn-on time	Ta=0°C , Ta=25°C, Ta=50°C	5	SMB_DAT=00H	
Electrical Efficiency	Output current 6mA(00H) Temperature Ta=0°C, Ta=25°C, Ta=50°C	5	Vin=14.4V, SMB_DAT=00H	
Optical Performance (Nits/W)	Output current SMBUS_DAT= 00H Temperature Ta=0°C, Ta=25°C, Ta=50°C	5	Vin=14.4V, SMB_DAT=00H	SEC test only
Stress Factor	Critical components	5	Voltage and power rating	
Display pattern check	SEC standard test pattern	5		SEC test only
Acoustic noise	Humming & clicking noise	5		
Temperature rise Measurement	Power on 2 hours under 25±5°C 60±5°C, measure key component' s body temperature.	5	Vin=14.4V, SMB_DAT=00H	

All functional test will perform by inverter supplier and LCD manufacturer(SEC).
And both company should be correct test results.

2. Reliability Test Items

No	Items	Test Condition	Sample size	Check Point
1	High temp. operation	Power on at max. input with load. Operation at Ta=50°C, 500Hours SMB_DAT=00H, 95%RH	20	Function test
2	Low temp. operation	Power on at min. input with load. Operation at Ta=0°C,500hours SMB_DAT=00H	20	Function test
3	High temp. storage	Power off High temperature 85°C, 500hours	10	Function test
4	Low temp. storage	Power off Low temperature –20°C, 500hours	10	Function test
5	Thermal Cycle	Power off storage Ta=-20°C(30min) ⇔ Ta=60°C(30min) 100cycles	20	Function test
6	Power On/Off test	Max. input & min. input. Power on full load(SMB_DAT= 00H) 10sec On/10sec Off, 30,000cycle	10 each	Function test
7	Signal On/Off test	Signal HI(SMB_DAT=00H), 10sec Signal Low(SMB_DAT=FFH), 10sec Max. Vinput, Power on full load. 30,000cycle	10	Function test
8	Hot Start test	After storage at Ta=50°C for 2hour, Then power on at min. Vinput, max. Ioutput. 10times.	10	Function test
9	Cold Start test	After storage at Ta=0°C for 2hour, Then power on at min. Vinput, min. Ioutput. 10times	10	Function test
10	PCB bending test	PCB bending rate : 1mm max.	20	Cosmetic inspection
11	MTBF demo stress Test	Power on at Ta=60°C Max. input voltage, Full load operation	100	MTBF
12	Vibration test (Storage)	2G, 10~500Hz, 30min. 500Hz~10Hz, 30min .	10	Function test

3. TEST Schedule

ITEM	D+1W	D+2W	D+3W	D+4W	D+5W	D+6W	D+7W	D+8W	remark
Functional test	Test by SEC/Maker →								
Reliability test		Test by Maker, 500hours →							
Long life test			Test by Maker, 1,000hours →						