



## ENGINEERING SPECIFICATIONS

### TFT COLOR LCD MODULE

#### TM396WX-71N31

- 101 cm (39.6 inch) diagonal
- XGA-Wide resolution (1280 x 768 pixels)
- Wide View Angle (SVA)
- LVDS Interface (RGB x 8 bits x 2 channels)
- Display Color: 16,777,216 colors (8 bits)
- With CFL backlight unit and Inverter
- Nonglare surface type

(TENTATIVE)

Ver. 6

June.10, 2003

SANYO Electric Co., Ltd.

LCD Business Unit

LCD Division



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## REVISION HISTORY

DATE	REVISION NO.	PAGE	DESCRIPTIONS
Nov. 28, 01	Ver. 1	-	Initial Release
Jan. 30, 02	Ver. 2	2	MECHANICAL CHARACTERISTICS (Thickness and Weight)
		3	ELECTRICAL CHARACTERISTICS of LOGIC (Power supply current IDD) ELECTRICAL CHARACTERISTICS of INVERTER (Power supply current IDDB and Operating frequency FO)
		14	INTERFACE SIGNAL TIMING PARAMETERS (DE_MODE) (Frequency fCLK of ODCLK and EDCLK)
		21	OUTER DIMENSIONS (Location and profile of mounting studs, and Thickness)
Apr. 26, 02	Ver. 3	2	ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS (Add the description of Vibration and Shock)
		3-4	ELECTRICAL CHARACTERISTICS of INVERTER (Add the description of External brightness control mode)
		5	EXTERNAL BRIGHTNESS CONTROL SEQUENCE REQUIREMENT LAMP LIFE
		6	OPTICAL CHARACTERISTICS (Define the measurement condition "(5) Inverter input", and Add the definition of brightnesses uniformity , and Change the measurement points of brightness)
		8	BLOCK DIAGRAM
		22	OUTER DIMENSIONS (Add back side drawing)
Sep. 5, 02	Ver. 4	3	ELECTRICAL CHARACTERISTICS of LOGIC (Power supply current: 850mA(Typ) → 750mA (Typ), 1400mA(Max) → 1800mA (Max)) ELECTRICAL CHARACTERISTICS of INVERTER (Power supply current of Max. Brightness and Min. Brightness, and Operating frequency) (Add the description about protection circuit of power source in Note 2)
		6	OPTICAL CHARACTERISTICS (Color of CIE Coordinate: (xW, yW)=(0.313, 0.329) → (0.280, 0.290))
		23	OUTER DIMENSIONS (Add back side Rev.C drawing) (Running change from Back Side Rev.B to Rev.C between September and October in 2002.)
Nov. 29, 02	Ver. 5	3	ELECTRICAL CHARACTERISTICS of INVERTER (Change the value of Power supply current)
		22	OUTER DIMENSIONS (Change the shape of inverter cover.)
		23	OUTER DIMENSIONS (Remove the page of Back Side Rev.B drawing)
Jun. 10, 03	Ver. 6	3	ELECTRICAL CHARACTERISTICS of LOGIC (The condition is specified.)
		6	OPTICAL CHARACTERISTICS (The condition is specified. Change and/or add the Max. and/or Min. values of optical characteristics)
		14	INTERFACE SIGNAL TIMING PARAMETERS ( DE_MODE ) (Add the Horizontal Frequency, Vertical Frequency and Note 4)
		18	PRECAUTIONS (INSTRUCTIONS FOR SAFE AND PROPER USE) (Add the description of 2-(9) and 2-(10))

## ***MECHANICAL CHARACTERISTICS***

Ta=25°C

ITEM	SPECIFICATION	UNIT
Module size	920.0(W) x 580.0(H) x 50.5 Max.(t)	mm
Resolution	1280 x RGB(W) x 768(H)	pixel
Sub pixel pitch	0.2245(W) x 0.6735(H)	mm
Pixel pitch	0.6735(W) x 0.6735(H)	mm
Active viewing area	862.080(W) x 517.248(H)	mm
Bezel opening area	866.7(W) x 524.4(H)	mm
Weight	14800 Typ.	g

## ***ELECTRICAL ABSOLUTE MAXIMUM RATINGS***

Ta=25°C

ITEM	SYMBOL	MIN	MAX	UNIT	NOTE
Power supply voltage	VDD-VSS	-0.3	6.0	V	Logic
	VDD-B-VSS	0.0	17.0	V	Inverter
Input voltage	VI	VSS -0.3	VDD +0.5	V	Logic
	VIB	VSS -0.3	VSS +7.0	V	Inverter

## ***ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS***

ITEM	SYMBOL	CONDITIONS	MIN	MAX	UNIT	NOTE
Ambient temperature	TST	Storage	-20	60	°C	Note 1
	TOP	Operation	0	50		
Humidity	-	Ta=40°C Max.	-	85	%RH	No condensation Note 2
Vibration	-	Storage	-	1.5	G	Note 3
Shock	-	Storage	-	50	G	XYZ 11ms/direction

[Note 1] Care should be taken so that the LCD module may not be subjected to the temperature beyond this specification.

[Note 2] Ta>40°C: Absolute humidity shall be less than that of 85%RH/40°C.

[Note 3] 10-200Hz, 30min/cycle, X/Y/Z each one cycle and except for resonant frequency.

## ***ELECTRICAL CHARACTERISTICS of LOGIC***

fCLK=40.2MHz, fH=48.3kHz, fV=60Hz, Ta=25°C

ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Power supply voltage	VDD-VSS		4.5	5.0	5.5	V	
Power supply current	IDD	Note 1		750	1800	mA	VDD=5.0V
LVDS Input logic voltage	VTH	High level	-	-	+100	mV	VDD=5.0V VCM=1.2V
	VTL	Low level	-100	-	-		
LVDS Input common mode voltage	VCM		1.0	1.2	1.4	V	VDD=5.0V
LVDS input termination resistor	RT		-	100	-	Ω	Internal

[Note 1] Display pattern of typical power supply current is 256 gray scale bar.

## ***ELECTRICAL CHARACTERISTICS of INVERTER***

This module has two inverters. The characteristics of single inverter are shown below.

Ta=25°C

ITEM		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Power supply voltage		VDD-B-VSS		13.0	14.0	15.0	V	
Power supply current		IDDB	Max. Brightness	5000	6000	7000	mA	VDD-B =14V
			Min. Brightness	1000	2000	3000		
Operating frequency		FO	Max. Brightness	54	60	66	kHz	
Internal PWM frequency		FBI		250	270	290	Hz	
External PWM frequency		FBE		50	-	300	Hz	
Backlight ON/OFF control (BLTC) voltage	ON	VHBLTC	or Open	2.0	-	5.0	V	
	OFF	VLBLTC		0.0	-	0.8		
Backlight ON/OFF control (BLTC) current		IBLTC		-1.0	-	1.5	mA	
Internal/External PWM select (PWSEL) voltage	Int.	VHPWSEL	or Open	2.0	-	5.0	V	
	Ext.	VLPWSEL		0.0	-	0.8		
Internal/External PWM select (PWSEL) current		IPWSEL		-1.0	-	1.5	mA	
Internal PWM brightness control (BRT2) voltage	Max.	VHBRT2	BRT1=VSS	-	1.0	-	V	
	Min.	VLBRT2		-	0.0	-		
Internal PWM brightness control (BRT2) current		IBRT2		-1.0	-	1.5	mA	
External PWM brightness control (B RTP) voltage	High	VHB RTP	PWSEL=L	2.0	-	5.0	V	
	Low	VLB RTP		0.0	-	0.8		
External PWM brightness control (B RTP) current		IB RTP			-1.0	-	1.5	mA
External PWM duty		DB RTP			30	-	100	%

[Note 1] The measurement is a result after 15 minutes of lighting.

[Note 2] The current capacity of power source for one inverter should be 20A or higher.

When power source capacity is lower than 20A, the protector circuit in inverter may not operate in case of a trouble. Therefore total current capacity of power source for this LCD module should be 40A or higher, because this module has two inverters.

If the power source of current capacity under above value, the protector circuit such as shutdown circuit at over current occurrence is necessary in power source.

[Note 3] The inverter generates heat at Backlight ON and causes temperature rise.

Therefore, take necessary heat radiating design to meet the specified operating temperature range for LCD module inside your system.

[Note 4] Backlight driving conditions (lamp operating frequency FO especially) may

interfere with horizontal frequency fH, causing the beat or flicker on the display. Therefore the horizontal frequency fH shall be adjusted in relation to lamp operating frequency FO to avoid interference.

### ***BACKLIGHT ON/OFF CONTROL (BLTC) FUNCTIONS***

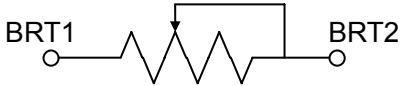
ITEM	INPUT	FUNCTION
BLTC	High level or Open	Backlight ON
	Low level	Backlight OFF

[Note 1] The function of BLTC is valid when Backlight power is ON.

### ***INTERNAL/EXTERNAL PWM SELECT (PWSEL) FUNCTIONS***

ITEM	INPUT	FUNCTION
PWSEL	High level or Open	Internal PWM Brightness Control mode
	Low level	External PWM Brightness Control mode

### ***INTERNAL PWM BRIGHTNESS CONTROL (BRT1, BRT2) FUNCTIONS***

ITEM	INPUT	FUNCTION
BRT1 BRT2	Volume Control: The Variable Resistor of 10K $\Omega$ type should be connected between BRT1 and BRT2. Brightness can be controlled by the value of resistance. 	Resistance value: 0 $\Omega$ : Minimum Brightness 10K $\Omega$ : Maximum Brightness
	Voltage Control: Brightness can be controlled by the value of input voltage between BRT1 and BRT2. BRT1: should be fixed to VSS BRT2: should be applied variable voltage	Voltage value: 0V: Minimum Brightness 1V: Maximum Brightness

[Note 1] The function of BRT1 and BRT2 are valid when PWSEL is High level or Open and B RTP is Open.

[Note 2] When the VDDB and BLTC are off, BRT2 should not be applied voltage.

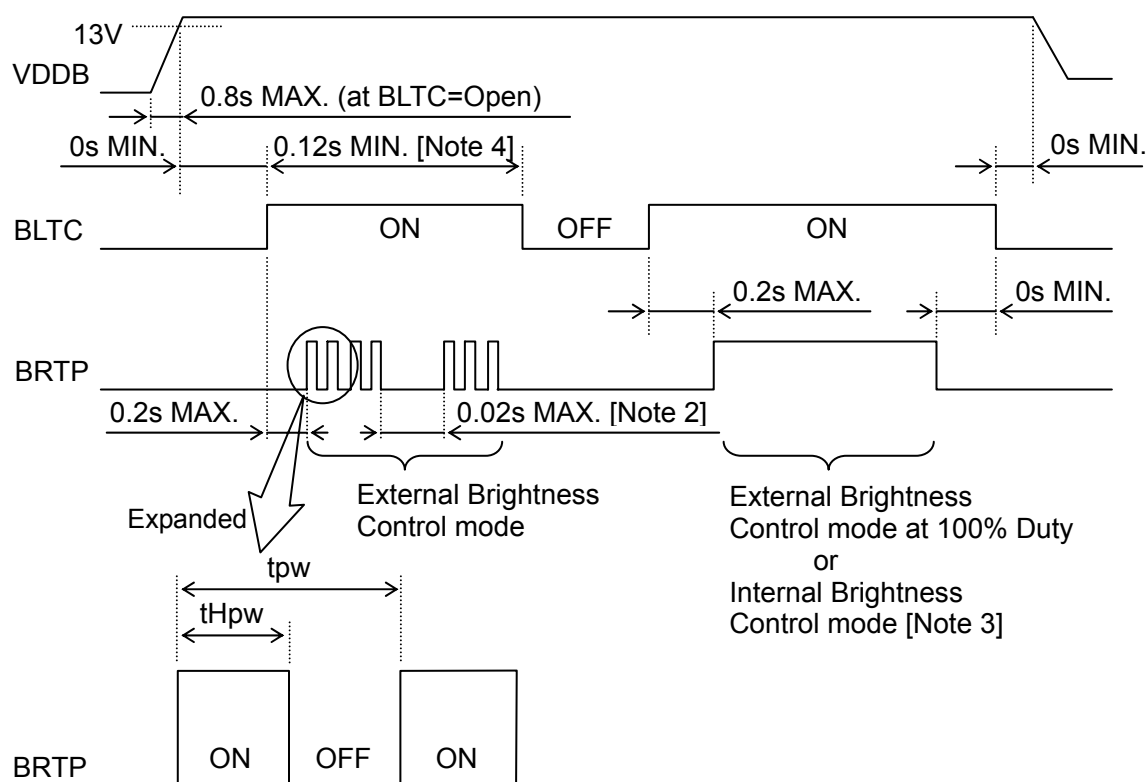
### ***EXTERNAL PWM BRIGHTNESS CONTROL (B RTP) FUNCTIONS***

ITEM	INPUT	FUNCTION
B RTP	Duty Control: Brightness can be controlled by the duty of input B RTP signal.	Duty value: 30%: Minimum Brightness 100%: Maximum Brightness

[Note 1] The function of B RTP is valid when PWSEL is Low level.

[Note 2] When the VDDB and BLTC are off, B RTP should not be applied voltage.

## EXTERNAL PWM BRIGHTNESS CONTROL SEQUENCE REQUIREMENT



[Note 1] External PWM duty  $DBRTP = tHpw / tpw$  : 30 - 100 %  
 External PWM frequency  $FBE = 1/tpw$  : 50 - 300 Hz

[Note 2] In External Brightness Control mode (BLTC=H, PWSEL=L), when the period of B RTP=L is more than 20 ms, Backlight turns off by protection circuit in inverter. In this case, even if B RTP=H is input again, Backlight will not turned on. Please input Power supply VDDB or BLTC again.

[Note 3] In Internal Brightness Control mode (BLTC=H, PWSEL=H or Open), B RTP must be High level or Open. If B RTP is Low, It gives priority to B RTP=L over Internal brightness control mode and Backlight turns off.

[Note 4] When the period of BLTC=H is under 120ms, Backlight isn't turned on normally because rush current prevention circuit functions. Therefore, the period of BLTC=H should be more than 120ms.

## LAMP LIFE

This module has the direct type backlight with 32 cold cathode fluorescent Lamps (CCFL). The life time of single Lamp is shown below.

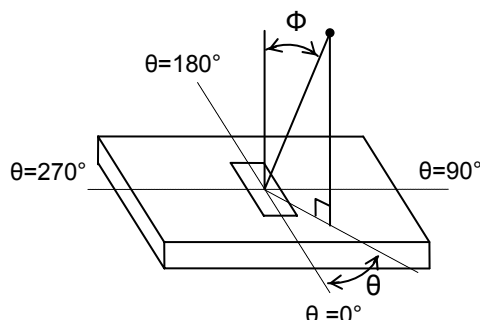
ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Lamp Life	tOL	Ta=25±2°C Max. Brightness	50000	-	-	hrs	

## OPTICAL CHARACTERISTICS

VDD=5.0V, fCLK=40.2MHz, fH=48.3kHz, fV=60Hz, Ta=25°C

ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Brightness	B	$\Phi = 0^\circ$	350	500	-	cd/m <sup>2</sup>	Note 4,8
Brightness uniformity	$\delta B$	$\Phi = 0^\circ$	-	-	1.30	-	Note 5,6,8
Contrast ratio	CR	$\Phi = 0^\circ$	400	600	-	-	Note 2,4,8
Viewing angle range	$\Phi$	CR>10	$\theta = 0^\circ$	70	85	-	deg. Note 1,2,4,8
			$\theta = 90^\circ$	70	85	-	
			$\theta = 180^\circ$	70	85	-	
			$\theta = 270^\circ$	70	85	-	
Response time	Rise	tr	$\Phi = 0^\circ$	-	14	40	ms. Note 3,4,8
	Fall	tf		-	8	20	
Color of CIE Coordinate	Red	x	$\Phi = 0^\circ$	0.614	0.664	0.714	- Note 4,8
		y		0.280	0.330	0.380	
	Green	x		0.236	0.286	0.336	
		y		0.552	0.602	0.652	
	Blue	x		0.091	0.141	0.191	
		y		0.011	0.061	0.111	
	White	x		0.250	0.280	0.310	
		y		0.260	0.290	0.320	
Color gamut	C	$\Phi = 0^\circ$ , to NTSC	-	75	-	%	Note 4,8

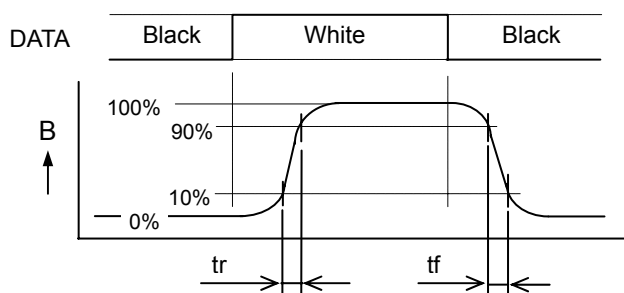
[Note 1] Definition of “ $\Phi$ ” and “ $\theta$ ”



[Note 2] Definition of Contrast ratio “CR”

$$CR = \frac{\text{Brightness at White}}{\text{Brightness at Black}}$$

[Note 3] Definition of Response time “tr” and “tf”



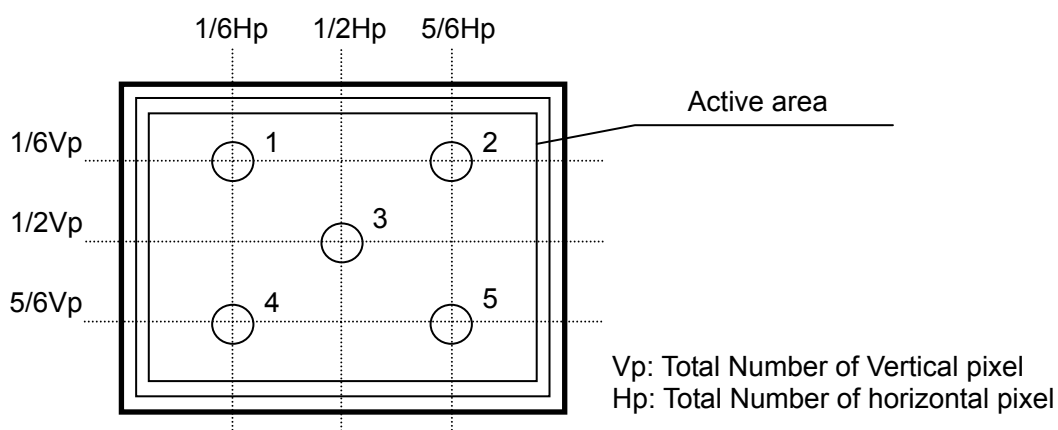
[Note 4] This shall be measured at center (point No.3 shown in Note 7).

[Note 5] This shall be measured at five points shown in Note 7.

[Note 6] Definition of Brightness uniformity “ $\delta_B$ ”

$$\delta_B = \frac{\text{Maximum brightness of five points}}{\text{Minimum brightness of five points}}$$

[Note 7] Measurement points

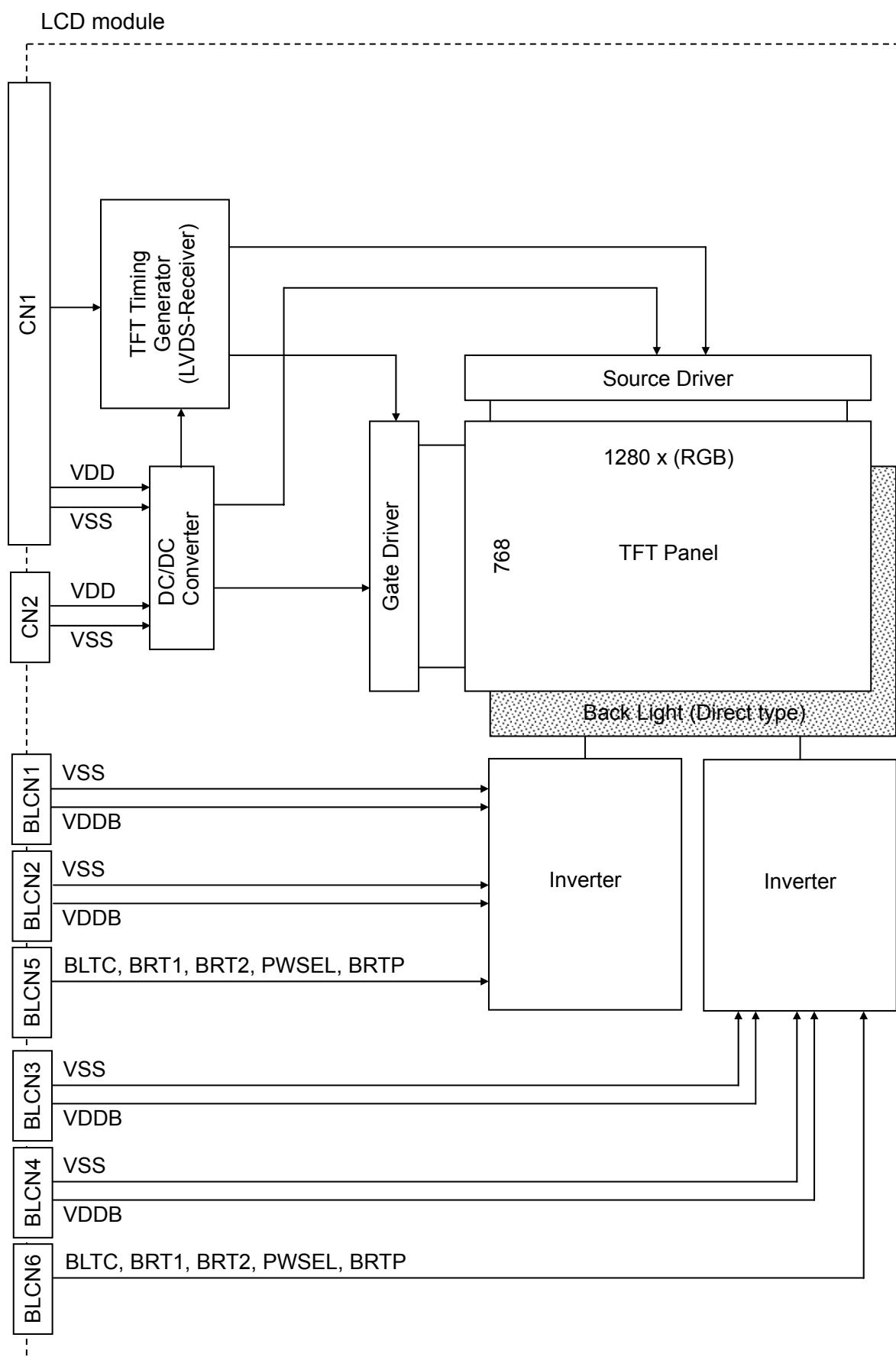


[Note 8] Measurement condition

- (1) Measurement equipment: BM-5A (TOPCON Corp.), Field=2°
- (2) Ambient temperature Ta: 25±2°C
- (3) LCD: All pixels are White or Black or Red or Green or Blue, VDD=5.0V, fCLK=40.2MHz, fH=48.3kHz, fV=60Hz
- (4) Measure after 30 minutes of Lamp warm up.
- (5) Inverter input: VDDB=14.0V, Maximum Brightness



# BLOCK DIAGRAM



## INTERFACE PIN CONNECTIONS of LOGIC

### LCM : CN1

PIN NO.	SYMBOL	FUNCTION
1	RX00-	Negative Transmission Data of Pixel 0 (ODD data)
2	RX00+	Positive Transmission Data of Pixel 0 (ODD data)
3	RX01-	Negative Transmission Data of Pixel 1 (ODD data)
4	RX01+	Positive Transmission Data of Pixel 1 (ODD data)
5	RX02-	Negative Transmission Data of Pixel 2 (ODD data)
6	RX02+	Positive Transmission Data of Pixel 2 (ODD data)
7	VSS	Power Ground
8	RXOC-	Negative Sampling Clock (ODD data)
9	RXOC+	Positive Sampling Clock (ODD data)
10	RX03-	Negative Transmission Data of Pixel 3 (ODD data)
11	RX03+	Positive Transmission Data of Pixel 3 (ODD data)
12	RXE0-	Negative Transmission Data of Pixel 0 (EVEN data)
13	RXE0+	Positive Transmission Data of Pixel 0 (EVEN data)
14	VSS	Power Ground
15	RXE1-	Negative Transmission Data of Pixel 1 (EVEN data)
16	RXE1+	Positive Transmission Data of Pixel 1 (EVEN data)
17	VSS	Power Ground
18	RXE2-	Negative Transmission Data of Pixel 2 (EVEN data)
19	RXE2+	Positive Transmission Data of Pixel 2 (EVEN data)
20	RXEC-	Negative Sampling Clock (EVEN data)
21	RXEC+	Positive Sampling Clock (EVEN data)
22	RXE3-	Negative Transmission Data of Pixel 3 (EVEN data)
23	RXE3+	Positive Transmission Data of Pixel 3 (EVEN data)
24	VSS	Power Ground
25	NC	No Connection
26	DE	DE Output
27	NC	No Connection
28	VDD	Logic Power Supply (5.0V normal)
29	VDD	Logic Power Supply (5.0V normal)
30	VDD	Logic Power Supply (5.0V normal)

CN1: FI-X30S-HF (JAE)

Suitable mating connector: FI-X30M/FI-X30H/FI-X30C (JAE)

[Note 1] Internal termination resistors of LVDS input lines are 100Ω.

### LCM : CN2

PIN NO.	SYMBOL	FUNCTION
1	VDD	Logic Power Supply (5.0V normal)
2	VDD	Logic Power Supply (5.0V normal)
3	VDD	Logic Power Supply (5.0V normal)
4	VDD	Logic Power Supply (5.0V normal)
5	VDD	Logic Power Supply (5.0V normal)
6	VDD	Logic Power Supply (5.0V normal)
7	VSS	Power Ground
8	VSS	Power Ground
9	VSS	Power Ground
10	VSS	Power Ground
11	VSS	Power Ground
12	VSS	Power Ground

CN1: 53261-1290 (MOLEX)

Suitable mating connector: 51021-1200 (MOLEX)

[Note 1] If the current capacity of the cable connected with VDD input pin of connector CN1 isn't enough, Connector CN2 should be used.

## ***INTERFACE PIN CONNECTIONS of INVERTER***

### **Inverter: BLCN1, BLCN2, BLCN3, BLCN4**

PIN NO.	SYMBOL	FUNCTION
1	VSS	Power Ground
2	VSS	Power Ground
3	VSS	Power Ground
4	VSS	Power Ground
5	VSS	Power Ground
6	VDDDB	Backlight Power Supply (14.0V normal)
7	VDDDB	Backlight Power Supply (14.0V normal)
8	VDDDB	Backlight Power Supply (14.0V normal)
9	VDDDB	Backlight Power Supply (14.0V normal)
10	VDDDB	Backlight Power Supply (14.0V normal)

BLCN1, BLCN2, BLCN3, BLCN4: DF3-10P-2H (HIROSE)

Suitable mating connector: DF3-10S2R26 (HIROSE)

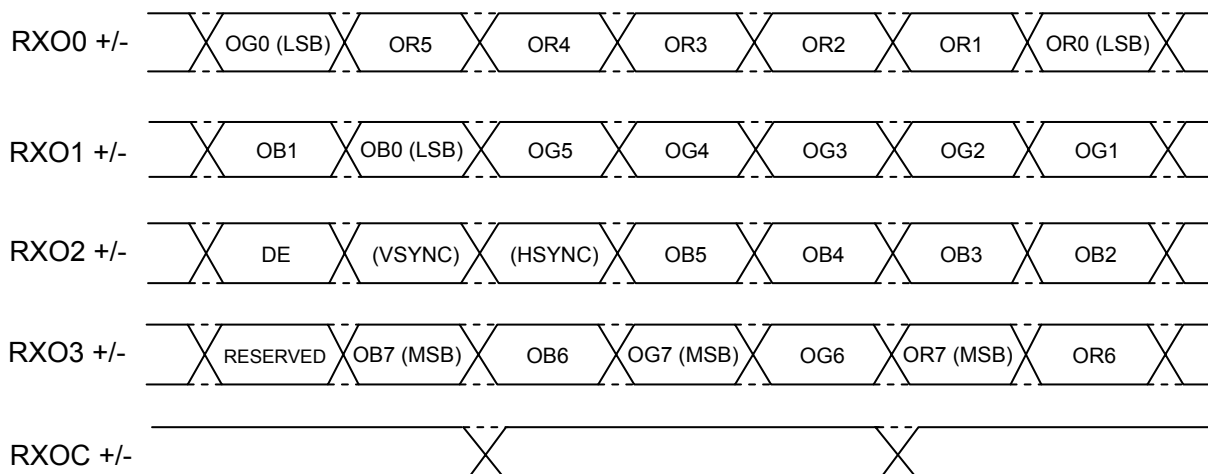
### **Inverter : BLCN5, BLCN6**

PIN NO.	SYMBOL	FUNCTION
1	VSS	Power Ground
2	VSS	Power Ground
3	NC	No Connection
4	BLTC	Backlight ON/OFF control
5	BRT1	Internal PWM Brightness Control 1
6	BRT2	Internal PWM Brightness Control 2
7	BRTP	External PWM Brightness Control
8	VSS	Power Ground
9	PWSEL	Internal/External Select

BLCN5, BLCN6: IL-Z-9PL-SMTY (JAE)

Suitable mating connector: IL-Z-9S-S125C3 (JAE)

### INTERFACE (LVDS) ODD DATA ASSIGNMENT



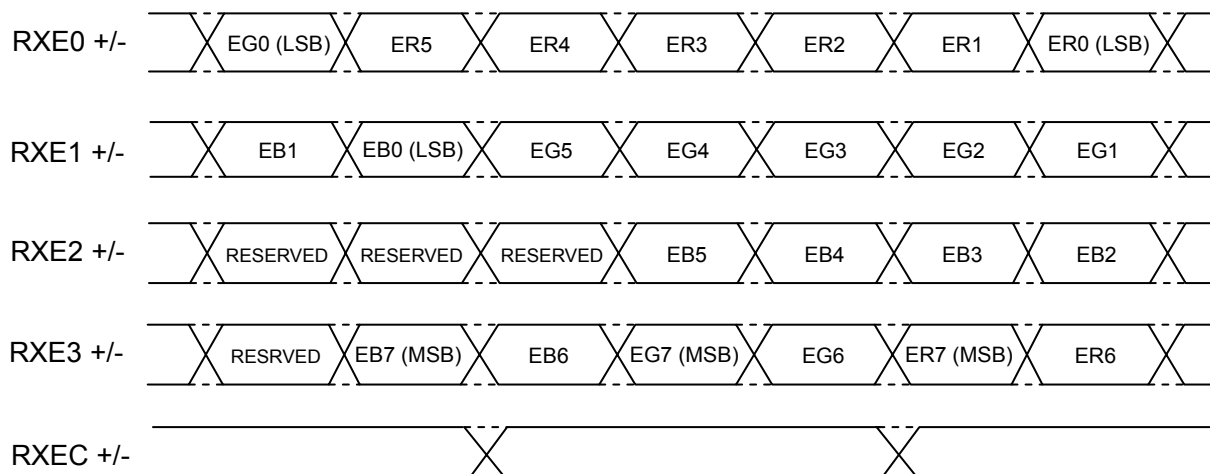
### INTERFACE ODD SIGNALS

SIMBOL	FUNCTION
ODCLK	Odd Data Clock
(HSYNC)	Horizontal Sync - This signal initiates a new line (negative).
(VSYNC)	Vertical Sync - This signal initiates a new frame (negative).
DE	Data Enable (positive)
OR0	Odd Red Data (LSB)
OR1	Odd Red Data
OR2	Odd Red Data
OR3	Odd Red Data
OR4	Odd Red Data
OR5	Odd Red Data
OR6	Odd Red Data
OR7	Odd Red Data (MSB)
OG0	Odd Green Data (LSB)
OG1	Odd Green Data
OG2	Odd Green Data
OG3	Odd Green Data
OG4	Odd Green Data
OG5	Odd Green Data
OG6	Odd Green Data
OG7	Odd Green Data (MSB)
OB0	Odd Blue Data (LSB)
OB1	Odd Blue Data
OB2	Odd Blue Data
OB3	Odd Blue Data
OB4	Odd Blue Data
OB5	Odd Blue Data
OB6	Odd Blue Data
OB7	Odd Blue Data (MSB)

[Note 1] The valid synchronous signals are ODCLK and DE, HSYNC and VSYNC are invalid.

[Note 2] INTERFACE SIGNALS are loaded from LVDS-transmitter to TFT Timing generator with LVDS sequence. (See **BLOCK DIAGRAM**.)

### INTERFACE (LVDS) EVEN DATA ASSIGNMENT



### INTERFACE EVEN SIGNALS

SIMBOL	FUNCTION
EDCLK	Even Data Clock
ER0	Even Red Data (LSB)
ER1	Even Red Data
ER2	Even Red Data
ER3	Even Red Data
ER4	Even Red Data
ER5	Even Red Data
ER6	Even Red Data
ER7	Even Red Data (MSB)
EG0	Even Green Data (LSB)
EG1	Even Green Data
EG2	Even Green Data
EG3	Even Green Data
EG4	Even Green Data
EG5	Even Green Data
EG6	Even Green Data
EG7	Even Green Data (MSB)
EB0	Even Blue Data (LSB)
EB1	Even Blue Data
EB2	Even Blue Data
EB3	Even Blue Data
EB4	Even Blue Data
EB5	Even Blue Data
EB6	Even Blue Data
EB7	Even Blue Data (MSB)

[Note 1] INTERFACE SIGNALS are loaded from LVDS-transmitter to TFT Timing generator with LVDS sequence. (See **BLOCK DIAGRAM**.)

## INTERFACE (LVDS) SIGNAL TIMING PARAMETERS

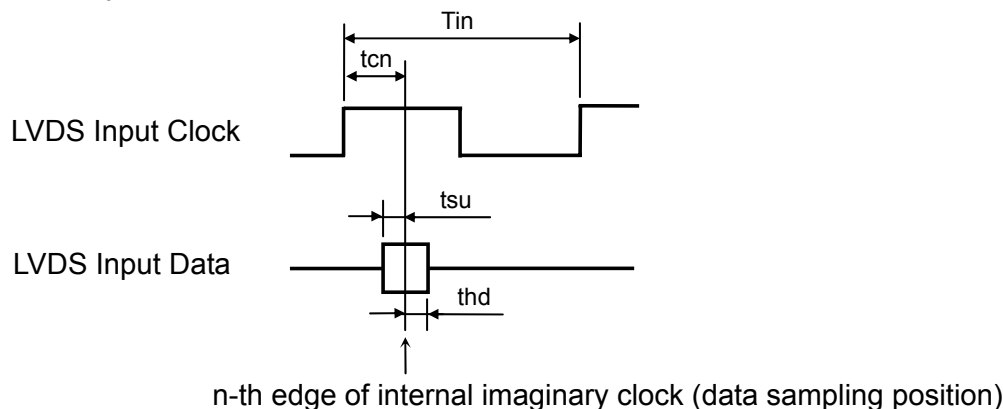
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Data Setup Time	tsu	900	-	-	ps	at Tin=25ns Note 1
Data Hold Time	thd	900	-	-	ps	

[Note 1] In the following timing waveform, the n-th edge of internal imaginary clock tcn, which is sampling position of LVDS input data signal, is given by:

$$tcn = (2n-1) T_{in} / 14 \quad (n=1,2, \sim 7)$$

where  $T_{in}$  is period of LVDS input clock.

For this imaginary clock edge, data setup time is t<sub>su</sub> and data hold time is t<sub>hd</sub>, respectively.



## CYCLE JITTER of LVDS CLOCK

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
P-P of jitter / 100 cycles	tcj1	-	-	300	ps	Note 1
Jitter rate	tcj2	-	-	20	ps/cycle	

[Note 1] Please confirm tcj2 (Jitter rate), only if tcj1 (P-P of jitter/100cycles) exceeds 300ps.

[Additional explanation]

Right diagram shows the example of CYCLE JITTER of LVDS CLOCK.

According to this diagram, tCLK MIN. is 25.0ns and tCLK MAX. is 25.42ns between 0nc and 100nc. The tcj1 (P-P of jitter / 100 cycles) in this sphere is

$$tcj1 = 25.42 - 25.0 = 0.42 \text{ ns}$$

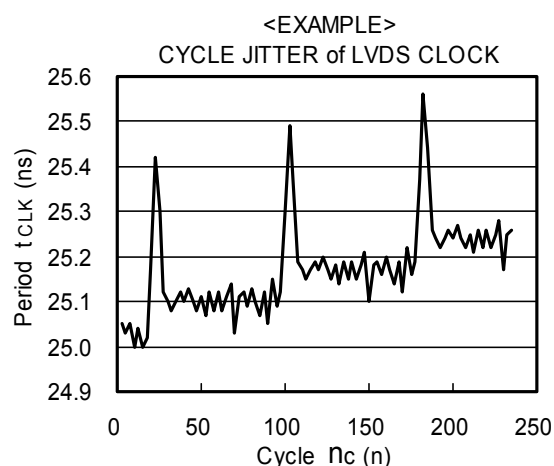
and out of specification (300ps MAX.). So, it is necessary to measure tcj2 (jitter rate) and to judge whether it conform to above specification.

According to the diagram, the sharpest fluctuation of tCLK is 0.4ns per 5nc. So that, the tcj2 in this sphere is

$$tcj2 = 0.4/5 = 0.08 \text{ ns/cycle}$$

and larger than specification (20ps/cycle MAX.).

In conclusion, normal function of the LCD module can not be assured in this case.



## INTERFACE SIGNAL TIMING PARAMETERS ( DE\_MODE )

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	NOTE
ODCLK	Frequency	f <sub>CLK</sub>	30.0	40.2	45.0	MHz	f <sub>CLK</sub> =1/t <sub>CLK</sub>
EDCLK	Duty	D	(0.40)	0.50	(0.60)	-	D=t <sub>CLKL</sub> /t <sub>CLK</sub>
DE	Setup Time	t <sub>SI</sub>	(3)	-	-	ns	for DCLK
	Hold Time	t <sub>HI</sub>	(1.5)	-	-	ns	
	Horiz. Period	t <sub>HP</sub>	690	832	1026	t <sub>CLK</sub>	
	Horiz. DE	t <sub>HDE</sub>	640	640	640	t <sub>CLK</sub>	
	Horiz. Frequency	f <sub>H</sub>	36.1	48.3	54.1	kHz	f <sub>H</sub> = 1/t <sub>HP</sub>
	Vert. Period	t <sub>VP</sub>	780	806	900	t <sub>HP</sub>	f <sub>V</sub> =60Hz Typ.
	Vert. DE	n <sub>VDE</sub>	768	768	768	n	
DATA	Setup Time	t <sub>SD</sub>	(3)	-	-	ns	for DCLK
	Hold Time	t <sub>HD</sub>	(1.5)	-	-	ns	

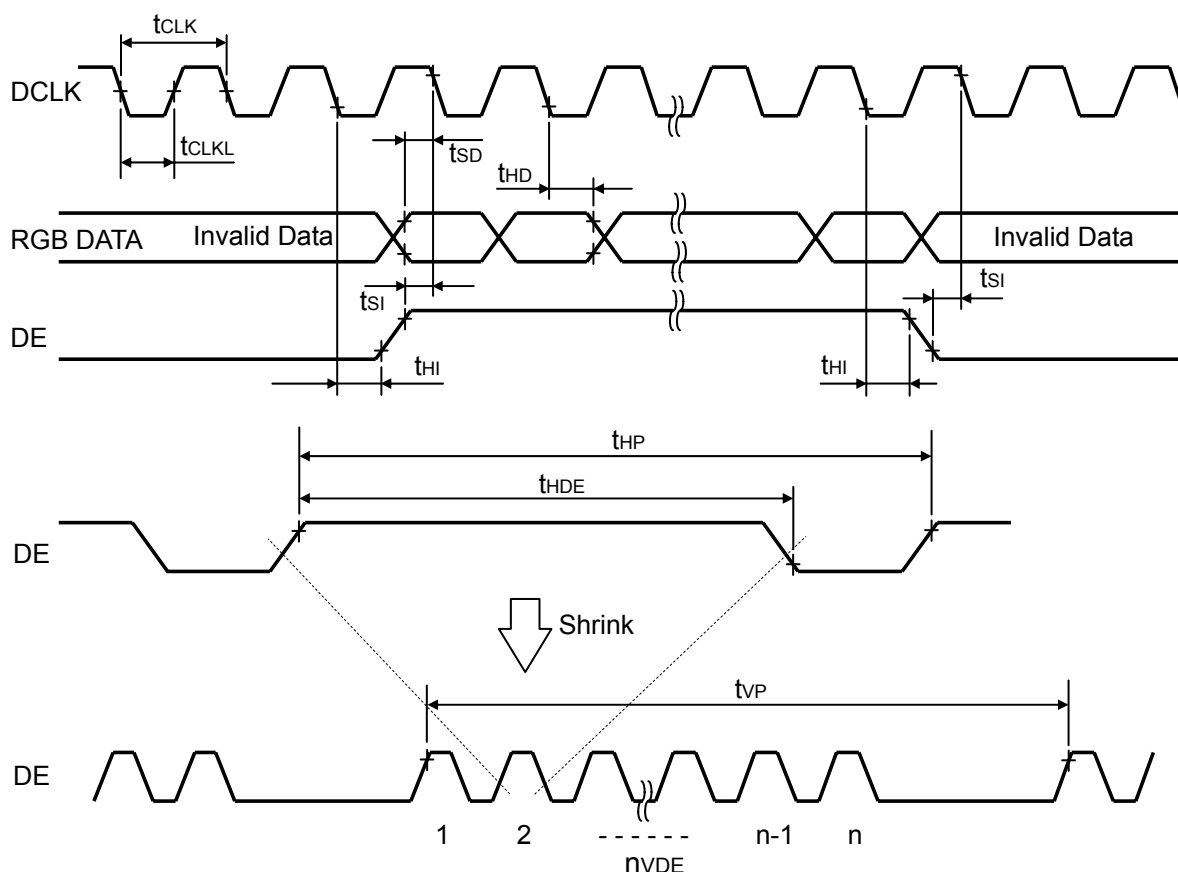
[Note 1] The relations between Horizontal period (t<sub>HP</sub>) and Horizontal DE (t<sub>HDE</sub>) must be kept  $t_{HP} \geq t_{HDE} + 50 [t_{CLK}]$ .

[Note 2] f<sub>H</sub> (Horizontal Frequency) = 1/t<sub>HP</sub>  
f<sub>V</sub> (Vertical Frequency) = 1/t<sub>VP</sub>

[Note 3] These signal timing parameters are specified at the digital inputs of LVDS transmitter.

[Note 4] The values in this table only show the normal operating conditions of internal logic circuit, and it does not assure the conditions for appearance and display quality. The conditions for appearance and display quality are shown in the inspection standard separately.

## INTERFACE SIGNAL TIMING DIAGRAM ( DE\_MODE )



## RELATIONSHIP BETWEEN INPUT DATA AND DISPLAY COLOR

DISPLAY COLOR	INPUT DATA	RED DATA								GREEN DATA								BLUE DATA							
		MSB				LSB				MSB				LSB				MSB				LSB			
		OR7	OR6	OR5	OR4	OR3	OR2	OR1	OR0	OG7	OG6	OG5	OG4	OG3	OG2	OG1	OG0	OB7	OB6	OB5	OB4	OB3	OB2	OB1	OB0
		ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	EG7	EG6	EG5	EG4	EG3	EG2	EG1	EG0	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0
BASIC COLOR	BLACK	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	RED(255)	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	GREEN(255)	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
	BLUE(255)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	CYAN	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
	MAGENTA	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	YELLOW	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
	WHITE	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
RED	BLACK	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	RED(1)	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	RED(2)	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	:	:								:								:							
	RED(253)	H	H	H	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	RED(254)	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	RED(255)	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	:	:								:								:							
GREEN	BLACK	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	GREEN(1)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
	GREEN(2)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
	:	:								:								:							
	GREEN(253)	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	H	L	L	L	L	L	L	L	L
	GREEN(254)	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L
	GREEN(255)	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
	:	:								:								:							
BLUE	BLACK	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	BLUE(1)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
	BLUE(2)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
	:	:								:								:							
	BLUE(253)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	H
	BLUE(254)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
	BLUE(255)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	:	:								:								:							

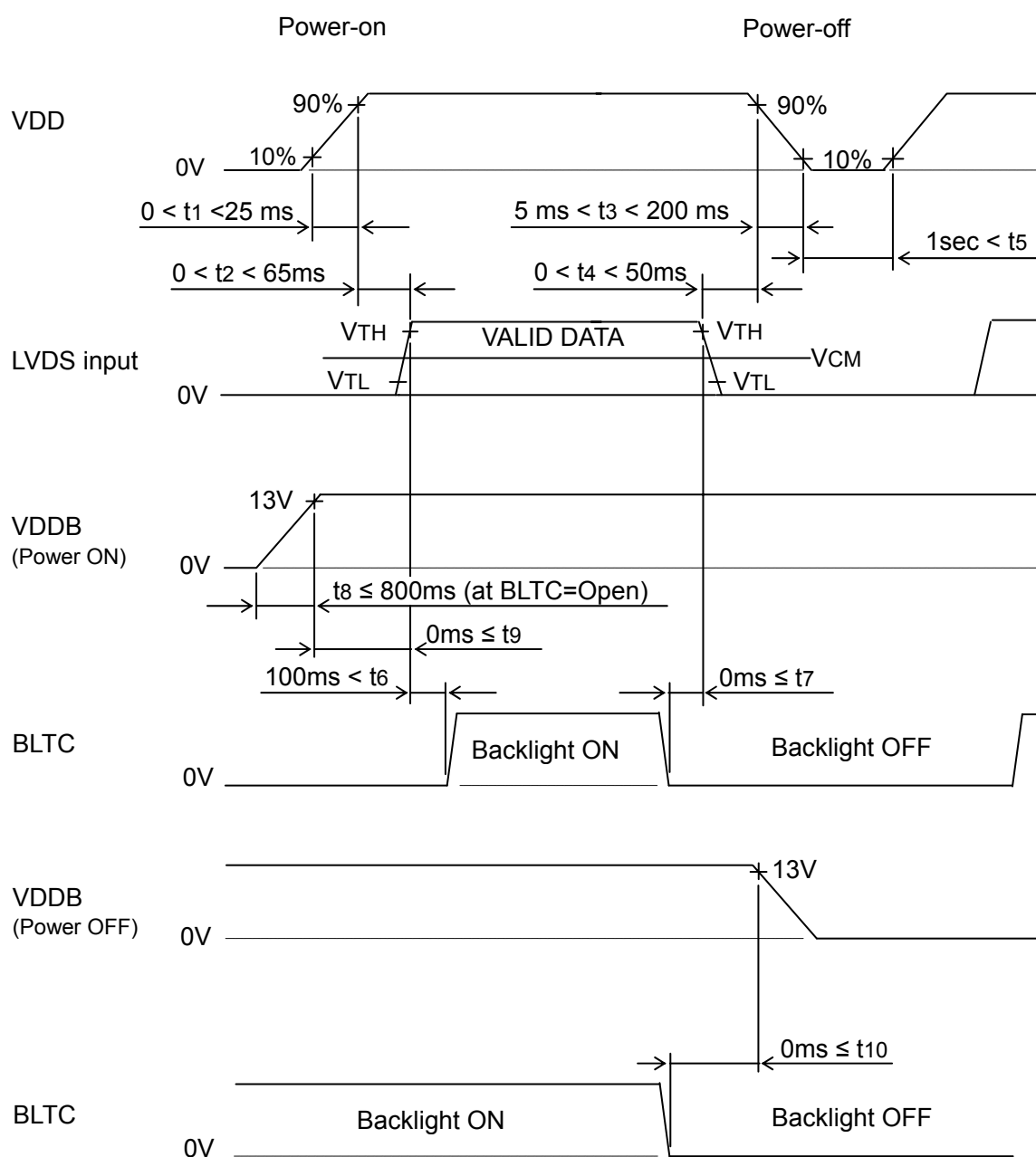
[Note 1] Color(n) --- 'n' indicates gray scale step.

## RELATIONSHIP BETWEEN INPUT DATA AND DISPLAY POSITION

Odd			Even					
R	G	B	R	G	B			
1.1	1.2	1.3	. . . . .			1.1279	1.1280	
2.1	2.2						2.1280	
3.1								
.								.
.								.
.								.
767.1							767.1280	
768.1	768.2	. . . . .				768.1279	768.1280	



## POWER ON/OFF SEQUENCE REQUIREMENT



When the VDD is off, LVDS input must be kept at either low level or high impedance.

Inverter (backlight) ON/OFF sequence is not related LVDS sequence, however it is recommended to consider some timing difference between logic input as shown above.

If backlight lights on before LCD starts function, or if backlight is kept on after LCD stopped function, screen may look white for a moment or abnormal image may be displayed.

This is caused by variation in output signal from timing generator at LVDS input on or off. It does not cause damage to liquid crystal molecule and driving circuit.

## ***PRECAUTIONS (INSTRUCTIONS FOR SAFE AND PROPER USE)***

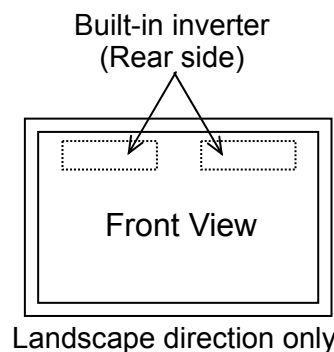
### **1. Instructions for safety**

- (1) Please do not disassemble or modify LCD module to avoid the possibility of electric shock, damage of electronic components, scratch at display surface and invasion of foreign particles. In addition, such activity may result in fire accident due to burning of electronic component.  
LCD module disassembled or modified by customer is out of warranty.
- (2) Please be careful in handling of LCD module with broken glass.  
When the display glass breaks, please pay attention not to injure your fingers. The display surface has the plastic film attached, which prevents dispersion of glass pieces, however touching broken edge will injure your fingers. Also Lamp (Cold Cathode Fluorescent Lamp) is made of glass, therefore please pay attention in the same way.
- (3) Please do not touch the fluid flown out of broken display glass.  
If the fluid should stick to hand or clothes, wipe off with soap or alcohol immediately and then wash it with water. If the fluid should get in eyes, wash eyes immediately with pure water for more than 15 minutes and then consult the doctor.
- (4) Lamp contains mercury inside. Please follow regulations or rules established by local autonomy at its disposal.
- (5) Please be careful to electric shock.  
Before handling LCD module, please switch off the power supply.  
Since high voltage is applied to Lamp terminal, cable, connector and inverter circuit in operation mode, touching them will cause electric shock.

### **2. Instructions for designing**

- (1) Mounting of LCD  
Please fix LCD module at all mounting holes and all mounting flanges shown in this specification for installation onto system. The used screws should have proper dimensions.  
Furthermore, designing of mounting parts should be adequate so that LCD module is not warped or twisted, to achieve good display quality.
- (2) Heat radiation  
Lamp generates heat at lighting and causes temperature rise inside system. Therefore, designing to radiate heat like radiation slits at cabinet is recommended to meet the specified operating temperature range for LCD module.
- (3) Noise on power line  
Spike noise contained in power line causes abnormal operation of driving circuit and abnormal display. To avoid it, spike noise should be suppressed below VDD  $\pm 100\text{mVp-p}$ . (In any case, absolute maximum rating should be kept.)
- (4) Power sequence  
Before LCD module is switched on, please make sure that power supply and input signals of system, testing equipment, etc. meet the recommended power sequence.
- (5) Absolute maximum rating  
Absolute maximum rating specified in this specification has to be kept in any case. It shows the maximum that cannot be exceeded.  
Exceeding it may cause burning or non-recoverable break of electronic components in circuit. Please make system design so that absolute maximum rating is not exceeded even if ambient temperature, input signal and components are varied.

- (6) Protection for power supply  
Please study to adapt protection for power supply against trouble of LCD module, depending on usage condition of system. Fuse installed on LCD module should be never modified. Any modification to make the function of fuse ineffective may cause burning or break of printed wiring board or other components at circuit trouble.
- (7) Protection against electric shock  
High voltage is applied to Lamp connector, inverter circuit and Lamp at lighting. Please make design not to expose or be accessible to such high voltage parts to avoid electric shock.
- (8) Protection cover and cut-off filter for ultraviolet rays  
When LCD module is used under severe condition like outdoor, it is recommended to use transparent protection cover over display surface to avoid scratches and invasion of dust and water. In addition, when LCD module is exposed to direct sun light for long time, use of cut-off filter for ultraviolet rays is also recommended. Please be careful not to get condensation.
- (9) Power supply for inverter  
If LCD display turned into reddish screen or remarkable brightness decreases by the end of CFL life, please make a consideration of design that the backlight is turned off immediately.
- (10) Setting direction of LCD  
Please install this LCD module in the following direction onto your system. Setting in the other direction may cause the un-uniform display



### 3. Instructions for use and handling

- (1) Protection against Static electricity  
C-MOS LSI and semiconductors are easily damaged by static discharge. LCD module should be handled on conductive mat by person grounded with wrist strap etc. to avoid getting static electricity. Please be careful not to generate static electricity during operation.
- (2) Protection against dust and stain  
LCD module should be handled in circumstance as clean as possible. It is recommended to wear fingerstalls or ductless and soft gloves before handling to avoid getting dust or stain on display surface.
- (3) Protection film for display surface  
It is recommended to remove protection film at nearly final process of assembling to avoid getting scratch or dust. To remove film, please pick up its edge with dull-head tweezers or cellophane tape at first and then remove film gradually taking more than 3 seconds. If film is removed quickly, static electricity may be generated and may damage semiconductors or electronic components.
- (4) Contamination of display surface  
When display surface of LCD module is contaminated, please wipe the surface softly with cotton swab or clean cloth. If it is not enough, please take it away with cellophane tape or wipe the surface with cotton swab or clean cloth containing benzene. In this case, please be careful so that benzene does not get in inside of LCD module, because it may be damaged.

- (5) Water drop on LCD surface  
Please do not leave LCD module with water drop. When the display surface gets water drop, please wipe it off with cotton swab or soft cloth immediately, otherwise display surface will be deteriorated.  
If water gets in inside of LCD module, circuit may be damaged.
- (6) Please make sure that LCD module is not warped or twisted at installation into system. Even temporary warp or twist may be the cause for failure.
- (7) Mechanical stress  
Please be careful not to apply strong mechanical stress like drop or shock to LCD module. Such stress may cause break of display glass and Lamp or may be the cause for failure.
- (8) Pressure to display surface  
Please be careful not to apply strong pressure to display surface. Such pressure may cause scratches at surface or may be the cause of failure.
- (9) Protection against scratch  
Please be careful not to hit, press or rub the display surface with hard material like tools. In addition, please do not put heavy or hard material on display surface, and do not stack LCD modules. Polarizer at front surface can be easily scratched.
- (10) Plugging in of connector  
Please be careful not to apply strong stress to connector part of LCD module at plugging in or out, because strong stress may damage the inside connection. At plugging in connector, place LCD module on the flat surface and hold the backside of connector on LCD module. Please make sure that connector is plugged in correctly. Insecure connection may be the cause for failure during operation.  
In addition, please be careful not to put the connecting cable between cabinet of system and LCD module at installing LCD module into system.
- (11) Handling of Lamp cable and FPC (Flexible Printed Circuit)  
Please be careful not to pull or scratch Lamp cable, because Lamp or soldered part of cable may be damaged consequently.  
Also FPC should not be pulled or scratched.
- (12) Switching off before plugging in connector  
Please make sure that power is switched off before plugging in connector.  
If power is on at plugging in or out, circuit of LCD module may be damaged.  
When LCD is switched on for test or inspection, please make sure that power supply and input signals of driving system meet the specified power sequence.
- (13) Temperature dependence of LCD display  
Response speed (optical response) of LCD display is dependent on temperature.  
Under low temperature, response speed is slower.  
Also brightness and chromaticity change slightly depending on temperature.
- (14) Slow light-up of Lamp under low temperature  
Under low temperature, start-up of Lamp gets difficult. (The time from switch-on to stable lighting becomes longer.)  
As characteristic of Lamp, operation under low temperature makes the life time shorter. To avoid this, it is recommended to operate under normal temperature.
- (15) Condensation  
LCD module may get condensation on its display surface and inside in the circumstance where temperature changes much in short time.  
Condensation can cause deterioration or failure. Therefore, please be careful not to get condensation.
- (16) Remaining of image  
Displaying the same pattern for long time may cause remaining of image even after changing the pattern. This is not failure but will disappear with time.

#### **4. Instructions for storage and transportation**

(1) Storage

Please store LCD module in the dark place of room temperature and low humidity in original packing condition, to avoid condensation that may cause failure.

Since sudden temperature change may cause condensation, please store in circumstance of stable temperature.

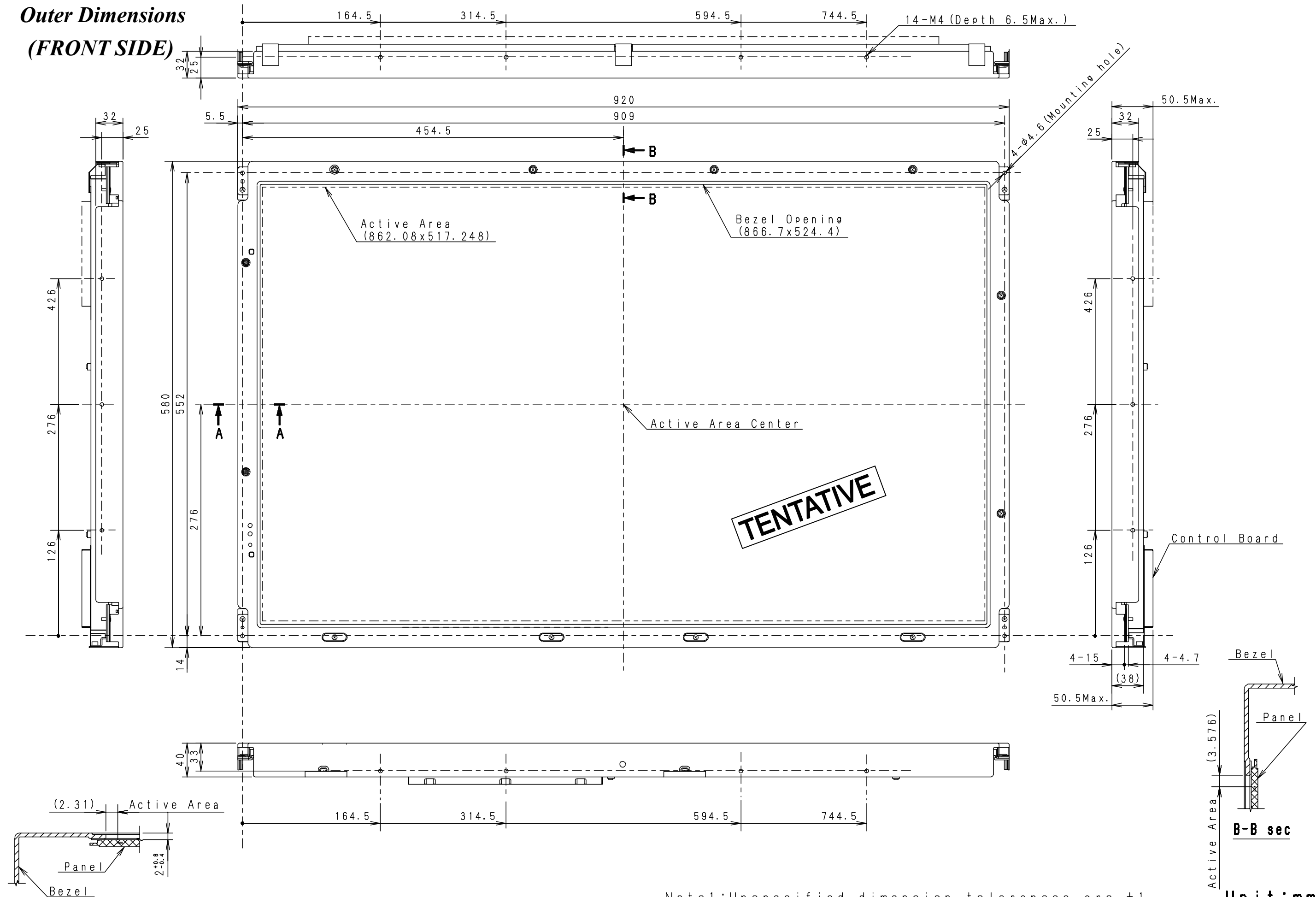
(2) Stacking number

Since excessive weight causes deformation and damage of carton box, please stack only up to the number stated on carton box for storage and transportation.

(3) Handling

Since LCD module consists of glass and precise electronic components, it will be damaged by excessive shock and drop. Therefore, please handle the carton box carefully to minimize shock at loading, reloading and transportation.

**Outer Dimensions  
(FRONT SIDE)**



Note1: Unspecified dimension tolerances are  $\pm 1$ .

Unit: mm

SANYO Electric Co., Ltd.

TM396WX-71N31

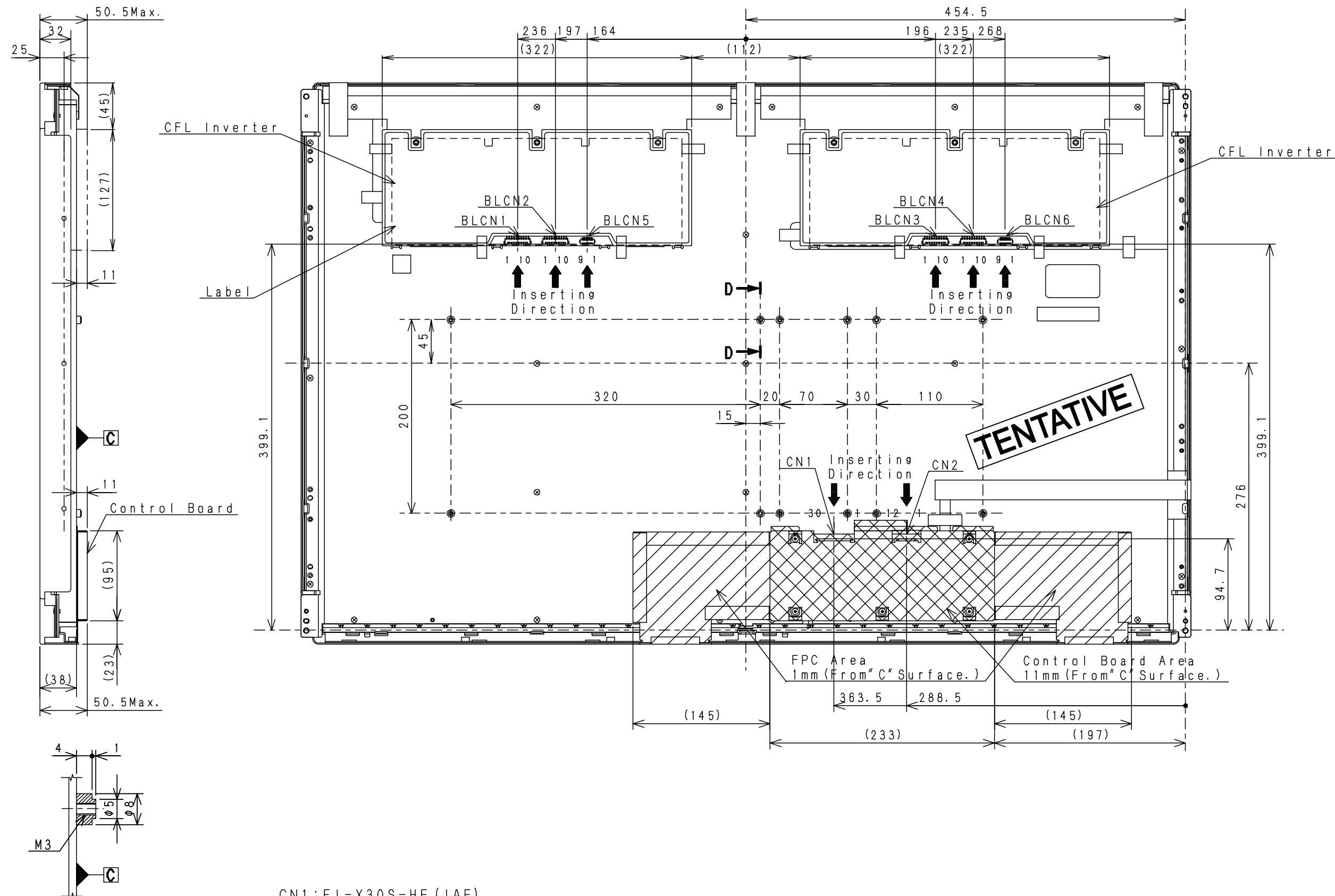
Ver. 6

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39631TWXASY-00300-B1

Outer Dimensions  
(BACK SIDE)



D-D sec (12 pieces)

CN1: FI-X30S-HF (JAE)  
CN2: 53261-1290 (MOLEX)  
BLCN1, 2, 3, 4: DF3-10P-2H (HRS)  
BLCN5, 6: IL-Z-9PL-SMTY (JAE)

Note1: Unspecified dimension tolerances are  $\pm 1$ .

Unit: mm