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DEVICE SPECIFICATION FOR

TFT-LCD Open cell

MODEL No.

LK235D3HA0S

**These parts have corresponded with the RoHS directive.
These parts don't include the level 1 environment-related
substances regulated by SS-00259.**

☐ CUSTOMER'S APPROVAL

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RECORDS OF REVISION

LK235D3HA0S

SPEC No.	DATE	REVISED No.	SUMMARY		NOTE				
			PAGE						
LD-23308A	Mar.31.2011	-	-	-	1 st Issue				
LD-23308B	Jun.22.2011	△1	21	Add Test item (Vibration test, Drop test	2 nd Issue				
			26	Add Packing form drawing					
LD-23308C	Jul.13.2011	△2	10	6-2-1. AC characteristic (1) Add Typ Source clock frequency	3 rd Issue				
			17	8. Optical characteristics Add Transmittance Change Luminance Uniformity to Transmittance Uniformity 1.33 → 1.25 Fig8-1,8-2 Revise LCD Module to LCD open cell & Backlight					
			19	Add Note7					
			22	12.1 Packing form Add e),f),g) for palette information 12.2 Label Revise cellbox label Lot No. description					
			23	Add c) palette label					
			LD-23308D	Aug.22.2011		△3	22	Chenge Open Cell Label	4 th Issue
			23	Revise Pallette serial No.					
25	Chenge Outline dimension of open cell label								
LD-23308E	Oct.14.2011	△4	3	Add 2 nd source conncter	5 th Issue				
			22	Open cell label: add suffix code Packing label: add suffix code					
			23	Pallet label: add suffix code					

1. Application

This specification sheets applies to the color 23.5" TFT-LCD Open Cell LK235D3HA0S.

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2. Overview

This Open Cell is a color active matrix LCD panel incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, a front polarizer, a back polarizer, driver ICs and Source PWB. Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with about 16,777,216 colors by using 8bit + mini-LVDS(Low Voltage Differential Signaling) to interface, driving signal and driving voltages.

The following contents can be achieved in using LQ0DZC0051 (LR388H5) Timing control IC that sharp specifies.

And in order to improve the response time of LCD, This Open Cell applies the Over Shoot driving (O/S driving) technology for the Timing control IC. In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

With combination of these technologies, motion blur can be reduced and clearer display performance can be realized.

This open cell can display 120Hz image in 2D mode and 240Hz image in 3D mode by using LQ0DZC0051 (LR388H5) Timing control IC that sharp specifies.

3. Mechanical Specifications

Parameter	Specifications	Unit
Display size	59.809 (Diagonal)	cm
	23.547 (Diagonal)	inch
Active area	521.28(H) x 293.22 (V)	mm
Pixel Format	1920(H) x 1080 (V)	pixel
	(1pixel = R + G + B dot)	
Pixel pitch	0.0905(H) x 0.2715 (V)	mm
Pixel configuration	R,G,B vertical stripe	
Display mode	Normally Black	
Open Cell Outline Dimensions *1	539.165(H) x 348.250(V) x 3.500(D)(*1)	mm
Mass	661 (TYP)	g
Surface treatment	Anti Glair Hard Coat 3H Haze 2.0%	

(*1)Outline dimensions are shown in Fig.1

4. Open Cell driving specifications

4-1. Driving interface of Source-PWB

CN11, CN12: Input signal from Timing control IC that SHARP specifies.

Using connector: CN11, CN12 502790-8091(MOLEX) or 106C80-103000-G2-R (Starconn) .△4

4-1-2. CN11, CN12

CN	CN11			CN12		
No	Signal	Note	I/O	Signal	Note	
1	SPI_WP	For future use (SPI I/F)	I	NC		
2	SPI_CK	For future use (SPI I/F)	I	NC		
3	SPI_DOUT	For future use (SPI I/F)	O	NC		
4	SPI_DIN	For future use (SPI I/F)	I	NC		
5	SPI_CS	For future use (SPI I/F)	I	NC		
6	VL_A	Gamma standard voltage	I	VL_A	Gamma standard voltage	I
7	VL_B	Gamma standard voltage	I	VL_B	Gamma standard voltage	I
8	VL_C	Gamma standard voltage	I	VL_C	Gamma standard voltage	I
9	VL0	Gamma standard voltage	I	VL0	Gamma standard voltage	I
10	GND	GND		GND	GND	
11	S8_LVCLKN	mini-LVDS(SOF8)	I	S4_LVCLKN	mini-LVDS(SOF4)	I
12	S8_LVCLKP	mini-LVDS(SOF8)	I	S4_LVCLKP	mini-LVDS(SOF4)	I
13	GND	GND		GND	GND	
14	S8_LV2N	mini-LVDS(SOF8)	I	S4_LV2N	mini-LVDS(SOF4)	I
15	S8_LV2P	mini-LVDS(SOF8)	I	S4_LV2P	mini-LVDS(SOF4)	I
16	S8_LV1N	mini-LVDS(SOF8)	I	S4_LV1N	mini-LVDS(SOF4)	I
17	S8_LV1P	mini-LVDS(SOF8)	I	S4_LV1P	mini-LVDS(SOF4)	I
18	S8_LV0N	mini-LVDS(SOF8)	I	S4_LV0N	mini-LVDS(SOF4)	I
19	S8_LV0P	mini-LVDS(SOF8)	I	S4_LV0P	mini-LVDS(SOF4)	I
20	GND	GND		GND	GND	
21	S7_LVCLKN	mini-LVDS(SOF7)	I	S3_LVCLKN	mini-LVDS(SOF3)	I
22	S7_LVCLKP	mini-LVDS(SOF7)	I	S3_LVCLKP	mini-LVDS(SOF3)	I
23	GND	GND		GND	GND	
24	S7_LV2N	mini-LVDS(SOF7)	I	S3_LV2N	mini-LVDS(SOF3)	I
25	S7_LV2P	mini-LVDS(SOF7)	I	S3_LV2P	mini-LVDS(SOF3)	I
26	S7_LV1N	mini-LVDS(SOF7)	I	S3_LV1N	mini-LVDS(SOF3)	I
27	S7_LV1P	mini-LVDS(SOF7)	I	S3_LV1P	mini-LVDS(SOF3)	I
28	S7_LV0N	mini-LVDS(SOF7)	I	S3_LV0N	mini-LVDS(SOF3)	I
29	S7_LV0P	mini-LVDS(SOF7)	I	S3_LV0P	mini-LVDS(SOF3)	I
30	GND	GND		GND	GND	
31	S6_LVCLKN	mini-LVDS(SOF6)	I	S2_LVCLKN	mini-LVDS(SOF2)	I
32	S6_LVCLKP	mini-LVDS(SOF6)	I	S2_LVCLKP	mini-LVDS(SOF2)	I
33	GND	GND		GND	GND	
34	S6_LV2N	mini-LVDS(SOF6)	I	S2_LV2N	mini-LVDS(SOF2)	I
35	S6_LV2P	mini-LVDS(SOF6)	I	S2_LV2P	mini-LVDS(SOF2)	I
36	S6_LV1N	mini-LVDS(SOF6)	I	S2_LV1N	mini-LVDS(SOF2)	I
37	S6_LV1P	mini-LVDS(SOF6)	I	S2_LV1P	mini-LVDS(SOF2)	I
38	S6_LV0N	mini-LVDS(SOF6)	I	S2_LV0N	mini-LVDS(SOF2)	I
39	S6_LV0P	mini-LVDS(SOF6)	I	S2_LV0P	mini-LVDS(SOF2)	I
40	GND	GND		GND	GND	
41	S5_LVCLKN	mini-LVDS(SOF5)	I	S1_LVCLKN	mini-LVDS(SOF1)	I
42	S5_LVCLKP	mini-LVDS(SOF5)	I	S1_LVCLKP	mini-LVDS(SOF1)	I
43	GND	GND		GND	GND	
44	S5_LV2N	mini-LVDS(SOF5)	I	S1_LV2N	mini-LVDS(SOF1)	I

45	S5_LV2P	mini-LVDS(SOF5)	I	S1_LV2P	mini-LVDS(SOF1)	I
46	S5_LV1N	mini-LVDS(SOF5)	I	S1_LV1N	mini-LVDS(SOF1)	I
47	S5_LV1P	mini-LVDS(SOF5)	I	S1_LV1P	mini-LVDS(SOF1)	I
48	S5_LV0N	mini-LVDS(SOF5)	I	S1_LV0N	mini-LVDS(SOF1)	I
49	S5_LV0P	mini-LVDS(SOF5)	I	S1_LV0P	mini-LVDS(SOF1)	I
50	GND	GND		GND	GND	
51	VCC	Logic voltage	I	VCC	Logic voltage	I
52	LS_L	LCD Source Driver driving signal	I	LS_R	LCD Source Driver driving signal	I
53	REV_L	LCD Source Driver driving signal	I	REV_R	LCD Source Driver driving signal	I
54	GND	GND		GND	GND	
55	VH0	Gamma standard voltage	I	VH0	Gamma standard voltage	I
56	VH_C	Gamma standard voltage	I	VH_C	Gamma standard voltage	I
57	VH_B	Gamma standard voltage	I	VH_B	Gamma standard voltage	I
58	VH_A	Gamma standard voltage	I	VH_A	Gamma standard voltage	I
59	VH255	Gamma standard voltage	I	VH255	Gamma standard voltage	I
60	VLS	Analog voltage		VLS	Analog voltage	
61	VLS	Analog voltage	I	VLS	Analog voltage	I
62	HVDD	Half analog voltage	I	HVDD	Half analog voltage	I
63	VCOM	Common voltage	I	VCOM	Common voltage	I
64	CS	CS voltage	I	CS	CS voltage	I
65	CS	CS voltage	I	CS	CS voltage	I
66	CS	CS voltage	I	CS	CS voltage	I
67	CS	CS voltage	I	CS	CS voltage	I
68	CS	CS voltage	I	CS	CS voltage	I
69	CS	CS voltage	I	CS	CS voltage	I
70	CS	CS voltage	I	CS	CS voltage	I
71	CS	CS voltage	I	CS	CS voltage	I
72	CS	CS voltage	I	CS	CS voltage	I
73	CS	CS voltage	I	CS	CS voltage	I
74	CS	CS voltage	I	CS	CS voltage	I
75	CS	CS voltage	I	CS	CS voltage	I
76	GOE	LCD Gate Driver driving signal	I	NC		
77	GCK	LCD Gate Driver driving signal	I	NC		
78	GSP	LCD Gate Driver driving signal	I	NC		
79	VGH	Gate ON voltage	I	NC		
80	VGL	Gate OFF voltage	I	NC		

[Note]

Be sure to use FPC matched mini-LVDS line impedance for connection Main board to Source-PWB.

4-2. Interface block diagram

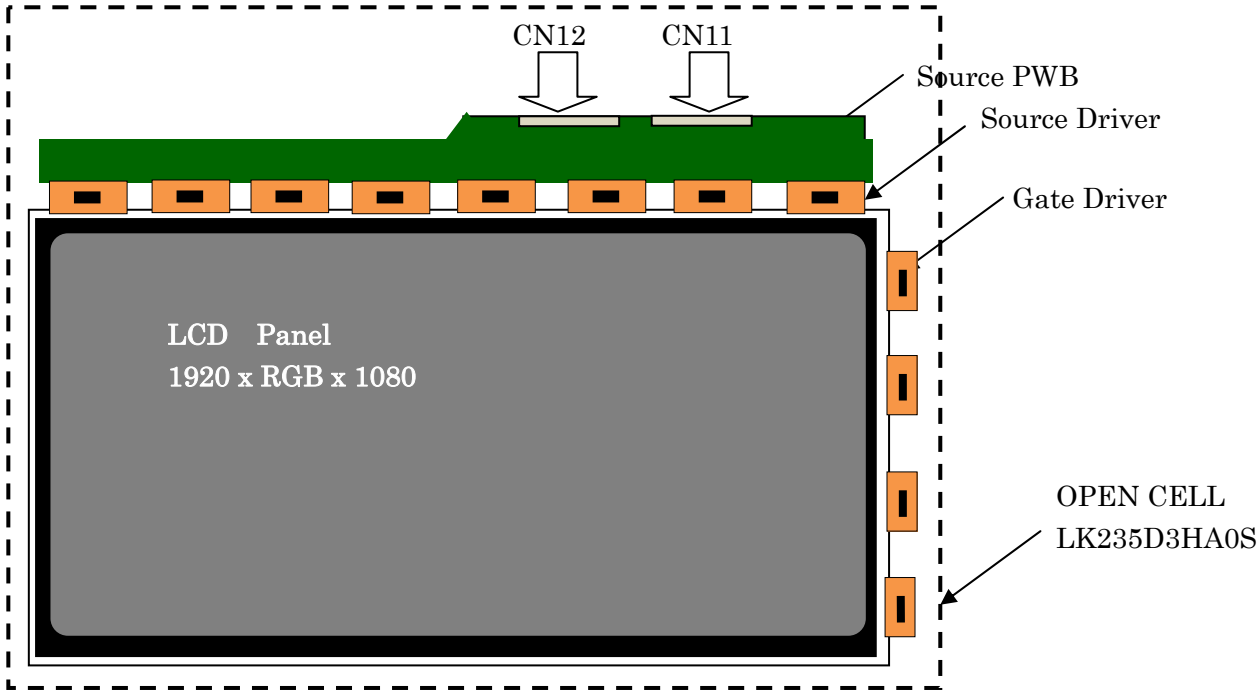


Fig.4-1 Interface block diagram

<p>CN11</p> <p><u>INPUT SIGNAL</u></p> <p>mini-LVDS DATA+ x16</p> <p>mini-LVDS DATA- x16</p> <p>Source driving signal</p> <p>Gate driving signal</p> <p>(SPI signal)</p> <p><u>POWER SUPPLY</u></p> <p>Power (Logic)</p> <p>Power (Analog)</p> <p>Power(Half analog)</p> <p>GND</p> <p>COM</p> <p>Gamma standard voltage</p> <p>Gate Power HIGH</p> <p>Gate Power LOW</p>	<p>CN12</p> <p><u>INPUT SIGNAL</u></p> <p>mini-LVDS DATA+ x16</p> <p>mini-LVDS DATA- x16</p> <p>Source driving signal</p> <p><u>POWER SUPPLY</u></p> <p>Power (Logic)</p> <p>Power (Analog)</p> <p>Power(Half analog)</p> <p>GND</p> <p>COM</p> <p>Gamma standard voltage</p>
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5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Digital Power Supply	VCC	Ta=25℃	-0.3~+4.0	V	
Analog Power Supply	VLS	Ta=25℃	-0.3~+18.0	V	【Note 1】
Half Analog Power Supply	HVDD	Ta=25℃	-0.3~+18.0	V	【Note 1】
Standard voltage terminal	VH0~VH255 VL0~VL255	Ta=25℃	-0.3~VLS+0.3	V	【Note 1】
Source incoming signal voltage	VIS	Ta=25℃	-0.3~VCC+0.3	V	
Gate High Power Supply	VGH	Ta=25℃	-0.3~48.0	V	【Note 2】
Gate Low Power Supply	VGL	Ta=25℃	-23.0~+0.3	V	【Note 2】
Gate Power voltage	VGH-VGL	Ta=25℃	-0.3~+48.0	V	【Note 2】
Gate incoming signal voltage	VIG	Ta=25℃	-0.3~VCC+0.3	V	
Operation temperature	Top	-	0~+50	℃	【Note 3,4】
Storage temperature	Tstg	-	-25~+60	℃	【Note 3,4】
Panel Surface Temperature	Tsf		≤ 60	℃	【Note 3,4】
Source Driver surface temperature	Tssf		≤ 100	℃	【Note 3,5】

【Note 1】 Standard voltage terminal voltage should be kept in the following order.

$VLS-0.2 \geq VH255 > VH_A > \dots > VH_C > VH0 \geq HVDD+0.2$

$HVDD-0.2 \geq VL0 > VL_C > \dots > VL_A > GND$

Please be careful, difference between VLS and VH0~VH255,

VL_A~VL255 and GND not to exceed 8.25V, when power on sequence.

【Note 2】 Set the gate drive voltage, so that $VGL \leq VGH$ is maintained when switching the power source on and off, and during its operation.

【Note 3】 Humidity 95%RH Max.(Ta≤40 ℃)

Maximum wet-bulb temperature at 39 degree or less. (Ta>40 ℃) No condensation.

【Note 4】 Since it becomes as a cause of phenomena, such as contrast unevenness, please make the temperature distribution within a field of a panel uniform.

【Note 5】 The measurement point of Source Driver surface temperature is drawn in Fig.1

A power supply sequence should be kept in the following order.

Source system : GND→VCC→VIS→VLS/VS/HVDD

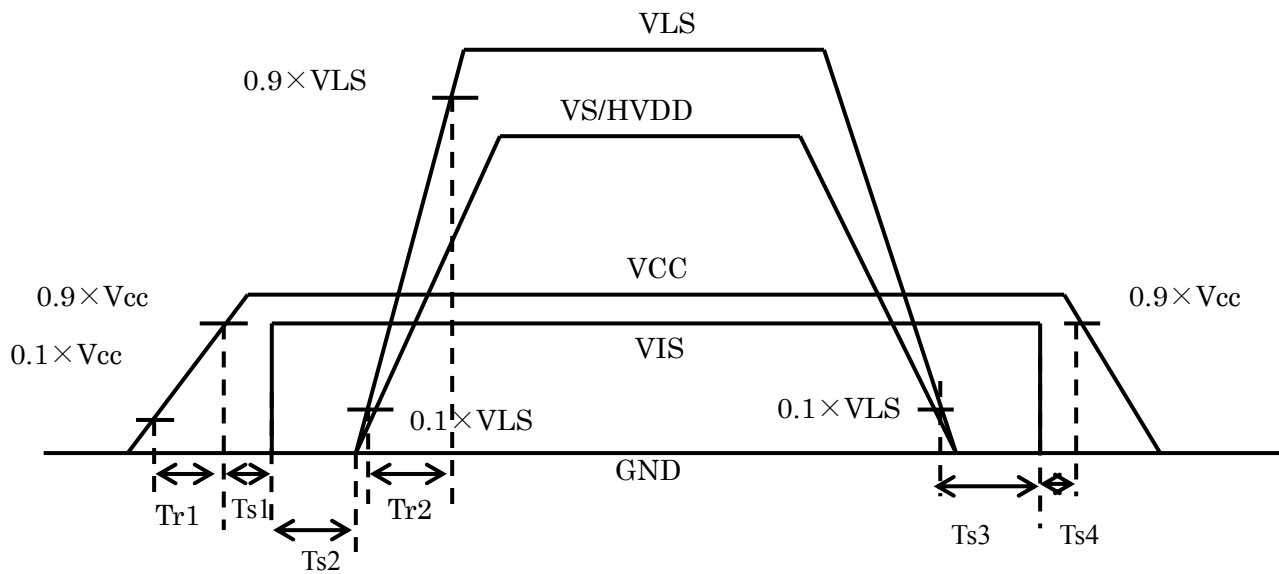


Fig.5-1 Timing sequence (source system)

$$0.5\text{ms} \leq \text{Tr1} \leq 20\text{ms}, \quad \text{Tr2} \leq 50\text{ms}, \quad 0\text{ms} \leq \text{Ts1}, \quad 0\text{ms} \leq \text{Ts2}, \quad 0\text{ms} \leq \text{Ts3}, \quad 0\text{ms} \leq \text{Ts4}$$

Gate system : GND→VCC→VIG→VGL→VGH

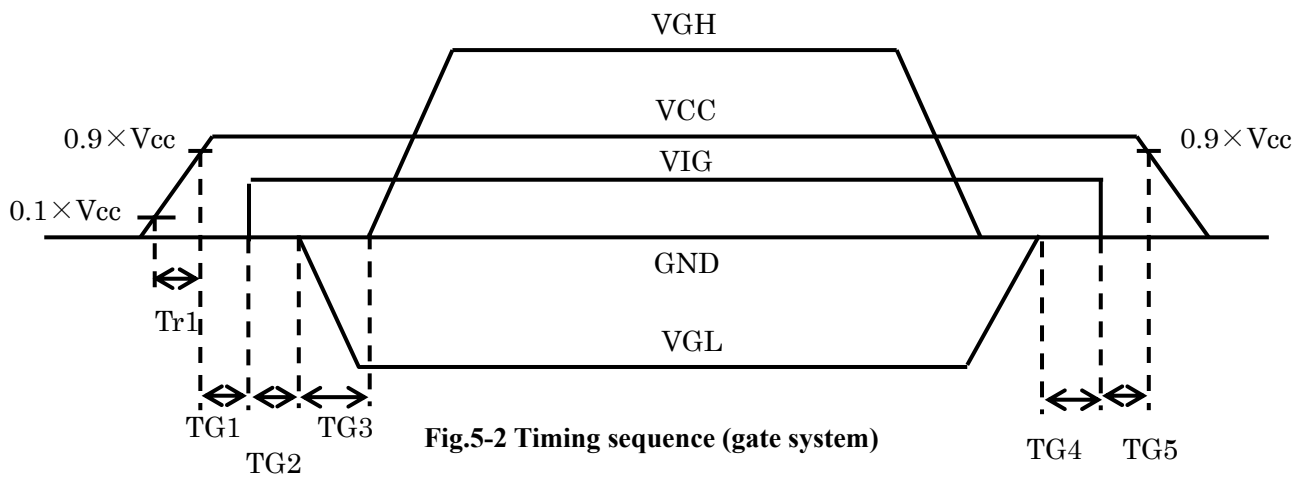


Fig.5-2 Timing sequence (gate system)

$$0\text{ms} \leq \text{TG1}, \quad 0\text{ms} \leq \text{TG2}, \quad 0\text{ms} < \text{TG3}, \quad 0\text{ms} \leq \text{TG4}, \quad 0\text{ms} \leq \text{TG5}$$

Please impress VGL and VGH, especially after VCC reaches 90% or more of setting voltage.

Please give as the above being reverse at the time of interception.

6. Electrical Characteristics

6-1. Proper operating condition

GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Digital Power Supply	VCC	3.0	3.3	3.6	V	
Analog Power Supply	VLS	14.0	15.6	16.5	V	
Half Analog Power Supply	HVDD	0.5VLS-1.0	0.5VLS	0.5VLS+1.0	V	
Standard voltage terminal	VS(VH0~VH255)	HVDD+0.2	-	VLS-0.2	V	【Note 1】
Standard voltage terminal	VS(VL_0~VL_A)	GND+0.2		HVDD-0.2	V	【Note 1】
Gate High Power Supply	VGH	15.0	35.0	36.0	V	
Gate Low Power Supply	VGL	-5.0	-6.0	-7.0	V	
Gate power supply voltage	VGH-VGL	20.0	41.0	43.0	V	
Source mini-LVDS Data Input Low voltage	VID	200		600	mV	$V_{CM_{mlvd}}=1.2\pm0.2\text{ V}$ 【Note 2】
Source mini-LVDS Data Input Standard Voltage Range	$V_{CM_{mlvd}}$	1.0	1.2	1.4	V	$VID\geq 0.2\text{ V}$ $VCC=3.0\sim 3.6\text{ V}$
Source Input Low voltage	VILS	GND		0.3VCC	V	【Note 3】
Source Input High voltage	VIHS	0.7VCC	-	VCC	V	【Note 3】
Gate Input Low voltage	VILG	GND	-	0.3VCC	V	【Note 4】
Gate Input High voltage	VIHG	0.7VCC	-	VCC	V	【Note 4】
Common mode voltage	VCOM	GND		0.5VLS	V	【Note 5】
Auxiliary capacity common mode voltage	CS	-	VCOM	-	V	【Note 5】

【Note 1】 ∴ Gray scale standard voltage can be applied as to following 5 readings (9 points).

V0(Black),V_C,V_B,V_A,V255(White)

$\left[\begin{array}{c} \text{VH0, VH}_C, \text{VH}_B, \text{VH}_A, \text{VH255} \\ \text{VL}_A, \text{VL}_B, \text{VL}_C, \text{VL0} \end{array} \right]$

Please follow below levels for a standard gray scale voltage.

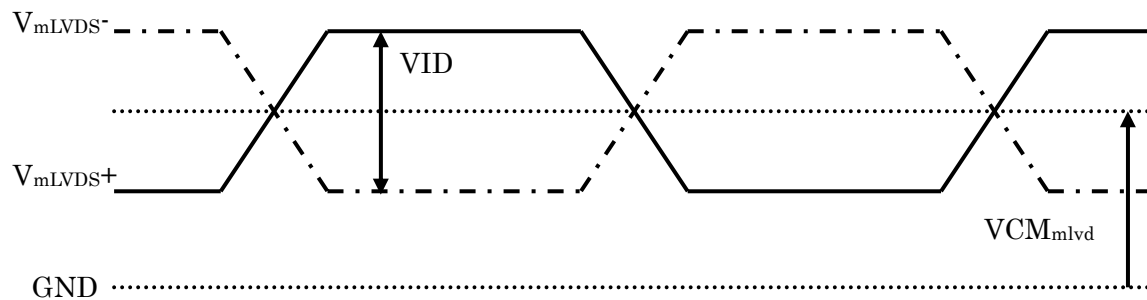
$\text{VLS}-0.2 \geq \text{VH255} > \text{VH}_A > \dots > \text{VH}_C > \text{VH0} \geq \text{HVDD}+0.2$

$\text{HVDD}-0.2 \geq \text{VL0} > \text{VL}_C > \dots > \text{VL}_A > \text{GND}+0.2$

【Note 2】 ∴ Applies to terminals for

$\text{S}^*_\text{LVCLKP/N}, \text{S}^*_\text{LV0P/N}, \text{S}^*_\text{LV1P/N}, \text{S}^*_\text{LV2P/N}$. (*=1 to 8)

The waveforms of signals are shown below.



【Note 3】 ∴ Applies to terminals for $\text{LS}_L, \text{LS}_R, \text{REV}_L, \text{REV}_R$.

【Note 4】 ∴ Applies to terminals for $\text{GSP}, \text{GCK}, \text{GOE}, \text{GSP}$.

【Note 5】 ∴ For COM adjustment, please adjust so that either i) flickers are minimized or ii) the contrast for each LCD module are maximized.

6-2. AC characteristic

6-2-1. AC characteristic (1)

Timing waveforms are shown at Fig 6-1,6-2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Source clock frequency $\Delta 2$	fck		324.0	380.0	MHz	S*_LVCLKP/N
Source clock High level pulse width	Tcwh	1.2	-	-	ns	
Source clock Low level pulse width	Tcwl	1.2	-	-	ns	
Source clock rise time	Tcr	-	-	1	ns	
Source clock fall time	Tcf	-	-	1	ns	
Data setup time	Tdsu	0.5	-	-	ns	S*_LV0~2P/N【Note1】
Data hold time	Tdho	0.5	-	-	ns	S*_LV0~2P/N【Note1】
Latch strobe pulse width	Tlsw	150		-	ns	LS_L,LS_R
Last data - Latch strobe time	Trls	20	-	-	CK	LS_L,LS_R
Electrode reversal - Latch strobe setup time	Tsurv	5	-	-	ns	LS_L/R,REV_L/R
Electrode reversal - Latch strobe hold time	Thrv	6	-	-	ns	LS_L/R,REV_L/R
RST signal High level pulse width	Twrst	12	-	-	ns	S*_LV0P/N
		3	-	-	CK	
LS signal – RST signal time	Tlsrst	150	-	-	ns	S*_LV0P/N
RST signal – LS signal time	Trstls	0	-	-	ns	LS1.LS2

【Note1】 DATA : S*_LV0~2P/N (*=1~8)

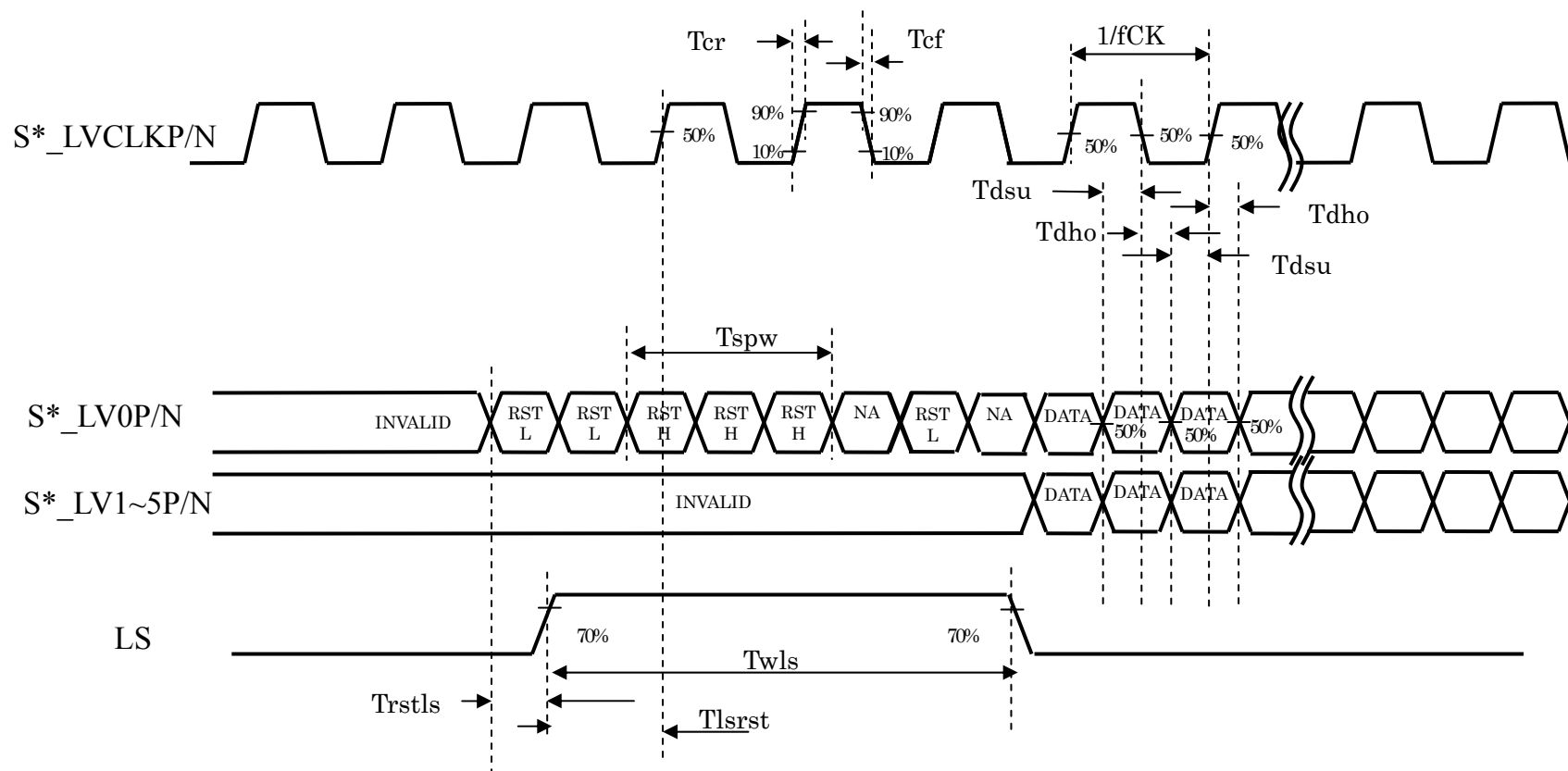


Fig.6-1 Timing waveform 1 (Source Driving Signal)

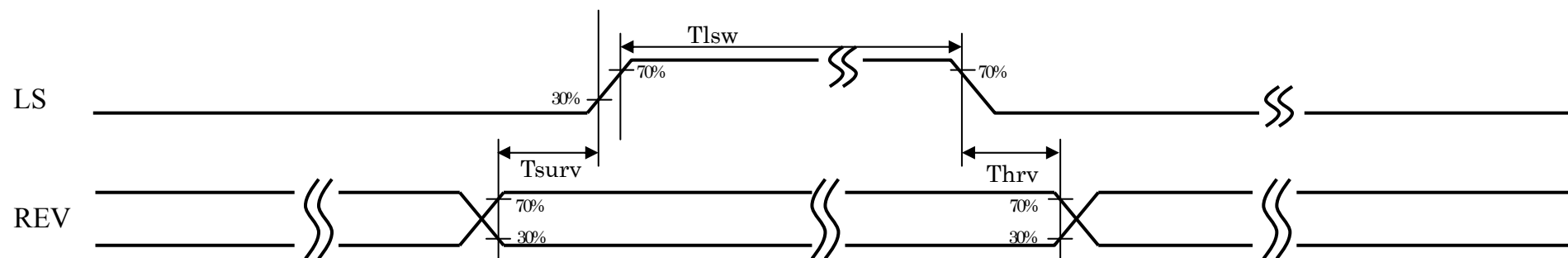
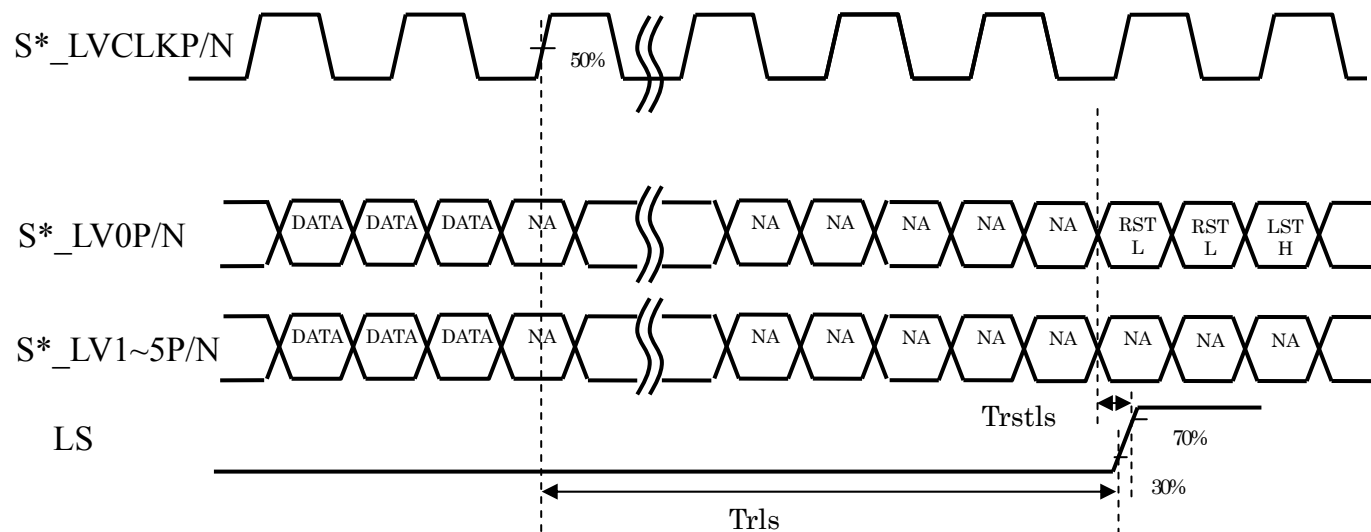


Fig. 6-2 Timing waveform 2 (Source Driving Signal)

6-2-2. AC characteristic (2)

Timing waveform is shown at Fig.6-3

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Gate clock frequency	fgck	-		200	KHz	GCK
Gate clock pulse High width	Twh	0.5		-	μs	
Gate clock pulse Low width	Twl	0.5		-	μs	
Gate clock rising time	Trcl	-	-	100	ns	
Gate clock falling time	Tfcl	-	-	100	ns	
Gate start pulse High width	Twsp	200			ns	GSP
Gate start pulse setup time	Tsu	100	-	-	ns	
Gate start pulse hold time	Th	100	-	-	ns	
Gate start pulse rising time	Trsp	-	-	100	ns	
Gate start pulse falling time	Tfsp	-	-	100	ns	

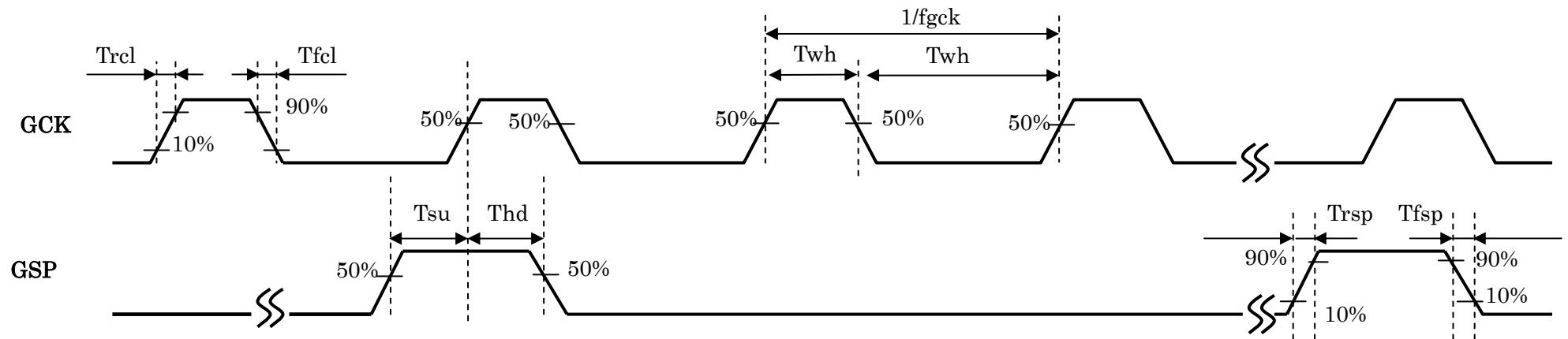


Fig.6-3 Timing waveform 3 (Gate Driving Signal)

6-3.Current consumption

Signal conditions (LR388H5 test pattern (240Hz), Reference Circuit)

Parameter	Symbol	Voltage conditions	Min.	Typ.	Max.	Unit	Remark
Source current (digital)	Ish	VCC=+3.3V	-	100	150	mA	【Note 1】
Source current (analog)	Ils	VLS=+15.6V	-	100	(450)	mA	【Note 1】
Gate current (High)	Igh	VGH=+35V	-	10	(30)	mA	【Note 1】
Gate current (Low)	Igl	VGL=-6V	-	10	(30)	mA	【Note 1】

【Note 1】 Display pattern

Typ 256 gray gradation

Max 2H Stripe pattern

(Make the heat of S-Dr radiate heat while MAX current is measured.)

7. Input Signal, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray scale	Data signal																											
		Gray Scale	R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7			
Basic Color	Black	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Blue	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1		
	Green	—	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0		
	Cyan	—	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
	Red	—	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Magenta	—	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1		
	Yellow	—	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0		
	White	—	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	↑	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Darker	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	↑	↓	↓								↓								↓										
	↓	↓	↓								↓								↓										
	Brighter	253	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	↓	254	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	↑	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Darker	2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	↑	↓	↓								↓								↓										
	↓	↓	↓								↓								↓										
	Brighter	253	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
	↓	254	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
	Green	255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0		
	Darker	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0		
	↑	↓	↓								↓								↓										
	↓	↓	↓								↓								↓										
	Brighter	253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	
	↓	254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	
	Blue	255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	

0 : Low level voltage, 1 : High level voltage.

Each basic color can be displayed in 256 gray scales of red, 256 gray scales of green, and 256 gray scales of blue from 8 bit data signals. According to the combination of total 24 bit data signals, 16,777,216 color display can be achieved on the screen.

8. Optical characteristics $\Delta 2$

The optical measurement at the time of driving on the following conditions is shown in the following table.

Ta=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	$\theta 21$ $\theta 22$	CR ≥ 10	70	88	—	【Note1,2,7】
	Vertical	$\theta 11$ $\theta 12$		70	88	—	Fig8-1,8-3
Contrast ratio	CR		—	5000	—		【Note2,7】 Fig8-2
Response time	τ_{drv}	$\theta = 0^\circ$	—	4	—	ms	【Note3,4,5,7】 Fig8-1,8-2 Fig.8-5
Chromaticity of white	x		0.248	0.278	0.308	—	【Note4,7】 Fig8-1,8-2
	y		0.258	0.288	0.318	—	
Chromaticity of red	x		0.620	0.650	0.680	—	
	y		0.310	0.340	0.370	—	
Chromaticity of green	x		0.271	0.301	0.331	—	
	y		0.615	0.645	0.675	—	
Chromaticity of blue	x		0.121	0.151	0.181	—	
	y		0.038	0.068	0.098	—	
Transmittance uniformity $\Delta 2$	δ_w		—	—	1.25	—	【Note6,7】 Fig8-2
Transmittance $\Delta 2$	%		3.8	4.5		%	【Note7】 Fig8-2

*The measurement shall be executed 30 minutes after lighting at rating.

Optical characteristics are based on SHARP standard backlight system.

Drive conditions: LQ0DZC0051 (LR388H5) Typical Input Timing

Liquid-crystal impression voltage: VH255 15.2V, the flicker optimal state.

Backlight unit condition: Brightness MAX.

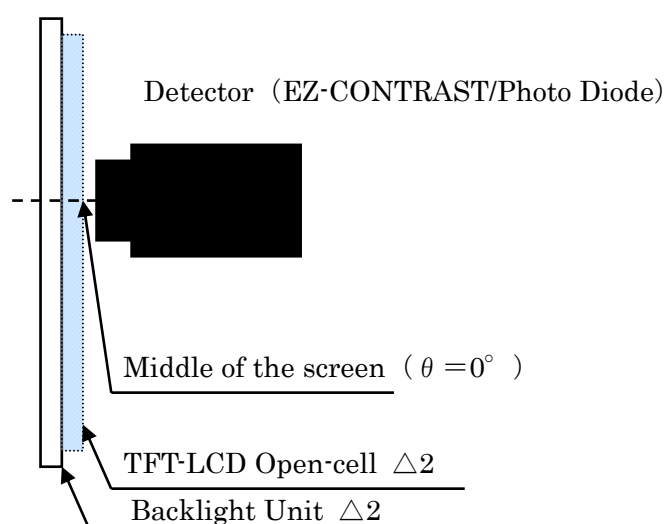


Fig.8-1 Measurement of viewing angle range and Response time.

Viewing angle range: EZ-CONTRAST
/Response time: Photo diode)

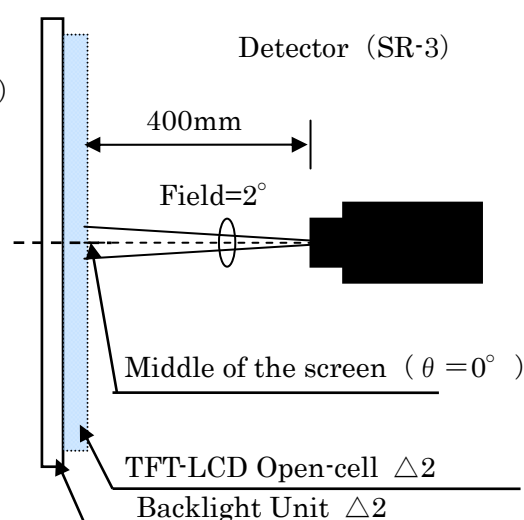


Fig.8-2 Measurement of luminance and chromaticity and Contrast.

【Note 1】 Definitions of viewing angle range

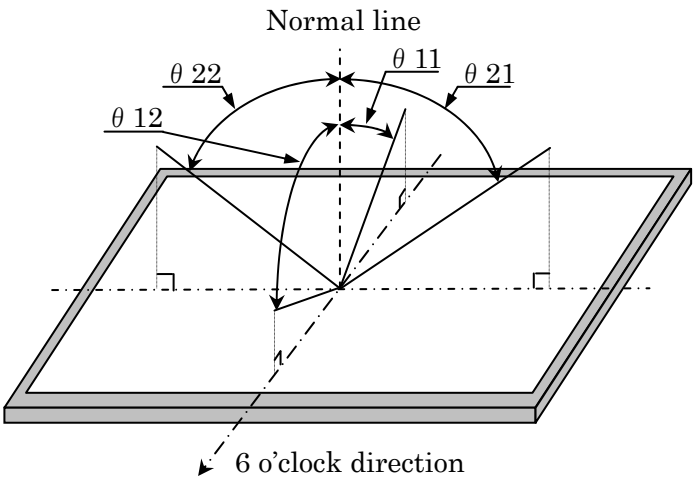


Fig. 8-3 Definitions of viewing angle range

【Note 2】 Definition of contrast ratio :

The contrast ratio is defined as the following.

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance(brightness) with all pixels white}}{\text{Luminance(brightness) with all pixels black}}$$

【Note 3】 Definition of response time

The response time of (τ_d and τ_r) is defined as the following figure.8-4 and shall be measured by switching the input signal for “any level of gray (0, 64, 128, 192, 255)” and “any level of (0, 64, 128, 192, 255)”.

	0	64	128	192	255
0		τ_{r0-64}	τ_{r0-128}	τ_{r0-192}	τ_{r0-255}
64	τ_{d64-0}		$\tau_{r64-128}$	$\tau_{r64-192}$	$\tau_{r64-255}$
128	τ_{d128-0}	$\tau_{d128-64}$		$\tau_{r128-192}$	$\tau_{r128-255}$
192	τ_{d192-0}	$\tau_{d192-64}$	$\tau_{d192-128}$		$\tau_{r192-255}$
255	τ_{d255-0}	$\tau_{d255-64}$	$\tau_{d255-128}$	$\tau_{d255-192}$	

t*:x-y...response time from level of gray(x) to level of gray(y)

$$\tau_r = \Sigma(\tau_{r:x-y})/10 \quad \tau_d = \Sigma(\tau_{d:x-y})/10 \quad \tau_{drv} = (\tau_r + \tau_d)/2$$

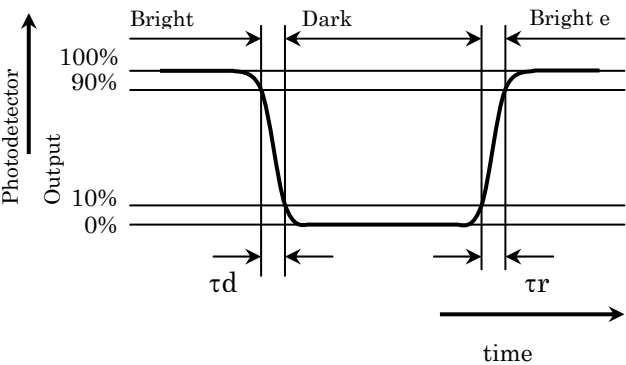


Fig. 8-4 Definitions of response time

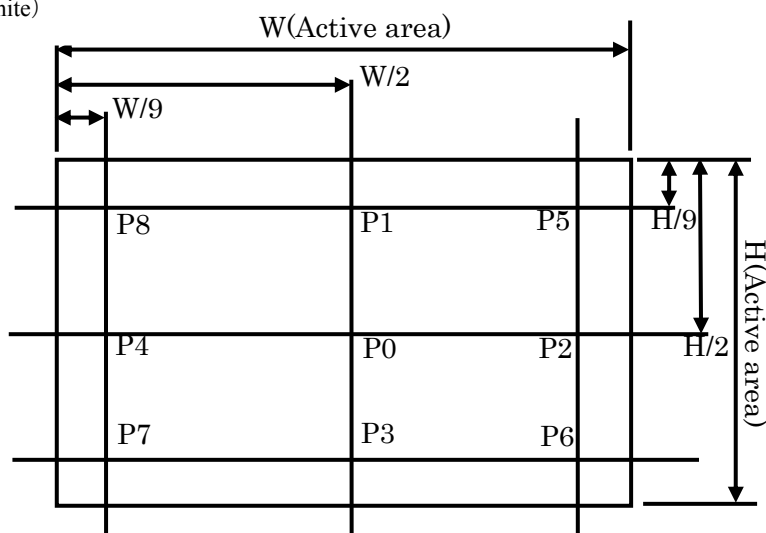
【Note 4】 This shall be measured at center of the screen.

【Note 5】 This value is valid when O/S driving is used at typical input time value.

【Note 6】 Definition of transmittance uniformity ; $\Delta 2$

Transmittance uniformity is defined as the following with nine measurements.(P0~P8)

$$\delta W = \frac{\text{maximum transmittance of nine points (White)}}{\text{minimum transmittance of nine points (White)}}$$

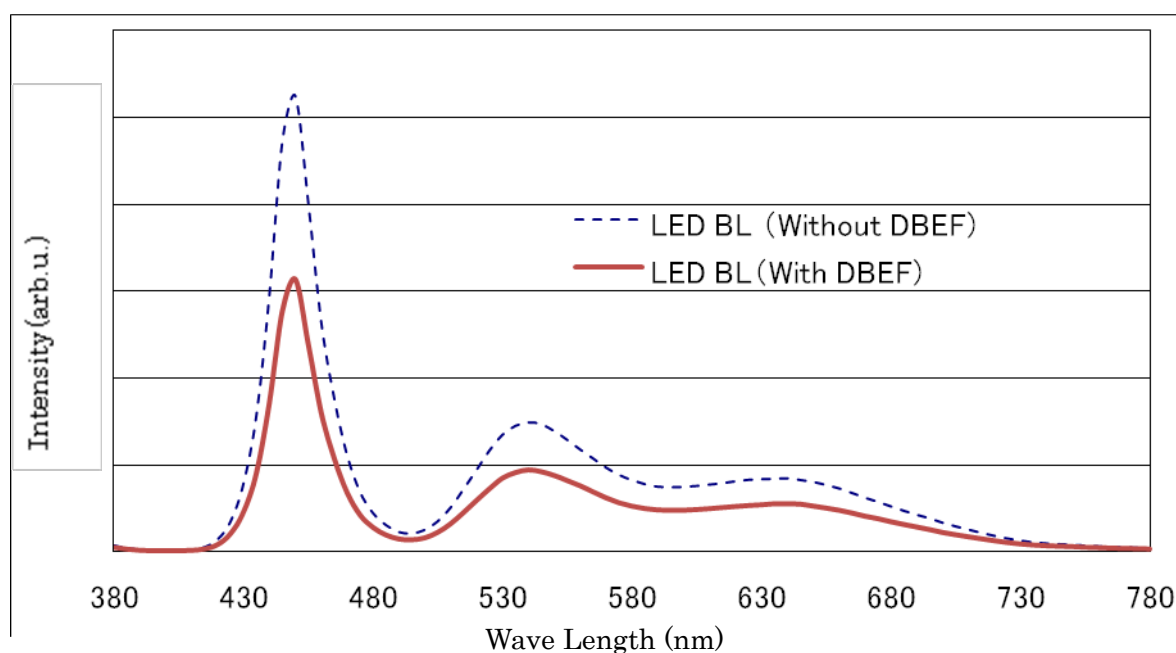


【Note 7】 SHARP standard backlight system $\Delta 2$

• Backlight

Parts	Specification	Remark
DBEF	DBEF-D3-260 (3M)	Need to remove DBEF when measuring the transmittance.
Upper Prism Sheet	BEF3-T-285 ASn (3M)	
Lower Prism Sheet	BEF3-T-285 ASn (3M)	
Diffuser Sheet	BS-910 (KEIWA)	
Light Guide Plate	PMMA $t=3.0$	
Reflection Sheet	E6SR-188 (Torey)	
LED	R.G phosphors type White LED (SHARP)	

• Spectrum each wavelength

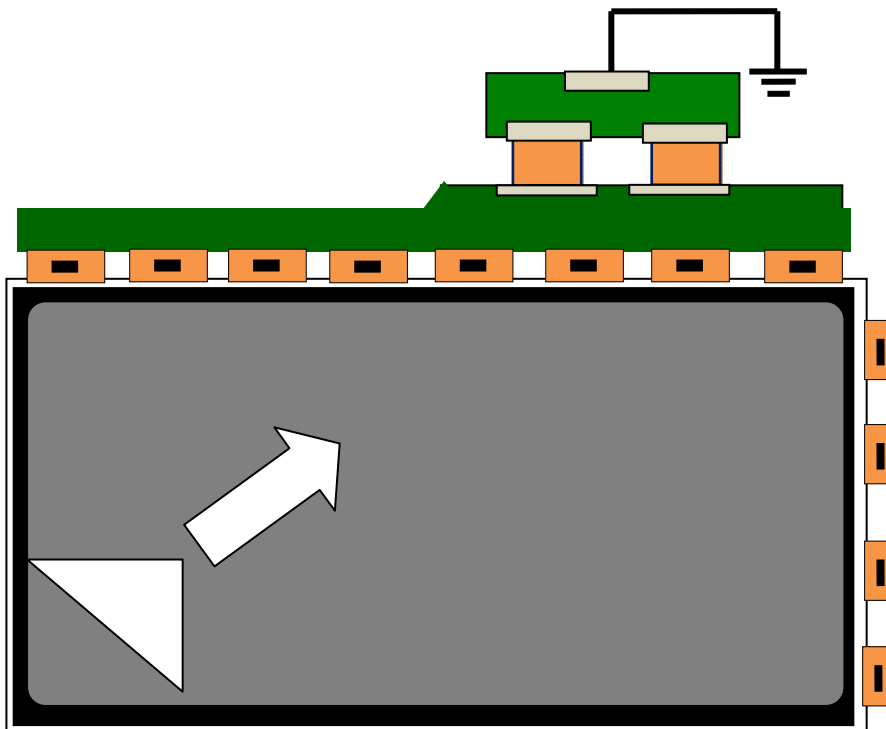


9. Display Quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standard.

10. Handling Precautions of the module

- a) Be sure to turn off the power supply when inserting or disconnecting the cable.
- b) Be sure to design the cabinet so that the Open Cell can be installed without any extra stress such as warp or twist.
- c) Since the polarizer is easily damaged, pay attention not to scratch it.
- d) Since long contact with water may cause discoloration or spots, wipe off water drop immediately.
- e) When the polarizer is soiled, wipe it with absorbent cotton or other soft cloth.
- f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.
- g) Precautions of peeling off the protection film.



- Be sure to peel off slowly (recommended more than 7sec) and constant speed.
- Peeling direction shows Fig.
- Be sure to ground person with adequate methods such as the anti-static wrist band.
- Be sure to ground S-PWB while peeling of the protection film.
- Ionized air should be blown over during peeling action.
- The protection film must not touch SOFs.
- If adhesive may remain on the polarizer after the protection film peeling off, please remove with isopropyl-alcohol.

- h) Since the Open Cell consists of TFT and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharges, persons who are handling the Open Cell should be grounded through adequate methods such as the anti-static wrist band. Connector pins should not be touched directly with bare hands.

- Reference : Process control standard of sharp

	Item	Management standard value and performance standard
1	Anti-static mat (shelf)	1 to 50 [M ohm]
2	Anti-static mat (floor, desk)	1 to 100 [M ohm]
3	Ionizer Attenuate	from +1000V to +100V within 2 sec
4	Anti-static wrist band	0.8 to 10 [M ohm]
5	Anti-static wrist band entry and ground resistance	Below 1000 [ohm]
6	Temperature	22 to 26 [°C]
7	Humidity	60 to 70 [%]

- i) The Open Cell has some PWBs, take care to keep them from any stress or pressure when handling or installing the Open Cell, otherwise some of electronic parts on the PWBs may be damaged.
- j) When handling the Open Cell and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the Open Cell.
- k) Applying too much force and stress to PWB and SOF may cause a malfunction electrically and mechanically. Particularly for the structure with bent or folded SOF(s), be sure to design the cabinet after enough evaluation of trial products.
- l) The Open Cell has high frequency circuits. Sufficient suppression to EMI should be done by system manufacturers.
- m) Please be careful since image retention may occur when a fixed pattern is displayed for a long time.
- n) The chemical compound, which causes the destruction of ozone layer, is not being used.
- o) This Open Cell is corresponded to RoHS. "R.C." label on the side of palette shows it.
- p) This Open Cell passes over the rust.
- q) For any reason, never disassemble the Open Cell.
- r) When any question or issue occurs, it shall be solved by mutual discussion.

11. Reliability test item

No	Test item	Conditions	Remark
1	High temperature storage test (Open cell)	Ta = +60°C 240h	
2	Low temperature storage test (Open cell)	Ta = -25°C 240h	
3	High temperature & high humidity operation test (Open cell)	Ta = +40°C ; 90%RH 240h (No condensation)	
4	High temperature operation test (Open cell)	Ta = +50°C 240h	
5	Low temperature operation test (Open cell)	Ta = 0°C 240h	
6	ΔI Vibration test (Cell Box with full Open Cells)	X and Y direction: 15min, Z direction: 60min. 5Hz to 50Hz acceleration: 1.0G Sweeping ratio: 3min	
7	ΔI Drop test (Palette with full Cell Box)	Height: 15cm (cantilever drop test) Number: 4times (edge 4times)	

[Result evaluation criteria]

Under the display quality test condition with normal operation state, there shall be no change, which may affect practical display function.

12. Packing for shipping

12.1 Packing form △2

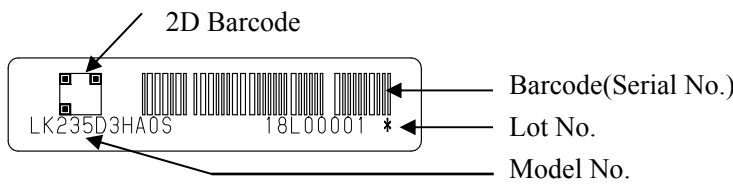
- a) Open Cell quantity in 1 cell box : 15 pcs
- b) Piling number of cell box : 8 Maximum
- c) 1 cell box size : 705(W) x 478(D) x 116(H) [mm]
- d) Total mass of 1 cell box filled with full open cells : 10.9[kg] Typ.
- e) Open Cell quantity in 1 palette : 240 pcs
- f) 1 palette size : 1000(W) x 750(D) x 1050(H) [mm]
- g) Total mass of 1 palette filled with full open cells : 187[kg] Typ.

[Note] Please refer to the attached drawing for details. (P26, P27)

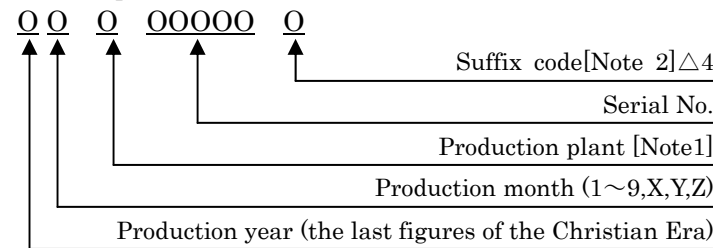
12.2 Label

- a) Open Cell Label (Size: 40(H) x 9(V) [mm]) △3

This label is stuck on the Source PWB.



How to express Lot No.



[Note1]

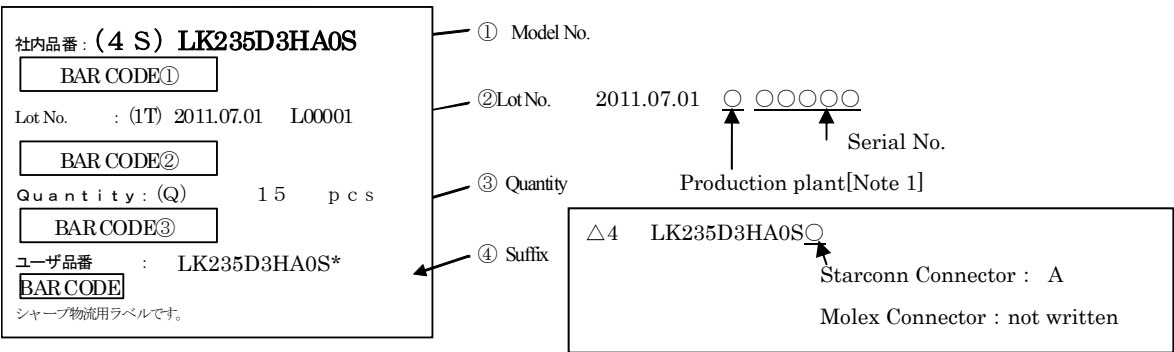
Code	Plant	Model No.
K	Kameyama	LK235D3HA0S
S	SMK	LK235D3HA0S
L	KYTC	LK235D3HA0S

[Note2] △4

Code	Using Connector
	Molex Connector
A	Starconn Connector

- b) Packing label (Size: 80mm(H) x 60mm(V)) △2

This label is stuck on the cell box.



c) Pallet label (Size: 105mm(H) x 168mm(V)) △2

This label is stuck on the palette.

2D Barcode

10N* 10701ZZZZ0000001

Panel shipment label
Kameyama Plant No.1

Destination : ZZZZ
Cell number : 240cells
Product number : (4S) LK235D3HA0S

BAR CODE①

Lot No. : (1T) 20110701 (20110701)

BAR CODE②

Quantity : (Q) 240 pcs

BAR CODE③

User Product number : LK235D3HA0S*

BAR CODE

PARTS NAME : LK235D3HA0S

PANEL BOX SET ID: *****

BAR CODE

R.C. Made In Japan

Palet serialNo
10N* ○ ○ ○ ○ ZZZZ ○ ○ ○ ○ ○ ○ ○ ○ △3

Serial No.
Shipping date : (MMDD)
Shipping year (the last figures of the Christian Era)

① ModelName
② Lot. No.
③ Quantity
④ Suffix

△4 User Product number : LK235D3HA0S○
Starconn Connector : 'A'
Molex Connector : not written

13. Cell box condition

Temperature	0°C to 40°C
Humidity	95% RH or less
Reference condition	20°C to 35°C, 85% RH or less (summer) 5°C to 15°C, 85% RH or less (winter) the total storage time (40°C, 95% RH) : 240h or less
Sunlight	Be sure to shelter a production from the direct sunlight.
Atmosphere	Harmful gas, such as acid and alkali which bites electronic components and/or wires must not be detected.
Notes	Be sure to put cartons on palette or base, don't put it on floor, and store them with removing from wall. Please take care of ventilation in storehouse and around cartons, and control changing temperature is within limits of natural environment.
Storage life	1 year.

14.Caring for the Liquid Crystal panel

General instructions of "Caring for the Liquid Crystal panel" to our customer are as follows;

1. Gently wipe the surface of the display panel with a soft cloth (cotton, flannel, etc.).
Wiping with a hard cloth or using strong force may scratch the surface of the display panel.
2. Use a soft damp cloth to gently wipe the display panel when it is really dirty.
(It may scratch the surface of the display panel when wiped strongly.)
3. If the display panel is dusty, use an anti-static brush, which is commercially available, to clean it.
4. To protect the display panel, do not use a dirty cloth, liquid cleaners, or a chemical cloth (wet/dry sheet type cloth, etc.).

This may damage the surface of the display panel.

*Note

Recommended treatment for the surface of Polarizer

1. Do not touch the surface of the Polarizer.
When transporting or working on the display, handle with care not to touch the Polarizer.
2. Use an anti-static brush, if the surface of the Polarizer is dusty.
Take care of damages and stains of the brush.
3. Do not stack the display modules.
4. Clean with following steps, if stains are on the surface.
 - a)Wipe with an approved clean cloth.
 - b)Breathe on the stain and wipe.
 - c)Wipe with a clean cloth damped with minimum quantity of IPA or Ethanol diluted with water.

"Caution"

:Do not use too much solvent.

It may causes spots, and the risk of scratches will increase to clean the spots.

:Take care of damages and stains of a cloth.

A change of cloths must be required regularly.

Old cloths may scratch the Polarizer.

:Make sure that the treatment is appropriate, first

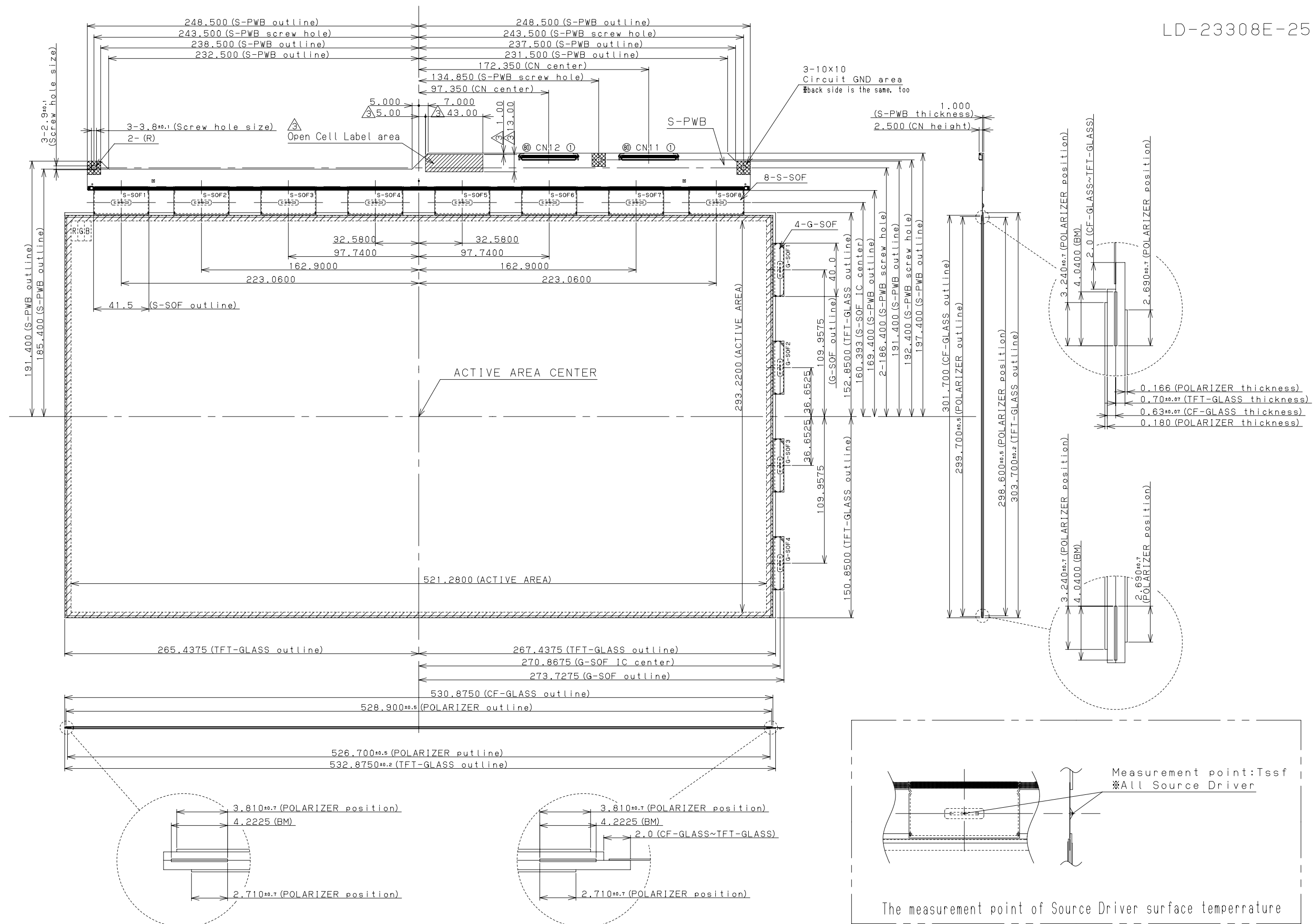
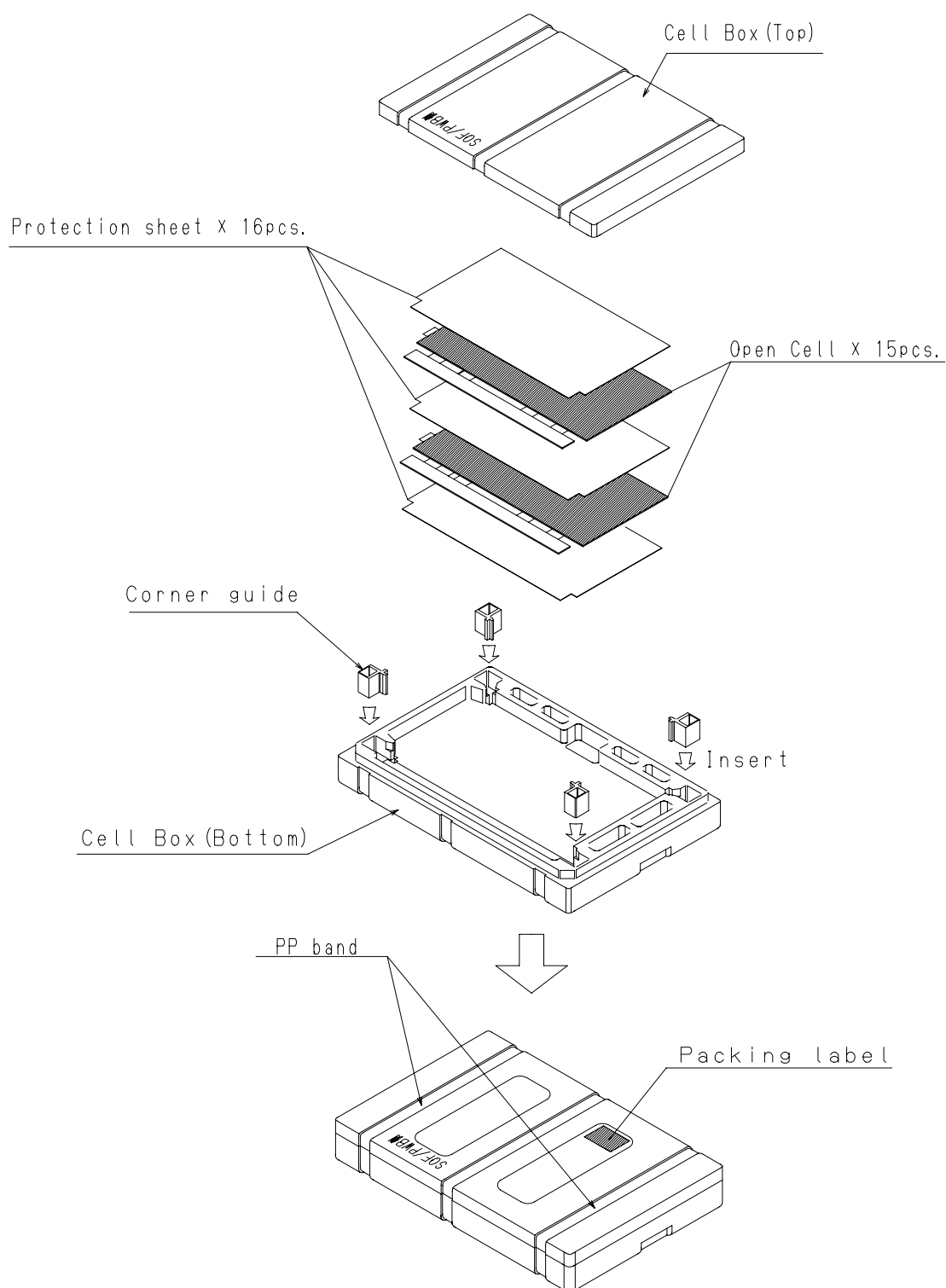
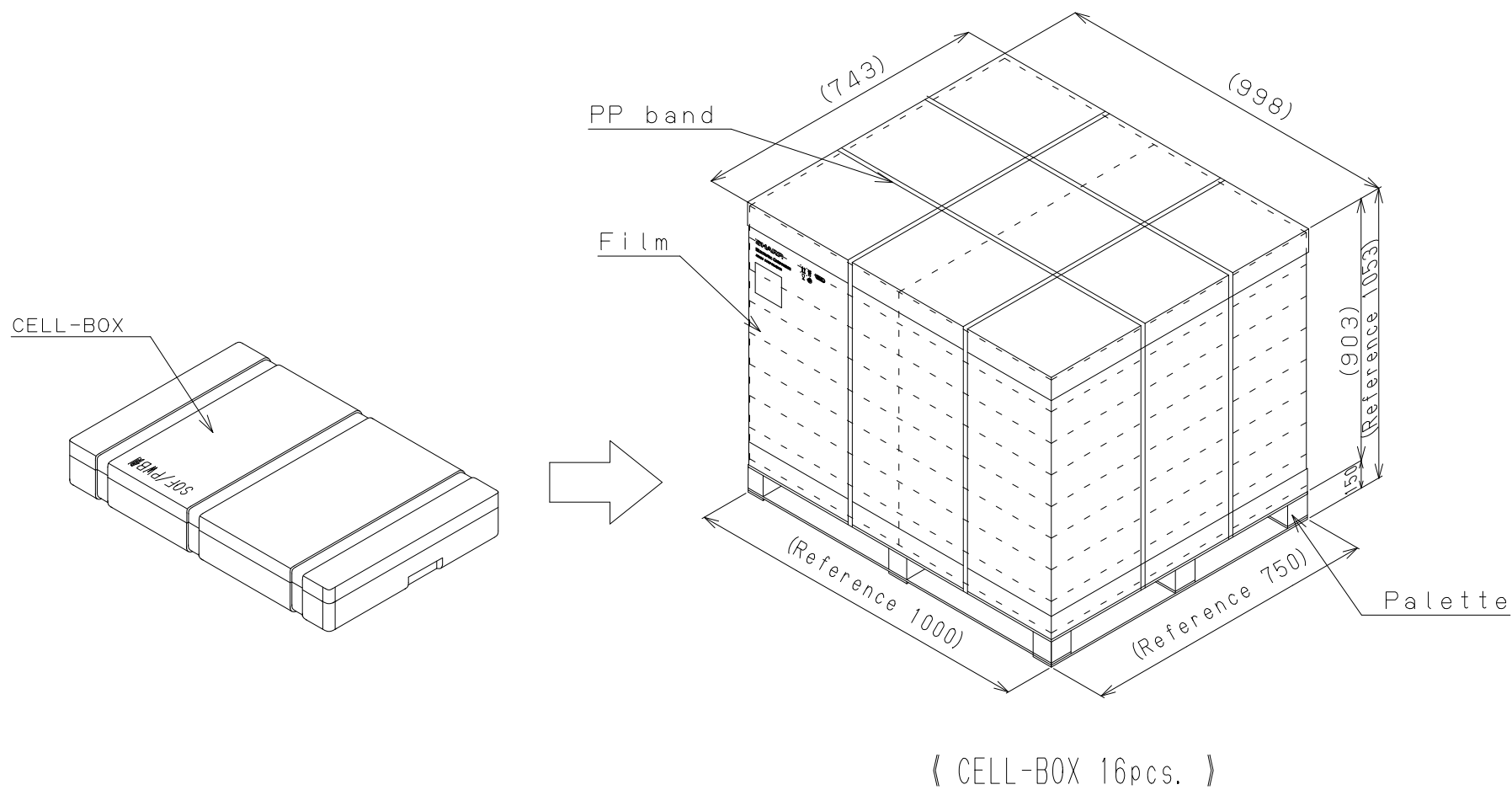


Fig.1 OPEN CELL OUTLINE DIMENTION (LK235D3HAS0S)



	Parts name	Material
1	Cell Box (Bottom)	EPS 30P (antistatic)
2	Cell Box (Top)	EPS 30P (antistatic)
3	Corner guide	LDPE
4	Protection sheet	PE sheet t1.0 (antistatic)

Fig.2-1 Packing Form (LK235D3HA0S)



△1 Fig.2-2 Packing form (LK235D3HA0S)