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# SPECIFICATION

DEVICE SPECIFICATION for

Passive Matrix Color LCD Module

(320 × RGB × 240 dots)

Model No.

**LM050QC1T01**

☐CUSTOMER'S APPROVAL

DATE _____

BY _____

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[HANDLING INSTRUCTIONS]

・General Precautions

1) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
2) Water droplets must be wiped off immediately as those may cause color changes and / or stains if remained for a long time. (If the surface of the LCD panel is soiled, wipe it swiftly with cotton or other soft cloth. If it is not still clear completely, blow on and wipe it.)
3) Dropping the LCD module or hitting hard object with the LCD module may cause a cracking of LCD glass or others parts.
4) Do not use any materials, which may emit gas. Epoxy resin (amine's hardener) and silicone adhesive agents (dealcohol or deoxym) are known as materials, which may cause a color change of polarizer etc.
5) Disassembling the LCD module may cause a permanent damage. It should be strictly avoided.

**WARNING**

**Don't use any materials, which emit following gas from epoxy resin (amines' hardener) and silicone adhesive agent (dealcohol or deoxym) to prevent change polarizer color owing to gas.**

・Precautions in Mounting

1) LCD module has viewing angle characteristics specified as in below. Take these into consideration when design customer's system. Set the LCD module in customer's system as the optimum viewing direction and viewing angle meet customer's purpose. For the specific values of θy, refer to the Table 9.

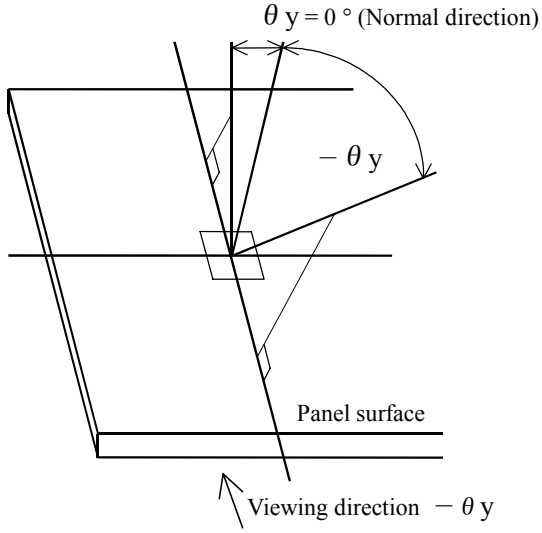


Fig.1 Definition of viewing angle

2) Keep following instructions to prevent electrostatic damages of CMOS LSIs, which are contained in the LCD module.

1. Operator

Electrostatic shielding clothes shall be worn to avoid electrostatic discharges from human body.

2. Equipment

There is a possibility that the static electricity is charged to equipment that has a function of peeling something or making friction (ex: conveyer, soldering iron, working table). These equipments should be grounded through approx. $1 \times 10^8$ ohms resistance.

3. Floor

Floor is an important part to leak static electricity, which is generated from human body or equipment. There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure (electrostatic earth: $1 \times 10^8$ ohms) should be made.

4. Humidity

Proper level of humidity of working area may reduce the resistance of the material that generates electrostatics charges and also reduce the chance of charging up something. Keep the humidity over 50 %.

5. Transportation and storage

Containers could also be easily charged up during transportation and storage. Make sure not to cause ESD (electrostatic discharges) during transportation and storage.

6. Others

The laminator (protective plastic film) is attached on the surface of LCD module to protect from scratches, stains and dust. Make sure to peel off the laminator slowly with using ion blower.

3) LCD module is susceptible to external mechanical force, and even a very light stress would cause color change. Therefore, make sure to mount LCD module to flat surface so that it will not be bent nor be twisted when installing the module in the customer system.

4) When the mating connector is inserted, it should be parallel to the used connector of LCD module and it should be inserted on horizontal firm base. When the mating connector is fixed to LCD connector, it should be inserted properly in order not to create a gap as shown “A”. Please insert the connector as both edge is placed to the connect position of LCD connector.

i) Method of correct insertion

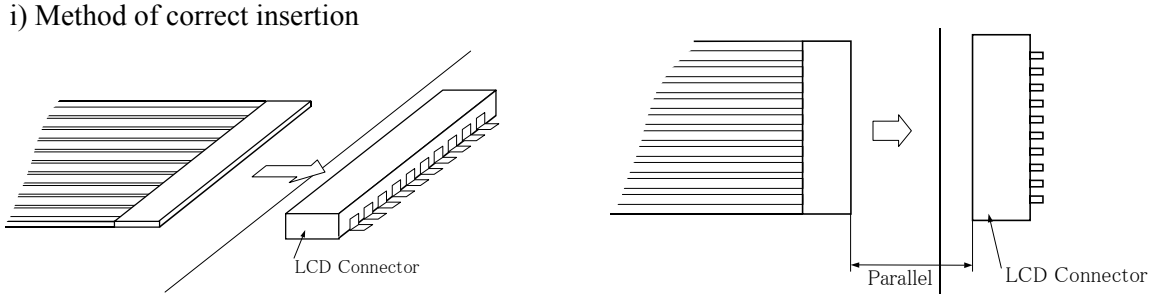


Fig.2

ii) Method of wrong insertion

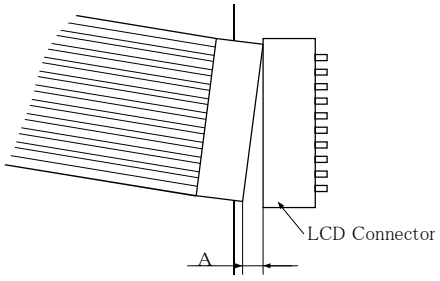


Fig.3

5) It is recommended to connect GND in the customer’s system to GND in the LCD module by high resistance means before the mating connector is inserted.

・Precautions for Storage

1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.

2) Liquid crystal may be frozen and be deteriorated if stored below the rated storage temperature. Liquid crystal may become an isotropic liquid if stored above the rated storage temperature and may not retain its original properties. The humidity outside of specified range may damage the polarizers.
Therefore, the LCD module should always be stored within specified temperature range.

・Precautions for LCD Operation

Be sure to perform a setup of LCD module within absolute rating given in the specifications.

It cannot guarantee about the failure by use with value other than specification regulation.

Please use this LCD module after sufficient evaluation and a check by the customer's production.

1) Keep power ON / OFF sequence specified in
2) Table 12 to prevent a latched-up of driver LSI and a DC charge to the LCD panel.
3) Applying DC voltage to LCD panel will cause a rapid degradation of liquid crystal.
   So, drive the LCD panel with an alternating pulse (M signal) continuously.
4) CCFT (Cold Cathode Fluorescent Tube) backlight should be kept OFF during VDD is “L” level.
5) This specification specifies the characteristics of LM050QC1T01 (320 × RGB × 240 dots) in no gray scale mode. Display quality in gray scale mode is not specified in this specification as it may vary depending on the method of gray scaling. Be carefully evaluated display quality by customer's production, because the quality is depending upon the gray scaling method of controller.
6) Set the value of frame cycle after sufficient evaluation because the frame cycle has influence on power consumption and display quality.
7) It is recommended to set lamp current of CCFT backlight less than 5.0 mArms so that heat radiation of CCFT backlight may affect the display quality.
8) Application of a fixed pattern for a long time may cause image retention; maintaining a displaying pattern. It is not deterioration of LCD. To prevent image retention, please do not apply the fixed pattern for a long time by pre-installing such programs at your side.
9) The appropriate design measures should be taken to prevent overcurrent in short-circuited state.

・Others

1) Specific brominated flame retardants are not used in the LCD module.
2) Plumbum and (DOP) DiOctyl Phthalate are not used in FFC (Flexible Flat Cable) and CCFT cables.

<Contents> Page

1. Application

This data sheet is to introduce the specification of LM050QC1T01, negative matrix type color LCD module with CCFT backlight.

2. Construction and Outline

Construction: 320 × RGB × 240 dots transmissive LCD panel, PWB (Printed Wiring Board) with electrical components mounted onto, TCP (Tape Carrier Package) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT backlight and bezel to fix them mechanically.

Signal ground (VSS) is connected with the metal bezel.

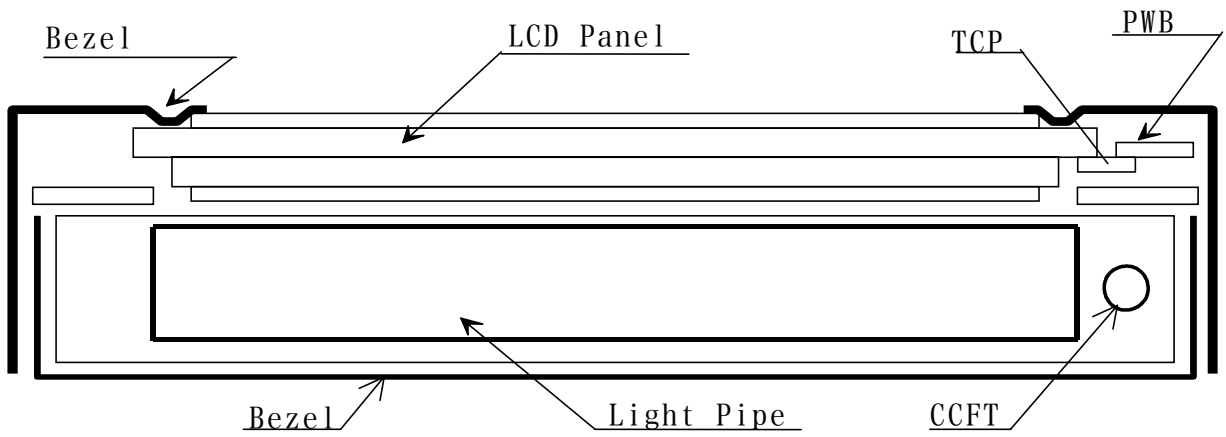


Fig.4

Outline: See Fig.16.

Connection: See Fig.16, Table 6 and 7.

The LCD module shall meet the following inspection standard: S-U-035-10.

3. Mechanical Specification

Table 1

| Parameter | Specifications | Unit |
|---|---|---|
| Outline dimensions | 134 ± 0.4 (W) × 100 ± 0.4 (H) × 8.5 ± 0.5 (D) | mm |
| Active area | 103.4 (W) × 78.3 (H) | mm |
| Display format | 320 (W) × RGB × 240 (H) | - |
| Dot size | 0.08 × RGB (W) × 0.29 (H) | mm |
| Dot spacing | 0.025 | mm |
| Base color *1 | Normally black*2 | - |
| Weight | Approx. 145 | g |

*1 Due to the characteristics of the LC material, display color varies with temperature.

*2 Negative-type display

Display data “H”: Display ON = transmission

Display data “L”: Display OFF = light isolation

4. Absolute Maximum Ratings

4-1. Electrical absolute maximum ratings

Table 2

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Logic supply voltage | VDD - VSS | 0 | 7.0 | V | Ta = 25 °C |
| Input signal voltage | VIN - VSS | - 0.3 | VDD + 0.3 | V | Ta = 25 °C |
| LCD supply voltage | VEE - VSS | 0 | 32 | V | Ta = 25 °C |

4-2. Environment conditions

Table 3

| Item | Tstg | | Topr | | Remark |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| Ambient temperature (Ta) | - 20 °C | + 60 °C | 0 °C | + 40 °C | Note 2) |
| Humidity | Note 1) | | | | No condensation |

Tstg: Storage temperature. Topr: Operating temperature.

Note 1) Ta ≦ 40 °C: 95 % RH Max.

Ta ＞ 40 °C: Absolute humidity shall be less than 95 % RH at Ta = 40 °C.

Note 2) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

4-3. Vibration and Shock conditions

(1) Vibration test

Table 4

| Frequency | 10 Hz to 57 Hz | 57 Hz to 500 Hz |
|---|---|---|
| Vibration level | - | 9.8 m/s² |
| Vibration width | 0.075 mm | - |
| Interval | 10 Hz to 500 Hz to 10 Hz / 11.0 min | |

Ta = 25 ± 5 °C. Non-operating.

2 hours for each direction of X, Y and Z (6 hours as total).

(2) Shock test

Ta = 25 ± 5 °C. Non-operating.

Acceleration: 490 m/s².

Pulse width: 11 ms.

3 times for each directions of ± X, ± Y and ± Z.

5. Electrical Specifications

5-1. Electrical characteristics

Table 5

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage (Logic) | $V_{DD}$ - $V_{SS}$ | Ta = 0 to 40 ℃ | | 3.0 | 3.3 | 3.6 | V |
| Supply voltage (LCD) (Note 1, 2) | $V_{EE}$ - $V_{SS}$ | Ta = 0 ℃ | | | 27 | 29 | V |
| | | Ta = 25 ℃ | | | 26 | | |
| | | Ta = 40 ℃ | | 22.5 | 25 | | |
| Input signal voltage for YD, LP, M, DISP | $V_{IH}$ | "H" level | Ta = 0 to 40 ℃ | 0.8 $V_{DD}$ | - | $V_{DD}$ | V |
| | $V_{IL}$ | "L" level | | 0 | - | 0.2 $V_{DD}$ | |
| Input signal voltage for XCK, D0 to 7 | $V_{IH}$ | "H" level | | 0.7 $V_{DD}$ | - | $V_{DD}$ | |
| | $V_{IL}$ | "L" level | | 0 | - | 0.3 $V_{DD}$ | |
| Supply current | $I_{DD}$ | Ta = 25 ℃ (Note 3) | | - | 0.6 | 1.0 | mA |
| | $I_{EE}$ | | | - | 8 | 12 | mA |
| Power consumption | Pd | Ta = 25 ℃ (Note 3, 4) | | - | 210 | 315 | mW |

Note 1) Maximum contrast ratio is obtained from a proper VEE value.

Note 2) Frame Cycle = 120 Hz.

Note 3) Frame Cycle = 120 Hz, VDD = 3.3 V, VEE – VSS = 26 V.

Display pattern = Checker pattern, shown as below;

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Note 4) Backlight power consumption is not included.

5-2. Interface signals

<LCD>

Table 6

| Pin No. | Symbol | Function | Level |
|---|---|---|---|
| 1 | YD | Scan Start-up signal | “H” |
| 2 | LP | Input data latch signal | “H” -> ”L” |
| 3 | VSS | Ground potential | - |
| 4 | XCK | Data input clock signal | “H” -> ”L” |
| 5 | VSS | Ground potential | - |
| 6 | M | Alternating signal | - |
| 7 | DISP | Display control signal | ”H” (ON), ”L” (OFF) |
| 8 | VDD | Power supply for logic | - |
| 9 | VEE | Power supply for LCD | - |
| 10 | VSS | Ground potential | - |
| 11 | D0 | Display data signal | ”H” (ON), ”L” (OFF) |
| 12 | D1 | Display data signal | ”H” (ON), ”L” (OFF) |
| 13 | D2 | Display data signal | ”H” (ON), ”L” (OFF) |
| 14 | D3 | Display data signal | ”H” (ON), ”L” (OFF) |
| 15 | D4 | Display data signal | ”H” (ON), ”L” (OFF) |
| 16 | D5 | Display data signal | ”H” (ON), ”L” (OFF) |
| 17 | D6 | Display data signal | ”H” (ON), ”L” (OFF) |
| 18 | D7 | Display data signal | ”H” (ON), ”L” (OFF) |
| 19 | VSS | Ground potential | - |
| 20 | VSS | Ground potential | - |

Used connector: 9632S-20A-T (IRISO Electronics Co., Ltd.)

Correspondence connector: FFC / FPC (0.5 mm pitch 20 pins).

Conductor width = 0.3 mm.

Conductor length = 3.0 mm MIN.

Insertion thickness = 0.3 mm.

<CCFT>

Table 7

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | HV | High voltage line |
| 2 | NC | - |
| 3 | GND | Ground line |

Used connector: BHR-03VS-1 (J.S.T. MFG. Co., Ltd.)

Correspondence connector: SM02(8.0)B-BHS-1-TB (J.S.T. MFG. Co., Ltd.)

S02(8.0)B-BHS (J.S.T. MFG. Co., Ltd.)

※Except above connector mentioned in <LCD> and <CCFT> shall be out of guaranty.

5-3. Interface timing ratings

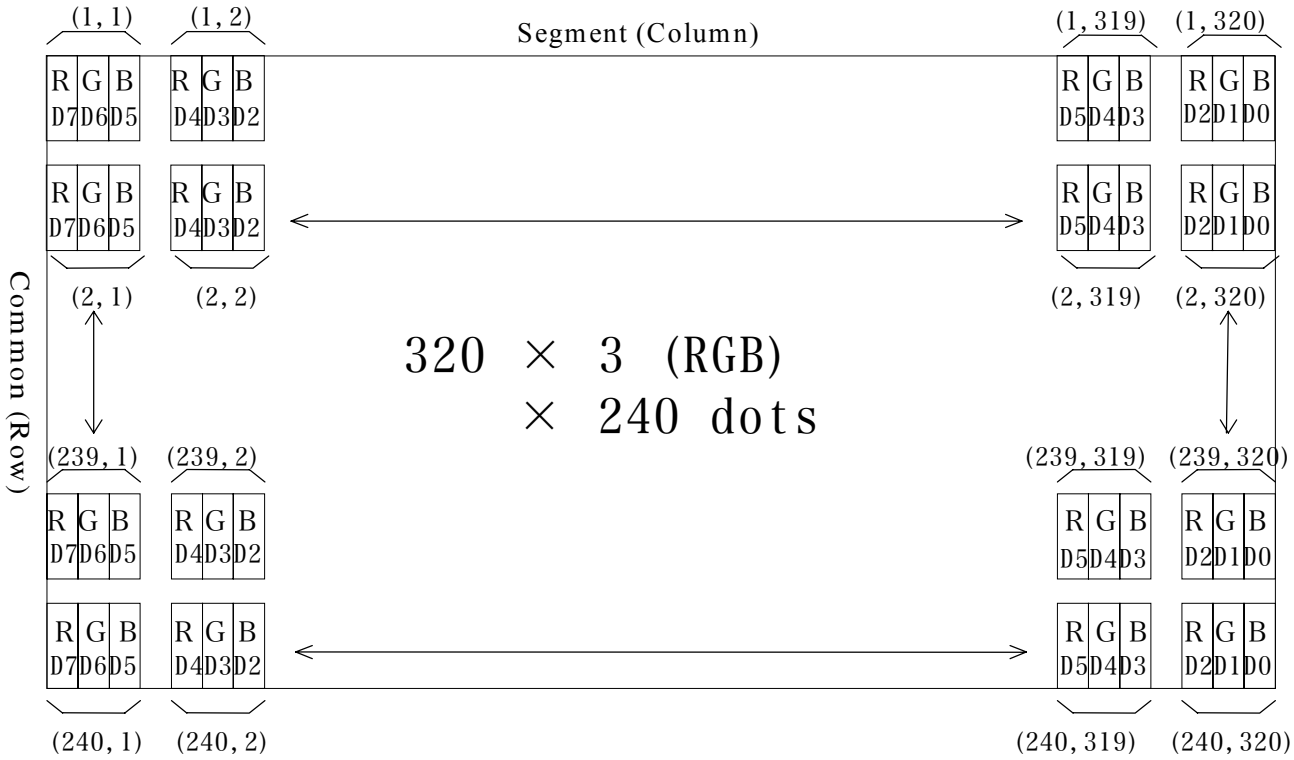
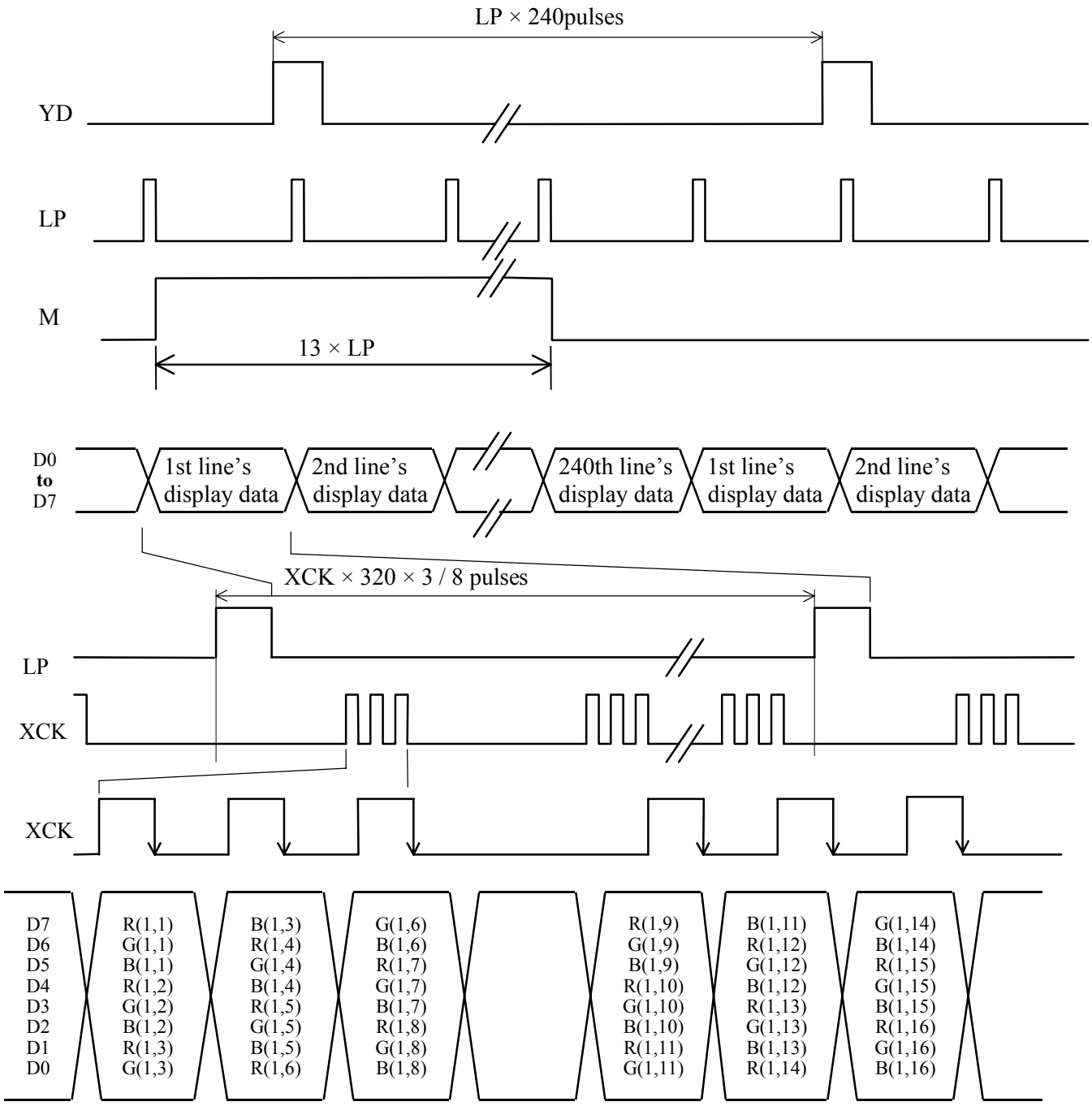
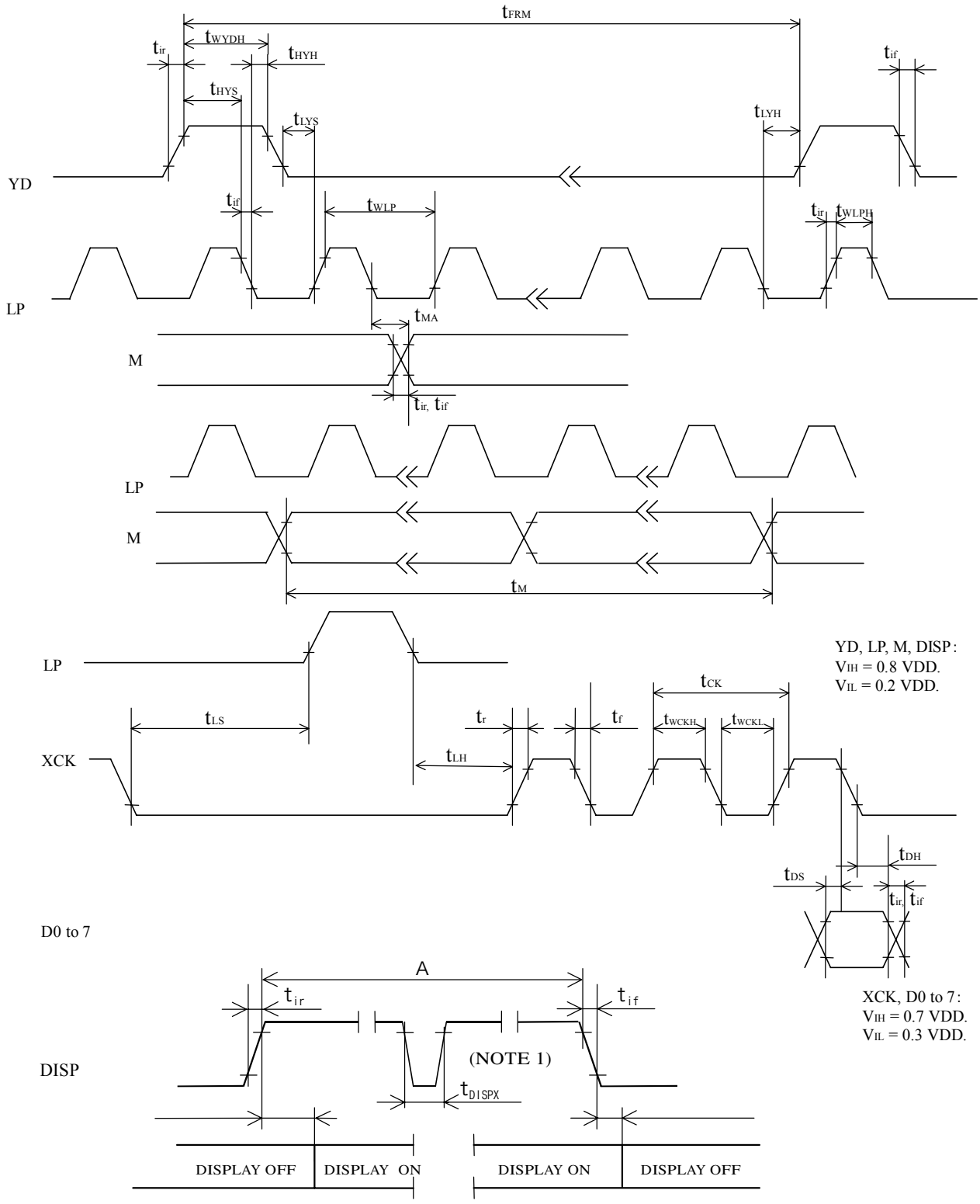



Fig.5 Dot chart of display area




*Electrical and optical characteristics are specified by above condition.

Fig.6 Data input timing chart




(NOTE1) In order to keep operating LCD display during "A" period, DISP signal should be "H" level so that $V_{IH}$ (0.8 VDD) do not break into the line. $t_{DISPX}$ = 0 ns MAX.

Fig.7 Interface timing chart

Table 8

Ta = 25 °C, VDD = 3.3 V ± 10 %

| Item | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | MIN. | TYP. | MAX. | |
| Frame cycle *2 | $t_{FRM}$ | 5.56 | 8.33 | 16.67 | ms |
| XCK signal clock cycle | $t_{CK}$ | 81 | | | ns |
| "H" level clock width | $t_{WCKH}$ | 35 | | | ns |
| "L" level clock width | $t_{WCKL}$ | 35 | | | ns |
| LP signal "H" level pulse width | $t_{WLPH}$ | 200 | | | ns |
| Data set up time | $t_{DS}$ | 15 | | | ns |
| Data hold time | $t_{DH}$ | 25 | | | ns |
| YD signal "H" level set up time | $t_{HYS}$ | 100 | | | ns |
| YD signal "H" level hold time | $t_{HYH}$ | 100 | | | ns |
| YD signal "L" level set up time | $t_{LYS}$ | 100 | | | ns |
| YD signal "L" level hold time | $t_{LYH}$ | 100 | | | ns |
| YD signal "H" level pulse width | $t_{WYDH}$ | | | $t_{WLP}$ | |
| LP↑ allowance time from XCK↓ | $t_{LS}$ | 200 | | | ns |
| XCK↑ allowance time from LP↓ | $t_{LH}$ | 200 | | | ns |
| M signal clock cycle | $t_M$ | 13 × 2 × LP ↓ | | | pulses |
| M↑↓ allowance time from LP↓ | $t_{MA}$ | | | 50 | ns |
| XCK signal rise / fall time *1 | $t_r$,$t_f$ | | | 50 | ns |
| Input signal rise / fall time | $t_{ir}$,$t_{if}$ | | | 50 | ns |

*1 When LCD module is operated by high speed of XCK (shift clock), ($t_{CK}$ - $t_{WCKH}$ - $t_{WCKL}$) / 2 is maximum.

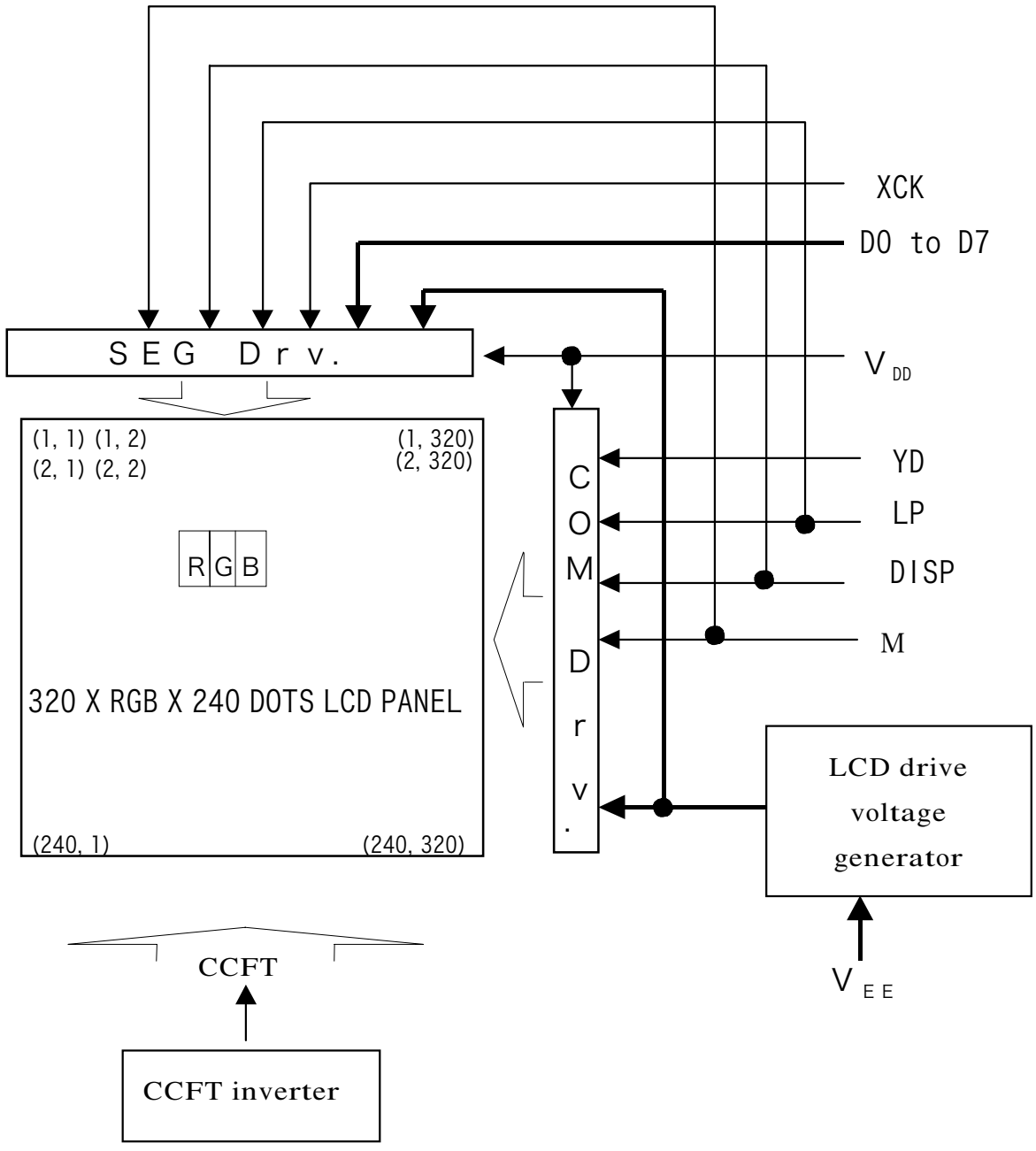
*2 Owing to the characteristics of LCD module, "shadowing" will become more eminent as frame cycle goes up, while flicker will be reduced. Since judgment of display quality is subjective and display quality such as "shadowing" is pattern dependent, it is recommended that decision of frame cycle, to which power consumption of the LCD module is proportional, be made based on your own through testing on the LCD module with every possible patterns displayed on it

*3 The intervals of one LP fall and next must be always the same, and LPs must be input continuously.

6. Module Driving Method

6-1. Circuit configuration

Fig.8 shows the block diagram of the module's circuitry.




Note1 : Signal ground (VSS) is connected with the metal bezel.

Fig.8 Circuit block diagram

6-2. Display face configuration

The display consists of 320 × 3 (RGB) × 240 dots as shown in Fig.5. The interface is single panel with single drive to be driven at 1 / 240 duty ratio.

6-3. Input data and control signal

The LCD driver (SEG Drv. shown in Fig.8) is 240 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits.

Input data for each row (320 dots × 3) will be sequentially transferred in the form of 8 bits parallel data through shift registers from top left of the display together with clock signal (XCK). When input of one row (320 dots × 3) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP) then, the corresponding drive signals will be transmitted to the (320 × 3) lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver (COM Drv. shown in Fig.8) to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and column electrodes of the LCD.

While the data of 1st row are being displayed, the data of 2nd row are entered. When the 2nd data for (320 × 3) dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 240th row of each display segment, from upper row to lower rows, to complete one frame of display by time-sharing method. Then data input proceeds to the next display frame. YD generates scan signal to drive scan electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive waveform shall be inverted at every display frame to prevent the generation of such DC voltage. Control signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display module goes up with the clock cycle of XCK. To reduce data transfer speed of XCK clock the LSI has the system of transferring 8 bits parallel data through the 8 lines of shift registers. Thanks to this system the power consumption of the display module is reduced. In this circuit configuration, 8 bits display data shall input to data input pins of D0 to 7.

Furthermore, the display module has bus line system for data input to reduce the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows: The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI right next side is selected when data of 240 dots (30 XCKs) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face. Thus data input will be made through 8 bits bus line sequentially from the left end of the display face.

Since this display module contains no refresh RAM, it requires the above data and timing pulse inputs even for static display.

The timing chart of input signals is shown in Fig.6,7 and Table 8.

7. Optical Characteristics

θx and θy are defined as angles from normal direction to parallel (x) direction and to perpendicular (y) direction, respectively, as shown in Fig.9.

Vmax is defined as the VEE value, where the contrast ratio [(brightness of "White") / (brightness of "Black")] will be maximum at normal direction (θx = θy = 0 °), as shown in Fig.10.

Following specifications are based upon $V_{EE}$ = Vmax.

Table 9

Ta = 25 °C, $V_{DD}$ = 3.3 V, $V_{EE}$ - $V_{SS}$ = Vmax.

| Parameter | | Symbol | Condition | | MIN. | TYP. | MAX. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|---|
| Viewing angle range | | θx | Co > 5.0 | θy = 0 ° | - | - 35 to 35 | - | degree | Note 1) |
| | | θy | | θx = 0 ° | - | - 25 to 15 | - | degree | |
| Contrast ratio | | Co | θx = θy = 0 ° | | - | 30 | - | - | Note2) |
| Response time | Rise | τr | θx = θy = 0 ° | | - | 230 | - | ms | Note3) |
| | Decay | τd | θx = θy = 0 ° | | - | 120 | - | ms | |
| Module chromaticity | white | x | θx = θy = 0 ° | | - | 0.31 | - | - | |
| | | y | θx = θy = 0 ° | | - | 0.34 | - | - | |

Note 1) The viewing angle range is defined as shown Fig.9.

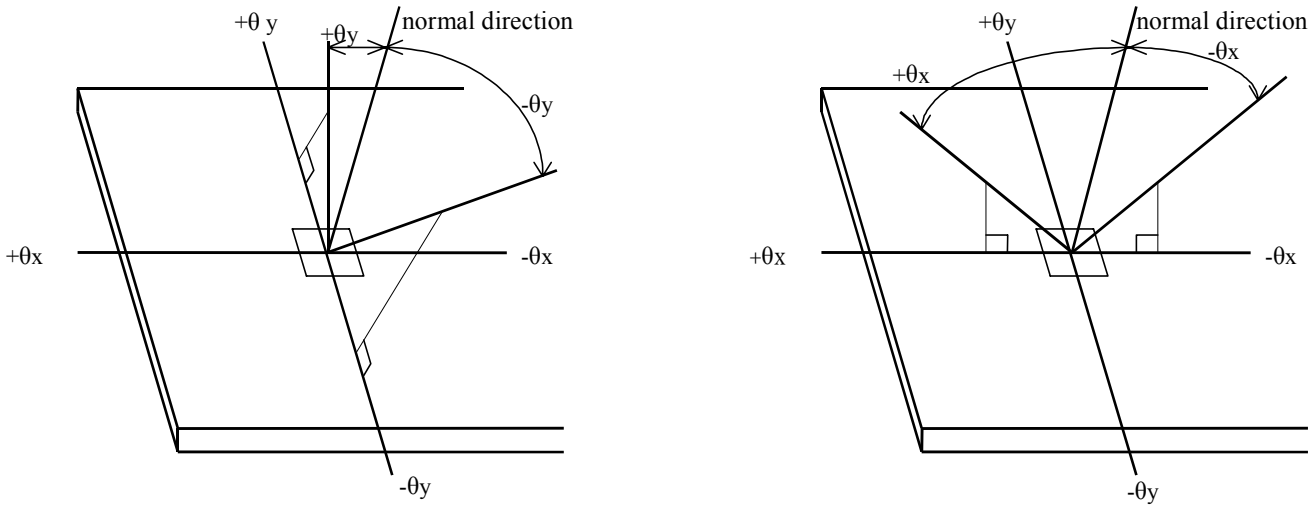



Fig.9 Definition of Viewing Angle

Note 2) Contrast ratio (Co) is defined as follows:

$$Co = \frac{\text{Luminance (brightness) all pixes "White" at Vmax}}{\text{Luminance (brightness) all pixes "dark" at Vmax}}$$

Note 3) The response times are defined as rising and decaying times of response waveform, which is photo-detector output induced by applying drive waveform to select and deselect the measuring dot, as shown in Fig.12.

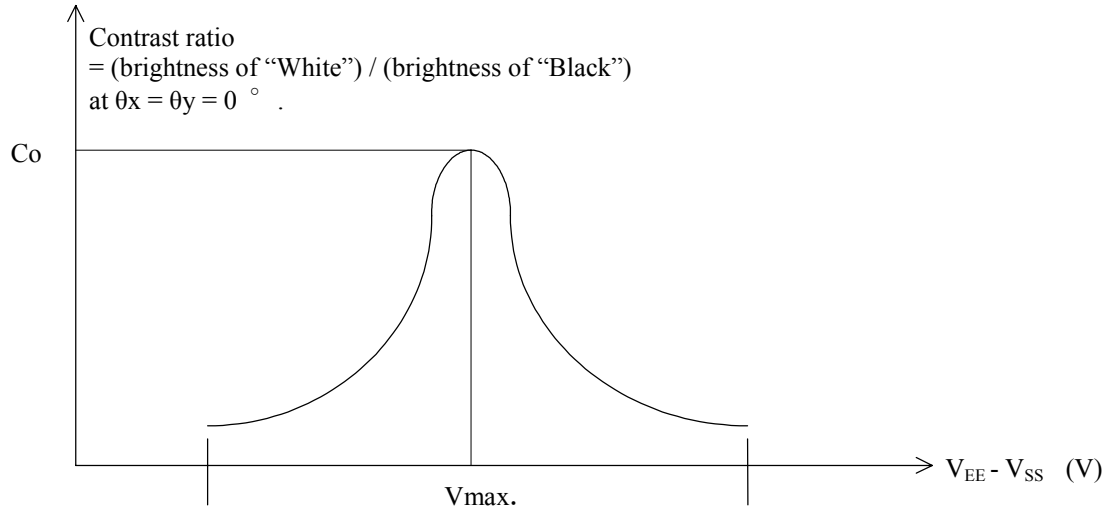



Fig.10 Definition of Vmax

Optical characteristics are measured by the method in Fig.11 and under the following conditions.

Conditions: In dark room. Ta = 25 °C.

Photo-detector: BM7 manufactured by TOPCON and quartz fiber.

Measuring spot size: φ10 mm. Measuring Field: 2 °.

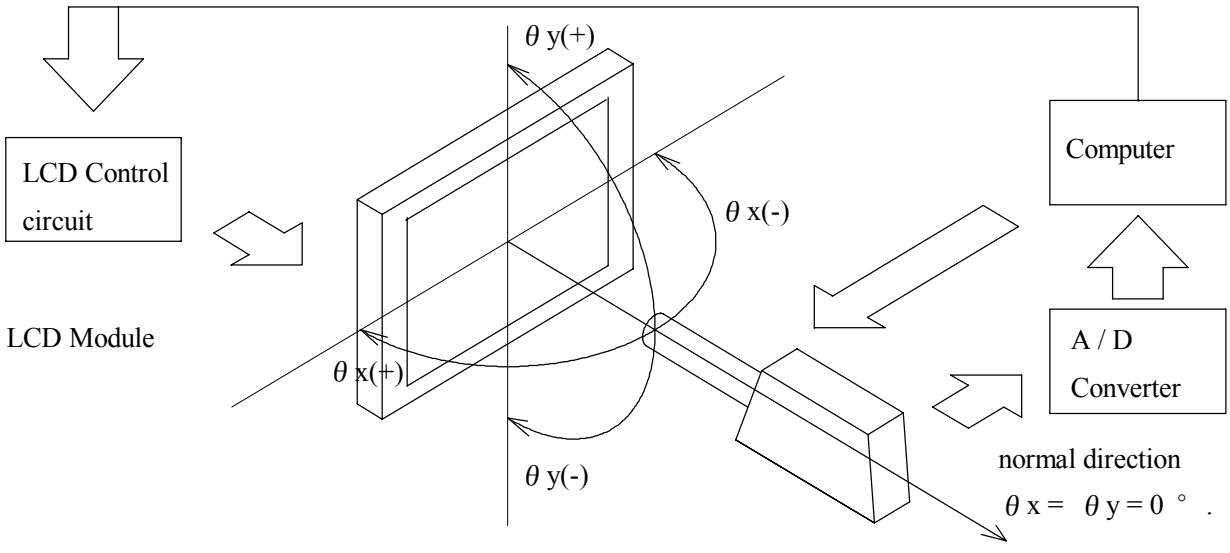
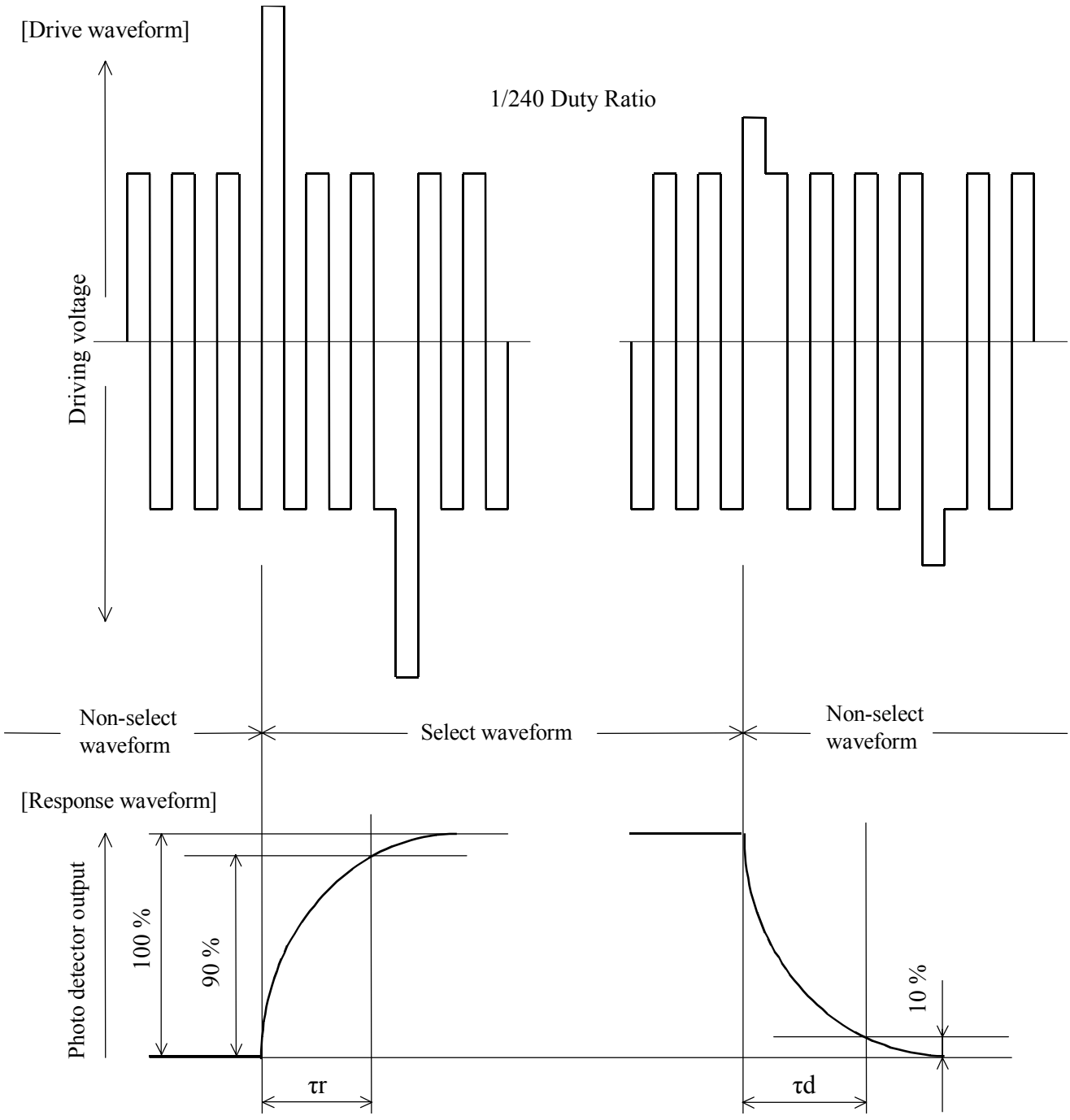



Fig.11 Optical characteristics measuring method




τr: Rise time

τd: Decay time

Fig.12 Definition of response time (1)

8. Characteristics of Backlight

The ratings are given on condition that the following conditions are satisfied.

8-1. Module brightness rating

Table 10

| Parameter | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|
| Brightness | 70 | 100 | - | cd / m² |

8-2. Measurement circuit

CXA-L0612-VJL (TDK) at $I_L$ = 5 mArms.

8-3. Measurement equipment

BM-7 (TOPCON Corporation).

8-4. Measurement conditions

1) Measurement circuit voltage at primary side: DC 12.0 V.

2) LCD: All digits White, VDD = 3.3 V, VEE - VSS = Vmax, D0 to 7 = ”H” (White), and Frame cycle = 120 Hz.

3) Ambient temperature: 25 °C.

Measurement shall be executed 30 minutes after turning on.

8-5. Lamp ratings

Table 11

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit | Remark |
|---|---|---|---|---|---|---|
| Lamp voltage | $V_L$ | 275 | 305 | 335 | Vrms | *1 |
| Lamp current | $I_L$ | - | 5.0 | 5.5 | mArms | - |
| Lamp power consumption | $P_L$ | - | 1.53 | - | W | *2 |
| Lamp frequency | $F_L$ | 30 | - | 100 | kHz | - |
| Kick-off voltage *3 | $V_S$ | 520 | - | 1500 | Vrms | Ta = 25 ℃ |
| | | 780 | - | 1500 | Vrms | Ta = 0 ℃ |
| Lamp life time *4 | $L_L$ | 25 000 | - | - | hours | Ta = 25 ℃ |

*1 It is recommended that IL be not more than 5.0 mArms so that heat radiation of CCFT backlight may affect the display quality.

*2 Power consumption excluded inverter loss.

*3 The circuit voltage of the inverter should be designed to have some margin, because kick-off voltage ($V_S$) may be increased due to the leak current in case of the LCD module.

*4 Life time of CCFT will be decreased when LCD is operating at lower temperature.

8-6. Operating life

The operating life time is defined as having ended when any of the following conditions occur;

-When the illuminence quantity of light has decreased to 50 % of the initial value.

-When the kick-off voltage has reached the maximum value in Table 11.

The operating life time is 25,000 hours or more at 5.0 mArms MAX. and at 25 ± 1 ℃. The inverter should be equivalent to CXA-L0612-VJL and meet the following conditions to keep the specified life time of used lamp;

-symmetric waveform in positive and negative without spike, and

-output frequency range: 30 kHz to 80 kHz.

Make sure the operating conditions by executing the burn-in enough time.

(NOTE) Module brightness ratings are defined as the average brightness inside the viewing area specified in Fig.13.

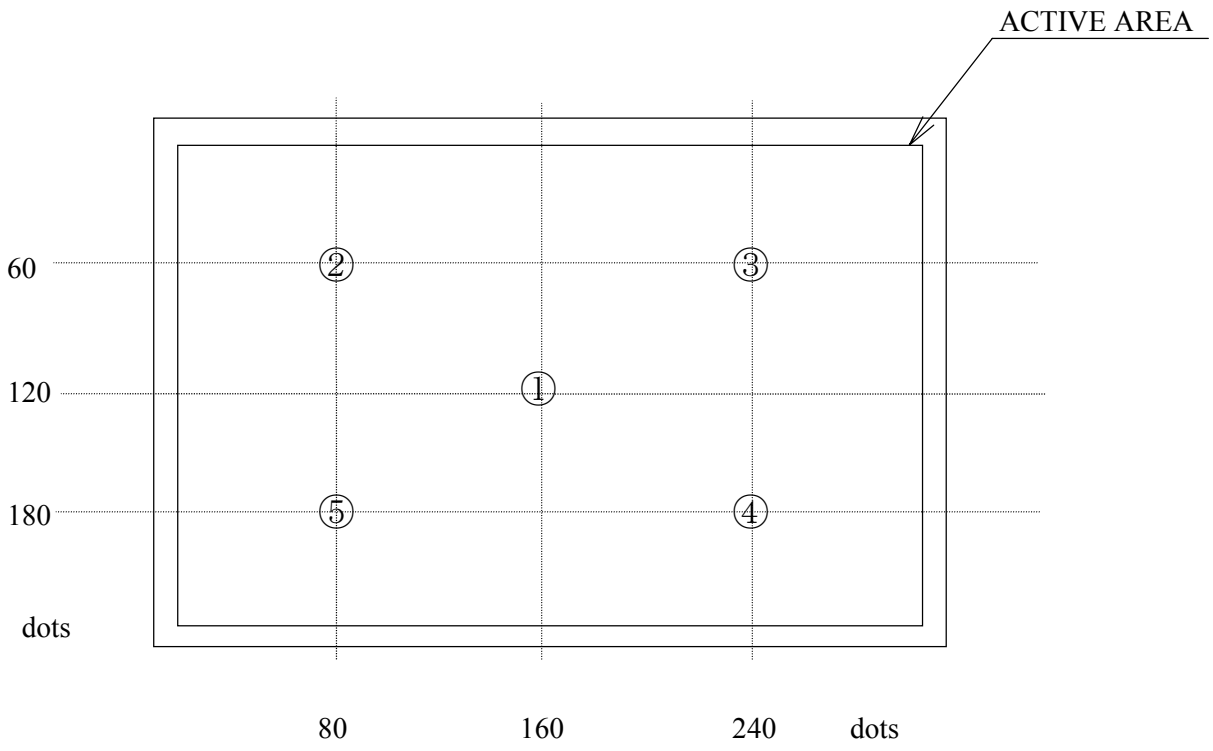



Fig.13 Measuring points (1 to 5)

9. Supply Voltage Sequence Condition

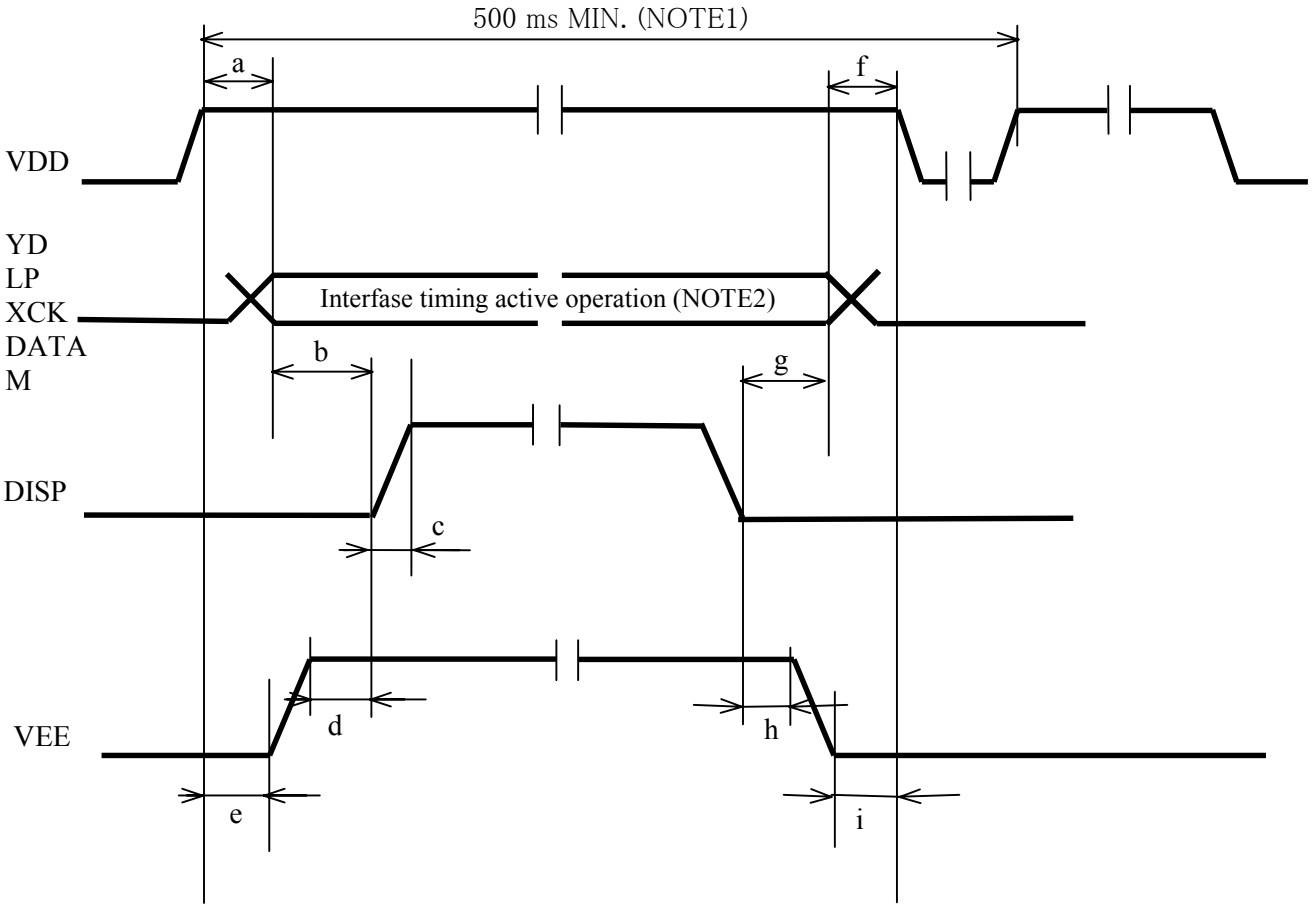



Fig.14 Supply voltage sequence condition △1

Table 12 △1

| | POWER ON | |
|---|---|---|
| Symbol | Allowable value | |
| a | 0 ms MIN. | 1 s MAX. |
| b | 20 ms MIN. | - |
| c | - | 50 ns MAX. |
| d | 0 ms MIN. | - |
| e | 0 ms MIN. | - |

| | POWER OFF | |
|---|---|---|
| Symbol | Allowable value | |
| f | 0 ms MIN. | 1 s MAX. |
| g | 0 ms MIN. | - |
| h | 0 ms MIN. | - |
| i | 0 ms MIN. | - |

(NOTE 1) Power ON / OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON / OFF.

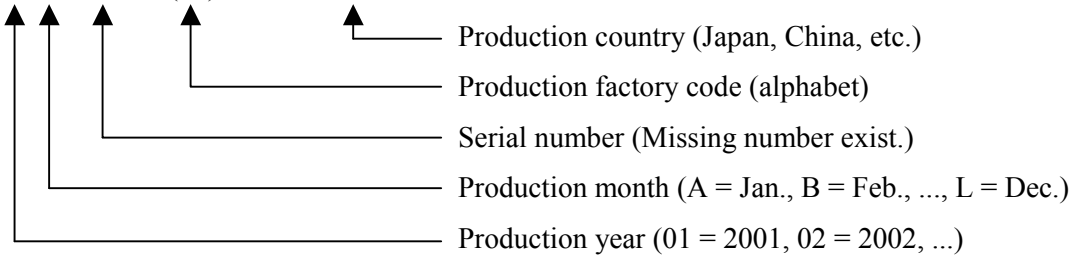
(NOTE 2) The signals which comply with the interface timing in Fig.6, 7, and Table 8, must be input.

(NOTE 3) The power supply voltages which comply with the electrical characteristics in Table 5 must be input.

10. Lot Number

Lot number is shown at the position mentioned in Fig.15 in accordance with the following numbering rule.

(Example) 02 E 00001 ( ) MADE IN JAPAN



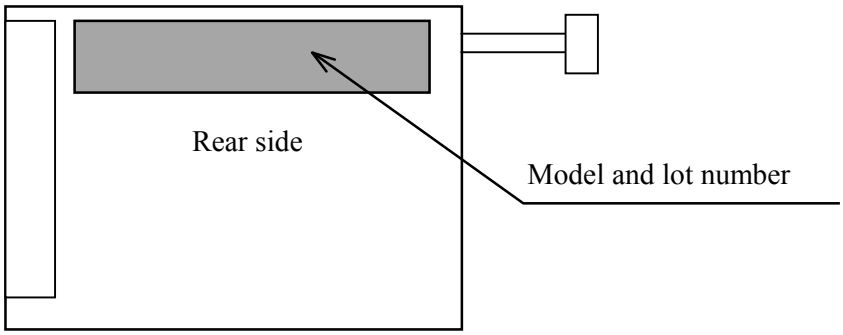
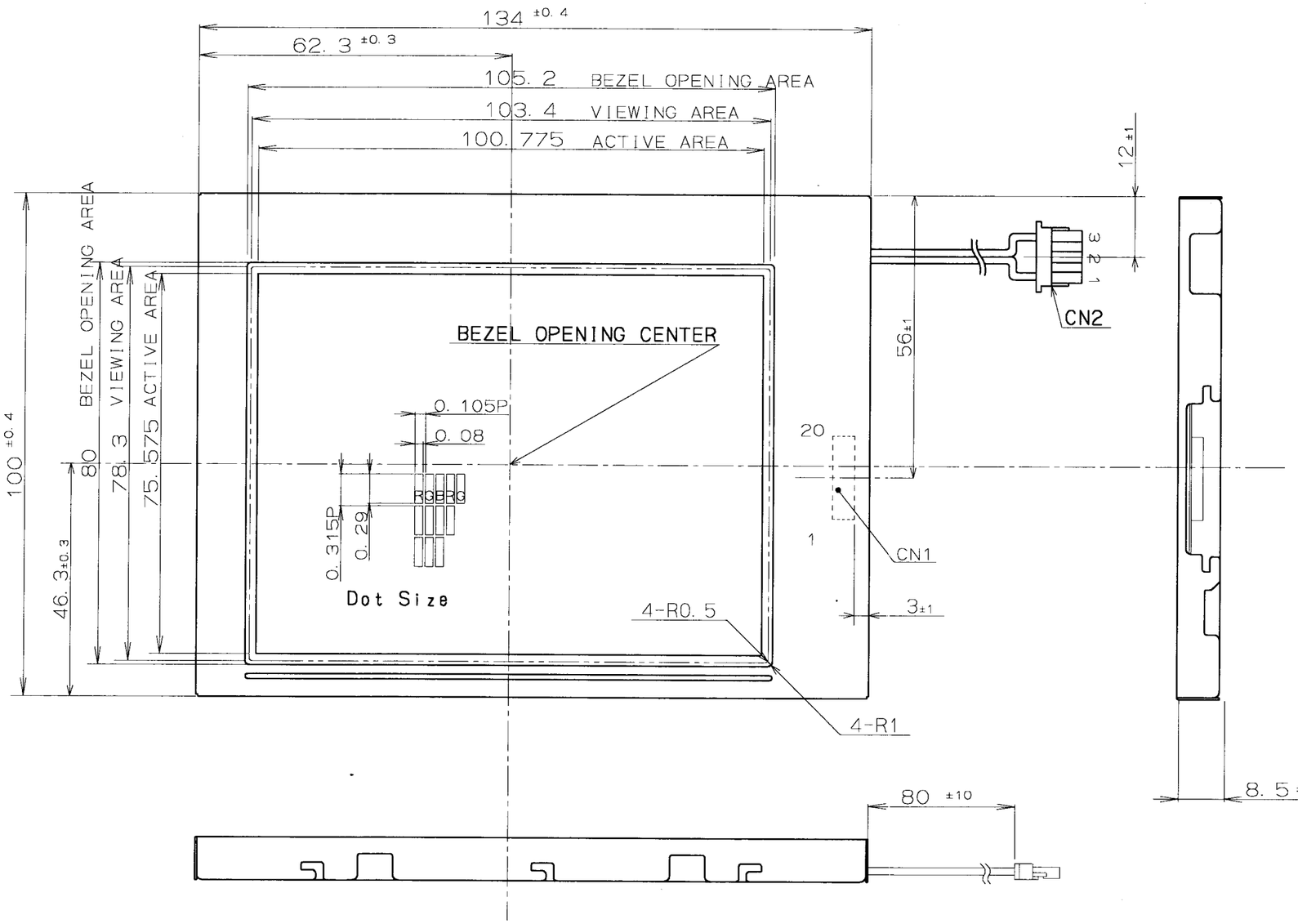




Fig.15



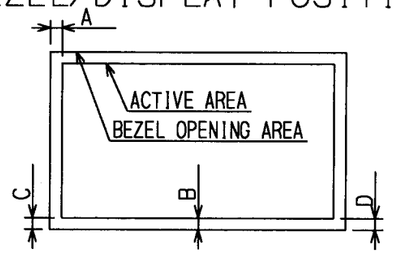

①INTERFACE CONNECTOR
9632S-20A-T
(IRISO Electronics)

| CN1 | | | |
|---|---|---|---|
| Pin No | | Pin No | |
| 1 | YD | 11 | D0 |
| 2 | LP | 12 | D1 |
| 3 | VSS | 13 | D2 |
| 4 | XCK | 14 | D3 |
| 5 | VSS | 15 | D4 |
| 6 | M | 16 | D5 |
| 7 | DISP | 17 | D6 |
| 8 | VDD | 18 | D7 |
| 9 | VEE | 19 | VSS |
| 10 | VSS | 20 | VSS |

②CCFT CONNECTOR
BHR-03VS-1(JST)

| CN2 | |
|---|---|
| Pin No | |
| 1 | HV |
| 2 | NC |
| 3 | GND |

## BEZEL/DISPLAY POSITION




1) TOLERANCE X-DIRECTION A:2.2±0.8
2) TOLERANCE Y-DIRECTION B:2.2±0.8
3) OBLIQUITY OF DISPLAY AREA |C-D|<0.8

UNSPECIFIED TOL TO BE ±0.3 mm

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 3 | | | | | | 名称 NAME | LCD Module Outline Dimensions |
| 2 | | | | | | アッセン ASSEMBLY | Duty Color 5.0型 320×3×240 Dots |
| 1 | 年月日 DATE | 訂正記事 REVISE | 設通No. | 担当 PREPA | LM050QC1T01 適用機種 MODEL | 部品コード PARTS CODE | |
| 材質 MATERIAL | | 板厚 THICK | 仕上 FINISH | | 尺度 SCALE 1/1 | 作成日付 DATE | 2002. 3. 19 |
| 設計 DESIGN | 写図 TRACE | 校図 CHECK | 検図 CHECK | 承認 APPROVE | SHARP CORPORATION | 図番 DRAWING No. | Fig. 16 |
| Y. Takao | | | | | MOBILE LIQUID CRYSTAL DISPLAY GROUP<br>MOBILE LCD DESIGN CENTER<br>ENGINEERING DEPARTMENT 1 | | |