PREPARED BY:	DATE
In Kobayashi	June . 5. 200
APPROVED BY:	DATE
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APPLICABLE GROUP

LIQUID CRYSTAL DISPLAY

**GROUP** 

LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION SPECIFICATION

DEVICE SPECIFICATION FOR

TFT-LCD module

MODEL No. LQ070Y5DG02

COSTOMER'S APPROVAL	
DATE	
	PRESENTED
BY	BY H. Yakushyam
	H.YAKUSIGAWA 🥖
	Department General manager
	Engineering Department.2
	Mobile LCD Design Center
	Mobile Liquid Crystal Display Group
	SHARP CORPORATION

# RECORDS OF REVISION

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#### 1. Application

The SHARP Color TFT-LCD module is an active matrix LCD (Liquid Crystal Display) produced by making the most of Sharp's expertise in liquid-crystal and semiconductor technologies.

The active device is amorphous silicon TFT (Thin Film Transistor).

Module geometry(Mechanical specification): Table 4-1

# 2. Summary and Features

- •Utilizes a panel with a 16:9 aspect ratio, which makes the module suitable for use in wide-screen systems.
- •The 7.0 screen produces a high resolution image that is composed of 384,000 pixels elements in a stripe arrangement.
- •Graphics and texts can be displayed on a 480×3×240 dots panel with 262,144 colors by supplying 18 bit data signals (6 bit/color).
- •Wide viewing field angle technology is employed. (The most suitable viewing angle is in the 6 o'clock direction.)
- •By adopting an active matrix drive, a picture with high contrast is realized.
- •Reduced reflection as a result of low reflection black matrix and an antiglare (AG) polarizer being adopted.
- •By COG method, realized a slim, lightweight, and compact module.
- •Through the use of TN-normally white mode, an image with highly natural color reproduction is realized
- •An inverted video display in the vertical and horizontal directions is possible.

#### 3. Construction and Outline

- The construction form figure : See Fig.1
- The module consists of a TFT-LCD panel, drivers, FPC, backlight, frame, front shielding cases.

#### 4. Mechanical specifications

Table 4-1

Parameter	Specifications	Units	Remarks
Screen size (Diagonal)	17.7[7.0"]	cm	
Active area	156.00 (W) ×83.28(H)	m m	
Display format	384,000	pixels	
	800×RGB×240	dots	
Dot pitch	0.065 (W) ×0.1735 (H)	mm	
Pixel configuration	R,G,B Stripe configuration		
Outline dimension	168.0(W)×94.0 (H)×8.75 (D)	mm	[Note4-1]
Mass	185 (MAX)	g	

### [Note 4-1]

Excluding protrusions. Typical values are given.

For detailed measurements and tolerances, please refer to Fig. 1.

5. Input terminal
5-1)TFT-LCD panel driving part

Table 5-1

Pin No.	Symbol	Description	Remarks
1	V10	The Power supply for gray image	Kemarks
2	V9	The Power supply for gray image	
3	V7	The Power supply for gray image	
4	V5	The Power supply for gray image	
5	V3	The Power supply for gray image	
6	V0	The Power supply for gray image	
7	VSHA	Power supply for source driver (Analog).	
8	SPR	Start signal for source driver.	[Note5-1]
9	LBR	Selection for horizontal scanning direction	[Note5-1]
10	GND	Ground	[Note3-1]
11	CK	Clock signal for source driver.	
12	GND	Ground	
13	GND	Ground	
14	LS	Data transfer signal in source driver.	
15	VSHD		
	В5	Power supply for source driver (Digital).	
16 17	B4	BLUE data signal(MSB) BLUE data signal	
18	В3		
19	B2	BLUE data signal BLUE data signal	
20	B1	C	
	B0	BLUE data signal BLUE data signal(LSB)	
21 22	GND	Ground	<u> </u>
	GND G5		<u> </u>
23	G3 G4	GREEN data signal(MSB)	<u> </u>
24	G3	GREEN data signal	<u> </u>
25	G2	GREEN data signal	<u> </u>
26	G2 G1	GREEN data signal	<u> </u>
27	G0	GREEN data signal	<u> </u>
28	GND	GREEN data signal(LSB)	<u> </u>
29 30	R5	Ground	<u> </u>
	R4	RED data signal(MSB)	
31	R3	RED data signal	
32	R2	RED data signal	
33		RED data signal	
34	R1	RED data signal	<u> </u>
35	R0 SPL	RED data signal(LSB)	[Notes 1]
36	CS	Start signal for source driver.	[Note5-1]
37	VCOM	CS electrode driving signal	
	VCOM	Common electrode driving signal	
39	VDD	Common electrode driving signal	
40	SPS	Power supply for gate driver (High level).	
41	CLS	Start signal for gate driver.  Clock signal for gate driver.	
42	U/L	Č Č	[Notes 1]
43	MODE1	Selection for vertical scanning direction	(Note5-1)
	MODE1	Control signal for gate driver.	
45	VCC	Control signal for gate driver.	[Note5-2]
46	OPEN	Power supply for logic circuit in gate driver(High level).	
47	VEE	This is open terminal	
48		Power supply for LCD's OFF voltage	
49	OPEN		
50	VSS	Power supply for logic circuit in gate driver(Low level).	

# (Note 5-1)

The control of scanning direction

Table 5-2

Mode	U/L	LBR	SPL	SPR
Normal mode	Lo	Hi	Input	Output
Right/Left reverse mode	Lo	Lo	Output	Input
Up/Down reverse mode	Hi	Hi	Input	Output
Right/Left & Up/Down reverse mode	Hi	Lo	Output	Input

[caution] Lo=GND , Hi=VSHD

# [Note 5-2]

Refer to "Notes at the time of a power supply turning on" in clause 7-1 for the start-up and the standing lowering of the power supply.

The gate driver is selected to output by setting mode 1 and mode 2..

Table 5-3

MODE1	MODE2	
Hi	Hi	Normal mode
Lo	Hi	Don't use this mode.
Hi	Lo	Skip 2 pulse mode (See Fig.5-1)
Lo	Lo	The mode which fixes all the output on the VEE level

[caution] Lo=GND , Hi=VSHD

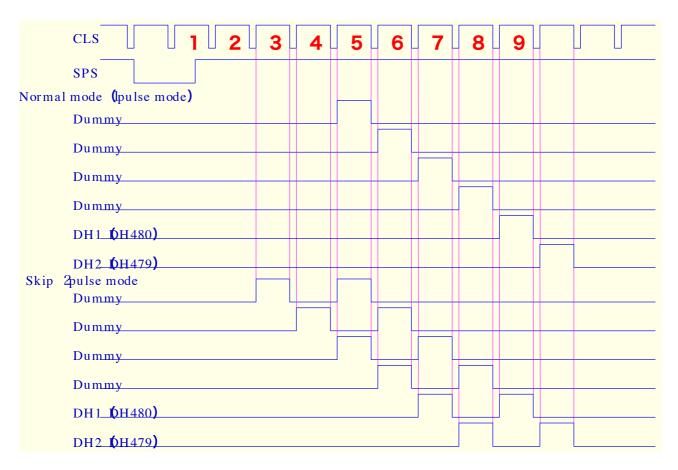


Fig5-1. Gate output timing

# 5-2)Backlight fluorescent tube driving part

Table 5-4

No.	Symbol	function	Remarks
1	VL1	input terminal (Low voltage side)	
2	VL2	input terminal (Hi voltage side)	

# 6. Absolute maximum ratings

Table 6-1 G N D = 0 V

Para	ameter	Symbol	MIN	MAX	Unit	Note
Power supply	Analog voltage	VSHA	-0.3	+6.0	V	$T a = 2.5 ^{\circ}C$
(source driver)	Digital voltage	VSHD	-0.3	+6.0	V	"
Power supply (gate	driver)	VDD	-0.3	+35.0	V	"
		VCC-VSS	-0.3	+6.0	V	"
		VEE-VSS	-0.3	+35.0	V	"
		VDD-VEE(VSS)	-0.3	+35.0	V	"
Input signal voltage	Digital input signal	VID	-0.3	VSHD+0.3	V	" [Note 6-1]
(source driver)	Analog input signal	VIA	-0.3	VSHA+0.3	V	" [Note 6-2]
Common electrode dr	iving signal	COM	-4	+6	V	"
Storage temperature		Tstg	-40	+85	°C	[Note 6-3,4]
Operating temperatu	re (panel surface)	Topr1	-30	+85	$^{\circ}\mathrm{C}$	[Note 6-5,6]
Operating temperature	(Ambient temperature)	Topr2	-30	+65	$^{\circ}\mathrm{C}$	[Note 6-6]

- [Note 6-1] SPL , SPR , R0~R5 , G0~G5 , B0~B5 , LS , CK , LBR , MODE1 , MODE2 , R/L , SPS , CLS
- [Note 6-2] V0, V3, V5, V7, V9, V10
- [Note 6-3] This rating applies to all parts of the module and should not be exceeded.
- [Note 6-4] Maximum wet-bulb temperature is 57°C. Condensation of dew must be avoided as electrical current leaks will occur, causing a degradation of performance specifications.
- [Note 6-5] The operating temperature only guarantees operation of the circuit.

  For contrast, speed response, and other factors related to display quality, determine operating temperature using the formula Ta=+25°C
- [Note 6-6] Ambient temperature when the backlight is lit (reference value).

#### 7. Electrical characteristics

7-1)TFT-LCD panel driving section

Table 7-1

GND = 0V, Ta = 25°C

Par	amete	r			Symbol	MIN	TYP	MAX	Unit	Remarks
Power supply	Analo	g vo	ltage		VSHA	+5.0	+5.3	+5.6	V	
(source driver)	Digita	l vo	ltage		VSHD	+2.5	+2.7	+3.6	V	
Power supply	TFT	Н	igh lev	/el	VDD	+14.8	+15.0	+15.2	V	
(gate driver)	drivin	_	ow	AC	VEE AC	_	COM AC	_	Vp-p	[Note7-1]
	circui	le le	vel	DC	VEE DC	-11.8	-12.0	-12.2	V	
	Logic	н	igh lev	<i>i</i> e1	VCC	VSS+VSHD	VSS+	VSS+VSHD	V	[Note7-2]
	circui		ign ic	7 ( 1	VCC	-0.1	VSHD	+0.1		
	CII Cu I	Lo	ow lev	el	VSS	-17.0	-17.4	-17.8	V	
Power supply (gr	ay ima	ige)			V0~V10	0		VSHA	V	[Note7-3]
Input signal volt	age H	Iigh	level		VIHS	$0.8 \times VSHD$	1	VSHD	V	[Note7-4]
for source driver	I	ow	level		VILS	GND		$0.2 \times VSHD$	V	
Input signal curr	ent H	High level		IIHS1		1	10	$\mu$ A	[Note7-4]	
for source driver					IIHS2			400	$\mu$ A	[Note7-5]
	I	ow	level		IILS	_		10	$\mu$ A	[Note7-6]
Input signal volt	age H	Iigh	level		VIHG	$0.8 \times VSHD$	1	VSHD	V	[Note7-7]
for gate driver	I	ow	level		VILG	GND	l	$0.2 \times VSHD$	V	
Input signal curr	ent I	Iigh	level		IIHG			1.0	$\mu$ A	
for gate driver	I	ow	level		IILG			1.0	$\mu$ A	
Common electroc	ie A	AC c	om pon	ent	COMAC	_	±3.4	±4.0	Vp-p	[Note7-8]
driving signal	I	OC c	ompor	ent	COMDC1	+0.5		+2.5	V	
Cs electrode	A	AC c	om pon	ent	COMAC		±3.4	±4.0	Vp-p	[Note7-1]
driving signal	Ι	OC c	ompor	ent	COMDC2	-5.3	-5.8	-6.3	V	

· Notes at the time of a power supply turning on

Please turn on and turn off power supply in simultaneous or the following order.

<Turn on> VSHD, VSHA, VSS, VCC → Logic signal, VEE → VDD → MODE1, MODE2 <Turn off> VDD → VEE, Logic signal, MODE1, MODE2 → VSS, VCC, VSHA, VSHD

\*Condition: VSS < VCC

At the MODE1 and MODE2 signals, please hold Low voltage for more than 2 vertical synchronous term after Low voltage is input at the time of a power supply turning on and VDD rises completely. Then, please hold High voltage until the power supply is turned off.

- [Note 7-1] Please carry out polar reversal in the same amplitude and the same phase as VCOM.
- [Note 7-2] Condition:  $2.5V \le VCC-VSS \le 3.6V$

[Note 7-3] It is a standard power supply for gray scale. Whenever the polarity of common electrode drive signal (VCOM) is changed, please also change this standard voltage. V0 (black) power supply becomes the reverse characteristic of VCOM, and V10 (white) becomes the same polarity as VCOM.

Please shift the center value of each power supply amplitude to the plus(+) direction according to the characteristic of liquid crystal as it will go to white side like V3, V5, V7, V9, V10, if the center value of each power supply amplitude is based on the center value of V0 (black).

After DC adjustment of VCOM signal is adjusted in case of the V0 gray scale display, please adjust this amount of shifts so that a flicker does not occur in the power supply display of each gray scale.

- [Note 7-4] Apply to the terminal R0-R5, G0-G5, B0-B5, SPR, SPL, CK, LS, and LBR
- [Note 7-5] Apply to the terminal PS
- [Note 7-6] Apply to the terminal R0-R5, G0-G5, B0-B5, SPR, SPL, CK, LS, LBR, and PS
- [Note 7-7] Apply to the terminal CLS, SPS, MODE1, MODE2, and R/L

[Note 7-8] Please switch polarity of amplitude COMAC by center value of amplitude that is COMDC for every one level scan and every one vertical scan. Moreover, please adjust COMDC so that contrast becomes the maximum and a flicker becomes the minimum for every module.

#### 7-2)Backlight driving section

Table 7-2

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
lamp voltage	VL7	640	720	800	Vrms	I L = 6 m Arm s
lamp current	IL	5.5	6.0	6.5	mArms	Ordinary state
	ILB	-	_	9.0	mArms	At the boost [Note 7-9]
lamp frequency	WL	_	4.32	_	W	When lighting up in the
						standard
Discharge pipe	fL	30	_	100	kHz	
electric power						
kick-off voltage	VS		_	2100	Vrms	Ta=+25°C
		_	_	2200	Vrms	$Ta = -30^{\circ}C$

Inverter: HIU - 288 [HARISON TOSHIBA LIGHTING co., ltd]

(Output capasitor: 22pF, frequency: 49kHz)

# [Caution]

Please use the inverter which has the one of the sine wave. With regards to the inverter, it should be negative/positive wave symmetry and the spike wave should not be occurred.

[Note 7-9] Within 5 minutes. The temperature is less than  $0^{\circ}$ C.

Table 7-3 VSHA = +5.3V, VSHD = 2.7V, GND = 0V, Ta = 25°C

	Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
	Operating Clock frequency	fck	_	33.2	34.6	MHz	DCLK
S	High level clock width	Tcwh	12	_	_	ns	
0	Low level clock width	Tcwl	13	_	_	ns	
U	Clock rise time	Tcr	_	_	4	ns	
R	Clock fall time	Tcf	_	_	4	ns	
C	Start pulse frequency	fsp	_	31.5	31.8	kHz	SPR
Е	Start pulse set up time	Tsusp	4	_	_	ns	SPL
	Start pulse hold time	Thsp	0	_	_	ns	[Note7-10]
	Stapt pulse width	Twsp	1/fck	1/fck	1.5/fck	ns	
	LS pulse frequency	flp	_	fsp	_	kHz	LS
	LS pulse set up time (CLS)	Tsulp	5.0	_	_	$\mu$ s	
	LS pulse set up time (SPOI,SPIO)	Tsulpsp	1/fck	_	_	ns	
	LS pulse hold time (DCLK)	Thlpck	20	_	_	ns	
	High level LS pulse wide	Twlp	1/fck	_	_	ns	
	Data set up time	Tsud	15	_	_	ns	R0∼R5,G0∼
	Data hold time	Thd	10	_	_	ns	G5 , B0∼B5
	On anotin a Clask fraguency	fcls	_	fsp	_	kHz	CLS
	Operating Clock frequency	1018		rsp		KIIZ	CLS
	Clock pulse with	Twl	5.5	— —	(1/fcls)-53	$\mu$ s	CLS
G		+		-			CLS
A	Clock pulse with	Twl	5.5	_	(1/fcls)-53	μs	CLS
A T	Clock pulse with Clock rise time	Twl Trcl	5.5	_	(1/fcls)-53 1/fck	μs ns	SPS
A	Clock pulse with Clock rise time Clock fall time	Twl Trel Tfel	5.5	_ _ _	(1/fcls)-53 1/fck 1/fck	μs ns ns	
A T	Clock pulse with Clock rise time Clock fall time Start pulse frequency	Twl Trcl Tfcl fsps	5.5 - -	_ _ _ _ _ 60	(1/fcls)-53 1/fck 1/fck 65	μs ns ns Hz	
A T	Clock pulse with Clock rise time Clock fall time Start pulse frequency Start pulse set up time	Twl Trcl Tfcl fsps Tsusps	5.5 - - - 100	- - - 60 -	(1/fcls)-53 1/fck 1/fck 65	μs ns ns Hz ns	
A T	Clock pulse with Clock rise time Clock fall time Start pulse frequency Start pulse set up time Start pulse hold time	Twl Trel Tfel fsps Tsusps Thsps	5.5 - - 100 300	- - - 60 - -	(1/fcls)-53 1/fck 1/fck 65 —	μs ns ns Hz ns	
A T E	Clock pulse with Clock rise time Clock fall time Start pulse frequency Start pulse set up time Start pulse hold time Start pulse rise time	Twl Trcl Tfcl fsps Tsusps Thsps Trsps	5.5 - - 100 300 -	- - - 60 - -	(1/fcls)-53 1/fck 1/fck 65 - 100	μs ns ns Hz ns ns	SPS
A T E	Clock pulse with Clock rise time Clock fall time Start pulse frequency Start pulse set up time Start pulse hold time Start pulse rise time Start pulse fall time	Twl Trcl Tfcl fsps Tsusps Thsps Trsps Tfsps	5.5 - - 100 300 - -	- - - 60 - -	(1/fcls)-53 1/fck 1/fck 65 - 100 100	μs ns ns Hz ns ns ns	SPS
A T E	Clock pulse with Clock rise time Clock fall time Start pulse frequency Start pulse set up time Start pulse hold time Start pulse rise time Start pulse fall time OM signal set up time	Twl Trcl Tfcl fsps Tsusps Thsps Trsps Tfsps Tfsps Tsucom	5.5 - - 100 300 - - 3	- - - 60 - - - -	(1/fcls)-53 1/fck 1/fck 65 - 100 100	μs ns ns Hz ns ns ns μs μs	SPS
A T E	Clock pulse with Clock rise time Clock fall time Start pulse frequency Start pulse set up time Start pulse hold time Start pulse rise time Start pulse fall time OM signal set up time	Twl Trcl Tfcl fsps Tsusps Thsps Trsps Tfsps Tsucom Thcom	5.5 - - 100 300 - - 3	- - - 60 - - - -	(1/fcls)-53 1/fck 1/fck 65 100 100	μs ns ns Hz ns ns ns ns μs μs	SPS
A T E	Clock pulse with Clock rise time Clock fall time Start pulse frequency Start pulse set up time Start pulse hold time Start pulse rise time Start pulse fall time OM signal set up time OM signal hold time OM signal rise time	Twl Trcl Tfcl fsps Tsusps Thsps Trsps Tfsps Tsucom Thcom Trcom	5.5 - - 100 300 - - 3 0	- - - 60 - - - - -	(1/fcls)-53 1/fck 1/fck 65 100 100 2	μs ns ns ns ns ns ns ns μs ns	VCOM CS V0,V3,V5
CC CC CC V0	Clock pulse with Clock rise time Clock fall time Start pulse frequency Start pulse set up time Start pulse hold time Start pulse rise time Start pulse fall time OM signal set up time OM signal rise time OM signal rise time OM signal fall time OM signal fall time OM signal fall time OV 10 signal set up time	Twl Trcl Tfcl fsps Tsusps Thsps Trsps Tfsps Tsucom Thcom Trcom Tfcom	5.5 - 100 300 - - 3 0 -	- - - 60 - - - - - -	(1/fcls)-53 1/fck 1/fck 65 100 100 2 2	μs ns μs μs μs	SPS  VCOM  CS
CCC CCC CCC V00 V00	Clock pulse with Clock rise time Clock fall time Start pulse frequency Start pulse set up time Start pulse hold time Start pulse rise time Start pulse fall time OM signal set up time OM signal rise time OM signal rise time OM signal fall time OM signal fall time OM signal set up time	Twl Trel Tfel fsps Tsusps Thsps Trsps Tfsps Tsucom Thcom Trcom Tfcom Tsuv0	5.5 - - 100 300 - - 3 0 - - 3	- - - 60 - - - - - - -	(1/fcls)-53 1/fck 1/fck 65 100 100 2 2	μs ns ns ns ns ns ns ns us μs μs μs μs μs	VCOM CS V0,V3,V5

# [Note7-10]

The rising pulse in DCLK is existed only 1 time during Hi period (Twsp) on start pulse.

Table 7-4  $T = 2.5 \,^{\circ}C$ 

Parameter		Symbol	Conditions	MIN	ΤΥΡ	MAX	Unit
Current for	Analog	ISHA	VSHA=+5.3V		40	95	m A
source driver	Digital	ISHD	VSHD = +2.7V		8.0	19	m A
Current for	Hi	IDD	VDD = +15.0V		0.20	0.35	m A
gate driver	Lo	IEE	$VEE = -12.0 \pm 3.4V$		-0.20	-0.35	m A
	Logic Hi	ICC	VCC = -14.7V		0.05	0.10	m A
	Logic Lo	ISS	VSS = -17.4V	_	-0.10	-0.20	m A

# \*Max current situation:

Vertical stripe pattern alternating 21 gray scale (GS21) with 42 gray scale (GS42) every 1 dot. Timing: fck=33.2MHz, fsp=30.3kHz, fsps=60Hz

In case of using exclusive control-IC (LZ9JG17).

# 7-5) Input Data Signals and Display Position on the screen



D1,DH1	D2,DH1	D3,DH1		D800,DH1
D1,DH2	D2,DH2			
D1,DH3				
	1	R	G B	
D1,DH480				D800,DH480

Display position of input data (H,V)

Table8-1

ſ	Table8-									0.1										
	Colors &										_									
	Gray scale	Gray Scale	R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	В3	B4	B5
	Black	_	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	_	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Ва	Green	_	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
sic	Cyan	_	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Basic color	Red	_	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
or	Magenta	_	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	_	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	_	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gra	仓	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Sca	仓	$\downarrow$			1						\	V						<b>L</b>		
	Û	$\downarrow$			\	ν <u> </u>					\	ν <u> </u>					\	ν <u> </u>		
of red	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
ed	Û	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
G	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of green	仓	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
y S	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
cal	仓	$\downarrow$				V			₩					$\downarrow$						
e 01	Û	$\downarrow$			\	<b>ν</b>			<b>↓</b>				<b>↓</b>							
J.B.	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
eer	Û	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Эrа	仓	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
y S	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Gray Scale	仓	$\downarrow$		<b>V</b>					<b>↓</b>						<b>V</b>					
le o	Û	$\rightarrow$		$\downarrow$				↓						₩						
of blue	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
lue	Û	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Bleu	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

0: Low level voltage 1: High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals. According to the combination of total 18 bit data signals, the 262,144-color display can be achieved on the screen.

Table 9-1  $Ta=25^{\circ}C$ 

Parameter	Parameter Symbol		Condition	Min	Тур	Max	Unit	Remarks
Viewing ang	le	$\theta$ 21, $\theta$ 22	CR≧5	60	65	_	° (degree)	Note 9-
range		θ 11		60	65	_	° (degree)	1,2]
		θ 12		55	60	_	° (degree)	
Contrast rat	io	CRmax	Optimal	100	_	_		[Note 9-2]
			viewing angle					
Response	Rise	τr	$ heta=0^{\circ}$	_	30	60	ms	[Note 9-3]
time	Fall	τd		_	50	100	ms	
Luminance		Y	IL=6.0mArms	285	380	_	cd/m <sup>2</sup>	[Note 9-4]
White		X	IL=6.0mArms	0.263	0.313	0.363		[Note 9-4]
chromaticity		у	IL=0.0mArms	0.279	0.329	0.379		
Lamp life	+25°C	_	continuation	10,000		_	hour	[Note 9-5]
time	−30°C	_	intermission	2,000	_	_	time	[Note 9-6]

<sup>\*</sup>Measuring after 30minutes operation. The measurement of the optical character is measured by using the method of fig.9-1 and fig.9-2 under the condition which is equal to the darkroom or the darkroom.

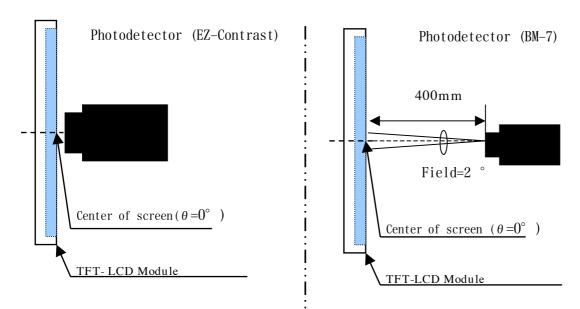
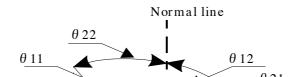


Fig9-1 Viewing angle / Range / Contrast / Response time measurement method

Fig9-2 Luminance / Chromaticity measurement method

[Note 9-1] Viewing angle range is defined as follows.

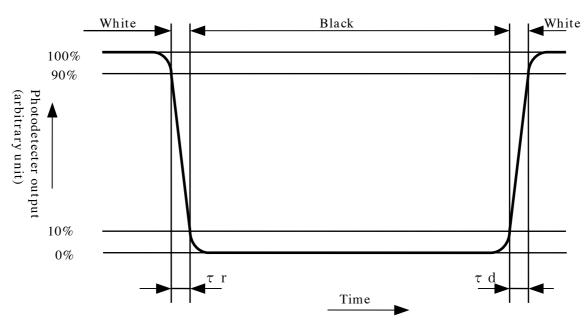


# definition for viewing angle

[Note 9-2] Contrast ratio of transmission is defined as follows:

Contrast ratio(CR) =  $\frac{\text{Photo detector output with LCD being "white"}(GS63)}{\text{Photo detector output with LCD being "black"}(GS0)}$ 

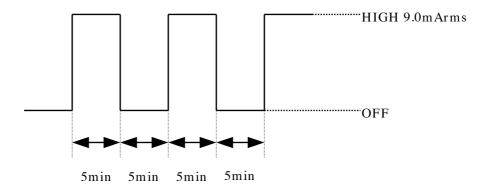
[Note 9-3] Response time is obtained by measuring the transition time of photo detector output, when input signals are applied so as to make the area "black" to and from "white".



- [Note 9-4] Measured on the center area of the panel at a viewing cone 1° by TOPCON luminance meter BM-7.(After 30 minutes operation)DC/AC inverter driving frequency: 49kHz
- [Note 9-5] Lamp life time is defined as the time when the brightness of the panel not to become less than 50% of the original value in the continuous operation under the condition of lamp current IL=6.0mArms and PWM dimming  $100\%\sim5\%$ .
- [Note 9-6] The intermittent cycles is defined as a time when brightness not to become under 50% of the original value under the condition of following cycle.

(Lighting condition)

Ambient temperature: -30°C



# 10. Display quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standard.

#### 11. Mechanical characteristics

11-1) External appearance

Do not exist extreme defects. (See Fig.1)

# 11-2) Panel toughness

The panel shall not be broken ,when 19N is pressed on the center of the panel by a smooth sphere having 15 mm diameter.

[Caution] In spite of very soft toughness, if, in the long-term, add pressure on the active area, it is possible to occur the functional damage.

# 11-3) I/O connector performance

A)Input/output connectors for the operation of LCD module

1)Applicable FPC : FH12-50S-0.5SH(HRS)

2)FPC flexibility : I. Slit on the film cover lay (Fig.1 ①)

If it had been tested bending under radius 0.6 mmR and bending angle 90 degrees condition, the FPC should not be cut at 30 times in or less.

II. Slit on the film cover lay coat part of one side printing (Fig.1 ②)

If it had been tested bending under radius nothingness and bending angle 180degrees, the FPC should not be cut.

(It should be bend by hand and only at once).

### B)I/O connector of backlight driving circuit (JST)

1			,
	Symbol	Used Connector	Corresponding connector
	CN1	BHSR-02VS-1	SM02B-BHSS-1-TB
			(assembled on PWB)

#### 12. Handling instructions

- 12-1) Handling of FPC
  - ① Please bend FPC only at a film cover lay slit part (Fig.1 A)

② Please do not hang a LCD module or do not apply excessive power for FPC.

#### 12-2) Mounting of module

① The TFT-LCD module is be sure to fix the module on the same plane, taking care not to wrap or twist the module.

Don't reach the pressure of touch-switches of the set side to a module directly, because images may be disturbed

- 2 Please power off the module when you connect the input/output connector.
- 3 Please connect the metallic shielding cases of the module and the ground pattern of the inverter circuit surely. If that connection is not perfect, there may be a possibility that the following problems happen.
  - a) The noise from the backlight unit will increase.
  - b) The output from inverter circuit will be unstable. Then, there may be a possibility that some problems happen.
  - c) In some cases, a part of module will heat.

# 12-3) Precautions in mounting

Polarizer which is made of soft material and susceptible to flaw must be handled carefully. Protective film (Laminator) is applied on the surface to protect it against scratches and dirties. It is recommended to peel off the laminator immediately before the use, taking care of static electricity.

Precautions in peeling off the laminator.

#### A) Working environment

When the laminator is peeled off, static electricity may cause dust to stick to the polarizer surface.

To avoid this, the following working environment is desirable.

a) Floor: Conductive treatment of  $1M\Omega$  or more on the tile.

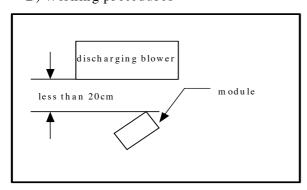
(conductive mat or conductive paint on the tile)

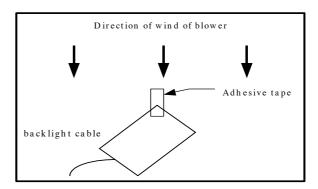
- b) Clean room free form dust and with an adhesive mat on the doorway.
- c) Advisable humidity:50%~70%

Advisable temperature:15°C~27°C

d) Workers shall wear conductive shoes, conductive work clothes, conductive gloves and an earth band.

### B) Working procedures





a) Direct the wind of discharging blower somewhat downward to ensure that module is blown sufficiently.

Keep the distance between module and discharging blower within 20 cm.

- b) Attach adhesive tape to the laminator part near discharging blower so as to protect polarizer against flaw.
- c) Peel off laminator, pulling adhesive tape slowly to your side taking 5 or more second.
- d) On peeling off the laminator, pass the module to the next work process to prevent the module to get dust.

- e) Method of removing dust from polarizer
  - Blow off dust with N2 blower for which static electricity preventive measure has been taken.
  - Since polarizer is vulnerable, wiping should be avoided.

    But when the panel has stain or grease, we recommend to use adhesive tape to softly remove them from the panel.

When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth. For stubborn dirties, wipe the part, breathing on it.

Wipe off water drop or finger grease immediately. Long contact with water may cause discoloration or spots.

TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Handle with care. Since CMOS LSI is used in this module, take care of static electricity and earth your body when handling.

# 12-4) Caution of product design

Please following items strictly when the product is designed by using this module.

- The LCD module shall be protected against water salt-water by the waterproof cover.
- Please take measures to interferential radiation from module, to do not interfere surrounding appliances.

#### 12-5) Others

- ① Do not expose the module to direct sunlight or intensive ultraviolet rays for several hours; liquid crystal is deteriorated by ultraviolet rays.
- ② Store the module at a temperature near the room temperature. At lower than the rated storage temperature, liquid crystal solidifies, causing the panel to be damaged. At higher than the rated storage temperature, liquid crystal turns into isotropic liquid and may not recover.
- 3 he voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
- 4 If LCD panel breaks, there may be a possibility that the liquid crystal escapes from the panel. Since the liquid crystal is injurious, do not put it into the eyes or mouth. When liquid crystal sticks to hands, feet or clothes, wash it out immediately with soap.
- ⑤ Please adjust the Common electrode drive signal DC bias(COM DC) in the final state of the product. Causes the display fineness decrease when not adjusting COM DC.
- 6 Observe all other precautionary requirements in handling general electronic components.

#### 13. Packing form

13-2)

a)Piling number of cartons : MAX 12

b)Conditions for storage

Environment

①Temperature: 0~40°C

②Humidity : 60%RH or less (at 40°C)

No dew condensation at low temperature and high humidity.

- 3Atmosphere: Harmful gas, such as acid or alkali which bites electronic components and/or wires, must not be detected.
- 4 Period : about 3 months
- ⑤ Opening of the package: In order to prevent the LCD module from breakdown by

electrostatic charges, please control the room humidity over 50%RH and open the package taking sufficient countermeasures against electrostatic charges, such as

earth, etc.

#### 14. Others

14-1)Indication of lot number

①Attached location of the label : See Fig.1 (Outline Dimensions).

②Indicated contents of the label

LQ070Y5DG02

model No. lot No.

contents of lot No. the 1st figure · · production year (ex. 2003: 3)

the 2nd figure · · production month 1,2,3,· · · · · · ,9,X,Y,Z

the 3rd $\sim$ 8th figure ··· serial No. 000001 $\sim$  the 9th figure ··· revision marks A,B,C ···

# 15. Reliability Test Conditions for TFT-LCD Module

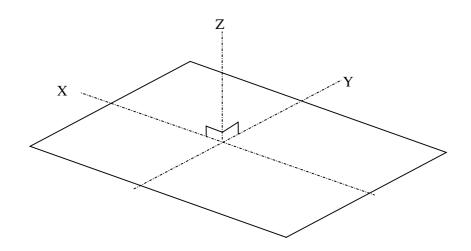
Remark) Temperature condition is based on operating temperature conditions on 6.-Table 6-1.

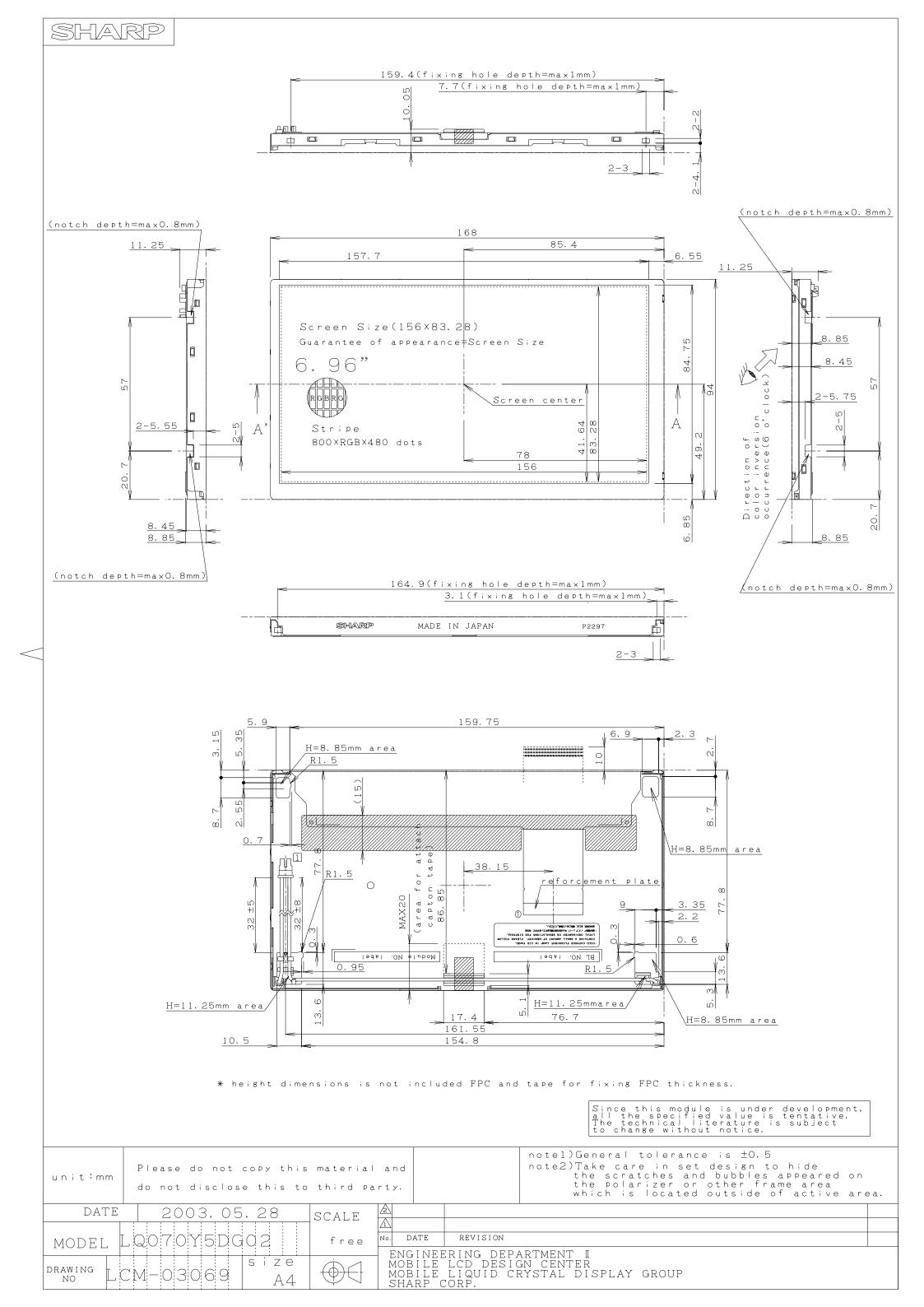
No.	Test items	Test conditions
1	High temperature storage test	$Ta = +85^{\circ}C$ 240h
2	Low temperature storage test	$Ta = -40^{\circ}C \qquad 240h$
3	High temperature and high humidity operating test	Tp=+60°C 90 %RH 240h
4	High temperature operating test	$Tp = +85^{\circ}C \qquad 240h$
5	Low temperature operating test	$Ta = -30^{\circ}C $ 240h
6	Electro static discharge test	$\pm 200 \mathrm{V} \cdot 200 \mathrm{pF}(0 \Omega)$ 1 time for each terminals
7	Shock test	980m/s <sup>2</sup> · 6ms, ±X; ±Y; ±Z 3 times for each direction (JIS C0041, A-7 Condition C)
8	Vibration test	Frequency range: 8~33.3Hz, Stroke: 1.3mm Frequency range: 33.3Hz~400Hz, Acceleration: 29.4m/s² Sweep cycle: 15 minutes X,Z 2 hours for each directions, 4 hours for Y direction [caution] (total 8 hours) (JIS D1601)
9	Heat shock test	$Ta = -30^{\circ}C \sim +85^{\circ}C / 200 \text{ cycles}$ (0.5h) (0.5h)

[Note] Ta= Ambient temperature, Tp= Panel temperature

[Check items] In the standard condition, there shall be no practical problems that may affect the display function.

[caution] X,Y,Z directions are shown as follows:





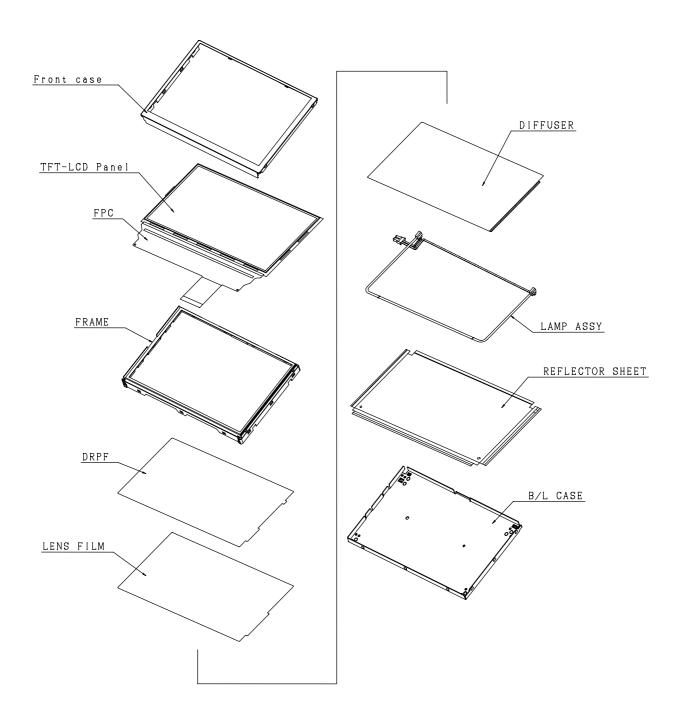


Fig.2 STRUCTURE OF THE MODULE

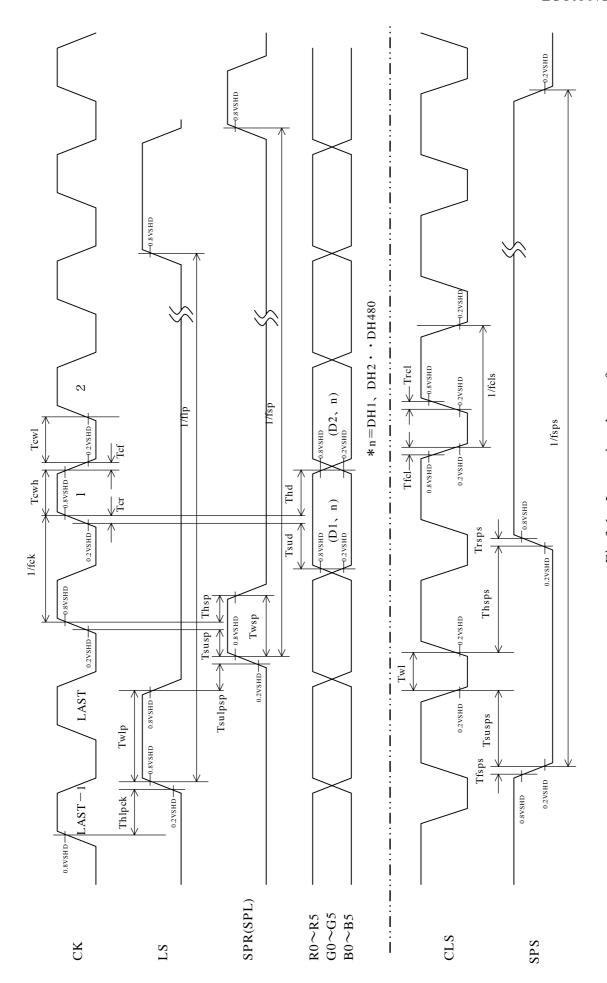


Fig.3-1 Input signal waveform

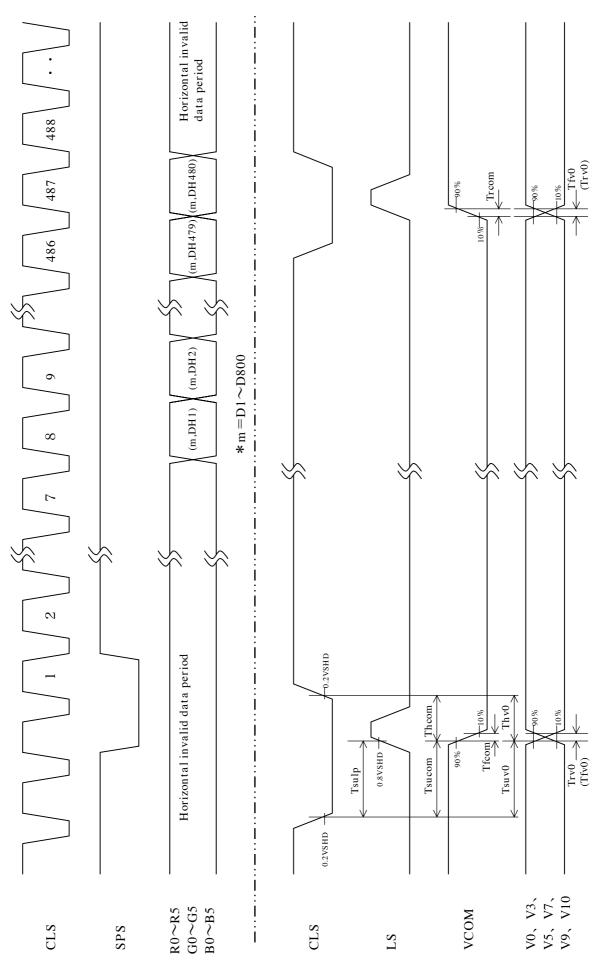


Fig.3-2 Input signal waveform

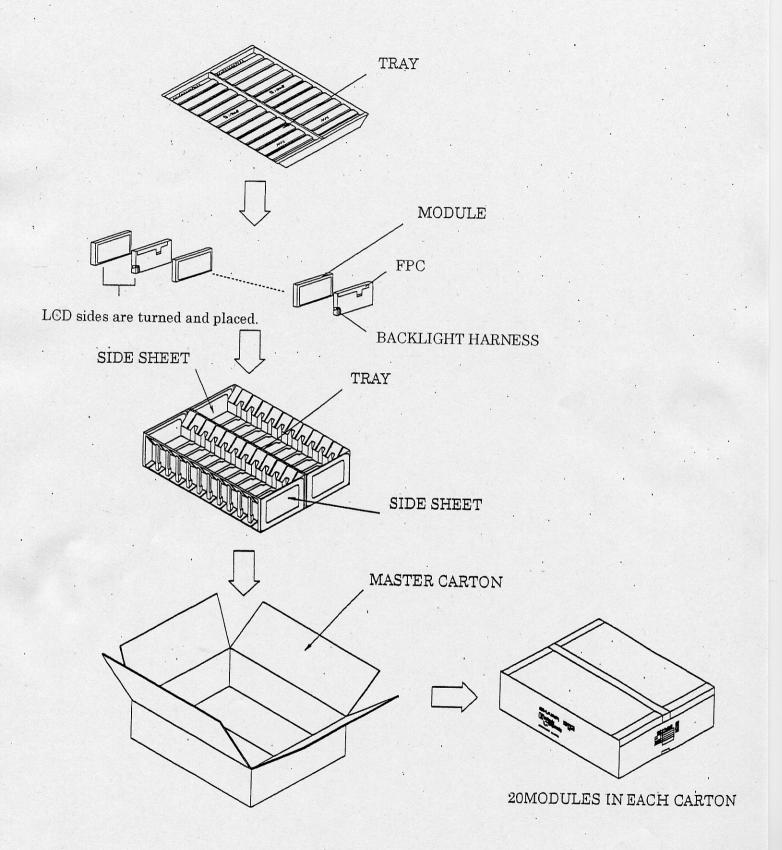


Fig. 4 Packing Form

# (Appendix)

# Adjusting method of optimum common electrode DC bias voltage

To obtain optimum DC bias voltage of common electrode driving signal (VCDC), photoelectric devices are very effective, and the accuracy is with 0.1V. (In visual examination method, the accuracy is about 0.5V because of the difference among individuals.)

To gain optimum common electrode DC bias, there is the method that uses photoelectric devices.

#### Measurement of flicker

DC bias voltage is adjusted so as to minimize VSY flicker.

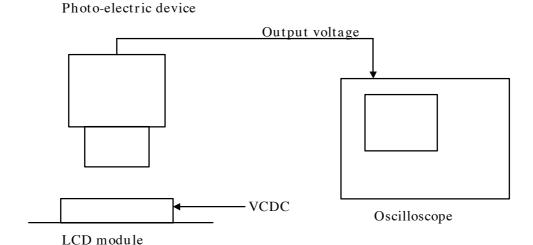


Fig. A Measurement system

#### 《Measurement of flicker》

Photoelectric output voltage is measured by an oscilloscope at a system show in Fig. A. DC bias voltage must be adjusted so as to minimize the VSY flicker with DC bias voltage changing slowly. (Fig.B)

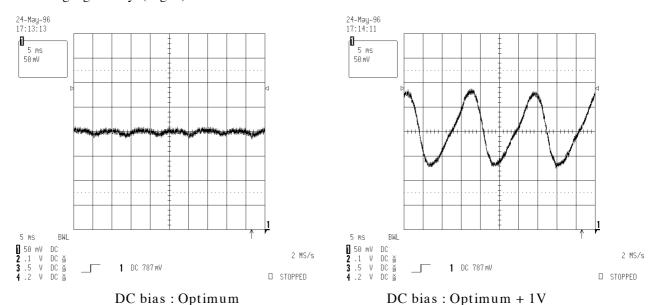


Fig. B Waveforms of flicker