SHARP

No.	LD -23751A
DATE	Jul. 25. 2011

TECHNICAL LITERATURE

FOR

TFT - LCD OPEN-CELL

These parts have corresponded with the RoHS directive.

MODEL No. LQ235D1xxxx

The technical literature is subject to change without notice. So, please contact SHARP or its representative before designing your product based on this literature.

DEVELOPMENT DEPARTMENT I
LIQUID CRYSTAL DISPLY DIVISION Ⅱ
DISPLAY DEVICE BUSINESS GROUP
SHARP CORPORATION

RECORDS OF REVISION

LQ235D1xxxx

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-23751A	Jul.25.2011	-	-	-	1st Issue

1. Application

This technical literature applies to the color 23.5” TFT-LCD Open Cell LQ235D1xxxx.

* In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

* Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

* SHARP assumes no responsibility for any damage resulting from the use of the device which does not comply with the instructions and the precautions specified in this technical literature.

* Contact and consult with a SHARP sales representative for any questions about this device.

2. Overview

This Open Cell is a color active matrix LCD panel incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, a front polarizer, a back polarizer, driver ICs and Source PWB. Graphics and texts can be displayed on a 1920×RGB×1080 dots panel with about 16,777,216 colors by using 8bit + mini-LVDS(Low Voltage Differential Signaling) to interface, driving signal and driving voltages.

The following contents can be achieved in using (LR388H5) Timing control IC that sharp specifies.

And in order to improve the response time of LCD, This Open Cell applies the Over Shoot driving (O/S driving) technology for the Timing control IC. In the O/S driving technology, signals are being applied to the Liquid Crystal according to a pre-fixed process as an image signal of the present frame when a difference is found between image signal of the previous frame and that of the current frame after comparing them.

With combination of these technologies, motion blur can be reduced and clearer display performance can be realized.

This open cell can display 120Hz image in 2D mode and 240Hz image in 3D mode by using (LR388H5) Timing control IC that sharp specifies.

3. Mechanical Specifications

Parameter	Specifications	Unit
Display size	59.809（Diagonal）	cm
	23.547 （Diagonal）	inch
Active area	521.28(H) x 293.22 (V)	mm
Pixel Format	1920(H) x 1080 (V)	pixel
	（1pixel = R + G + B dot）	
Pixel pitch	0.0905(H) x 0.2715 (V)	mm
Pixel configuration	R,G,B vertical stripe	
Display mode	Normally Black	
Open Cell Outline Dimensions *1	539.165(H) x 348.250(V) x 3.500(D)(*1)	mm
Mass	661 （TYP）	g
Surface treatment	Anti Glair Hard Coat 3H Haze 2.0%	

(*1)Outline dimensions are shown in Fig.1

4. Open Cell driving specifications

4-1. Driving interface of Source-PWB

CN11, CN12: Input signal from Timing control IC that SHARP specifies.

Using connector: CN11, CN12 (502790-8091(MOLEX))or equivalent connector

4-1-2. CN11, CN12

CN	CN11			CN12		
No	Signal	Note	I/O	Signal	Note	
1	SPI_WP	For future use (SPI I/F)	I	NC		
2	SPI_CK	For future use (SPI I/F)	I	NC		
3	SPI_DOUT	For future use (SPI I/F)	O	NC		
4	SPI_DIN	For future use (SPI I/F)	I	NC		
5	SPI_CS	For future use (SPI I/F)	I	NC		
6	VL_A	Gamma standard voltage	I	VL_A	Gamma standard voltage	I
7	VL_B	Gamma standard voltage	I	VL_B	Gamma standard voltage	I
8	VL_C	Gamma standard voltage	I	VL_C	Gamma standard voltage	I
9	VL0	Gamma standard voltage	I	VL0	Gamma standard voltage	I
10	GND	GND		GND	GND	
11	S8_LVCLKN	mini-LVDS(SOF8)	I	S4_LVCLKN	mini-LVDS(SOF4)	I
12	S8_LVCLKP	mini-LVDS(SOF8)	I	S4_LVCLKP	mini-LVDS(SOF4)	I
13	GND	GND		GND	GND	
14	S8_LV2N	mini-LVDS(SOF8)	I	S4_LV2N	mini-LVDS(SOF4)	I
15	S8_LV2P	mini-LVDS(SOF8)	I	S4_LV2P	mini-LVDS(SOF4)	I
16	S8_LV1N	mini-LVDS(SOF8)	I	S4_LV1N	mini-LVDS(SOF4)	I
17	S8_LV1P	mini-LVDS(SOF8)	I	S4_LV1P	mini-LVDS(SOF4)	I
18	S8_LV0N	mini-LVDS(SOF8)	I	S4_LV0N	mini-LVDS(SOF4)	I
19	S8_LV0P	mini-LVDS(SOF8)	I	S4_LV0P	mini-LVDS(SOF4)	I
20	GND	GND		GND	GND	
21	S7_LVCLKN	mini-LVDS(SOF7)	I	S3_LVCLKN	mini-LVDS(SOF3)	I
22	S7_LVCLKP	mini-LVDS(SOF7)	I	S3_LVCLKP	mini-LVDS(SOF3)	I
23	GND	GND		GND	GND	
24	S7_LV2N	mini-LVDS(SOF7)	I	S3_LV2N	mini-LVDS(SOF3)	I
25	S7_LV2P	mini-LVDS(SOF7)	I	S3_LV2P	mini-LVDS(SOF3)	I
26	S7_LV1N	mini-LVDS(SOF7)	I	S3_LV1N	mini-LVDS(SOF3)	I
27	S7_LV1P	mini-LVDS(SOF7)	I	S3_LV1P	mini-LVDS(SOF3)	I
28	S7_LV0N	mini-LVDS(SOF7)	I	S3_LV0N	mini-LVDS(SOF3)	I
29	S7_LV0P	mini-LVDS(SOF7)	I	S3_LV0P	mini-LVDS(SOF3)	I
30	GND	GND		GND	GND	
31	S6_LVCLKN	mini-LVDS(SOF6)	I	S2_LVCLKN	mini-LVDS(SOF2)	I
32	S6_LVCLKP	mini-LVDS(SOF6)	I	S2_LVCLKP	mini-LVDS(SOF2)	I
33	GND	GND		GND	GND	
34	S6_LV2N	mini-LVDS(SOF6)	I	S2_LV2N	mini-LVDS(SOF2)	I
35	S6_LV2P	mini-LVDS(SOF6)	I	S2_LV2P	mini-LVDS(SOF2)	I
36	S6_LV1N	mini-LVDS(SOF6)	I	S2_LV1N	mini-LVDS(SOF2)	I
37	S6_LV1P	mini-LVDS(SOF6)	I	S2_LV1P	mini-LVDS(SOF2)	I
38	S6_LV0N	mini-LVDS(SOF6)	I	S2_LV0N	mini-LVDS(SOF2)	I
39	S6_LV0P	mini-LVDS(SOF6)	I	S2_LV0P	mini-LVDS(SOF2)	I
40	GND	GND		GND	GND	
41	S5_LVCLKN	mini-LVDS(SOF5)	I	S1_LVCLKN	mini-LVDS(SOF1)	I
42	S5_LVCLKP	mini-LVDS(SOF5)	I	S1_LVCLKP	mini-LVDS(SOF1)	I
43	GND	GND		GND	GND	
44	S5_LV2N	mini-LVDS(SOF5)	I	S1_LV2N	mini-LVDS(SOF1)	I

45	S5_LV2P	mini-LVDS(SOF5)	I	S1_LV2P	mini-LVDS(SOF1)	I
46	S5_LV1N	mini-LVDS(SOF5)	I	S1_LV1N	mini-LVDS(SOF1)	I
47	S5_LV1P	mini-LVDS(SOF5)	I	S1_LV1P	mini-LVDS(SOF1)	I
48	S5_LV0N	mini-LVDS(SOF5)	I	S1_LV0N	mini-LVDS(SOF1)	I
49	S5_LV0P	mini-LVDS(SOF5)	I	S1_LV0P	mini-LVDS(SOF1)	I
50	GND	GND		GND	GND	
51	VCC	Logic voltage	I	VCC	Logic voltage	I
52	LS_L	LCD Source Driver driving signal	I	LS_R	LCD Source Driver driving signal	I
53	REV_L	LCD Source Driver driving signal	I	REV_R	LCD Source Driver driving signal	I
54	GND	GND		GND	GND	
55	VH0	Gamma standard voltage	I	VH0	Gamma standard voltage	I
56	VH_C	Gamma standard voltage	I	VH_C	Gamma standard voltage	I
57	VH_B	Gamma standard voltage	I	VH_B	Gamma standard voltage	I
58	VH_A	Gamma standard voltage	I	VH_A	Gamma standard voltage	I
59	VH255	Gamma standard voltage	I	VH255	Gamma standard voltage	I
60	VLS	Analog voltage		VLS	Analog voltage	
61	VLS	Analog voltage	I	VLS	Analog voltage	I
62	HVDD	Half analog voltage	I	HVDD	Half analog voltage	I
63	VCOM	Common voltage	I	VCOM	Common voltage	I
64	CS	CS voltage	I	CS	CS voltage	I
65	CS	CS voltage	I	CS	CS voltage	I
66	CS	CS voltage	I	CS	CS voltage	I
67	CS	CS voltage	I	CS	CS voltage	I
68	CS	CS voltage	I	CS	CS voltage	I
69	CS	CS voltage	I	CS	CS voltage	I
70	CS	CS voltage	I	CS	CS voltage	I
71	CS	CS voltage	I	CS	CS voltage	I
72	CS	CS voltage	I	CS	CS voltage	I
73	CS	CS voltage	I	CS	CS voltage	I
74	CS	CS voltage	I	CS	CS voltage	I
75	CS	CS voltage	I	CS	CS voltage	I
76	GOE	LCD Gate Driver driving signal	I	NC		
77	GCK	LCD Gate Driver driving signal	I	NC		
78	GSP	LCD Gate Driver driving signal	I	NC		
79	VGH	Gate ON voltage	I	NC		
80	VGL	Gate OFF voltage	I	NC		

[Note]

Be sure to use FPC matched mini-LVDS line impedance for connection Main board to Source-PWB.

4-2. Interface block diagram

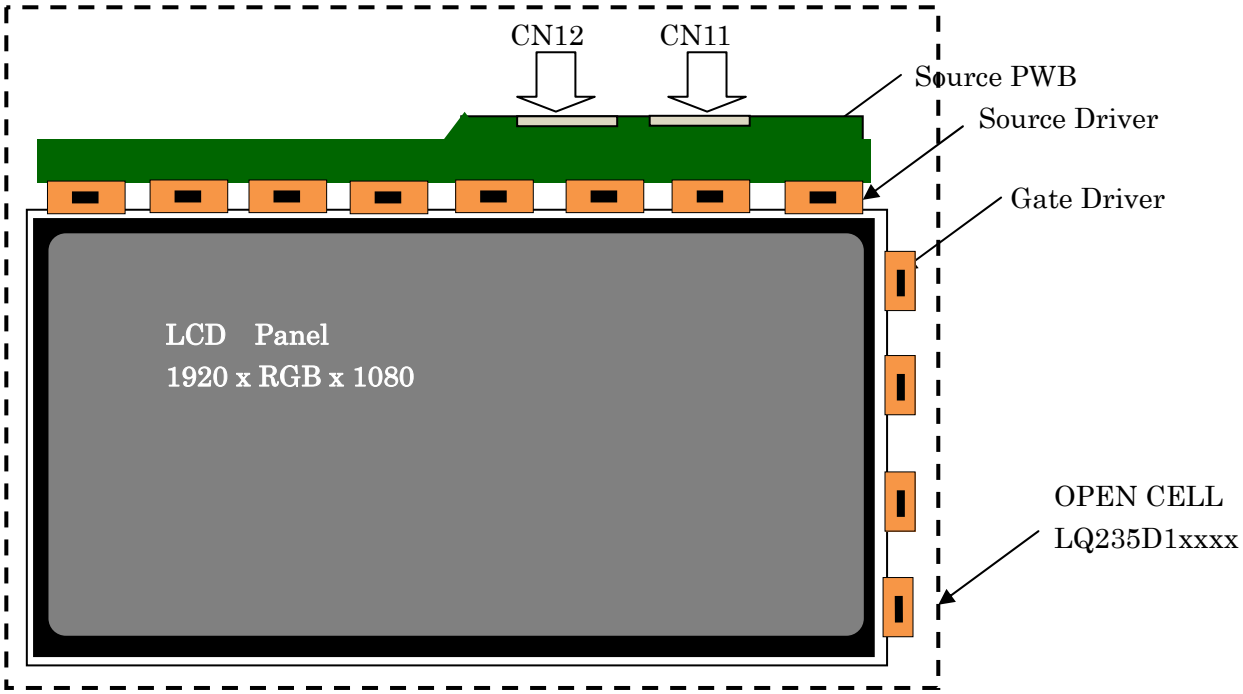


Fig.4-1 Interface block diagram

CN11	CN12
<u>INPUT SIGNAL</u>	<u>INPUT SIGNAL</u>
mini-LVDS DATA+ x16	mini-LVDS DATA+ x16
mini-LVDS DATA- x16	mini-LVDS DATA- x16
Source driving signal	Source driving signal
Gate driving signal	
（SPI signal）	<u>POWER SUPPLY</u>
	Power (Logic)
<u>POWER SUPPLY</u>	Power (Analog)
Power (Logic)	Power(Half analog)
Power (Analog)	GND
Power(Half analog)	COM
GND	Gamma standard voltage
COM	
Gamma standard voltage	
Gate Power HIGH	
Gate Power LOW	

5. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit	Remark
Digital Power Supply	VCC	Ta=25℃	-0.3～+4.0	V	
Analog Power Supply	VLS	Ta=25℃	-0.3～+18.0	V	【Note 1】
Half Analog Power Supply	HVDD	Ta=25℃	-0.3～+18.0	V	【Note 1】
Standard voltage terminal	VH0～VH255 VL0～VL255	Ta=25℃	-0.3～VLS+0.3	V	【Note 1】
Source incoming signal voltage	VIS	Ta=25℃	-0.3～VCC+0.3	V	
Gate High Power Supply	VGH	Ta=25℃	-0.3+48.0	V	【Note 2】
Gate Low Power Supply	VGL	Ta=25℃	-23.0～+0.3	V	【Note 2】
Gate Power voltage	VGH-VGL	Ta=25℃	-0.3～+48.0	V	【Note 2】
Gate incoming signal voltage	VIG	Ta=25℃	-0.3～VCC+0.3	V	
Operation temperature	Top	-	0～+50	℃	【Note 3,4】
Storage temperature	Tstg	-	-25～+60	℃	【Note 3,4】
Panel Surface Temperature	Tsf		≦60	℃	【Note 3,4】
Source Driver surface temperature	Tssf		≦100	℃	【Note 3,5】

【Note 1】Standard voltage terminal voltage should be kept in the following order.

VLS-0.2 ≧ VH255 > VH_A >…>VH_C > VH0 ≧ HVDD+0.2

HVDD-0.2 ≧ VL0 > VL_C>… > VL_A > GND

Please be careful, difference between VLS and VH0～VH255,

VL_A～VL255 and GND not to exceed 8.25V, when power on sequence.

【Note 2】Set the gate drive voltage, so that VGL≦VGH is maintained when switching the power source on and off, and during its operation.

【Note 3】Humidity 95%RH Max.(Ta≦40 ℃)

Maximum wet-bulb temperature at 39 degree or less. (Ta>40 ℃) No condensation.

【Note 4】Since it becomes as a cause of phenomena, such as contrast unevenness, please make the temperature distribution within a field of a panel uniform.

【Note 5】The measurement point of Source Driver surface temperature is drawn in Fig.1

A power supply sequence should be kept in the following order.

Source system : GND→VCC→VIS→VLS/VS/HVDD

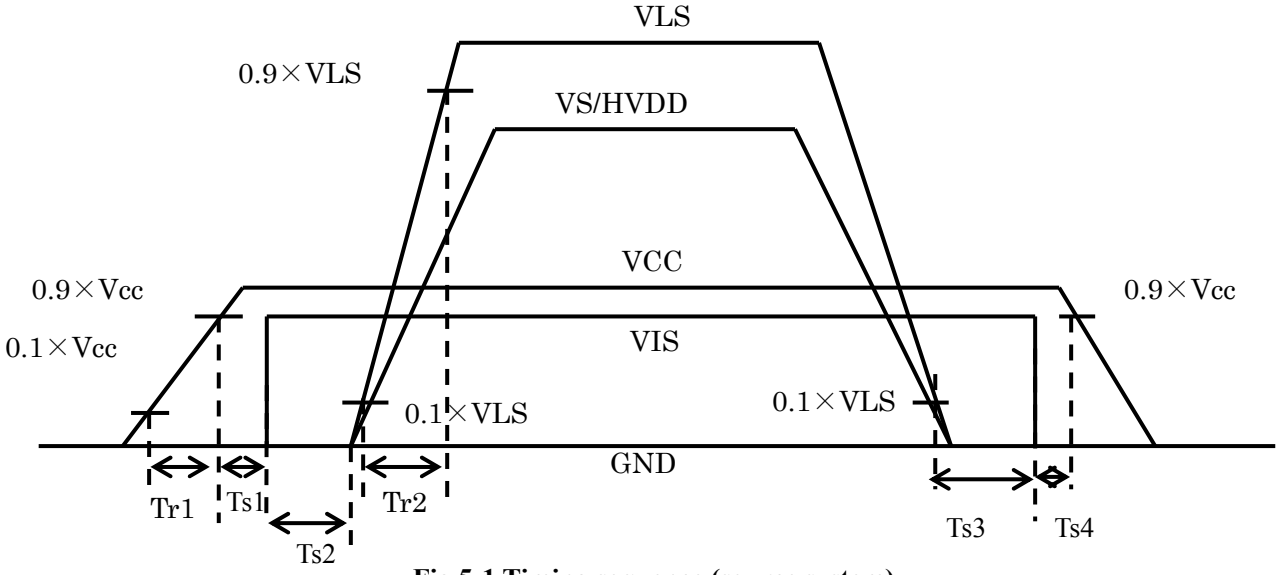


Fig.5-1 Timing sequence (source system)

0.5ms ≦ Tr1 ≦ 20ms, Tr2 ≦ 50ms, 0ms ≦ Ts1, 0ms ≦ Ts2, 0ms ≦ Ts3, 0ms ≦ Ts4

Gate system : GND→VCC→VIG→VGL→VGH

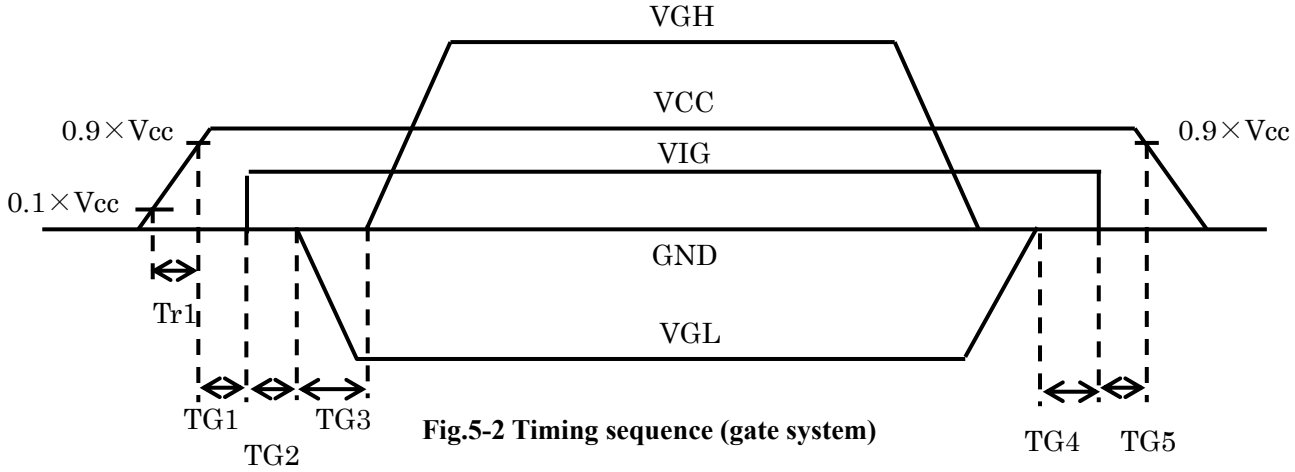


Fig.5-2 Timing sequence (gate system)

0ms ≦ TG1, 0ms ≦ TG2, 0ms ＜ TG3, 0ms ≦ TG4, 0ms ≦ TG5

Please impress VGL and VGH, especially after VCC reaches 90% or more of setting voltage.

Please give as the above being reverse at the time of interception.

6. Electrical Characteristics

6-1. Proper operating condition GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Digital Power Supply	VCC	3.0	3.3	3.6	V	
Analog Power Supply	VLS	14.0	15.6	16.5	V	
Half Analog Power Supply	HVDD	0.5VLS-1.0	0.5VLS	0.5VLS+1.0	V	
Standard voltage terminal	VS(VH0～VH255)	HVDD+0.2	-	VLS-0.2	V	【Note 1】
Standard voltage terminal	VS(VL_0～VL_A)	GND+0.2		HVDD-0.2	V	【Note 1】
Gate High Power Supply	VGH	15.0	35.0	36.0	V	
Gate Low Power Supply	VGL	-5.0	-6.0	-7.0	V	
Gate power supply voltage	VGH-VGL	20.0	41.0	43.0	V	
Source mini-LVDS Data Input Low voltage	VID	200		600	mV	VCM_{mlvd}=1.2±0.2 V 【Note 2】
Source mini-LVDS Data Input Standard Voltage Range	VCM_{mlvd}	1.0	1.2	1.4	V	VID≧0.2V VCC=3.0～3.6V
Source Input Low voltage	VILS	GND		0.3VCC	V	【Note 3】
Source Input High voltage	VIHS	0.7VCC	-	VCC	V	【Note 3】
Gate Input Low voltage	VILG	GND	-	0.3VCC	V	【Note 4】
Gate Input High voltage	VIHG	0.7VCC	-	VCC	V	【Note 4】
Common mode voltage	VCOM	GND		0.5VLS	V	【Note 5】
Auxiliary capacity common mode voltage	CS	-	VCOM	-	V	【Note 5】

【Note 1】 ∴ Gray scale standard voltage can be applied as to following 5 readings (9 points).

V0(Black),V_C,V_B ,V_A ,V255(White)

(VH0, VH_C, VH_B,VH_A, VH255
VL_A,VL_B, VL_C VL0)

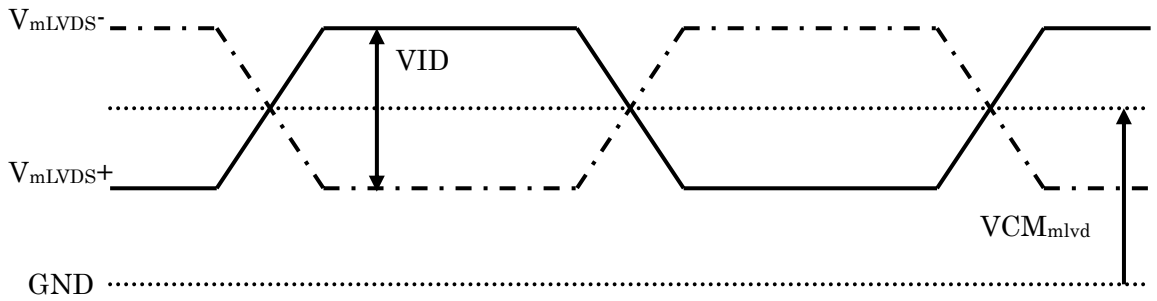
Please follow below levels for a standard gray scale voltage.

VLS-0.2 ≧ VH255 > VH_A > ⋯ > VH_C > VH0 ≧ HVDD+0.2

HVDD-0.2 ≧ VL0 > VL_C>… > VL_A > GND+0.2

【Note 2】 : Applies to terminals for
S*_LVCLKP/N ,S*_LV0P/N,S*_LV1P/N,S*_LV2P/N . (*=1 to 8)

The waveforms of signals are shown below.



【Note 3】 : Applies to terminals for LS_L,LS_R, REV_L,REV_R,.

【Note 4】 : Applies to terminals for GSP,GCK,GOE,GSP.

【Note 5】 : For COM adjustment, please adjust so that either i) flickers are minimized or ii) the contrast for each LCD module are maximized.

6-2. AC characteristic

6-2-1. AC characteristic (1)

Timing waveforms are shown at Fig 6-1,6-2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Source clock frequency	fck		(324.0)		MHz	S*_LVCLKP/N
Source clock High level pulse width	Tcwh	1.2	-	-	ns	
Source clock Low level pulse width	Tcwl	1.2	-	-	ns	
Source clock rise time	Tcr	-	-	1	ns	
Source clock fall time	Tcf	-	-	1	ns	
Data setup time	Tdsu	0.5	-	-	ns	S*_LV0~2P/N【Note1】
Data hold time	Tdho	0.5	-	-	ns	S*_LV0~2P/N【Note1】
Latch strobe pulse width	Tlsw	150		-	ns	LS_L,LS_R
Last data - Latch strobe time	Trls	20	-	-	CK	LS_L,LS_R
Electrode reversal - Latch strobe setup time	Tsurv	5	-	-	ns	LS_L/R,REV_L/R
Electrode reversal - Latch strobe hold time	Thrv	6	-	-	ns	LS_L/R,REV_L/R
RST signal High level pulse width	Twrst	12	-	-	ns	S*_LV0P/N
		3	-	-	CK	
LS signal – RST signal time	Tlsrst	150	-	-	ns	S*_LV0P/N
RST signal – LS signal time	Trstls	0	-	-	ns	LS1.LS2

【Note1】 DATA : S*_LV0~2P/N (*=1～8)

【Note2】Timing Controller:(LR388H5)

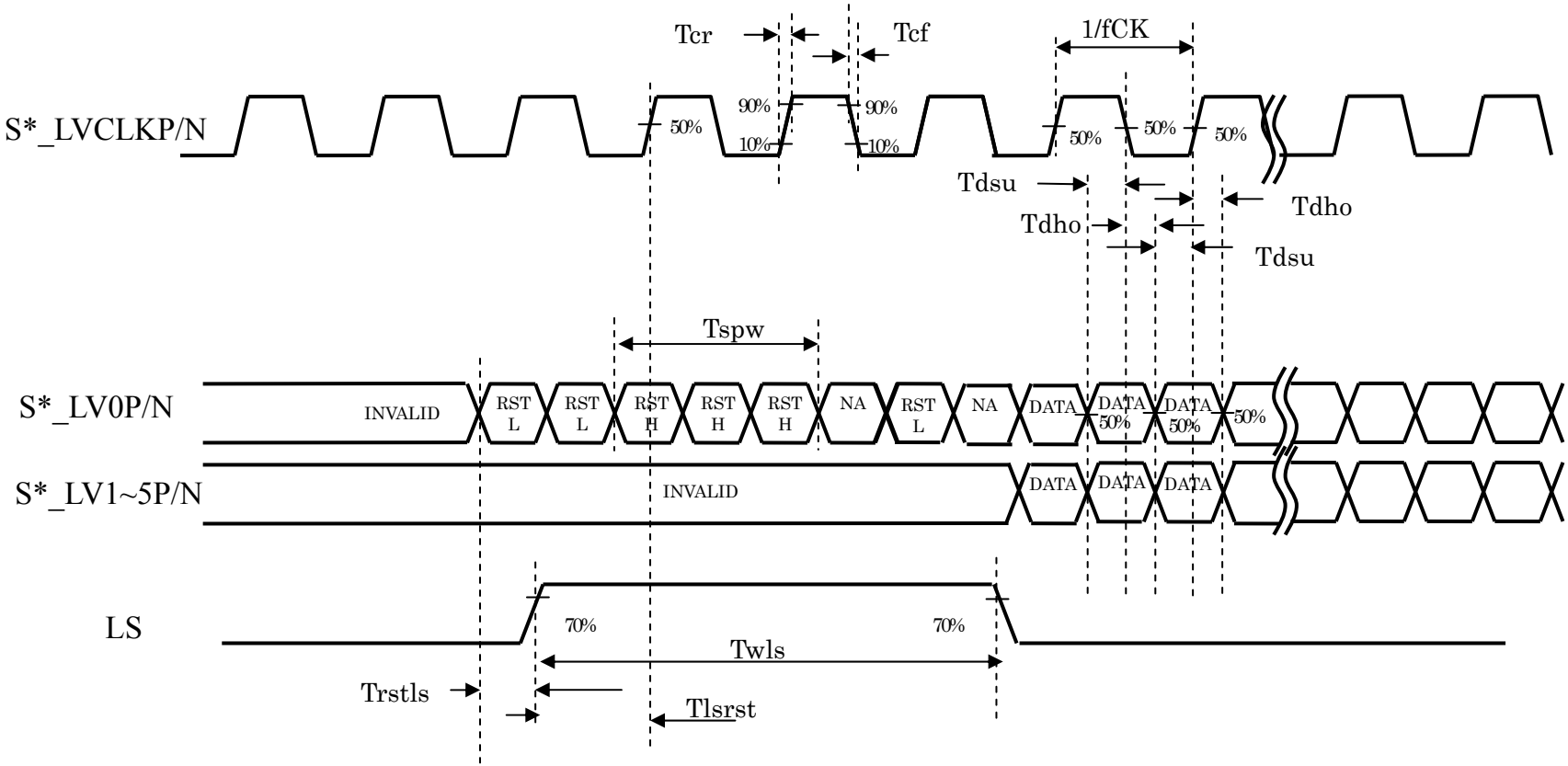
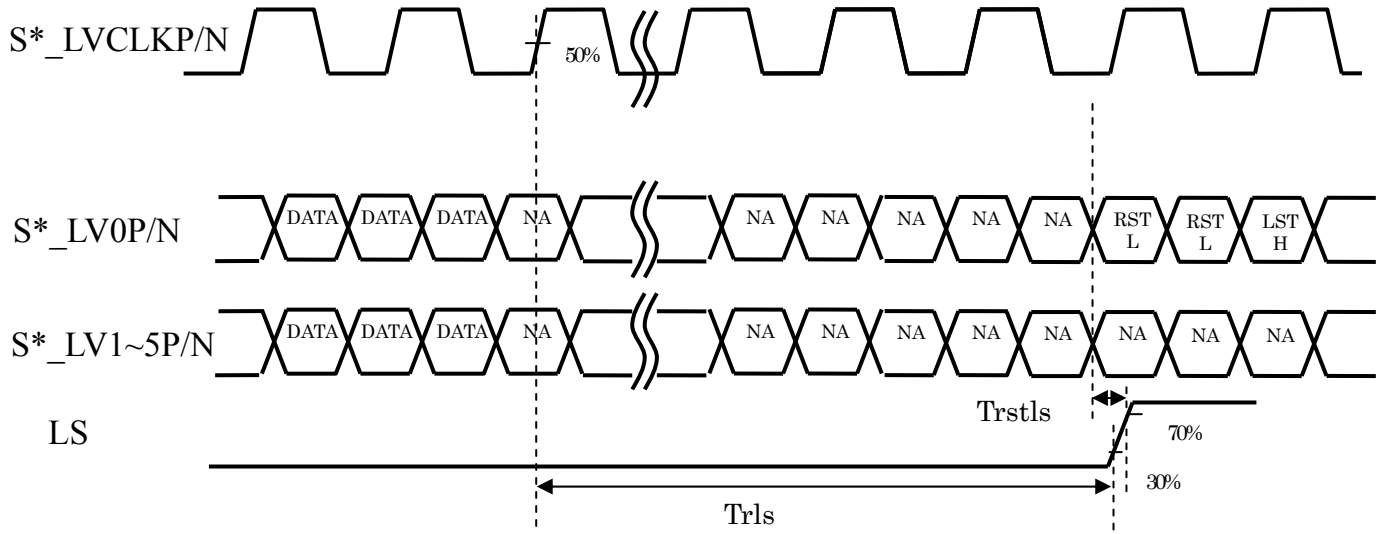


Fig.6-1 Timing waveform 1 (Source Driving Signal)



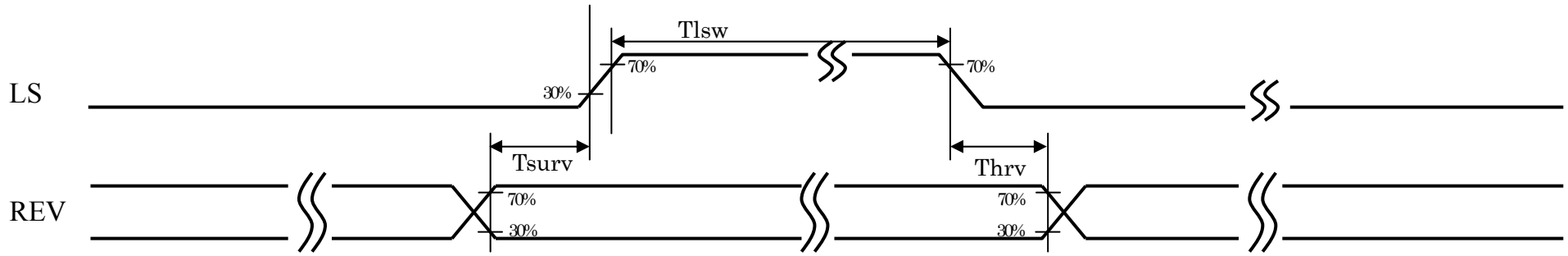


Fig. 6-2 Timing waveform 2 (Source Driving Signal)

6-2-2. AC characteristic (2)

Timing waveform is shown at Fig.6-3

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Gate clock frequency	fgck	-		200	KHz	GCK
Gate clock pulse High width	Twh	0.5		-	μs	
Gate clock pulse Low width	Twl	0.5		-	μs	
Gate clock rising time	Trcl	-	-	100	ns	
Gate clock falling time	Tfcl	-	-	100	ns	
Gate start pulse High width	Twsp	200			ns	GSP
Gate start pulse setup time	Tsu	100	-	-	ns	
Gate start pulse hold time	Th	100	-	-	ns	
Gate start pulse rising time	Trsp	-	-	100	ns	
Gate start pulse falling time	Tfsp	-	-	100	ns	

【Note】Timing Controller：(LR388H5)

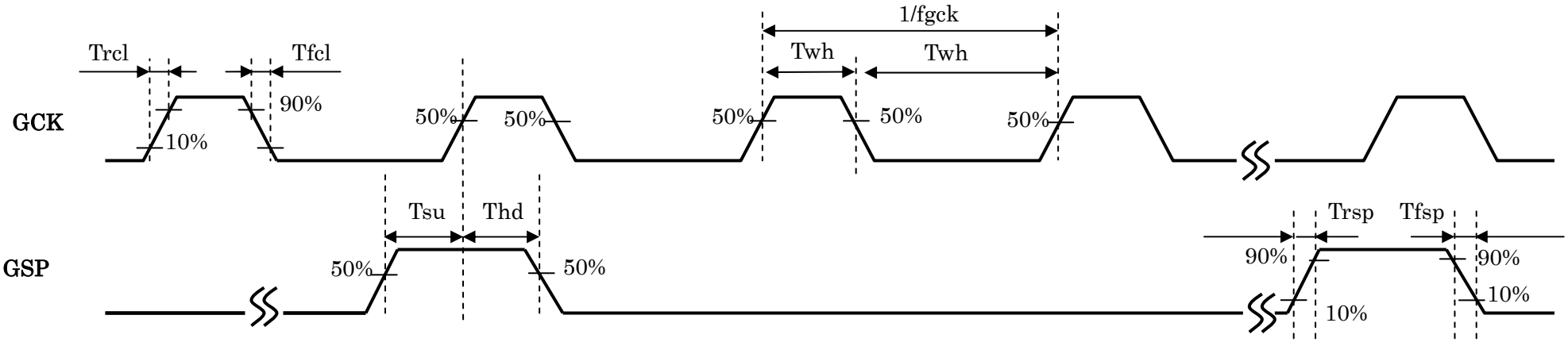


Fig.6-3 Timing waveform 3 (Gate Driving Signal)

7. Input Signal, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray scale	Gray Scale	Data signal																							
			R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Basic Color	Black	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	—	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	—	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	—	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	—	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	—	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	—	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓								↓								↓				
	⇩	↓				↓								↓								↓				
	Brighter	253	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	254	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓								↓								↓				
	⇩	↓				↓								↓								↓				
	Brighter	253	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	⇩	254	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	⇧	↓				↓								↓								↓				
	⇩	↓				↓								↓								↓				
	Brighter	253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	⇩	254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

0 : Low level voltage, 1 : High level voltage.

Each basic color can be displayed in 256 gray scales of red, 256 gray scales of green, and 256 gray scales of blue from 8 bit data signals. According to the combination of total 24 bit data signals, 16,777,216 color display can be achieved on the screen.

8. Optical characteristics

The optical measurement at the time of driving on the following conditions is shown in the following table.

Ta=25℃

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ 21 θ 22	CR≧10	70	88	—	Deg	【Note1,2,7】
	Vertical	θ 11 θ 12		70	88	—	Deg	Fig8-1,8-3
Contrast ratio		CR		—	5000	—		【Note2,7】 Fig8-2
Response time		τdrv		—	4	—	ms	【Note3,4,5,7】 Fig8-1,8-2 Fig.8-5
Chromaticity of white		x	θ =0°	0.248	0.278	0.308	—	【Note4,7】 Fig8-1,8-2
		y		0.258	0.288	0.318	—	
Chromaticity of red		x		0.620	0.650	0.680	—	
		y		0.310	0.340	0.370	—	
Chromaticity of green		x		0.271	0.301	0.331	—	
		y		0.615	0.645	0.675	—	
Chromaticity of blue		x		0.121	0.151	0.181	—	
		y		0.038	0.068	0.098	—	
Transmittance uniformity		δ_w		—	—	1.25	—	【Note6,7】 Fig8-2
Transmittance		%		3.8	4.5		%	【Note7】Fig8-2

*The measurement shall be executed 30 minutes after lighting at rating.

Optical characteristics are based on SHARP standard backlight system.

Drive conditions: LR388H5 Typical Input Timing

Liquid-crystal impression voltage: VH255 15.2V, the flicker optimal state.

Backlight unit condition: Brightness MAX.

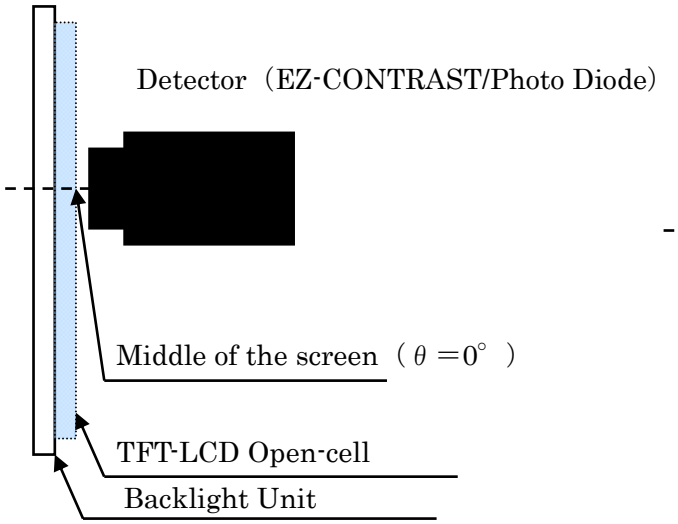


Fig.8-1 Measurement of viewing angle range and Response time.

Viewing angle range:EZ-CONTRAST

/Response time: Photo diode)

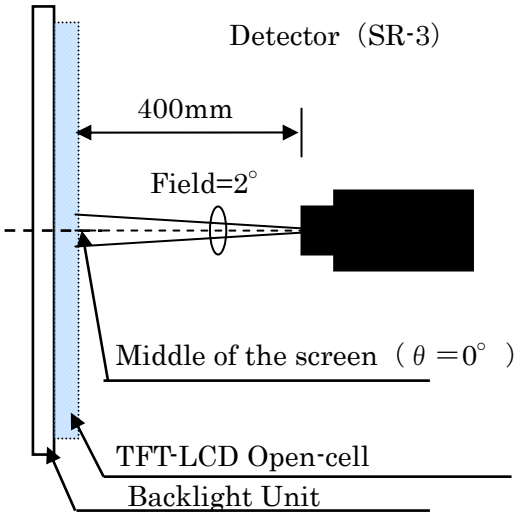


Fig.8-2 Measurement of luminance and chromaticity and Contrast.

【Note 1】Definitions of viewing angle range

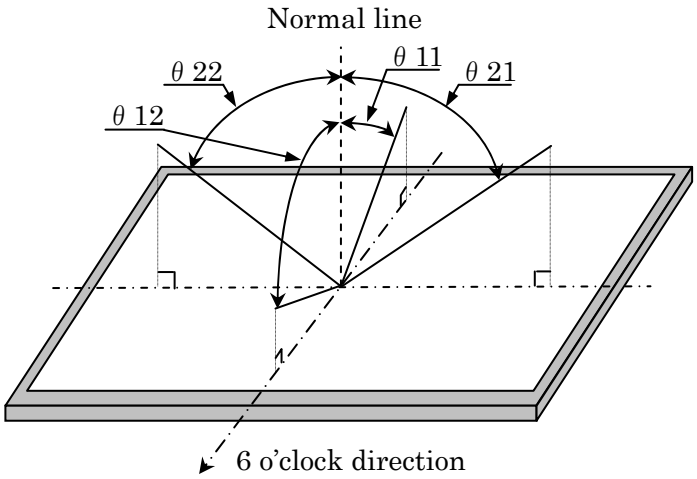


Fig. 8-3 Definitions of viewing angle range

【Note 2】Definition of contrast ratio :

The contrast ratio is defined as the following.

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance(brightness) with all pixels white}}{\text{Luminance(brightness) with all pixels black}}$$

【Note 3】Definition of response time

The response time of （τd and τr） is defined as the following figure.8-4 and shall be measured by switching the input signal for "any level of gray (0, 64, 128, 192, 255)" and "any level of (0, 64, 128, 192, 255)".

	0	64	128	192	255
0		τr0-64	τr0-128	τr0-192	τr0-255
64	τd64-0		τr64-128	τr64-192	τr64-255
128	τd128-0	τd128-64		τr128-192	τr128-255
192	τd192-0	τd192-64	τd192-128		τr192-255
255	τd255-0	τd255-64	τd255-128	τd255-192	

t*:x-y...response time from level of gray(x) to level of gray(y)

τr =Σ(tr:x-y)/10　τd = Σ(td:x-y)/10　τdrv = (τr + τd)/2

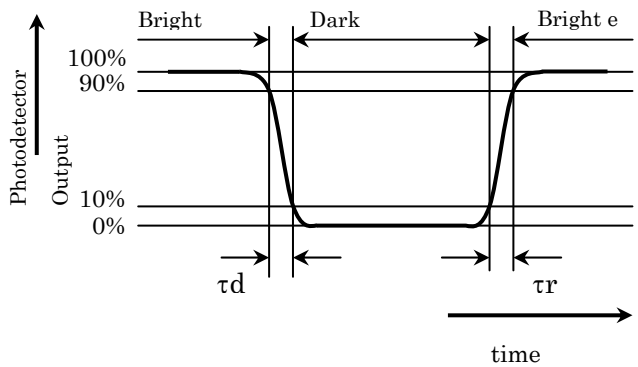


Fig. 8-4 Definitions of response time

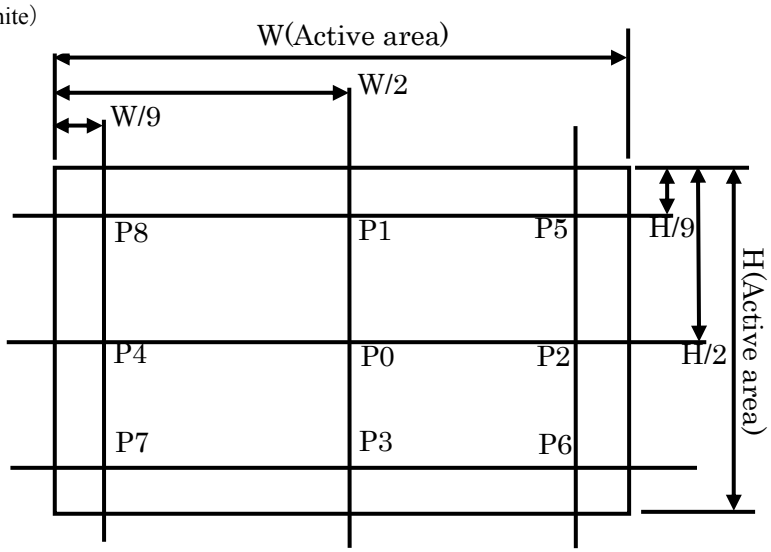
【Note 4】This shall be measured at center of the screen.

【Note 5】This value is valid when O/S driving is used at typical input time value.

【Note 6】Definition of transmittance uniformity ;

Transmittance uniformity is defined as the following with nine measurements.(P0～P8)

$$\delta W = \frac{\text{maximum transmittance of nine points (White)}}{\text{minimum transmittance of nine points (White)}}$$

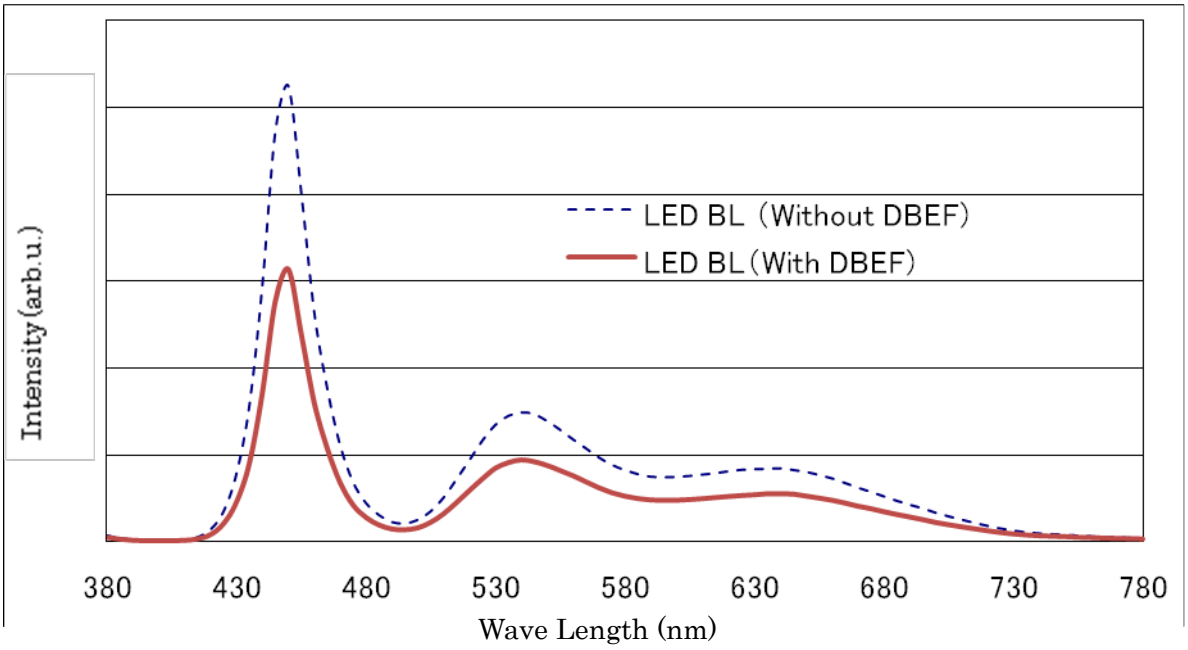


【Note 7】SHARP standard backlight system

・Backlight

Parts	Specification	Remark
DBEF	DBEF-D3-260 (3M)	Need to remove DBEF when measuring the transmittance.
Upper Prism Sheet	BEF3-T-285 ASn (3M)	
Lower Prism Sheet	BEF3-T-285 ASn (3M)	
Diffuser Sheet	BS-910 (KEIWA)	
Light Guide Plate	PMMA t=3.0	
Reflection Sheet	E6SR-188 (Torey)	
LED	R.G phosphors type White LED (SHARP)	

・Spectrum each wavelength



LD-23751A-19

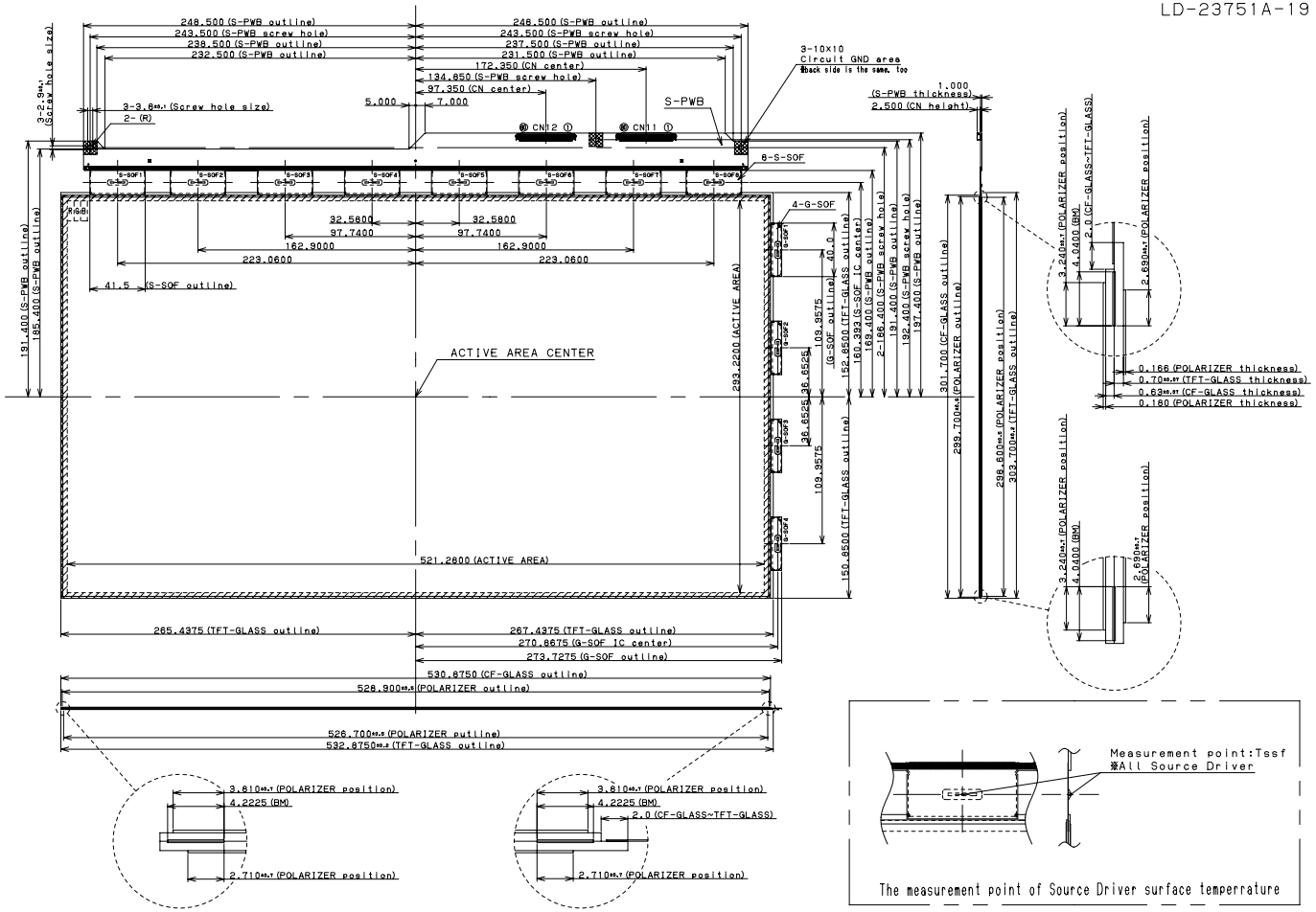


Fig.1 OPEN CELL OUTLINE DIMENTION (LQ235D1XXXX)