Application Information for Sharp's LS013B4DN02 Memory LCD

Sharp Microelectronics of the Americas

INTRODUCTION

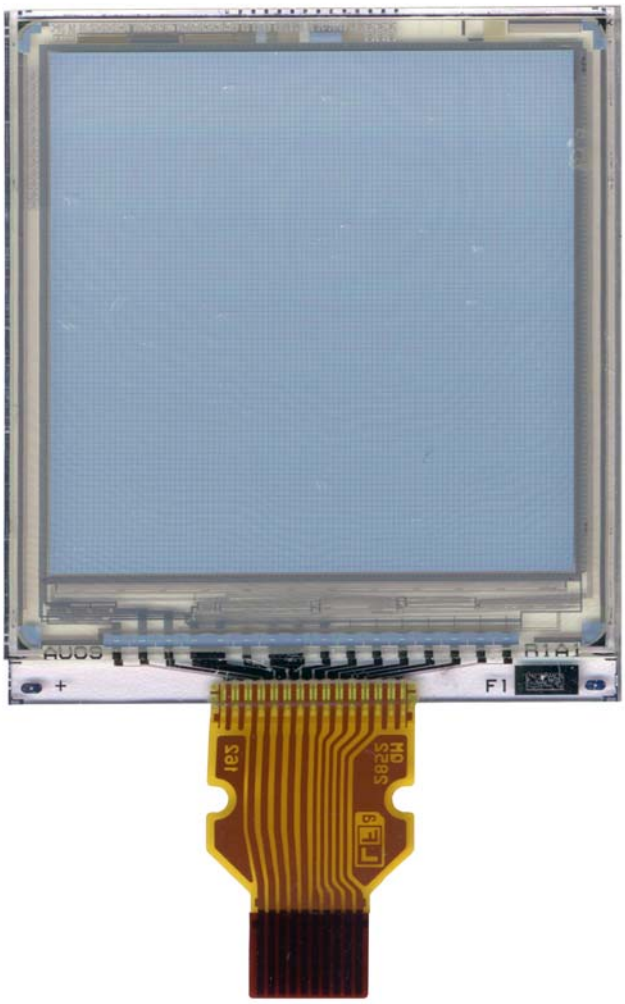
This Application Note provides additional design assistance for Sharp's LS013B4DN02 Memory LCD. This module is a reflective, monolithic active-matrix liquid crystal module utilizing Sharp's CG-silicon thin-film transistor process. It offers high performance and power efficiency for compact display applications, with a serial interface for simple integration.

Subjects covered will be:

- Mechanical Specifications, including dimension drawings and connector specifications
- Absolute Maximum Ratings
- Optical Specifications, including view angles, reflectivity, contrast, and risetime
- Electrical Characteristics, including interfacing and signal timing information
- Design Notes
- Manufacturing Information, including handling and storage
- Reliability Information

This Note is based on Sharp's document number LCY-12T09303A and is designed to provide supplementary information for the Specifications for this part.

Always refer to the latest Specifications when designing with these devices.



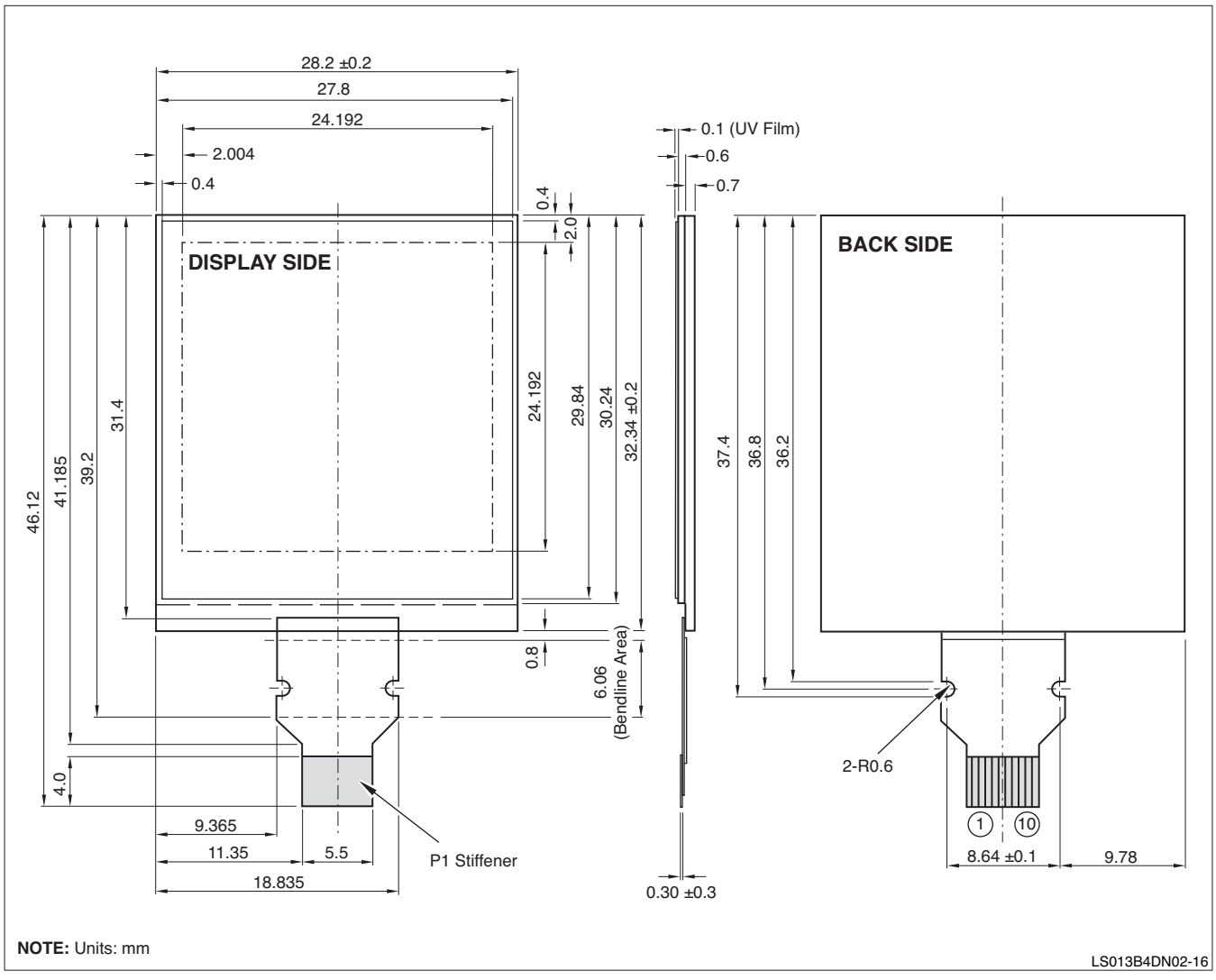
FEATURES

- Reflective monochrome panel
- Square aspect ratio (1:1)
- 1.35-inch screen with 96 × 96 resolution in a 9,216-pixel stripe array
- Serial interface for display control
- Screen data is arbitrarily renewable by line
- Built-in, 1-bit internal memory for data storage
- Super low power consumption TFT panel
- RoHS compliant

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATION	UNIT
Screen Size	1.35	Inch
Viewing Area	24 (H) × 24 (V)	mm
Dot Configuration (Square panel)	96 (H) × 96 (V)	Dots
Dot Pitch	0.252 (H) × 0.252 (V)	mm
Pixel Array	Stripe Array	-
External Dimensions	28.2 (W) × 32.34 (H) × 1.4 (D)	mm
Mass	3.6 (TYP.)	g
Surface Hardness	3H	Pencil hardness

External Dimensions



NOTE: Units: mm

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Connector Specifications

Table 1. Input Terminals and Functions

TERMINAL	SYMBOL	I/O	FUNCTION	NOTES
1	SCLK	INPUT	Serial clock signal	
2	SI	INPUT	Serial Data input signal	
3	SCS	INPUT	Chip select signal	
4	EXTCOMIN	INPUT	External COM inversion signal input (H: enable)	1
5	DISP	INPUT	Display ON/OFF signal	2
6	VDDA	POWER	Power supply (Analog)	
7	VDD	POWER	Power supply (Digital)	
8	EXTMODE	INPUT	COM inversion select terminal	3
9	VSS	POWER	GND (Digital)	
10	VSSA	POWER	GND (Analog)	

NOTES:
1. EXTCOMIN is HIGH enabled. When LOW, the serial input flag is enabled. See Figure 13 and Figure 14 for recommended circuits.
2. DISP enables/disables the display. All pixels will revert to Normal mode (reflective) when LOW. When DISP = H, data in the pixel memories displays normally.
3. EXTMODE pin must be connected to VDD for HIGH, and to VSS for LOW. See FIGURE in *Interfacing and Signals.*

Absolute Maximum Ratings

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTES
Power Supply Voltage	Analog	VDDA	-0.3	+5.8	V	
	Logic	VDD	-0.3	+5.8	V	1
Input Signal Voltage (HIGH)				VDD	V	2
Input Signal Voltage (LOW)			-0.3		V	
Storage Temperature		Tstg	-30	+80	°C	3
Operation Temperature (at panel surface)		Topr1	-20	+70	°C	4

NOTES:
1. Applies to EXTMODE.
2. Applies to SCLK, SI, SCS, DISP, EXTCOMIN.
3. Do not exceed this temperature in any part of the module.
4. Maximum wet bulb temperature is 57°C or lower. No condensation is allowed. Condensation will cause electrical leakage and may cause the module to fail to meet this Specification.
5. “Operating Temperature” is the guaranteed temperature limits for operation.
6. For contrast, response time, and other display quality determination, use Ta = + 25°C.

OPTICAL SPECIFICATIONS

Ta = 25°C

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Viewing Angle CR ≥ 5	H	θ21, θ22		TBD		° (degrees)	1
	V	θ11		TBD		° (degrees)	1
		θ12		TBD		° (degrees)	1
Contrast Ratio		CR	5	10			2
Reflectivity Ratio		R		50		%	2
Response Time	Rise	tr		50		ms	3
	Fall	tf		50		ms	3
Chromaticity	White	x		0.313			2
		y		0.338			2

NOTES:

1. Viewing Angle is described as clock positions: θ12 = 12 o'clock, θ11 = 6 o'clock, θ21 = 3 o'clock, θ22 = 9 o'clock. See Figure 1.
2. Contrast Ratio, Reflectivity Ratio, and Chromaticity are measured through the use of an integrating sphere. See Figure 2.
3. Response Time is measured by the change interval in an optical receiver when the test panel's signal is transitioned from white to black to white. See Figure 3 for the measurement setup and Figure 4 for the output waveshape.

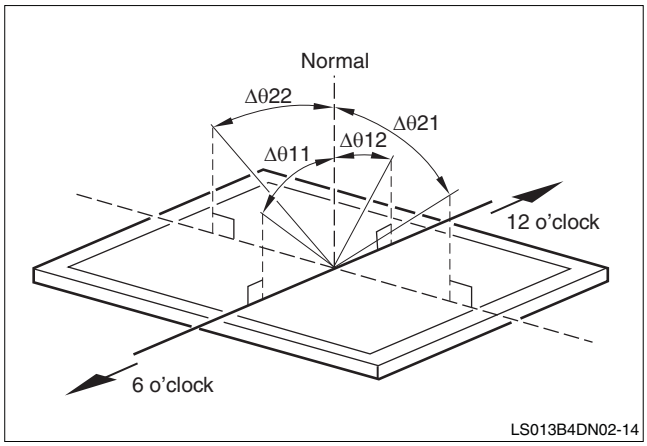


Figure 1. Viewing Angle

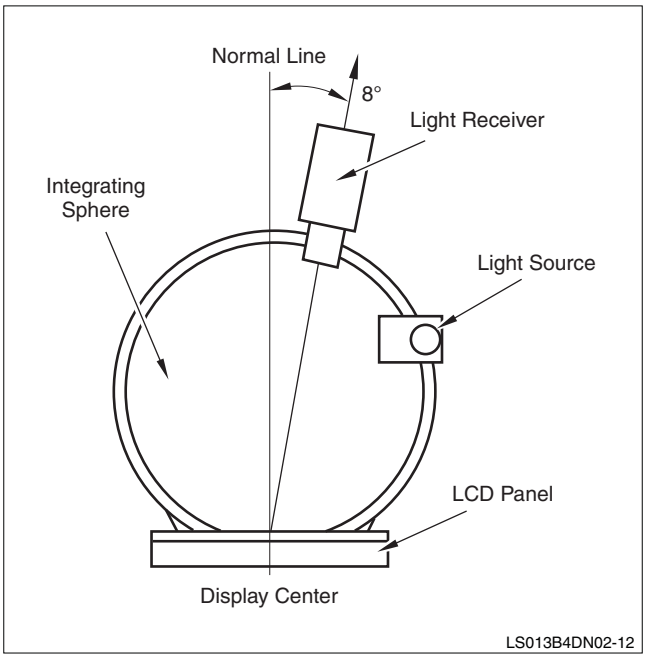


Figure 2. Setup for Contrast, Reflection Ratio, and Chromaticity

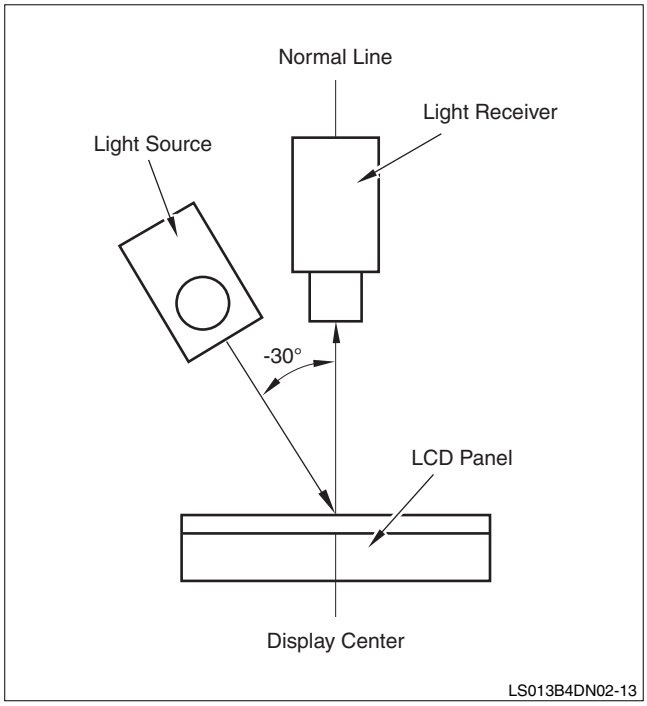


Figure 3. Setup for Response Time

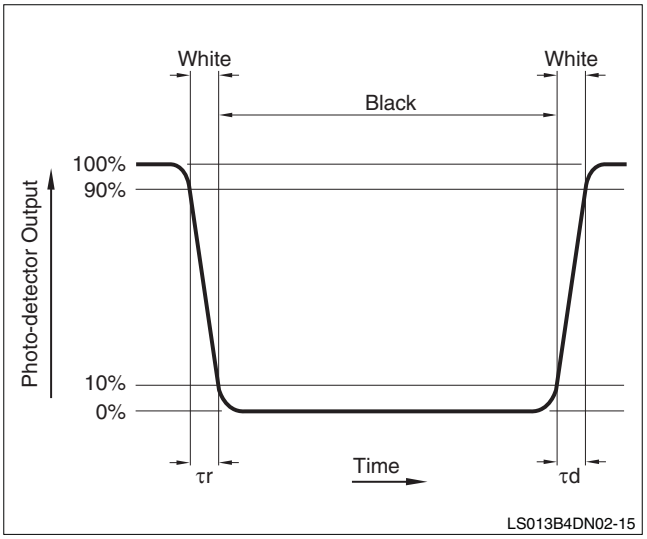


Figure 4. Response Time

ELECTRICAL SPECIFICATIONS

Here are the Recommended Operating Conditions for this module, with VSS (GND) = 0V and Ta = 25°C.

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Power supply	Analog	VDDA	+4.8	+5.0	+5.5	V	
	Logic	VDD	+4.8	+5.0	+5.5	V	1
Input signal voltage	HIGH	VIH	+2.70	+3.0	<VDD	V	2
	LOW	VIL	VSS	VSS	VSS + 0.15	V	
Input leakage current	HIGH	IOH			TBD	µA	3
	LOW	IOL			TBD	µA	4

NOTES:
1. 3 V or less is recommended; never exceed VDD.
2. EXTMODE = H
3. VI = 3 V; applies to SCLK, SI, SCS, DISP, EXTCOMIN
4. VI = 0 V; applies to SCLK, SI, SCS, DISP, EXTCOMIN

Power Consumption

This module has the ability to shut down most of its logic circuits when in Static mode (not being updated). It has two levels of power consumption: Static and Dynamic Display.

Static Display: 15 µW (TYP.) Vertical stripe display; fully static, no display updates.

- This includes a 1 Hz VCOM toggle, and VDD = 5 V, VDDA = 5 V, ƒSCLK = 1 MHz, ƒSCS = 1 Hz

Dynamic Display: 30 µW (TYP.) Vertical stripe display; updated at a 1 Hz rate.

- VDD = 5 V, VDDA = 5 V, ƒSCLK = 1 MHz, ƒSCS = 1 Hz

These numbers represent average power, not peak power usage when driving VCOM. Always allow for a margin in power supply design.

Decoupling Capacitors

Use of a decoupling capacitor on VDD and VDDA is recommended, even when the two supplies are tied together. See Figure 5.

Values for these capacitors:

C1: DISP to VSS: rank B, 0.1 µF Ceramic

C2: VDDA to VSS: rank B, 1 µF Ceramic

C3: VDD to VSS: rank B, 1 µF Ceramic

These are recommended values; actual values should be determined by the final design. Always place the decoupling capacitors as close as possible to the part as the impedance of the VDD and VSS lines is low when the module is operating.

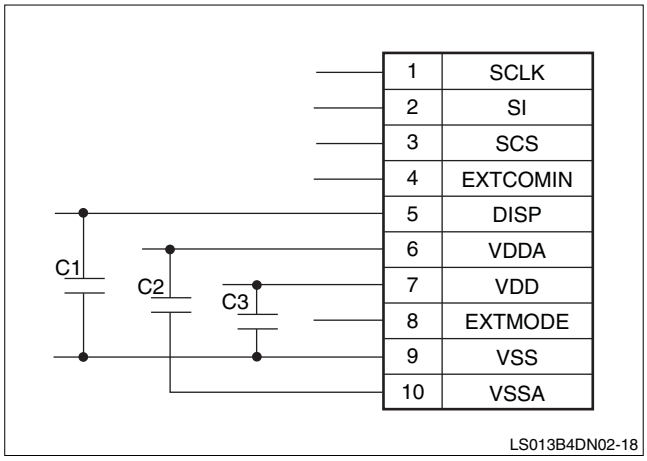


Figure 5. Decoupling Capacitors

Power Supply Sequencing

This device requires proper supply sequencing on both startup and shutdown to prevent latching of the logic circuits. Refer to Figure 6.

POWER-UP

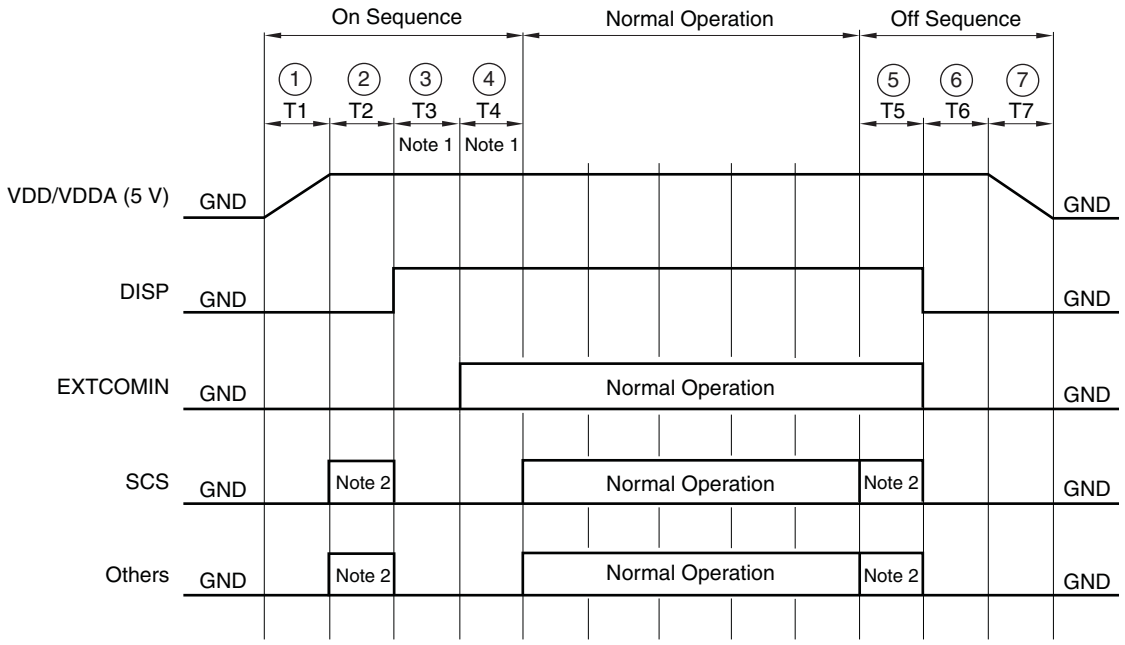
VDD and VDDA must rise together or VDD must rise faster than VDDA.

- 5 V rises to nominal
- Initialize pixel memory: send D2 CLEAR ALL flag or set the display to all-white (requires >1 V)
- Latch cancellation for TCOM; requires a period to cancel the COM latch circuit by DISP = HIGH (requires > 30 µS)
- TCOM polarity initialization by EXTCOMIN (requires > 30 µS)

POWER-DOWN

VDD and VDDA must fall together or VDDA must fall faster than VDD.

- Initialize pixel memory (requires >1 V)
- Initialize VA, VB, and VCOM (requires >1 V)
- 5 V falls



NOTES:

1. The order of (3) and (4) can be reversed, in this case, VCOM polarity inversion timing controlled by EXTCOMIN (doesn't work during DISP = 'L').
2. Setup value for initialization of pixel memory data.
3. Precautions at power on and power off.

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Figure 6. Power Supply Sequencing

SIGNAL DESCRIPTIONS

Input signal characteristics are given in Table 2 and Table 3.

All measurements are at VDDA = +5.0 V, VDD = +5.0 V, GND = 0 V, Ta = 25°C.

Table 2. Signal Frequencies

PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
ƒSCS	Frame frequency	1	-	60	Hz
ƒSCLK	Clock frequency		1	2	MHz
tV	Vertical Interval	16.66	-	1000	ms
ƒCOM	COM Frequency	0.5	-	30	Hz

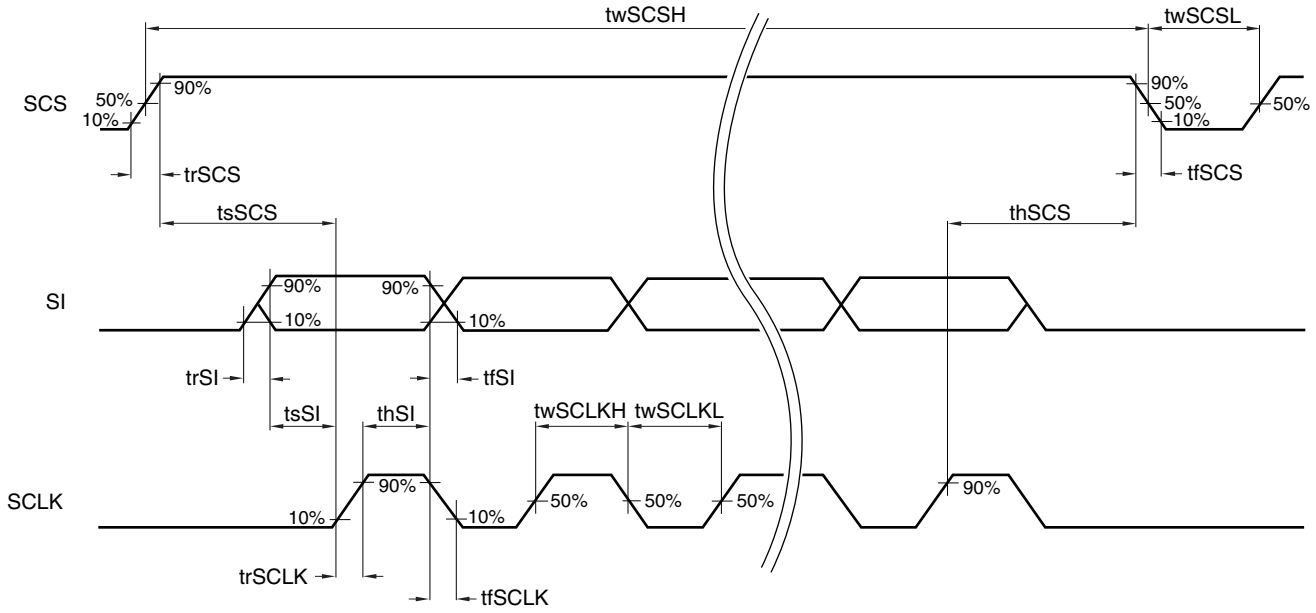
Table 3. Signal Transition Times

PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTES
trSCS	SCS Risetime			50	ns	
tfSCS	SCS Falltime			50	ns	
twSCSH	SCS HIGH Duration	68			µs	2
		12			µs	3
twSCSL	SCS LOW Duration	(1)			µs	
tsSCS	SCS setup time	(3)			µs	
thSCS	SCS hold time	(1)			µs	
ƒSI	SI frequency		0.5	1	MHz	
trSI	SI Risetime			50	ns	
tfSI	SI Falltime			50	ns	
tsSI	SI setup time	(120)			ns	
thSI	SI hold time	(125)			ns	
trSCLK	SCLK Risetime			50	ns	
tfSCLK	SCLK Falltime			50	ns	
twSCLKH	SCLK HIGH duration	200	450		ns	
twSCLKL	SCLK LOW duration	200	450		ns	
ƒEXTCOMIN	EXTCOMIN frequency		1	60	Hz	4
trEXTCOMIN	EXTCOMIN Risetime			50	ns	
tfEXTCOMIN	EXTCOMIN Falltime			50	ns	
thlEXTCOMIN	EXTCOMIN HIGH duration	1			µs	
trDISP	DISP Risetime			50	ns	
tfDISP	DISP Falltime			50	ns	

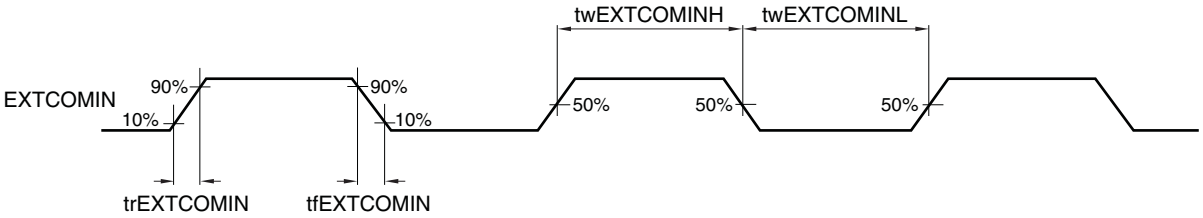
NOTES:
1. Parentheses indicate preliminary values.
2. Dynamic Mode (continuously updating display)
3. Static Mode (no display updating)
4. ƒEXTCOMIN must always be less than ƒSCS (Table 2)

Timing Diagrams

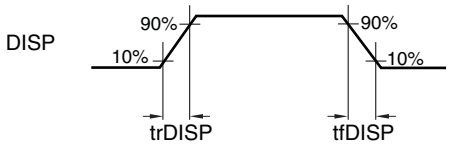
SCS, SI, SCLK Signal



EXTCOMIN Signal



DISP Signal



NOTES:
1. SCS, SI, SCLK, DISP: 3 V Amplitude
2. EXTCOMIN: 5 V Amplitude

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Figure 7. SCS, SI, SCLK, EXTCOMIN, and DISP Signals

PROGRAMMING

For software commands, see the Application Note, *Programming Sharp's Memory LCDs,* by Ken Green.

In all the following diagrams and descriptions, these conventions are used:

- M0: MODE
  When M0 is 'H', the module enters Dynamic Mode, where pixel data will be updated.
  When M0 is 'L' the module remains in Static Mode, where pixel data is retained.
- M1: VCOM
  This polarity-inversion flag enables a periodic polarity inversion on the panel to keep a latent charge from building up within the Liquid Crystal cells. When M1 is 'H' then VCOM = 'H' is output. If M1 is 'L' then VCOM = 'L' is output.
  When EXTMODE = 'H', M1 value = XX (don't care). See *COM Inversion and Signal Selection.*
- M2: CLEAR ALL
  When M2 is 'L' then all flags are cleared. When a full display clearing is required, refer to *CLEAR ALL.*
- D1 - D96: Display data
  Setting D(*n)* = 'L' sets that pixel to black. Conversely, Setting D(*n)* = 'H' sets that pixel to white.
- DUMMY DATA: Dummy data
  Dummy data is typically 'XX (don't care); however Sharp recommends setting bits to 'L'.

Data Addressing and Positions

This part uses mixed addressing for columns and lines. Columns (X direction) are addressed using a 7-bit binary scheme, and lines (Y direction) are addressed directly as 96 bits. One line is the minimum addressable unit in the display; even if only one pixel in the line is to be updated, the entire line must be sent.

Dynamic Mode

For software commands, see Sharp's Application Note, *Programming Sharp's Memory LCDs,* by Ken Green.

MULTIPLE LINE WRITE

Dynamic Mode assumes the updating of at least one line in the display. During the Data Write period, data is stored in the panel's binary latch. During Data Transfer, the data from the latch is written to the panel memory, line-by-line. During the write to panel memory, data for the next line is latched.

Dynamic Mode is entered by sending M0 = H and M2 = L.

Figure 9 shows an example of writing multiple lines.

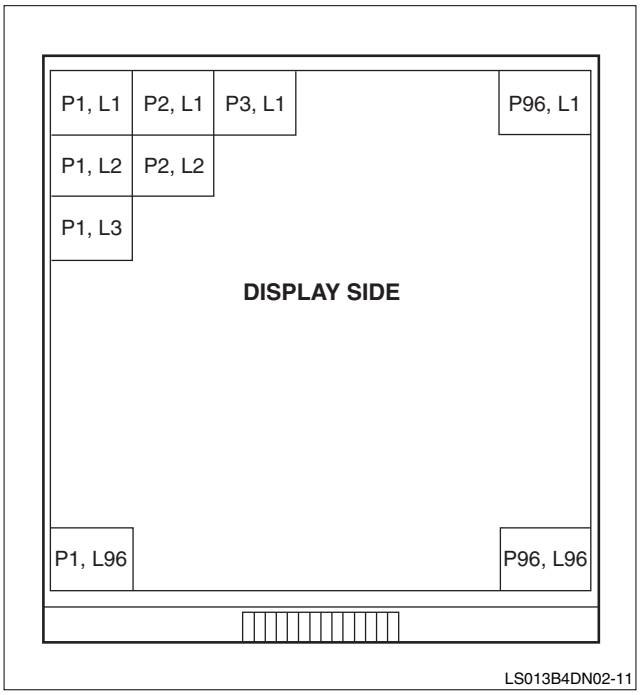


Figure 8. Display Data Position

Table 4. Column (X direction) Addressing

LINE ADDRESS	COLUMN ADDRESS						
	CA0	CA1	CA2	CA3	CA4	CA5	CA6
L1	H	L	L	L	L	L	L
L2	L	H	L	L	L	L	L
L3	H	H	L	L	L	L	L
:	:	:	:	:	:	:	:
L94	L	H	H	H	H	L	H
L95	H	H	H	H	H	H	L
L96	L	L	L	L	L	H	H

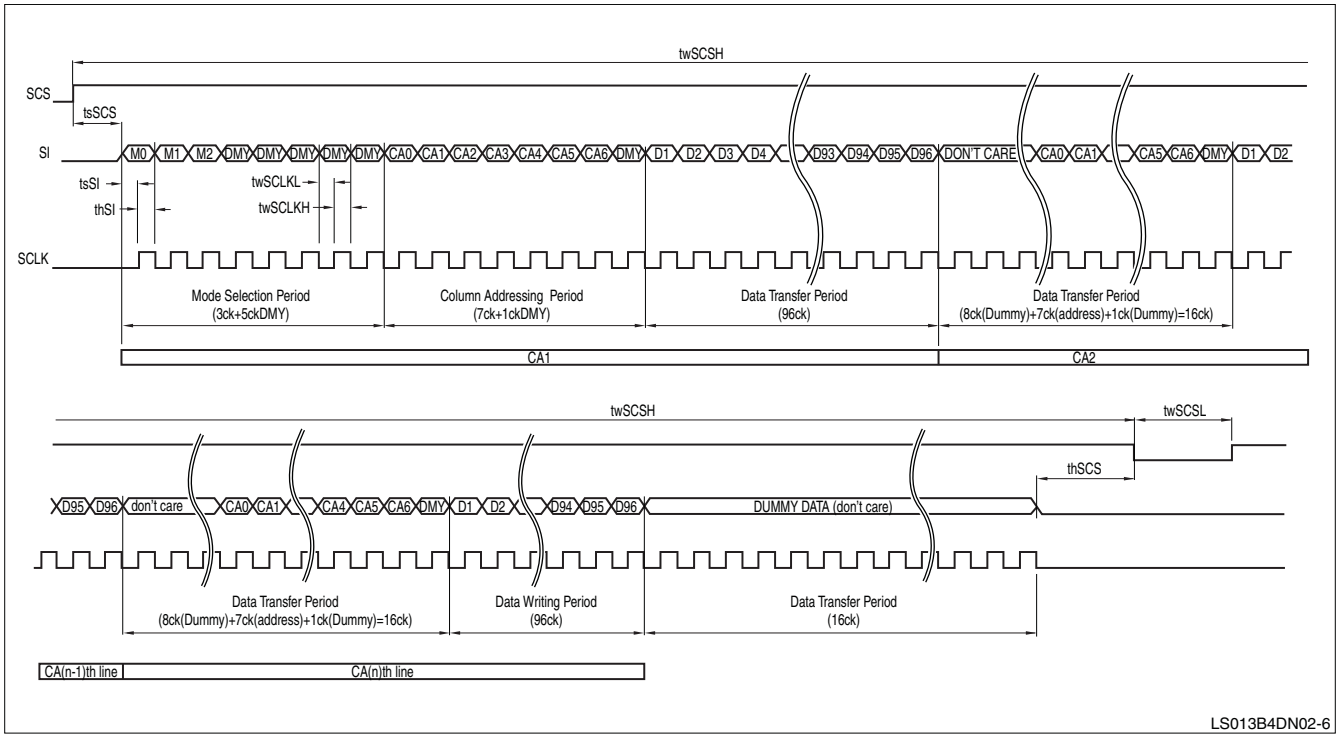


Figure 9. Dynamic Mode Timing Diagram, Writing Multiple Lines

SINGLE LINE WRITE

Writing a single line of data is much the same as writing multiple lines. During the Data Write period, data is stored in the panel's binary latch. During Data Transfer, the data from the latch is written to the panel memory, line-by-line. During the write to panel memory, data for the next line is latched.

Dynamic Mode is entered the same way, by sending M0 = H and M2 = L.

Figure 10 shows an example of writing a single line.

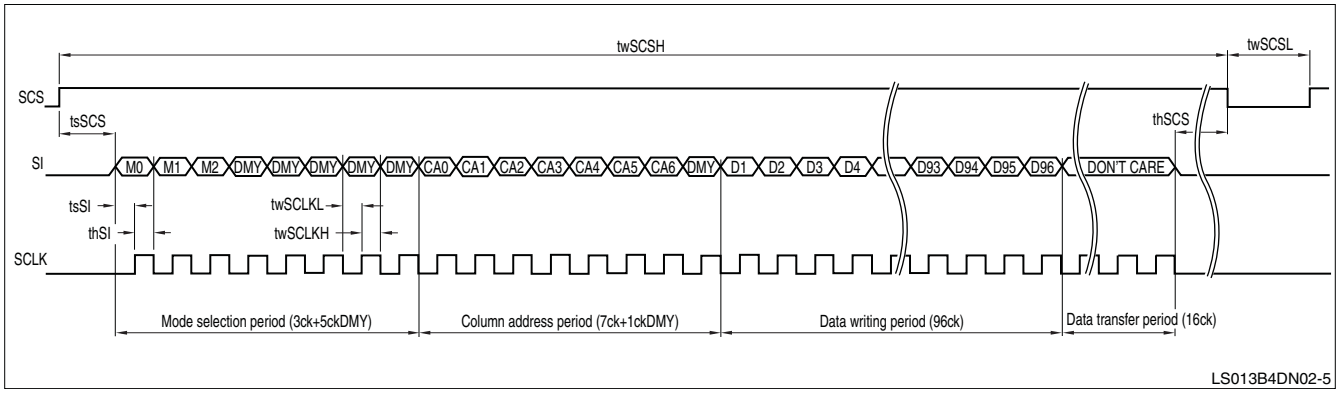


Figure 10. Dynamic Mode Timing Diagram, Writing a Single Line

Static Mode

Static Mode is the module's lowest-power mode, with data latches and other circuitry powered down. Static Mode can be held indefinitely; as long as the panel has power and VCOM is toggled periodically.

Sharp recommends keeping maximum time between VCOM toggles to no more than one second, and refreshing data every two hours, to prevent stuck pixels.

Static Mode is entered by sending M0 = L and M2 = L.

CLEAR ALL

CLEAR ALL will clear all data from pixel memories and the display will revert to its normal white color.

CLEAR ALL is invoked by sending M0 = L and M2 = H.

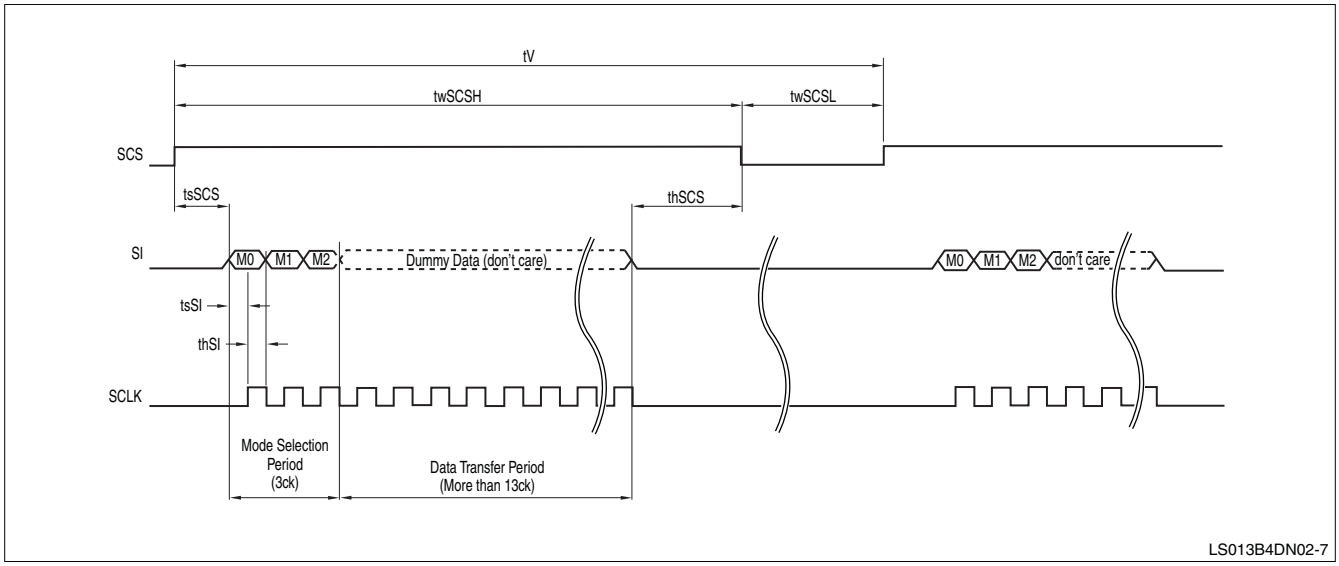


Figure 11. Static Mode Timing Diagram

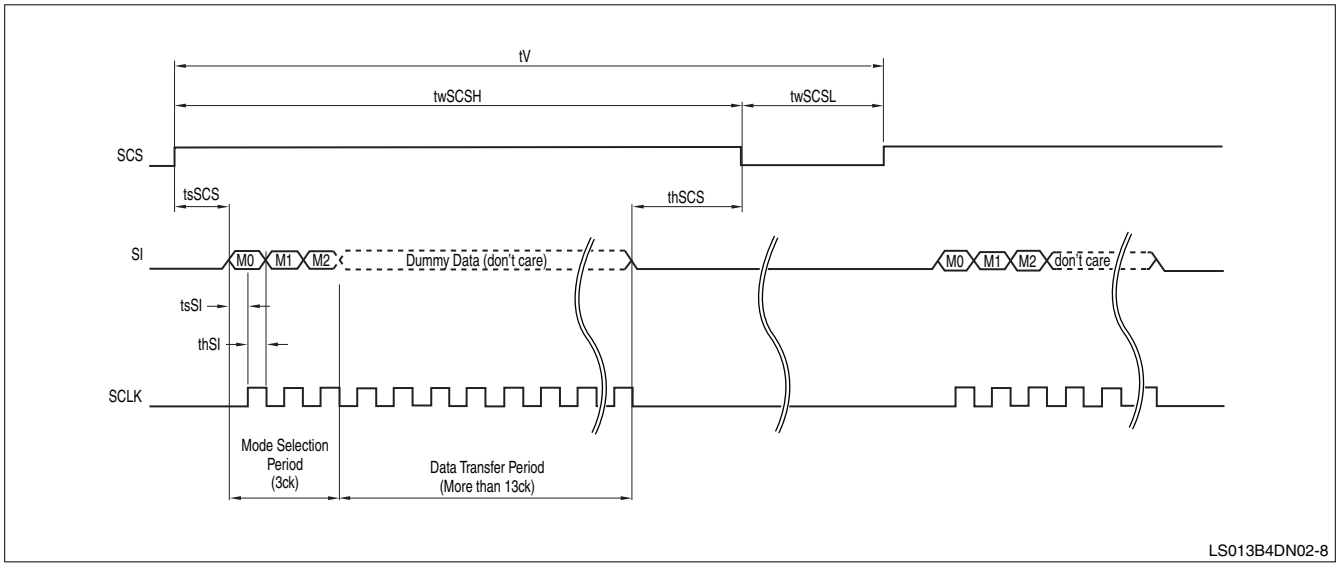


Figure 12. CLEAR ALL Timing Diagram

VCOM Inversion

Periodic VCOM inversion impresses a periodic polarity inversion across the panel to keep a latent charge from building up within the Liquid Crystal cell. It can be implemented either through software or through hardware. In either implementation, the positive and negative inversion intervals should be kept as equal as possible, and intervals should not exceed one second.

To implement VCOM inversion in software, the M1 bit is periodically toggled. When M1 is 'H' then VCOM = 'H' is output to the panel. If M1 is 'L' then VCOM = 'L' is output to the panel. To set the panel for software toggling of M1, tie EXTMODE to VSS as shown in Figure 13.

When implementing a VCOM toggle through hardware, EXTMODE is set to 'H', and the M1 value becomes XX (don't care). Hardware then toggles EXTCOMIN, and the timing between toggles of this line sets the VCOM inversion interval. Therefore, it's important not to allow the toggling interval of EXTCOMIN to exceed one second. To set the panel for software toggling of M1, tie EXTMODE to VDD as shown in Figure 14.

The LC cell inversion polarity toggle is armed when EXTCOMIN rises. Internal signal COMZ toggles with each rise of EXTCOMIN, and latches the VCOM transition. The VCOM transition takes place upon the next clock transition of SCS. Again, keep the duty cycle of EXTCOMIN at 50%.

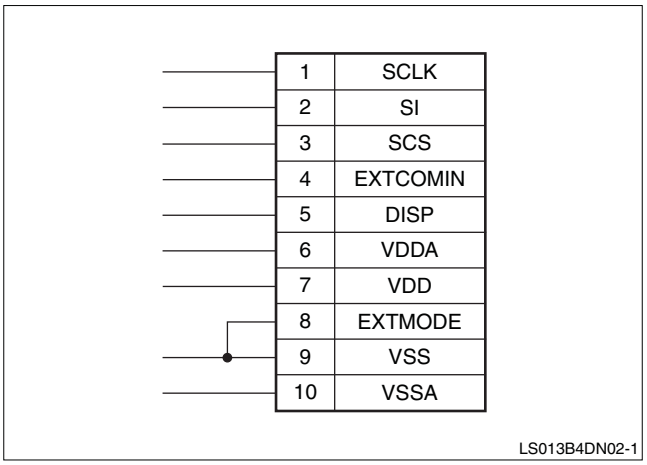


Figure 13. VCOM Software Input

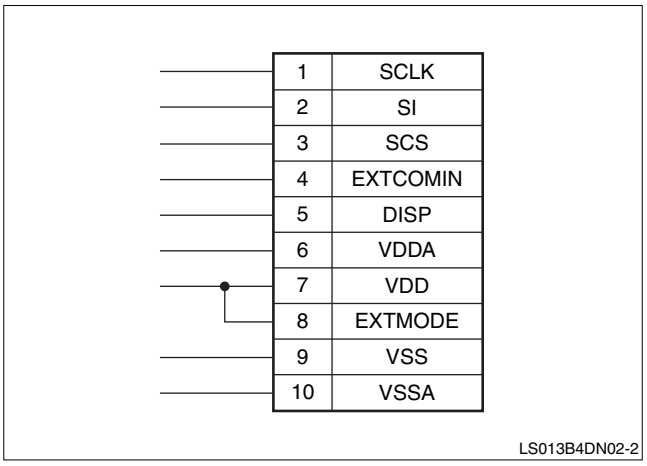


Figure 14. VCOM Hardware Input

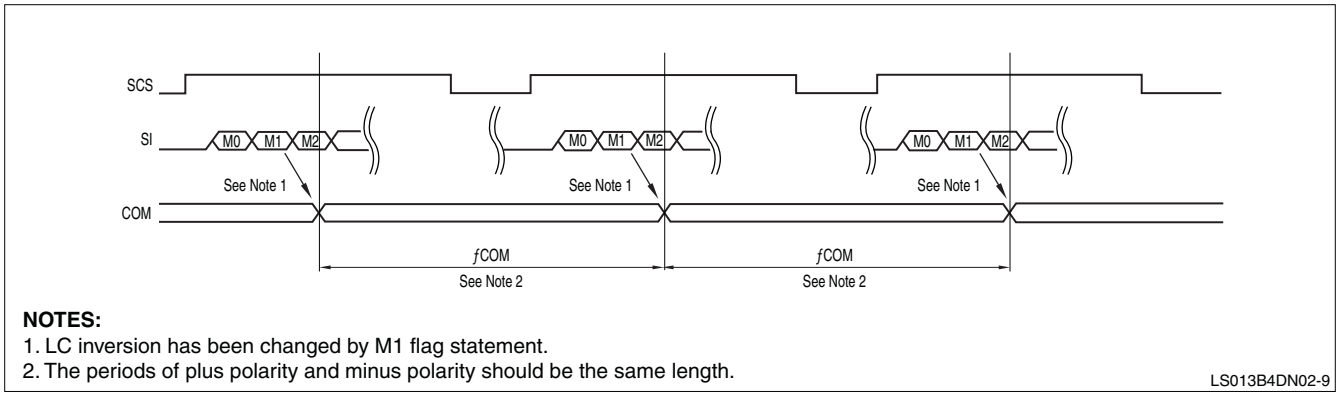
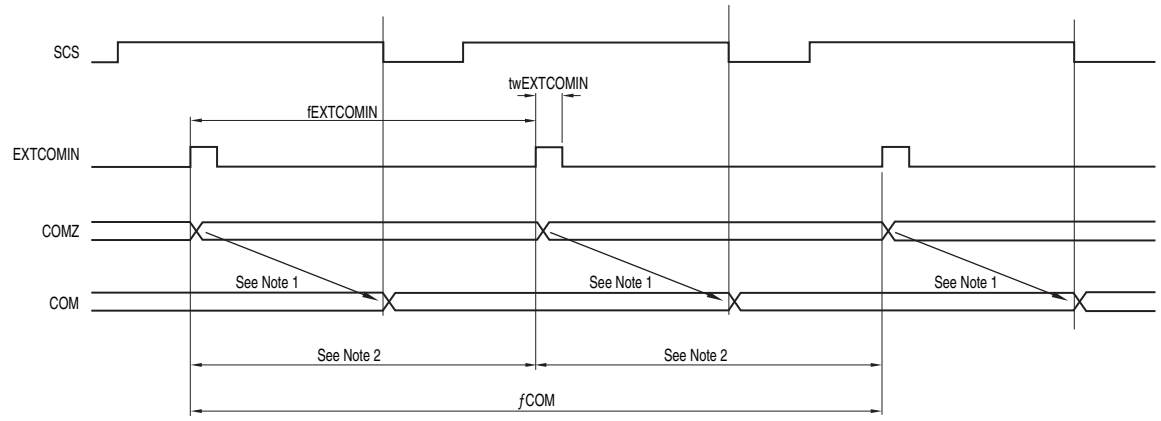


Figure 15. EXTMODE = L, Software VCOM Toggle



NOTES:
1. LC inversion polarity has been latched by the rise time of EXTCOMIN internally as COMZ, and when SCS falls, LC inversion occurs as VCOM.
2. The duty cycle of EXTCOMIN should be 50%.

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Figure 16. EXTMODE = H, Hardware VCOM Toggle

These Truth Tables show how VCOM is implemented in both hardware and software.

Table 5. EXTMODE = L

EXTCOMIN	COM
L	Depends entirely on status of M1
L	
H (rising edge)	
H (rising edge)	

Table 6. EXTMODE = H Relationship of COMZ to VCOM

COMZ	VCOM	
	SCS = L	SCS = H
L	L	Qn-1
H	H	Qn-1

NOTE: Qn-1: VCOM changes polarity at the falling edge of SCS.

Table 7. EXTMODE = H, Relationship of COMZ to EXTCOMIN

EXTCOMIN	COMZ	
	Before Inversion	After Inversion
L	L	L
L	H	H
H (rising edge)	L	H
H (rising edge)	H	L

NOTE: COMZ is inverted with each rising of EXTMODE.

DESIGN NOTES

1. This device is static sensitive. Handle it only in a static-safe environment.
2. Do not press on the surface of the module, and do not stack modules in such a way that pressure will be applied to the surfaces or to the connector area. The safest place for temporary storage of modules is in their shipping tray.
3. The connector on this module is designed for a limited number of insertions. Do not attempt to solder directly to the connector.
4. This set of Specifications gives definite environmental, electrical, and signal drive conditions for the operation of this module. Operating it outside of these given limits can reduce image quality, shorten its life, or cause it to fail altogether.
5. When displaying static images, Sharp recommends refreshing the image data every two hours to prevent stuck pixels.
6. When storing this module, keep it from long periods of exposure to direct sunlight or other sources of ultraviolet light. Recommended storage is in a dark place.
7. The liquid crystal material in this module will solidify if stored below the rated temperature, and will become an isotropic liquid if stored above the rated storage temperatures. After such storage, the material may not return to its original properties.
8. Use of decoupling capacitors is recommended. See *Electrical Specifications.*
9. This device can be powered from a 3V system with these power supply ICs. See *Power Supply Reference Circuits* for more information.
   – SII: S-8821 Charge Pump Power Supply IC
   – National Semiconductor: LM2750 Charge Pump Power Supply IC

Table 10. Electrical Specifications for 3 V Step-up Power Supply ICs

PART NUMBER	V IN (V)		V OUT (V)			I OUT (mA)
	MIN.	MAX.	MIN.	TYP.	MAX.	
S-8821	2.8	5.0	4.9	5.0	5.1	40
LM2750	2.7	5.6	4.8	5.0	5.2	40

NOTES:
1. Refer to each manufacturer's specifications for more information.
2. This information is for reference. Evaluate the parts in actual use.

POWER SUPPLY REFERENCE CIRCUITS

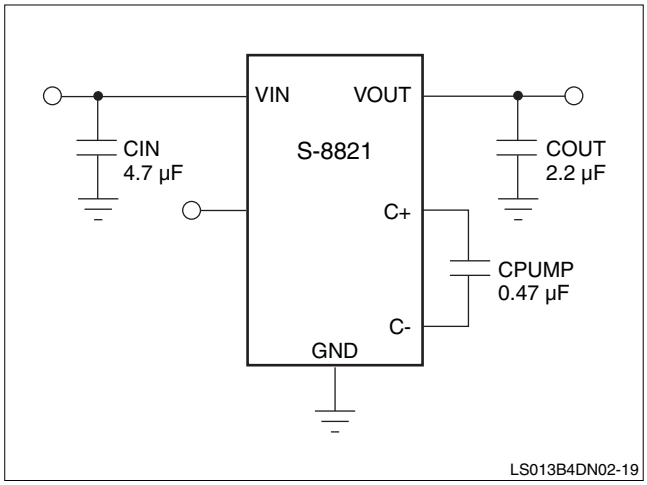

Figure 17. S-8821 Reference Circuit

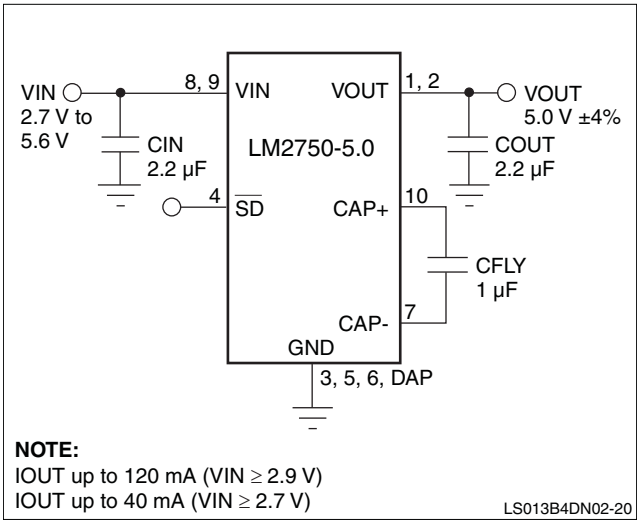

Figure 18. LM2750 Reference Circuit

HANDLING, STORAGE, AND PACKAGING

1. This module is not made to be disassembled. Doing so may cause permanent damage.
2. The liquid crystal material in this module is injurious to humans. Do not allow it to get into the eyes or mouth. If any liquid crystal material gets on skin or clothing, immediately wash it out with soap and water.
3. This module is RoHS compliant, and does not use any ODS (1,1,1-Trichloroethane, CCL4) in its materials or in its production processes.
4. When discarding this module, dispose of it as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal cell contains an extremely small amount of liquid crystal (approx.100 mg) and therefore will not leak; even if the panel should break.
5. The material used in this panel has a median lethal dose (LD50) of greater than 2,000 mg/kg and tests negative (Aims test) for mutagenic properties.

Storage

1. Store these devices at a temperature range between 0°C and 40°C, at 60% RH or less.
2. Use within 3 months.
3. Open the package within an area that has proper static control precautions, and more than 50% RH.
4. When storing this module, keep it from long periods of exposure to direct sunlight or other sources of ultraviolet light. Recommended storage is in a dark place.

Packaging

Figure 19 shows the serial number schema.

Figure 20 shows the location where the serial number is printed.

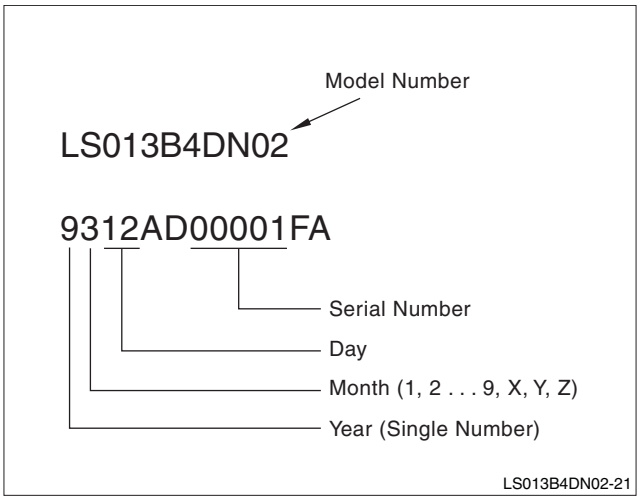

Figure 19. Serial Number

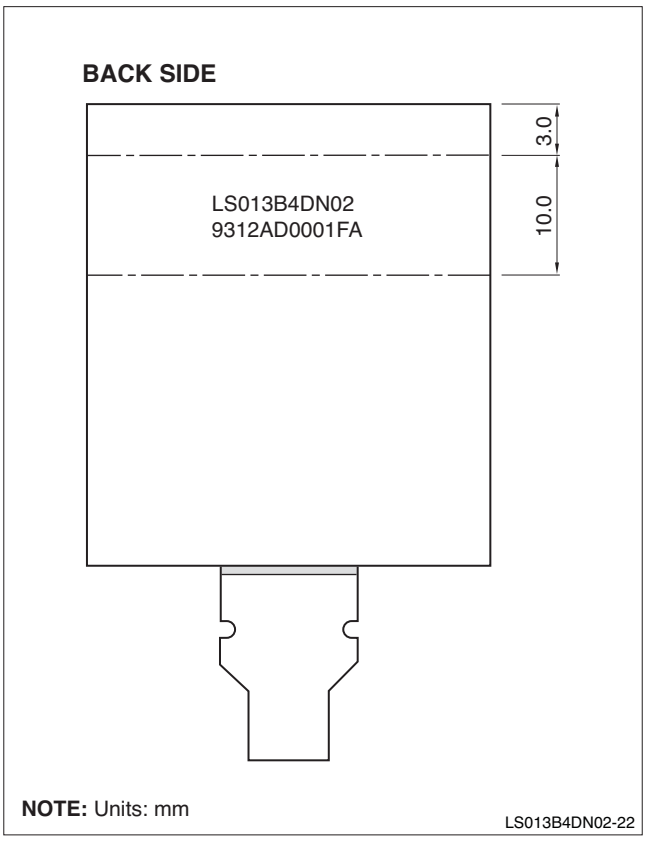

Figure 20. Serial Number Location

Packaging Diagrams

Stack no more than 12 cartons high. Product is packed in lots of 800.

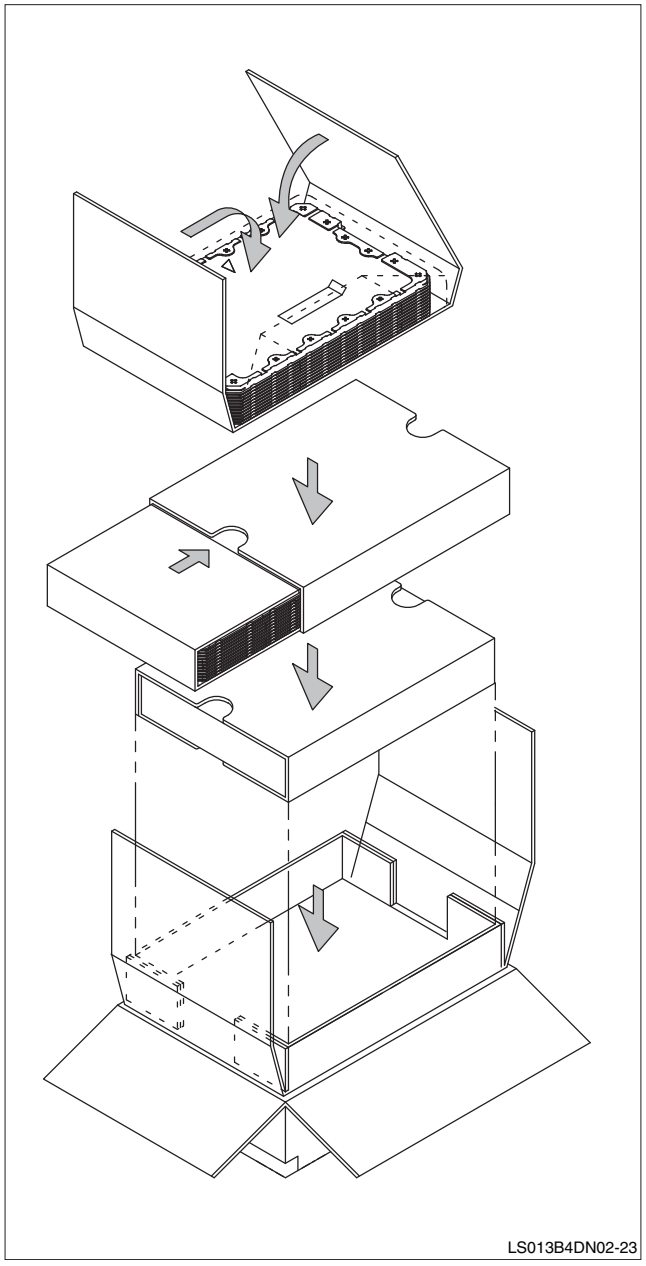

Figure 21. Packaging Format

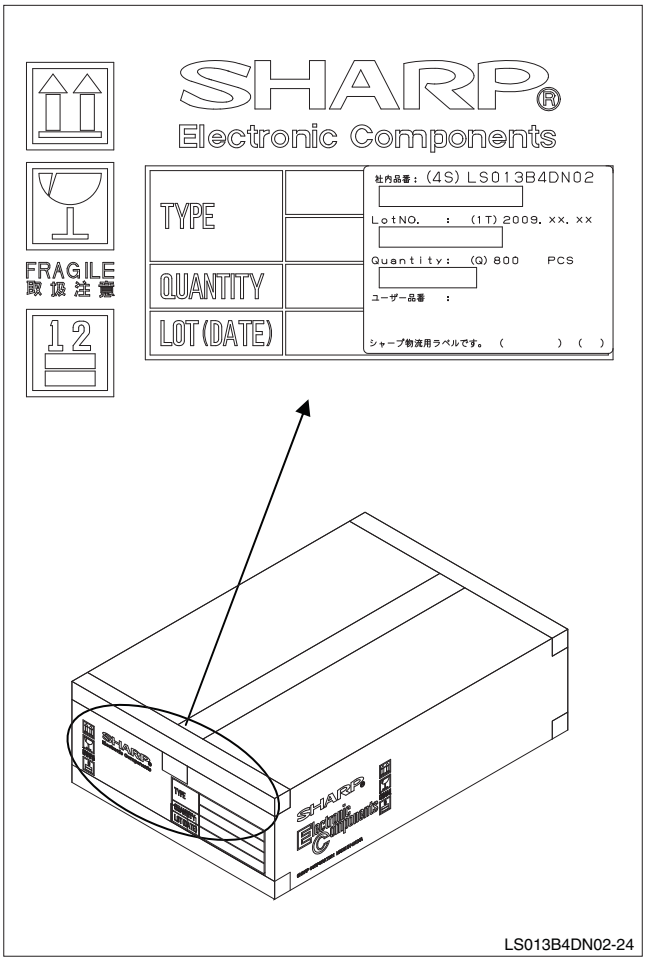

Figure 22. Package Labeling

RELIABILITY

Environmental Reliability

Table 5. Test Item Reliability

NO.	TEST ITEM	TEST CONDITION
1	High temperature storage test	Ta = 80°C, 240h
2	Low temperature storage test	Ta = 35°C, 240h
3	High temperature and high humidity operating test	Tp = 40°C/95% RH, 240h
4	High temperature operating test	Tp = 70°C, 240h
5	Low temperature operating test	Tp = -20°C, 240h
6	Shock test (non-operating)	Ta = -30°C (1h) to +80°C (1h) / 5 cycles
7	Electrostatic discharge test	±200 V, 200 pF (0 Ω) once per terminal

NOTES:
1. Ta = ambient temperature, Tp = panel temperature
2. Check for any items which impair display function.

Physical Reliability

The Panel surface stress specification parameter is the stress force [N] before image failure.

Load test: Minimum 120[N]; on an LCD panel with UV protection film, fixed to a test stage.

Pressure point is the center of the panel, with a φ10 mm column, at 1 mm/minute.

Full pressure is held for 5 seconds after achievement, then released.

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

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