

### Application Information for Sharp's LS044Q4DH01 Memory LCD

*Sharp Microelectronics of the Americas*

#### INTRODUCTION

This Application Note provides additional design assistance for Sharp's LS044Q4DH01 Memory LCD. This module is a reflective, active-matrix QVGA liquid crystal module utilizing Sharp's CG-silicon thin-film transistor process. It offers high performance and power efficiency for compact display applications, with a serial interface for simple integration.

Subjects covered will be:

- Mechanical Specifications, including dimension drawings and connector specifications
- Absolute Maximum Ratings
- Optical Specifications, including view angles, reflectivity, contrast, and risetime
- Electrical Characteristics, including interfacing and signal timing information
- Design Notes
- Manufacturing Information, including handling and storage
- Reliability Information

This Note is based on Sharp's document number LCP-2110039 and is designed to provide supplementary information for the Specifications for this part.

Always refer to the latest Specifications when designing with these devices.



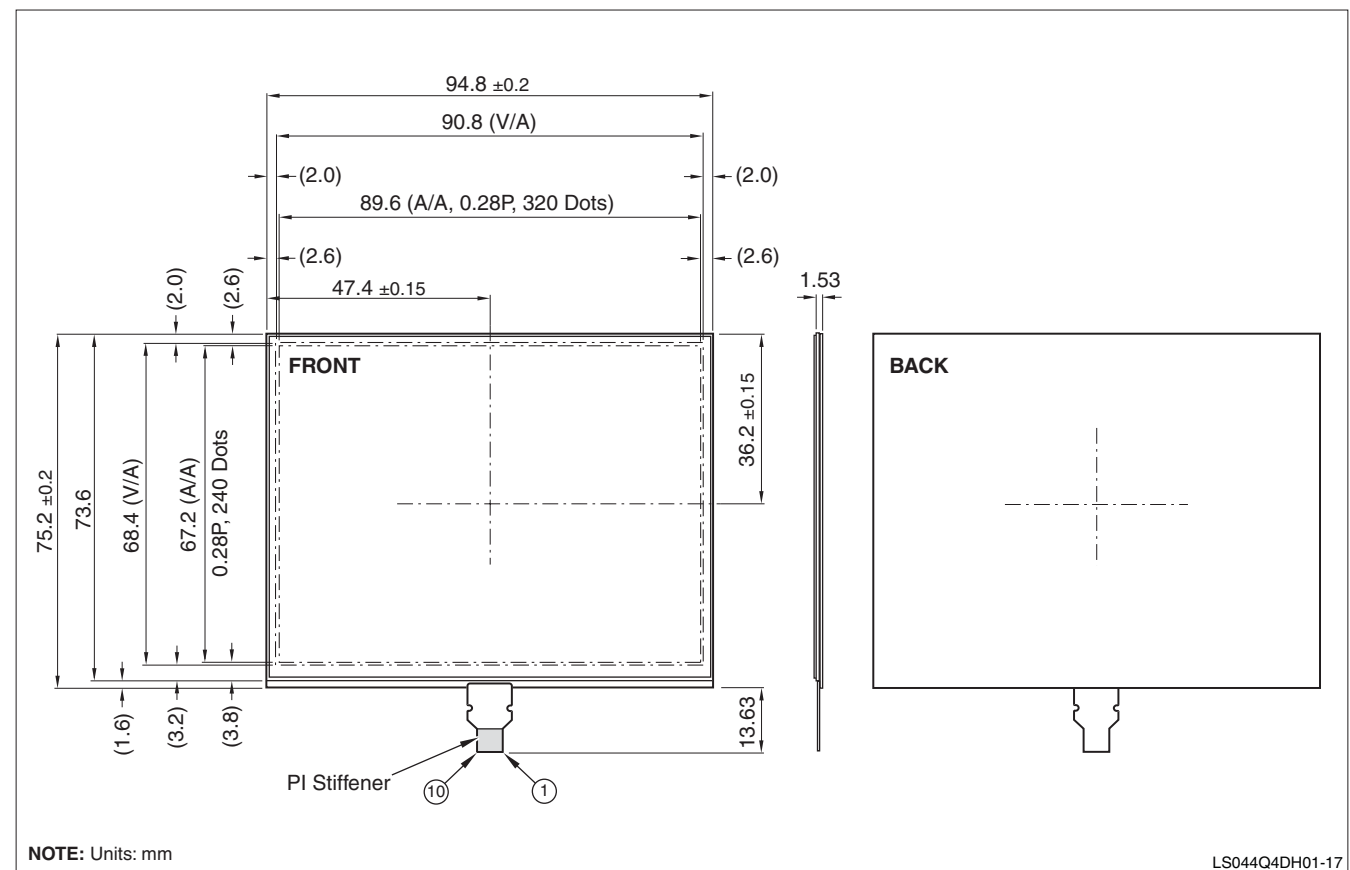
#### FEATURES

- Highly Reflective Thin-film-transistor (HR-TFT) monochrome panel
- QVGA Resolution (320 × 240)
- Serial interface for display control
- Screen data is arbitrarily renewable by line
- Built-in, 1-bit internal memory for data storage
- Super low power consumption TFT panel
- Attached FPC connector
- RoHS compliant

## MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATION	UNIT
Screen Size	4.4	Inch
Viewing Area	89.6 (H) × 67.2 (V)	mm
Dot Configuration (Square panel)	320 (H) × 240 (V)	Dots
Dot Pitch	0.280 (H) × 0.280 (V)	mm
Pixel Array	Stripe Array	-
External Dimensions	94.8 (W) × 75.2 (H) × 1.53 (D)	mm
Mass	26 (approx.)	g
Surface Hardness	3H or more	Pencil hardness

## External Dimensions



## Connector Specifications

Table 1. Input Terminals and Functions

TERMINAL	SYMBOL	I/O	FUNCTION	NOTES
1	SCLK	INPUT	Serial clock signal	
2	SI	INPUT	Serial data input signal	
3	SCS	INPUT	Chip select signal	
4	EXTCOMIN	INPUT	External COM inversion signal input (H: enable)	1
5	DISP	INPUT	Display ON/OFF signal	2
6	VDDA	POWER	Power supply (Analog)	
7	VDD	POWER	Power supply (Digital)	
8	EXTMODE	INPUT	COM inversion select terminal	3
9	VSS	GND	GND (Digital)	
10	VSSA	GND	GND (Analog)	

### NOTES:

1. EXTCOMIN is HIGH enabled. When LOW, the serial input flag is enabled. See Figure 14 and Figure 15 for recommended circuits.
2. DISP enables/disables the display. All pixels will revert to Normal mode (reflective) when LOW. When DISP = H, data in the pixel memories displays normally.
3. EXTMODE pin must be connected to VDD for HIGH, and to VSS for LOW. See Figure 17 in *Interfacing and Signals*.

## Connector Bending Specifications

The connector is made to be bent underneath the module with a radius of not less than 0.45 mm. Do not allow the connector to be in contact with the glass, or the glass edge, in the final design. Do not allow the connector to be bent in the reverse direction (toward the front of the module) or allow any stress or force to be applied to the connector through pulling it or hanging the module by the connector.

The recommended bending area is 0.8 to 6.0 mm from the glass edge. See Figure 1 for guidance.

## Recommended Connector

SMK Top Contact: FP-12 series; CFP-4510-0150F

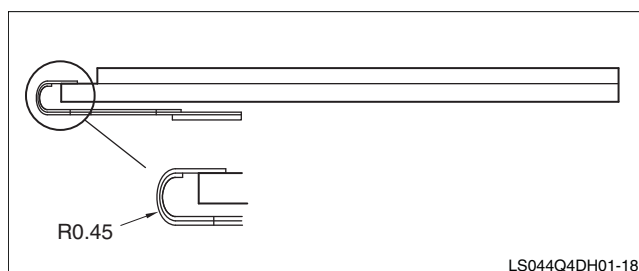


Figure 1. Connector Bending

## Absolute Maximum Ratings

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTES
Power Supply Voltage	Analog	VDDA	-0.3	+5.8	V	
	Logic	VDD	-0.3	+5.8	V	1
Input Signal Voltage (HIGH)				VDD	V	2
Input Signal Voltage (LOW)			-0.3		V	
Storage Temperature		Tstg	-30	+80	°C	3
Operating Temperature (at panel surface)		Topr1	-20	+70	°C	4

### NOTES:

1. Applies to EXTMODE.
2. Applies to SCLK, SI, SCS, DISP, EXTCOMIN.
3. Do not exceed this temperature in any part of the module.
4. Maximum wet bulb temperature is 57°C or lower. No condensation is allowed. Condensation will cause electrical leakage and may cause the module to fail to meet this Specification.
5. "Operating Temperature" is the guaranteed temperature limits for operation.
6. For contrast, response time, and other display quality determinations, use Ta = +25°C.

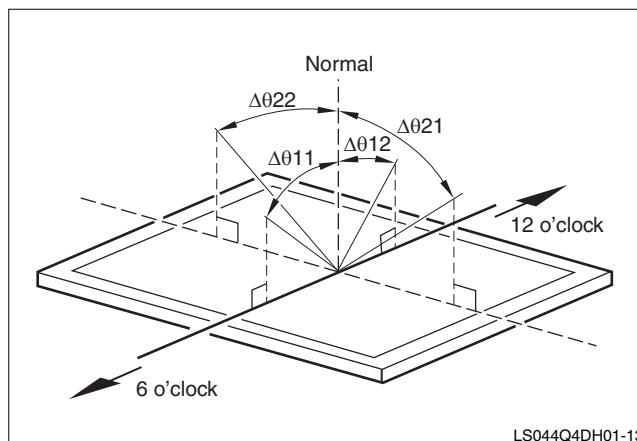
## OPTICAL SPECIFICATIONS

Ta = 25°C

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Viewing Angle CR ≥ 5	H	θ21, θ22	55			° (degrees)	1
	V	θ11	55			° (degrees)	1
		θ12	55			° (degrees)	1
Contrast Ratio		CR		(14)			2
Reflectivity Ratio		R		(17.5)		%	2
Response Time	Rise	τr		10		ms	3
	Fall	τf		20		ms	3
Chromaticity	White	x		0.307			2
		y		0.330			2

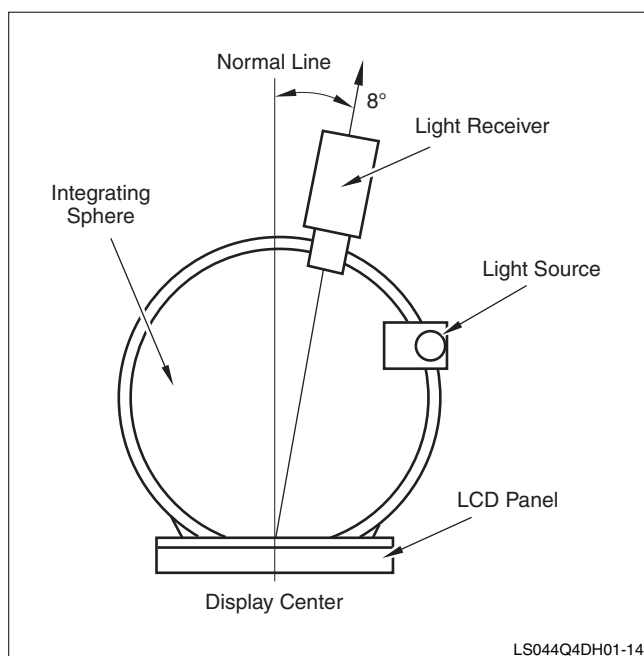
### NOTES:

1. Viewing Angle is described as clock positions: θ12 = 12 o'clock, θ11 = 6 o'clock, θ21 = 3 o'clock, θ22 = 9 o'clock. See Figure 2.
2. Contrast Ratio, Reflectivity Ratio, and Chromaticity are measured through the use of an integrating sphere. See Figure 3.
3. Response Time is measured by the change interval in an optical receiver when the test panel's signal is transitioned from white to black to white. See Figure 4 for the measurement setup and Figure 5 for the output waveshape. Measurements are conducted in a dark room or equivalent space.

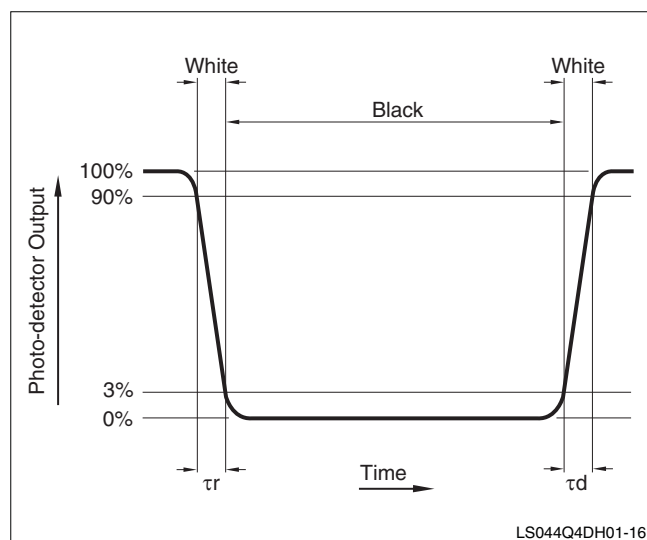


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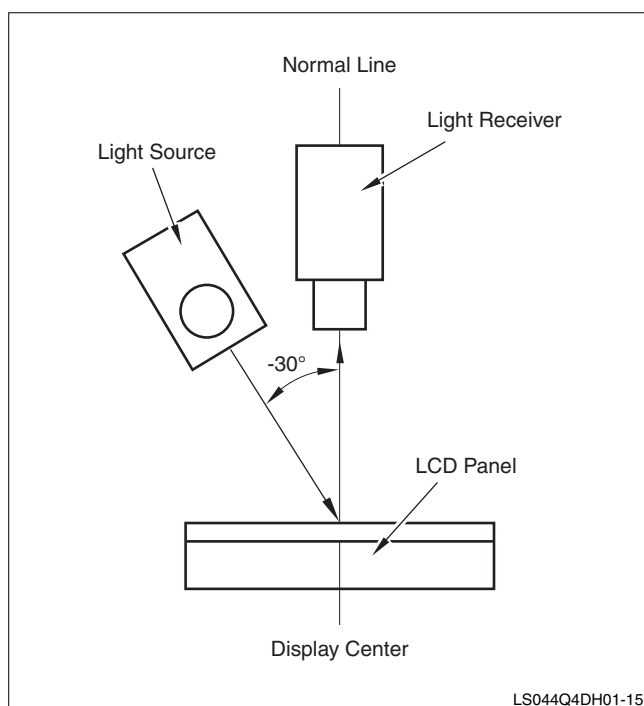
Figure 2. Viewing Angle



**Figure 3. Setup for Contrast, Reflection Ratio, and Chromaticity**



**Figure 5. Response Time**



**Figure 4. Setup for Response Time**

## ELECTRICAL SPECIFICATIONS

Here are the Recommended Operating Conditions for this module, with VSS (GND) = 0V and Ta = 25°C.

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Power supply	Analog	VDDA	+4.8	+5.0	+5.5	V	
	Logic	VDD	+4.8	+5.0	+5.5	V	1
Input signal voltage	HIGH	VIH	+2.70	+3.0	VDD	V	2
	LOW	VIL	VSS	VSS	VSS + 0.15	V	2

### NOTES:

1. EXTMODE = H
2. Functional below VDD; however 3.0V is recommended. Applies to SCLK, SI, SCS, DISP, EXTCOMIN

## Power Consumption

This module has the ability to shut down most of its logic circuits when in Static mode (not being updated). It has two levels of power consumption: Static and Dynamic Display.

Static Display: 250  $\mu$ W (TYP.); Vertical stripe display; fully static, no display updates.

- This includes a 1 Hz VCOM toggle, and VDD = 5 V, VDDA = 5 V,  $f_{SCLK}$  = 1 MHz,  $f_{SCS}$  = 1 Hz

Dynamic Display: 650  $\mu$ W (TYP.); Vertical stripe display; updated at a 1 Hz rate.

- VDD = 5 V, VDDA = 5 V,  $f_{SCLK}$  = 1 MHz,  $f_{SCS}$  = 1 Hz

These numbers represent average power, not peak power usage when driving VCOM. Always allow for a margin in power supply design.

## Decoupling Capacitors

Use of a decoupling capacitor on VDD and VDDA is recommended, even when the two supplies are tied together. See Figure 6.

Values for these capacitors:

C1: DISP to VSS: rank B, 0.1  $\mu$ F Ceramic

C2: VDDA to VSS: rank B, 1  $\mu$ F Ceramic

C3: VDD to VSS: rank B, 1  $\mu$ F Ceramic

These are recommended values; actual values should be determined by the final design. Always place the decoupling capacitors as close as possible to the part as the impedance of the VDD and VSS lines is low when the module is operating.

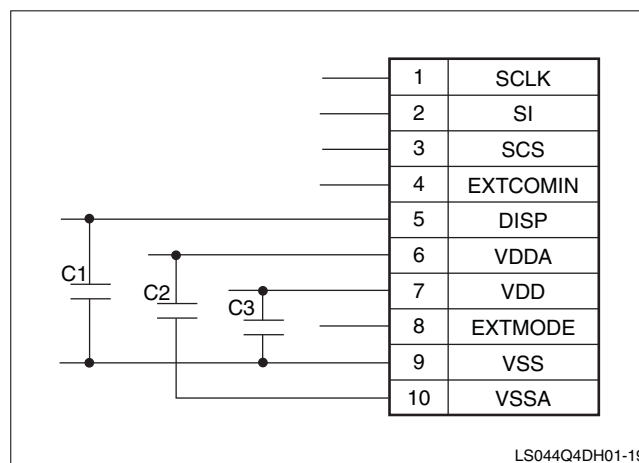


Figure 6. Decoupling Capacitors

## Power Supply Sequencing

This device requires proper supply sequencing on both startup and shutdown to prevent latching of the logic circuits. Refer to Figure 7.

### POWER-UP

VDD and VDDA must rise together or VDD must rise faster than VDDA.

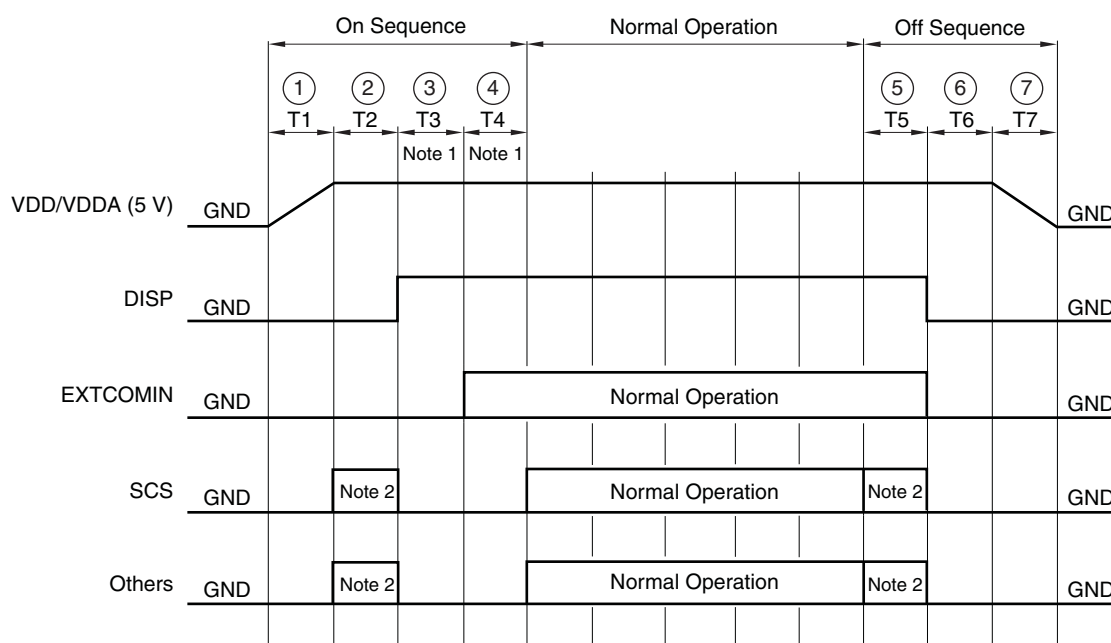
- 5 V rises to nominal
- Initialize pixel memory: send D2 CLEAR ALL flag or set the display to all-white (requires >1 V)

- Latch cancellation for TCOM; requires a period to cancel the COM latch circuit by DISP = HIGH (requires > 100  $\mu$ S). See T3 in Figure 7.
- TCOM polarity initialization by EXTCOMIN (requires > 100  $\mu$ S). See T4 in Figure 7.

### POWER-DOWN

VDD and VDDA must fall together or VDDA must fall faster than VDD.

- Initialize pixel memory (Same as T2 in Figure 7)
- Initialize VA, VB, and VCOM (See T6 in Figure 7)
- 5 V falls



#### NOTES:

1. The order of ③ and ④ can be reversed, in this case, VCOM polarity inversion timing controlled by EXTCOMIN (doesn't work during DISP = 'L').
2. Setup value for initialization of pixel memory data.
3. Precautions at power on and power off.

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Figure 7. Power Supply Sequencing

## SIGNAL DESCRIPTIONS

Input signal characteristics are given in Table 2 and Table 3; refer to Figure 8 for timing diagrams.

All measurements are at  $V_{DDA} = +5.0\text{ V}$ ,  
 $V_{DD} = +5.0\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_a = 25^\circ\text{C}$ .

**Table 2. Signal Frequencies**

PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
$f_{SCS}$	Frame frequency	1		20	Hz
$f_{SCLK}$	Clock frequency		1	2	MHz
tV	Vertical Interval	50.0		1000	ms
$f_{COM}$	COM Frequency	0.5		10	Hz

**Table 3. Signal Transition Times**

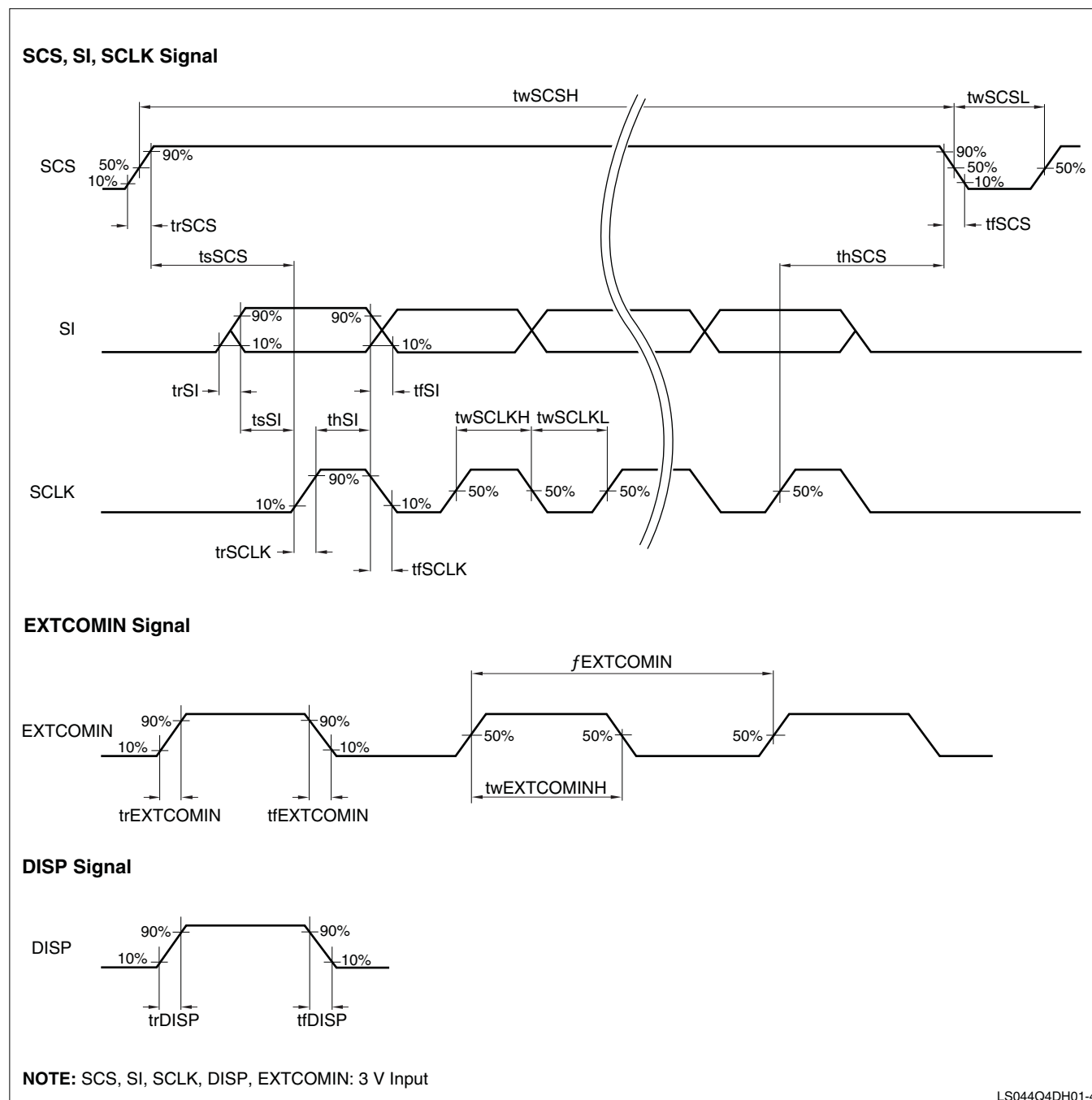
PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTES
trSCS	SCS Risettime			50	ns	
tfSCS	SCS Falltime			50	ns	
twSCSH	SCS HIGH Duration	180			$\mu\text{s}$	1
		12			$\mu\text{s}$	2
twSCSL	SCS LOW Duration	1			$\mu\text{s}$	
tsSCS	SCS setup time	3			$\mu\text{s}$	
thSCS	SCS hold time	1			$\mu\text{s}$	
trSI	SI Risettime			50	ns	
tfSI	SI Falltime			50	ns	
tsSI	SI setup time	120			ns	
thSI	SI hold time	190			ns	
trSCLK	SCLK Risettime			50	ns	
tfSCLK	SCLK Falltime			50	ns	
twSCLKH	SCLK HIGH duration	200	450		ns	
twSCLKL	SCLK LOW duration	200	450		ns	
$f_{EXTCOMIN}$	EXTCOMIN frequency	1		20	Hz	3
trEXTCOMIN	EXTCOMIN Risettime			50	ns	
tfEXTCOMIN	EXTCOMIN Falltime			50	ns	
thIEXTCOMIN	EXTCOMIN HIGH duration	1			$\mu\text{s}$	
trDISP	DISP Risettime			50	ns	
tfDISP	DISP Falltime			50	ns	

### NOTES:

1. Dynamic Mode (continuously updating display)
2. Static Mode (no display updating)
3.  $f_{EXTCOMIN}$  must always be less than  $f_{SCS}$  (Table 2)



## Timing Diagrams



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Figure 8. SCS, SI, SCLK, EXTCOMIN, and DISP Signals

## PROGRAMMING

For software commands, see the Application Note, *Programming Sharp's Memory LCDs*, by Ken Green.

In all the following diagrams and descriptions, these conventions are used:

- **M0: MODE**  
When M0 is 'H', the module enters Dynamic Mode, where pixel data will be updated.  
When M0 is 'L' the module remains in Static Mode, where pixel data is retained.
- **M1: VCOM**  
This polarity-inversion flag enables a periodic polarity inversion on the panel to keep a latent charge from building up within the Liquid Crystal cells. When M1 is 'H' then VCOM = 'H' is output. If M1 is 'L' then VCOM = 'L' is output.  
When EXTMODE = 'H', M1 value = XX (don't care). See *COM Inversion and Signal Selection*.
- **M2: CLEAR ALL**  
When M2 is 'L' then all flags are cleared. When a full display clearing is required, refer to *CLEAR ALL*.
- **D1 - D240: Display data**  
Setting D(n) = 'L' sets that pixel to black. Conversely, Setting D(n) = 'H' sets that pixel to white.
- **DUMMY DATA: Dummy data**  
Dummy data is typically 'XX' (don't care); however Sharp recommends setting bits to 'L'.

## Data Addressing and Positions

This part uses mixed addressing for columns and lines. Columns (X direction) are addressed using an 8-bit binary scheme, and lines (Y direction) are addressed directly as 240 bits. One line is the minimum addressable unit in the display; even if only one pixel in the line is to be updated, the entire line must be sent.

## Dynamic Mode

For software commands, see Sharp's Application Note, *Programming Sharp's Memory LCDs*, by Ken Green.

### MULTIPLE LINE WRITE

Dynamic Mode assumes the updating of at least one line in the display. During the Data Write period, data is stored in the panel's binary latch. During Data Transfer, the data from the latch is written to the panel memory, line-by-line. During the write to panel memory, data for the next line is latched.

Dynamic Mode is entered by sending M0 = H and M2 = L.

Figure 10 shows an example of writing multiple lines.

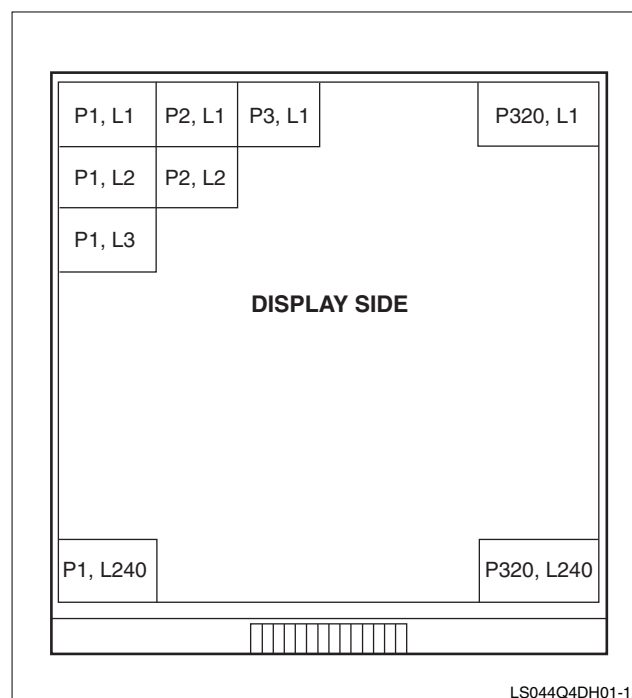


Figure 9. Display Data Position

Table 4. Column (X direction) Addressing

LINE ADDRESS	COLUMN ADDRESS							
	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7
L1	H	L	L	L	L	L	L	L
L2	L	H	L	L	L	L	L	L
L3	H	H	L	L	L	L	L	L
:	:	:	:	:	:	:	:	:
L238	L	H	H	H	L	H	H	H
L239	H	H	H	H	L	H	H	H
L240	L	L	L	L	H	H	H	H

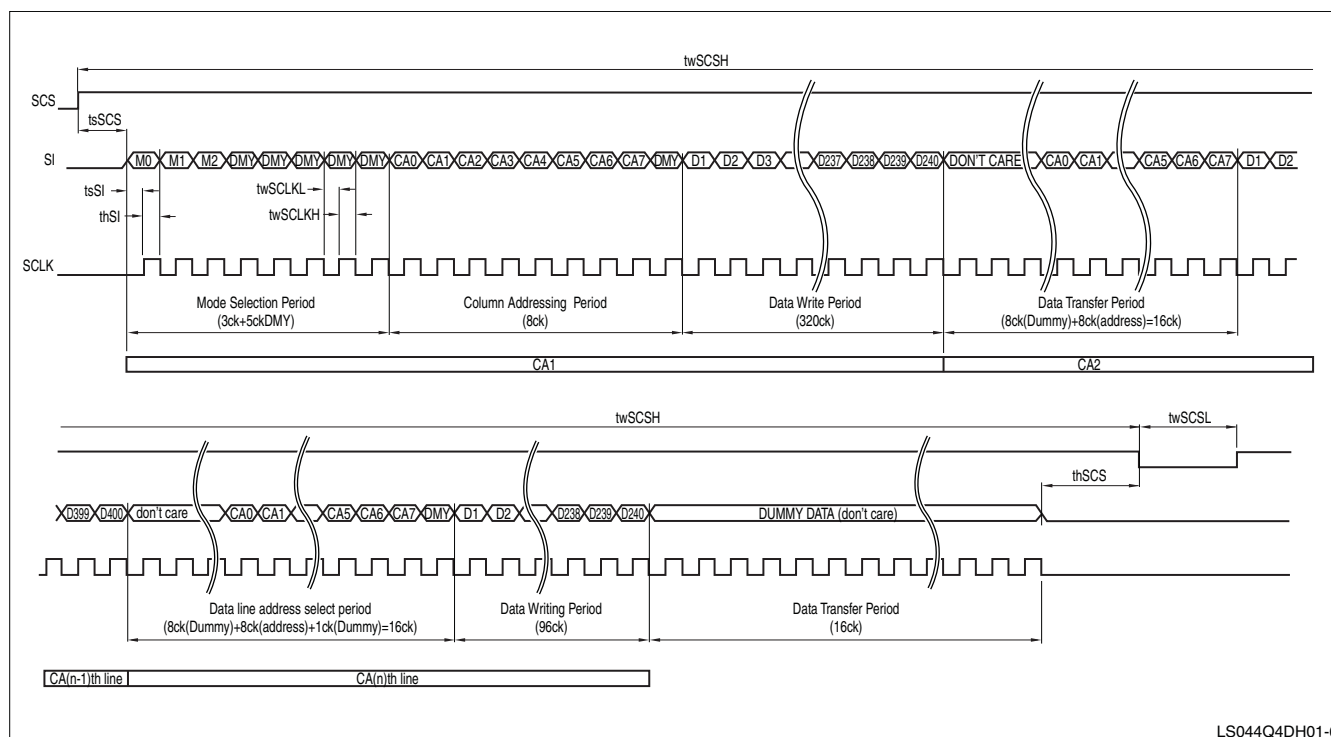


Figure 10. Dynamic Mode Timing Diagram, Writing Multiple Lines

### SINGLE LINE WRITE

Writing a single line of data is much the same as writing multiple lines. During the Data Write period, data is stored in the panel's binary latch. During Data Transfer, the data from the latch is written to the panel memory, line-by-line. During the write to panel memory, data for the next line is latched.

Dynamic Mode is entered the same way, by sending  $M0 = H$  and  $M2 = L$ .

Figure 11 shows an example of writing a single line.

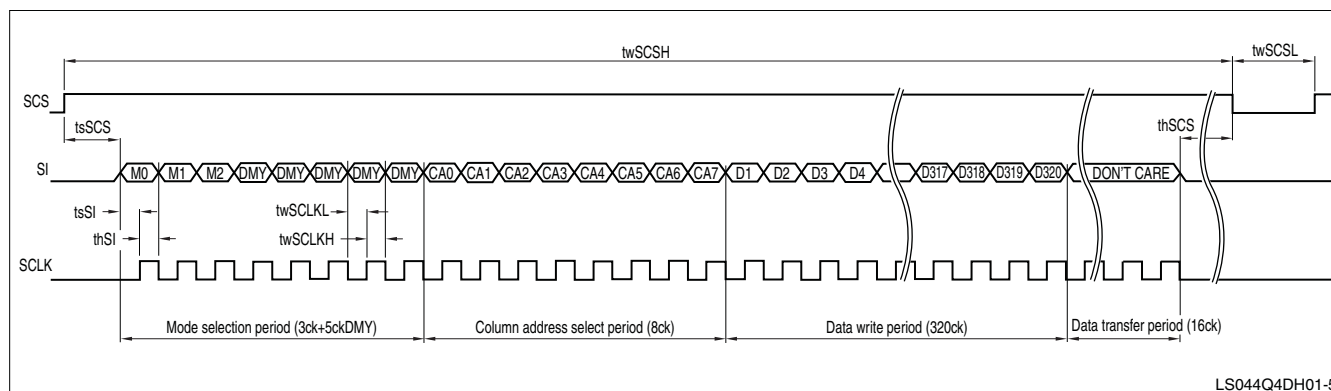


Figure 11. Dynamic Mode Timing Diagram, Writing a Single Line

## Static Mode

Static Mode is the module's lowest-power mode, with data latches and other circuitry powered down. Static Mode can be held indefinitely; as long as the panel has power and VCOM is toggled periodically.

Sharp recommends keeping maximum time between VCOM toggles to no more than one second, and refreshing data every two hours, to prevent stuck pixels.

Static Mode is entered by sending  $M0 = L$  and  $M2 = L$ .

## CLEAR ALL

CLEAR ALL will clear all data from pixel memories and the display will revert to its normal white color.

CLEAR ALL is invoked by sending  $M0 = L$  and  $M2 = H$ .

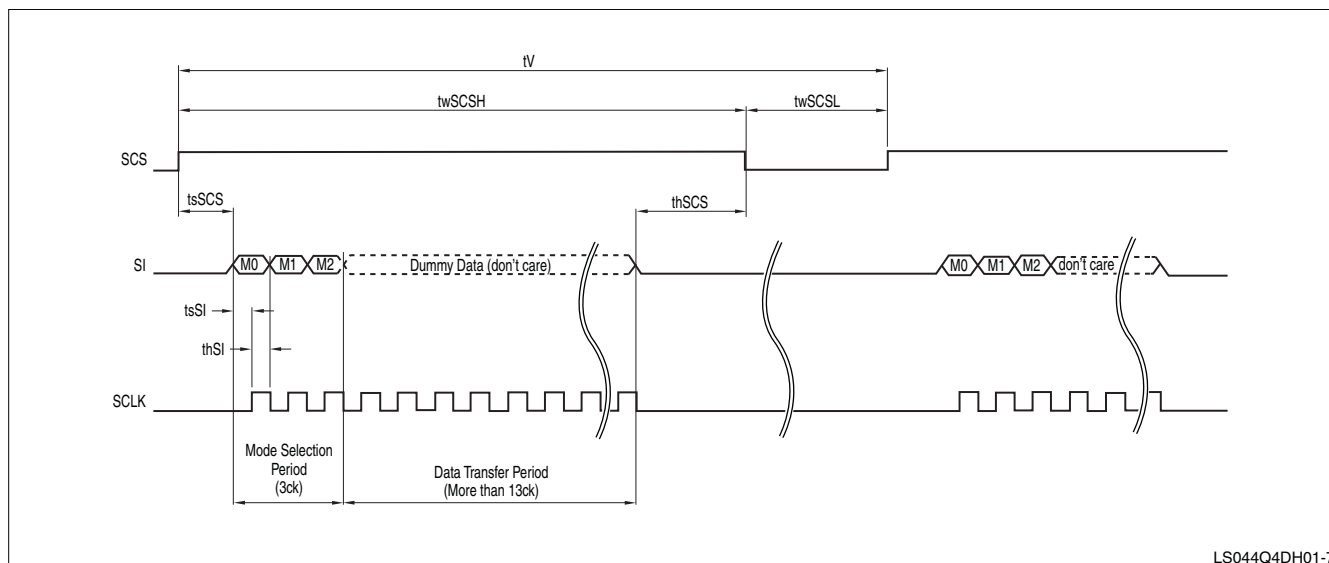


Figure 12. Static Mode Timing Diagram

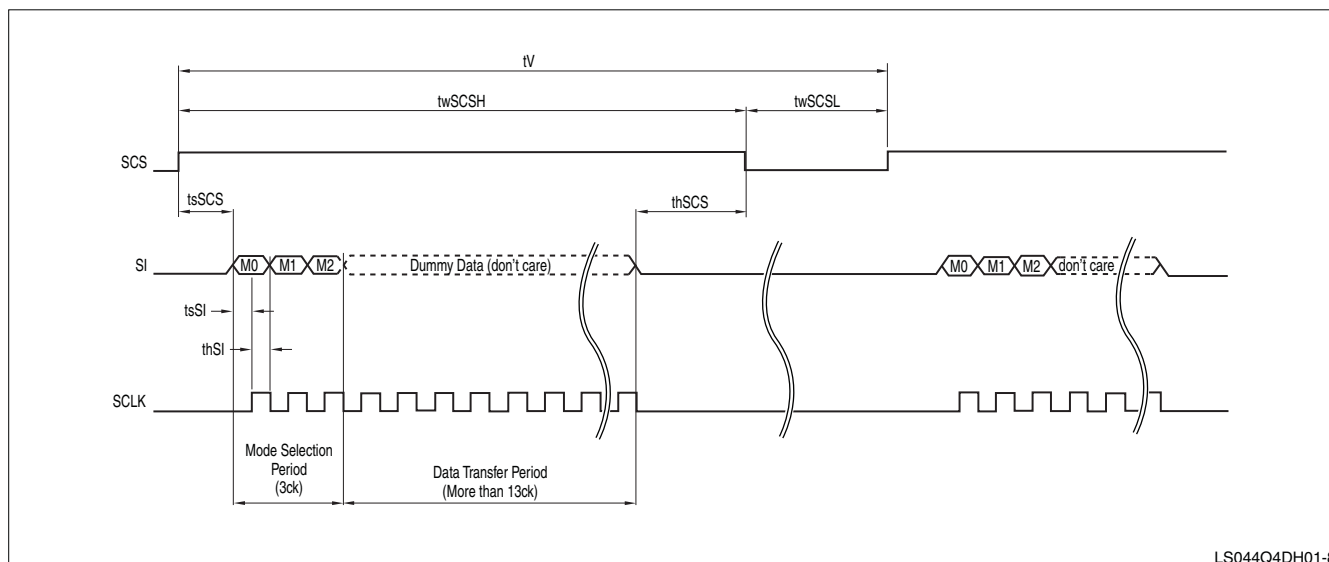


Figure 13. CLEAR ALL Timing Diagram

## VCOM Inversion

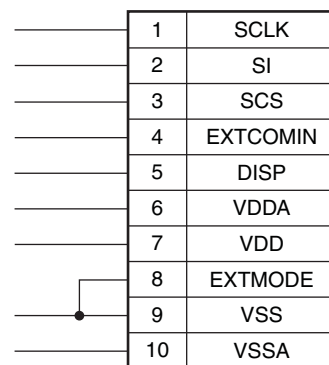
Periodic VCOM inversion impresses a periodic polarity inversion across the panel to keep a latent charge from building up within the Liquid Crystal cell. It can be implemented either through software or through hardware. In either implementation, the positive and negative inversion intervals should be kept as equal as possible, and intervals should not exceed one second.

To implement VCOM inversion in software, the M1 bit is periodically toggled. When M1 is 'H' then VCOM = 'H' is output to the panel. If M1 is 'L' then VCOM = 'L' is output to the panel. To set the panel for software toggling of M1, tie EXTMODE to VSS as shown in Figure 14.

When implementing a VCOM toggle through hardware, EXTMODE is set to 'H', and the M1 value becomes XX (don't care). Hardware then toggles EXTCOMIN, and the timing between toggles of this line sets the VCOM inversion interval. Figure 17 illustrates this action with a shorter duration SCS clock signal, and Figure 18 illustrates behavior under a longer duration SCS clock.

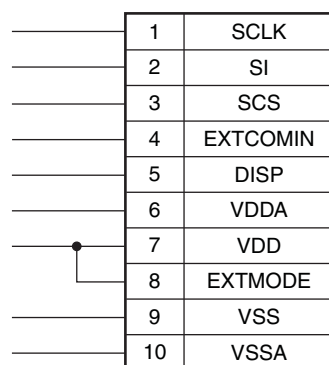
Therefore, it's important not to allow the toggling interval of EXTCOMIN to exceed one second. To set the panel for software toggling of M1, tie EXTMODE to VSS as shown in Figure 15.

The LC cell inversion polarity toggle is armed when EXTCOMIN rises. Internal signal COMZ toggles with each rise of EXTCOMIN, and latches the VCOM transition. The VCOM transition takes place upon the next clock transition of SCS. Again, it's best to keep the duty cycle of EXTCOMIN at 50%.



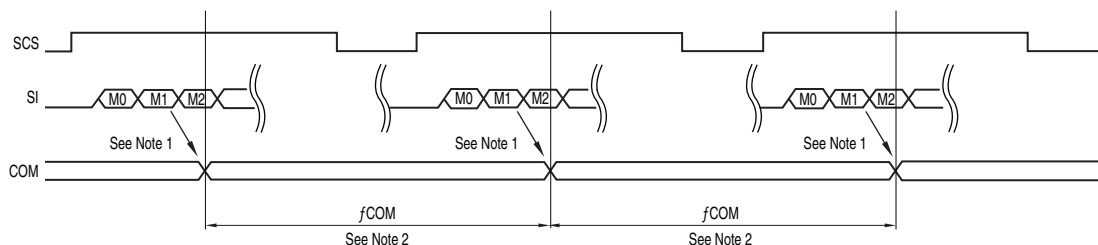
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Figure 14. VCOM Software Input



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Figure 15. VCOM Hardware Input

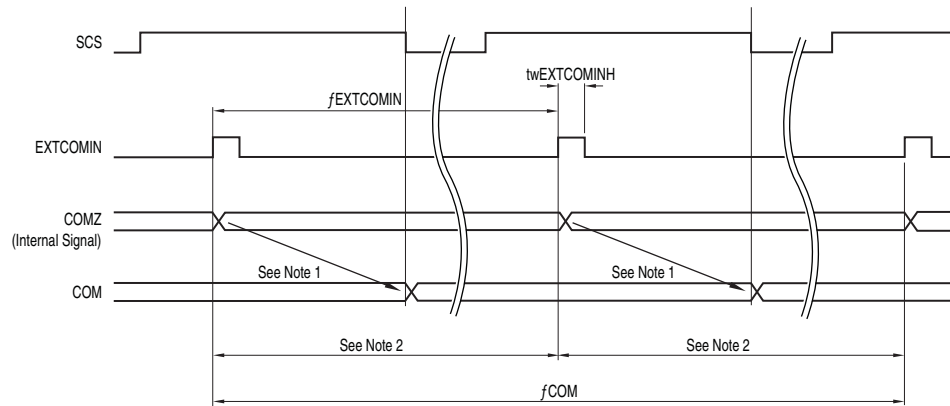


### NOTES:

1. LC inversion has been changed by M1 flag statement.
2. The periods of plus polarity and minus polarity should be the same length.

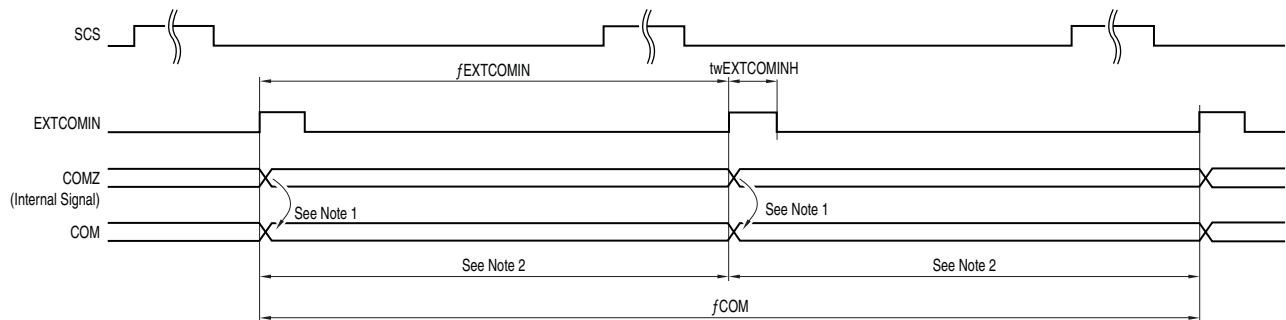
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Figure 16. EXTMODE = L, Software VCOM Toggle

**NOTES:**

1. LC inversion polarity has been latched by the rise time of EXTCOMIN in internal circuit block as COMZ signal.
2. The period of EXTCOMIN should be constant.

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**Figure 17. EXTMODE = H, Hardware VCOM Toggle Occuring When SCS = H****NOTES:**

1. LC inversion polarity has been latched by the rise time of EXTCOMIN.
2. The period of EXTCOMIN should be constant.

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**Figure 18. EXTMODE = H, Hardware VCOM Toggle Occuring When SCS = L**

## DESIGN NOTES

1. This device is static sensitive. Handle it only in a static-safe environment.
2. Do not press on the surface of the module, and do not stack modules in such a way that pressure will be applied to the surfaces or to the connector area. The safest place for temporary storage of modules is in their shipping tray.
3. The Specifications for this part and Application Note give definite environmental, electrical, and signal drive conditions for the operation of this module. Operating it outside of these given limits can reduce image quality, shorten its life, or cause it to fail altogether.
4. When displaying static images, Sharp recommends refreshing the image data every two hours to prevent stuck pixels.
5. Do not allow the gate driver area (the circuit areas outside of the LC glass) to be exposed to light in the final design. Shield this area.
6. Support for the module should be designed to avoid stress exceeding the maximums given in the Specifications.
7. Do not put a seal or adhesive materials on the glass surface. Picture uniformity defects can result.
8. Do not use chloroprene rubber in the design as it generates chlorine gas and can affect the reliability of the LCD module's connector areas.
9. The liquid crystal material in these modules will deteriorate from UV radiation. Do not store or operate the modules in direct sun or under strong UV radiation without some form of protection.
10. This part is shipped with a protective film over the front and rear of the module, to prevent scratches or other damage. Remove this film before use. Do not attempt to reattach this film once it has been removed. If the film is reattached and the LCD module is stored in this condition, the polarizer film may be affected enough to cause a picture quality failure.
11. Materials used in setting or epoxy resins (anime hardening agents) and silicon adhesives (dealcoholized or oxime) all release a gas which can affect the quality of the front and rear polarizer films. Always confirm compatibility with these materials.
12. The connector on this module is designed for a limited number of insertions. Do not attempt to solder directly to the connector.
13. The connector is made to be bent underneath the module with a radius of not less than 0.45 mm. Do not bend the connector in the reverse direction or apply force to the connector by pulling it or hanging the module by the connector.
14. These modules may exhibit some change in perceived black levels as the source, quality, and angle of illumination changes.
15. Use of decoupling capacitors is recommended. See *Electrical Specifications*.
16. Keeping the bus controller as close as possible to

the module is recommended as power supply impedance drops during operation.

17. This device can be powered from a 3 V system with these power supply ICs: (See *Power Supply Reference Circuits* for more information.)

- SII: S-8821 Charge Pump Power Supply IC
- National Semiconductor: LM2750 Charge Pump Power Supply IC

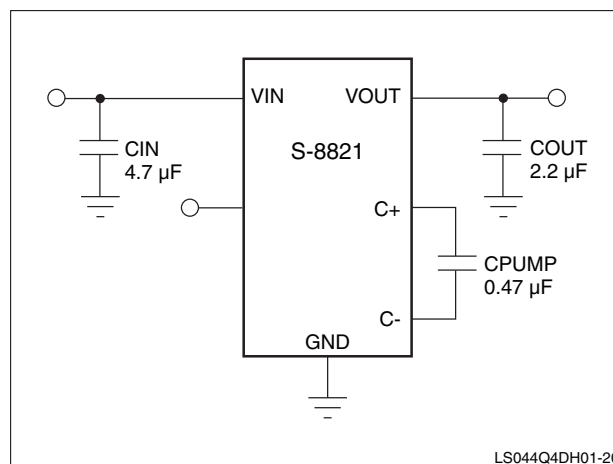
**Table 18. Electrical Specifications for 3 V Step-up Power Supply ICs**

PART #	V IN (V)			V OUT (V)		I OUT (mA)
	MIN.	MAX.	MIN.	TYP.	MAX.	
S-8821	2.8	5.0	4.9	5.0	5.1	40
LM2750	2.7	5.6	4.8	5.0	5.2	40

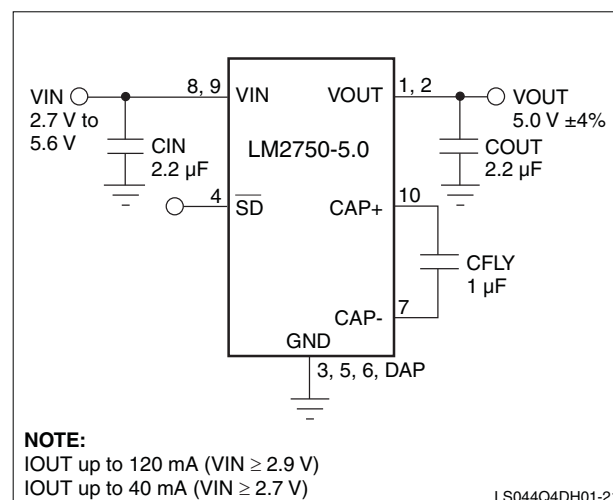
### NOTES:

1. Refer to each manufacturer's specifications for more information.
2. This information is for reference. Evaluate the parts in actual use.

## POWER SUPPLY REFERENCE CIRCUITS



**Figure 19. S-8821 Reference Circuit**



**Figure 20. LM2750 Reference Circuit**

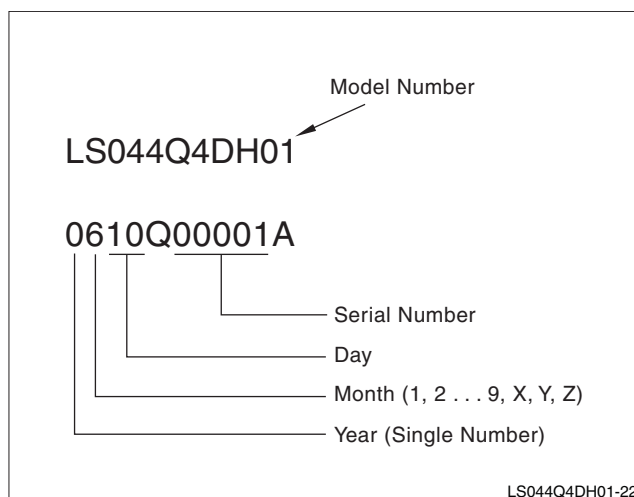
## HANDLING, STORAGE, AND PACKAGING

1. This module is not made to be disassembled. Doing so may cause permanent damage.
2. Handle modules with care as glass is used in the modules. Impacts to corners and sides should be avoided as they can cause cracks or chips. The edges of these modules may also be very sharp as they are glass.
3. The liquid crystal material in this module is injurious to humans. Do not allow it to get into the eyes or mouth. If any liquid crystal material gets on skin or clothing, immediately wash it out with soap and water.
4. The polarizer films on the front and back surfaces of this module are susceptible to damage from scratches or by allowing water to stand on the surface of the module. Any water on the surface must be immediately removed as it can cause defects or color changes if allowed to remain for long periods.
5. To clean the glass surface of the module, wipe it with absorbent cotton or a soft cloth. If further cleaning is necessary, use isopropyl alcohol and wipe lightly on the surface of the module only. Do not use organic solvents which could damage the terminal area; this area uses organic materials. Do not touch the terminal area with unprotected hands. If cleaning the terminals is necessary, wipe them with a soft cloth or a cotton swab.
6. This module is RoHS compliant, and does not use any ODS (1,1,1-Trichloroethane, CCL4) in its materials or in its production processes.
7. When discarding this module, dispose of it as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal cell contains an extremely small amount of liquid crystal (approx. 100 mg) and therefore will not leak; even if the panel should break.
8. The material used in this panel has a median lethal dose (LD50) of greater than 2,000 mg/kg and tests negative (Aims test) for mutagenic properties.
5. When storing this module, keep it from long periods of exposure to direct sunlight or other sources of ultraviolet light. Recommended storage is in a dark place.

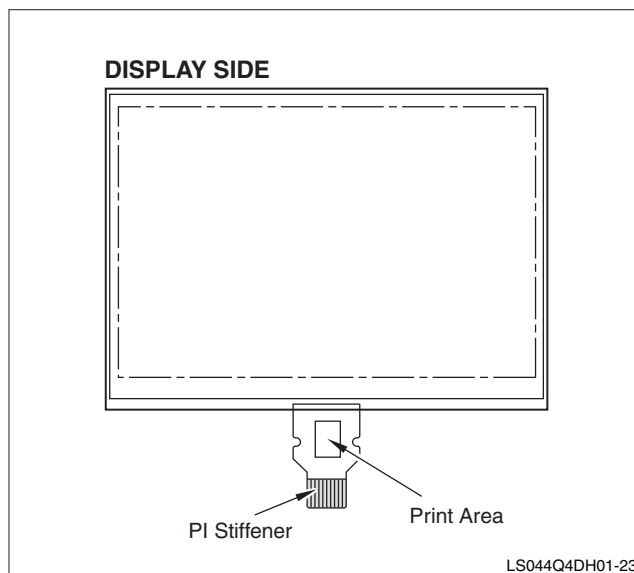
## Packaging

Figure 21 shows the serial number schema.

Figure 22 shows the location where the serial number is printed.



**Figure 21. Serial Number**



**Figure 22. Serial Number Location**

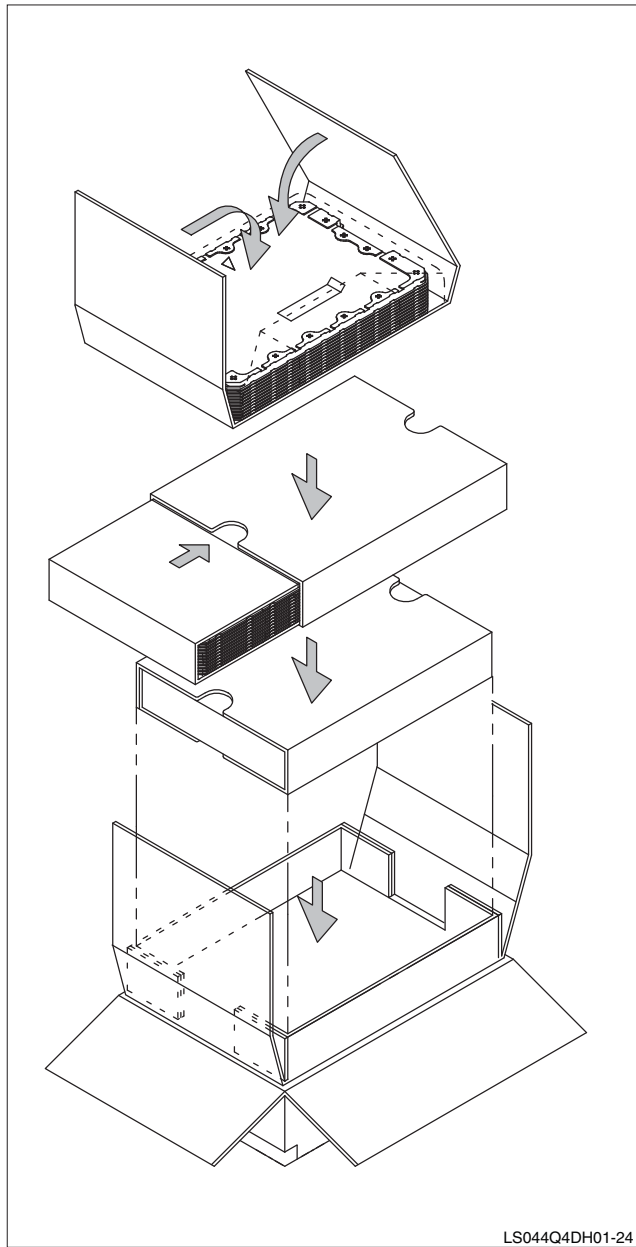
## Storage

1. Store these devices at a temperature range between 0°C and 40°C, at 60% RH or less.
2. Use within 3 months.
3. Open the package within an area that has proper static control precautions, and more than 50% RH.
4. The liquid crystal material in this module will solidify if stored below the rated temperature, and will become an isotropic liquid if stored above the rated storage temperatures. After such storage, the material may not return to its original properties.



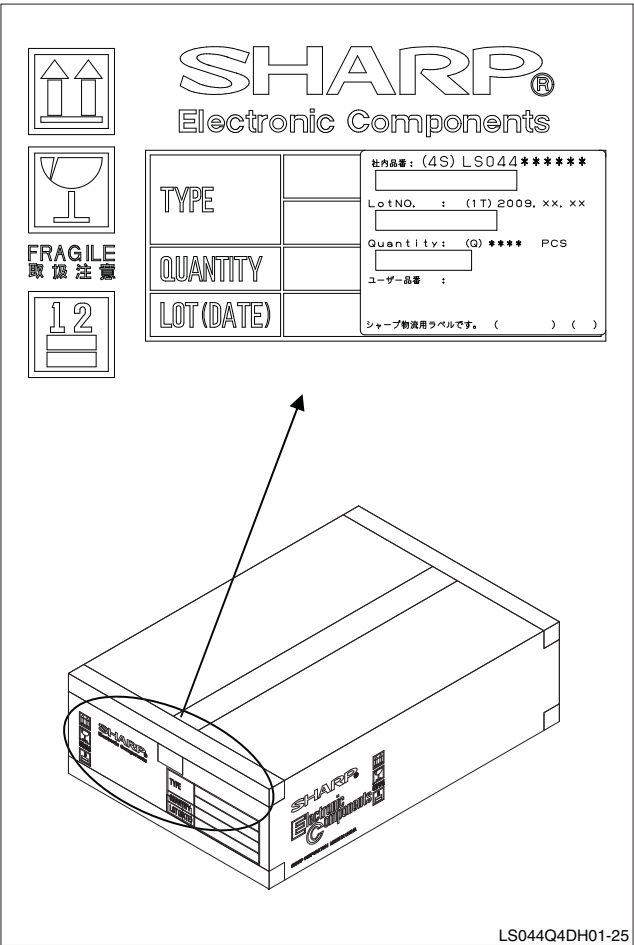
Packaging Diagrams

Stack no more than 12 cartons high. Product is packed in lots of 400.



LS044Q4DH01-24

Figure 23. Packaging Format



LS044Q4DH01-25

Figure 24. Package Labeling

## RELIABILITY

### Environmental Reliability

**Table 6. Test Item Reliability**

NO.	TEST ITEM	TEST CONDITION
1	High temperature storage test	Ta = 80°C, 240h
2	Low temperature storage test	Ta = 30°C, 240h
3	High temperature and high humidity operating test	Tp = 40°C/95% RH, 240h
4	High temperature operating test	Tp = 70°C, 240h
5	Low temperature operating test	Tp = -20°C, 240h
6	Shock test (non-operating)	Ta = -30°C (1h) to +80°C (1h) / 5 cycles
7	Electrostatic discharge test	±200 V, 200 pF (0 Ω) once per terminal

**NOTES:**

1. Ta = ambient temperature, Tp = panel temperature
2. Check for any items which impair display function.

### Physical Reliability

The Panel surface stress specification parameter is the stress force [N] before image failure.

Load test: Minimum 120[N]; on an LCD panel with polarizer film, fixed to a test stage.

Pressure point is the center of the panel, with a  $\phi 10$  mm column, at 1 mm/minute.

Full pressure is held for 5 seconds after achievement, then released.

**SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.**

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