PREPARED BY: DATE	SHARP	SPEC No. LCY-W-16405
		FILE No.
APPROVED BY: DATE	DISPLAY DEVICE BUSINESS GROUP SHARP CORPORATION	ISSUE May.5th.2016
		PAGE Pages 36
		APPLICABLE DIVISION DEVELOPMENT DEPT. I DESIGN CENTER I LCD DESIGN DEVELOPMENT DISPLAY DEVICE BUSINESS GROUP SHARP (CHINA) INVESTMENT CO.,LTD.

SPECIFICATION

DEVICE SPECIFICATION for
TFT LCD Module
(1536× RGB × 2560 dots)

Model No.

LS055R3SX01(G)

□CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED
BY _____

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[For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of thin glass, dropping the module or banging it against hard objects may cause cracks or fragmentation

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hurt polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ Floor

Floor is an important part to leak static electricity which is generated from human body or equipment.
There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure (electrostatic earth: $1\times10^{8}\Omega$) should be made.

④Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥Others

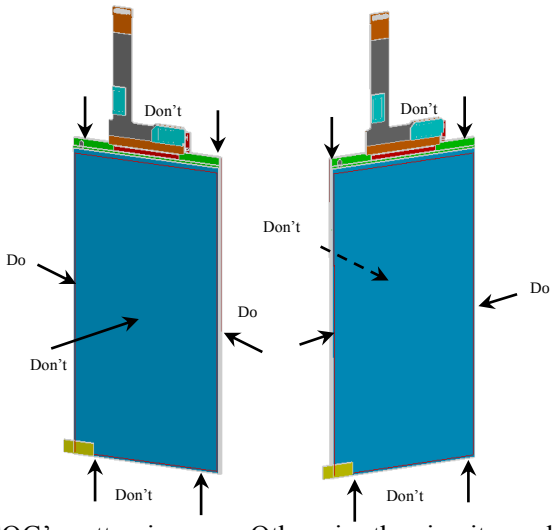
Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.



(15) Do not touch the COG's patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

(22) SHARP strongly recommend to use OCA as glue between LCD and tough window in case of direct bonding. If the customer use liquid glue as UV resin by direct bonding, it can easily cause chemical crack on polarizer film layers.

(23) LCD module is structurally very thin, therefore, please sustain the surface of polarizer.

(WE recommend touch panel to be directly adhered by OCA tape.)

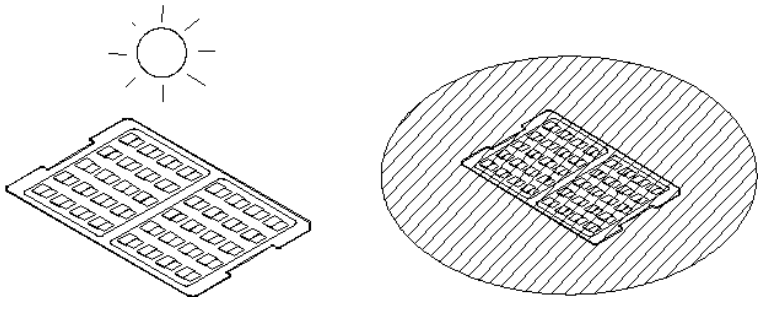
[For operating LCD module]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.
(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

[Precautions for Storage]

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.
(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.
*Under the condition of long time high temperature storage, module's warpage may happen, so the module should be stored at normal temperature(20±5℃).
*Under the condition of high humidity, module's warpage also may happen, so the module should be immediately stuck with Touch panel after being opened from the degas package. Otherwise don't store the module at the high humidity condition.
(3) Keeping Method
a. Don't keeping under the direct sunlight. b. Keeping in the tray under the dark place.

DON'T DO



(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) Be sure to prevent light striking the chip surface.

[Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VDDIO/VSP/VSN) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don't touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

(8) Be sure to use a power supply with the safety protection circuit such as the fuse for excess voltage, excess current, electric discharge waveform and Latch-up occurring.

(9) Epoxy resin (amine series curing agent), silicone adhesive material (dealcoholization series and oxime series), tray forming agent (azo compound) etc, in the cabinet or the packing materials may induce abnormal display with polarizer film deterioration regardless of contact or noncontact to polarizer film.
Be sure to confirm the component of them.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.
LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.
-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenic (Aims test: negative) material is employed.
FPC: Dispose of as similar way to circuit board from electric device.

1. Application

This data sheet is to introduce the specification of LS055R3SX01 active matrix 16,777,216color LCD module.
Main color LCD module is controlled by Driver IC (Samsung S6D1HA0).
If any problem occurs concerning the items not stated in this temporary specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

2. Construction and Outline

Construction: LCD panel, Driver , FPC with electric components,
16 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.
Outline: See page 31.
Connection: Board to Board Connector
(JAE, LCDM Side:WP9-P032VA1-R6000;User Side : WP9-S032VA1-R6000).
There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.
So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

3. Mechanical Specification

Table 1

Parameter		Specifications	Unit
Outline dimension(typ)		73.824(W) x 126.44(H) x 1.3(D)	mm
Main LCD Panel	Display mode	New Mode2	
	LCD mode	Transmissive	
	Active area	71.424mm x 119.04 mm	mm
	Display format	1536(H)×RGB×2560(V)	-
	Dot pitch	0.0155(W)×0.0465 (H)	mm
	Base color Note*1	Normally Black	-
Mass		21.1	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.

4. Absolute Maximum Ratings

(4-1) Electrical absolute maximum ratings

Table.2

Item	Symbol	Rating	Unit	Remark
Power Supply voltage(1)	VDDIO~GND	-0.3 to +5.0	V	Note 1,2
Power Supply voltage(2)	VSP~GND	-0.3 to +6.5	V	Note 1,3
Power Supply voltage(3)	GND~VSN	-0.3 to +6.5	V	Note 1,3

NOTE:

1.The absolute maximum rating is the limit value. When the IC is exposed to the operating environment beyond this range, the IC does not assure normal operations and may be damaged permanently, not be able to be recovered.

2. To make sure(High) VDDIO≥ GND(Low).

3.To make sure(High) VSP ≥ GND(Low), (High) GND ≥ VSN(Low)

(4-2) Environment Conditions

Table 3

Item	Top		Tstg		Remark
	Min	Max	Min	Max	
Ambient temperature	-20℃	+60℃	-30℃	+70℃	Note2
Humidity	Note1		Note1		No condensation

Note：

1. Ta ≤ 40 °C.....95 % RH Max
2. Ta > 40 °C.....Absolute humidity shall be less than Ta=40 °C /95 % RH.
3. As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable. Be sure not to exceed the rated voltage, otherwise a malfunction may occur.

5. Electrical Specifications

(5-1) Power Supply Voltage Range

Table 4

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply voltage	VSP	5.4	5.5	5.6	V	
Supply voltage	VSN	-5.6	-5.5	-5.4	V	
Supply voltage	VDDIO	1.7	1.8	1.9	V	

(5-2) DC characteristics

Table.5

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Input high voltage		V_{IH}	VDDIO=1.7V ~ 1.9V	0.7VDDIO	-	VDDIO	V	note 1
Input low voltage		V_{IL}		0	-	0.3VDDIO	V	
Output high voltage (CABC_PWM_OUT)		V_{OH1}	VDDIO=1.7V ~ 1.9V	0.8VDDIO	-	VDDIO	V	note 1
Output high voltage (CABC_PWM_OUT)		V_{OL1}	VDDIO=1.7V ~ 1.9V	0	-	0.2VDDIO	V	
Logic High level input current		I_{IH}	-	-	-	1	uA	
Logic Low level input current		I_{IL}	-	-1	-	-	uA	
Current consumption（video mode）	Normal Mode	I_{VDDIO}	1*1 dot checker	-	43.0	59.1	mA	note 2
		I_{VSP}		-	37.4	51.4	mA	
		I_{VSN}		-	33.7	46.3	mA	
Current consumption（CMD mode）	Normal Mode	I_{VDDIO}	1*1 dot checker	-	20.8	31.4	mA	note 3
		I_{VSP}		-	34.3	45.1	mA	
		I_{VSN}		-	30.4	40.0	mA	

Note:

1.The DC/AC electrical characteristics of Module are guaranteed at -20°C ~ +60°C.

2. Conditions: Ta=25℃,VSP=5.5V,VSN=-5.5V,VDDIO=1.8V,MIPI-DSI Video Mode,4 lane,1/2 compress
Refresh rate=58Hz,1GMbps,CABC/CE OFF

3. Conditions: Ta=25℃,VSP=5.5V,VSN=-5.5V,VDDIO=1.8V,MIPI-DSI CMD Mode,4 lane,1/2 compress
Refresh rate=58Hz, 1GMbps,CABC/CE OFF

(5-3) MIPI DSI characteristics

(5-3-1) HS and LP signal timing

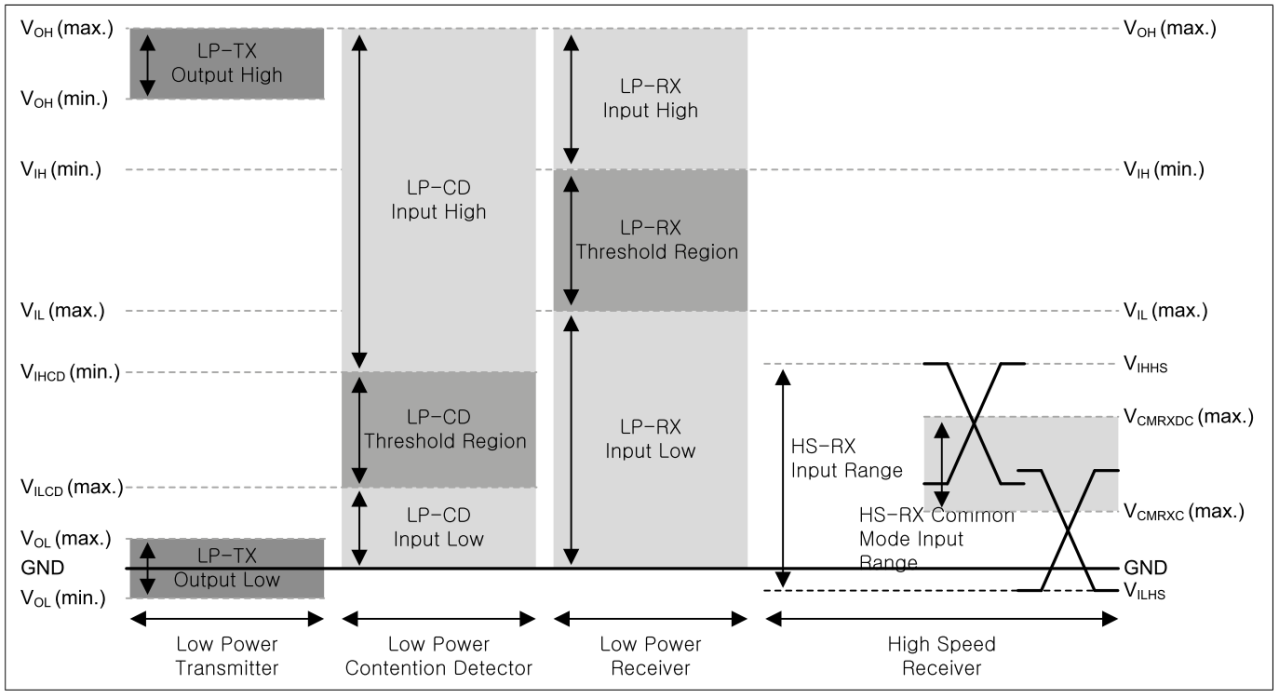


Fig.1 HS and LP signal levels

Table.6 Characteristics for MIPI DC

Item		Parameter	Min.	Nom.	Max.	Unit
LP_TX	Thevenin output high level	VOH	1.1	1.2	1.3	V
	Thevenin output low level	VOL	– 50	-	50	mV
	Output impedance of LP transmitter	ZOLP	110	-	-	Ω
HS_RX	Common-mode voltage HS receive mode	VCM-RX (DC)	70	-	330	mV
	Differential input high threshold	VIDTH	-	-	70	
	Differential input low threshold	VIDTL	– 70	-	-	
	Single-ended input high voltage	VIHHS	-	-	460	
	Single-ended input low voltage	VILHS	– 40	-	-	
	Single-ended threshold for HS termination enable	VTERM-EN	-	-	450	
	Differential input impedance	ZID	80	100	125	Ω
LP_RX	Logic1 input voltage	VIH	880	-	-	mV
	Logic0 input voltage, not in ULP State	VIL	-	-	550	
	Input hysteresis	VHYST	25	-	-	
LP_CD	Logic1 contention threshold	VIHCD	450	-	-	
	Logic0 contention threshold	VILCD	-	-	200	

(5-3-2)HS Data-Clock Timing

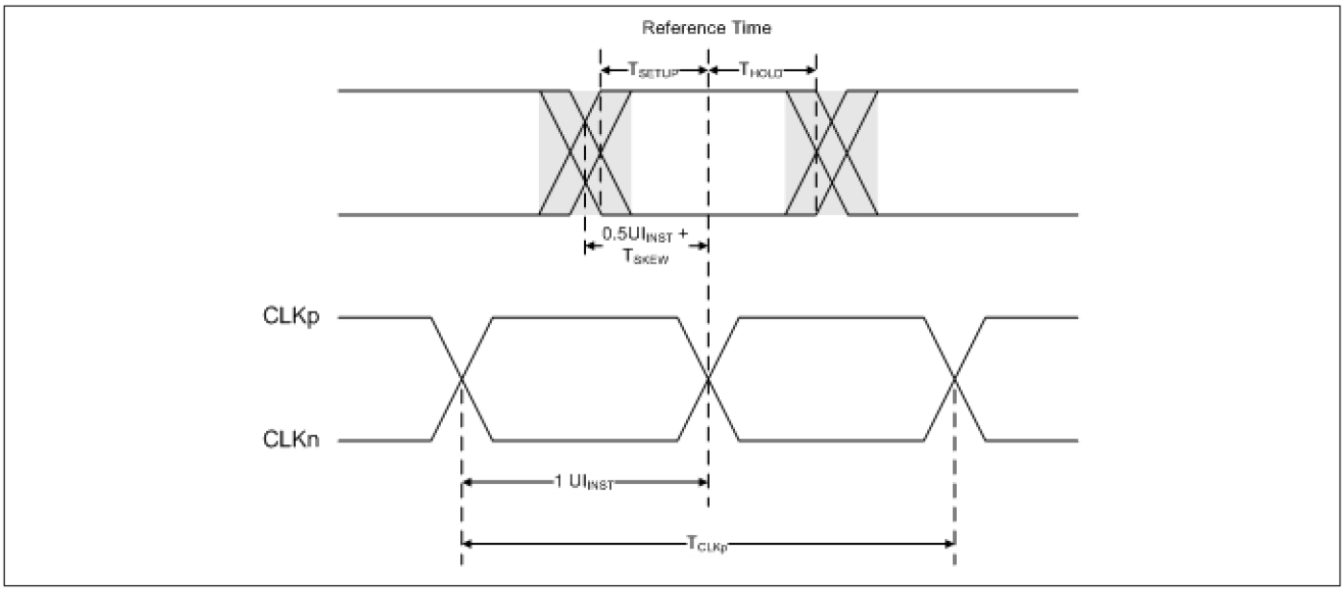


Fig.2 MIPI Data to Clock Timing Definitions

Table.7 HS Data Transmission Timing Parameters

Clock Parameter	Symbol	1. of d-lane	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	4	1	-	12.5	ns	(1) (2)

NOTE:

1. This value corresponds to a minimum 80 Mbps data rate
2. The minimum UI shall not be violated for any single bit period, i.e, any DDR half cycle within a data burst.

Table.8 Data to Clock Timing Specifications

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Skew (Measured at transmitter)	$T_{SKEW[TX]}$	– 0.15	-	0.15	UIINST	(1)
Data to Clock Setup Time (Receiver)	$T_{SETUP[RX]}$	0.15	-	-		(2) (3)
Clock to Data Hold Time (Receiver)	$T_{HOLD[RX]}$	0.15	-	-		

NOTE:

1. Total silicon and package delay budget of 0.3 × UIINST
2. Total setup and hold window for receiver of 0.3 × UIINST
3. TSETUP[Rx] and THOLD[RX] are only for Rx without FPCB and connector and guaranteed by design.

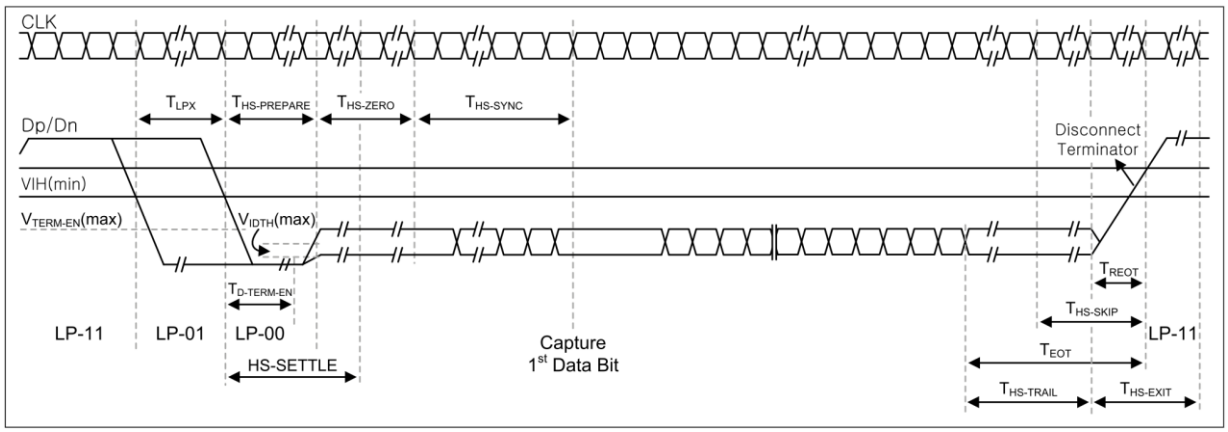


Fig.3 High Speed Data Transmission timing sequence

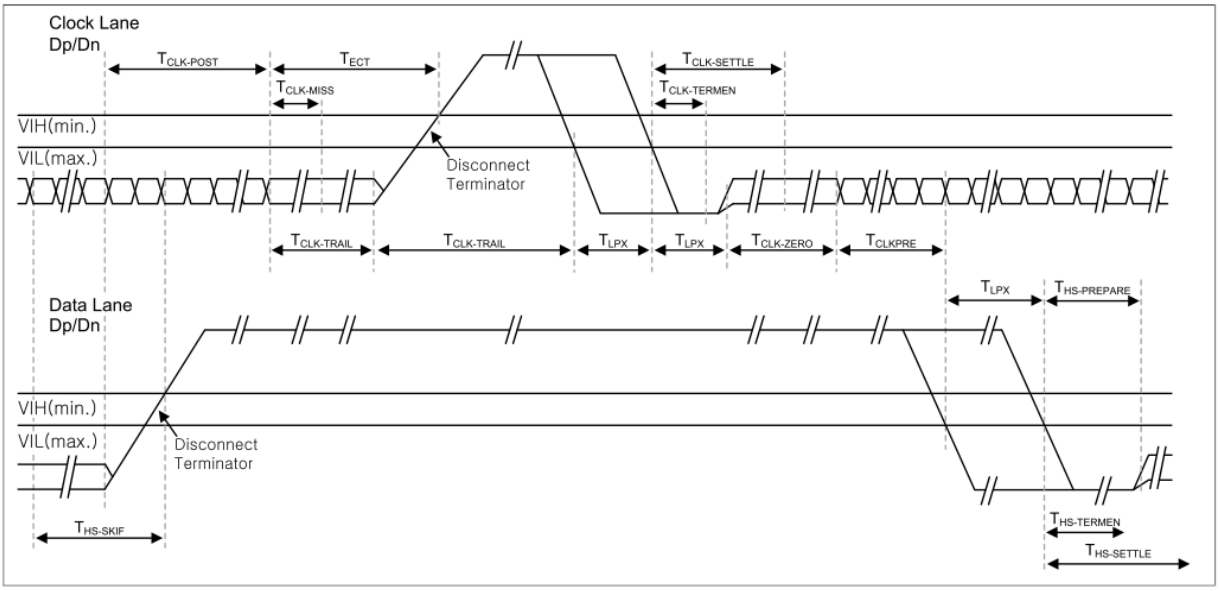


Fig.4 Switching the Clock Lane between Clock Transmission and LP Mode

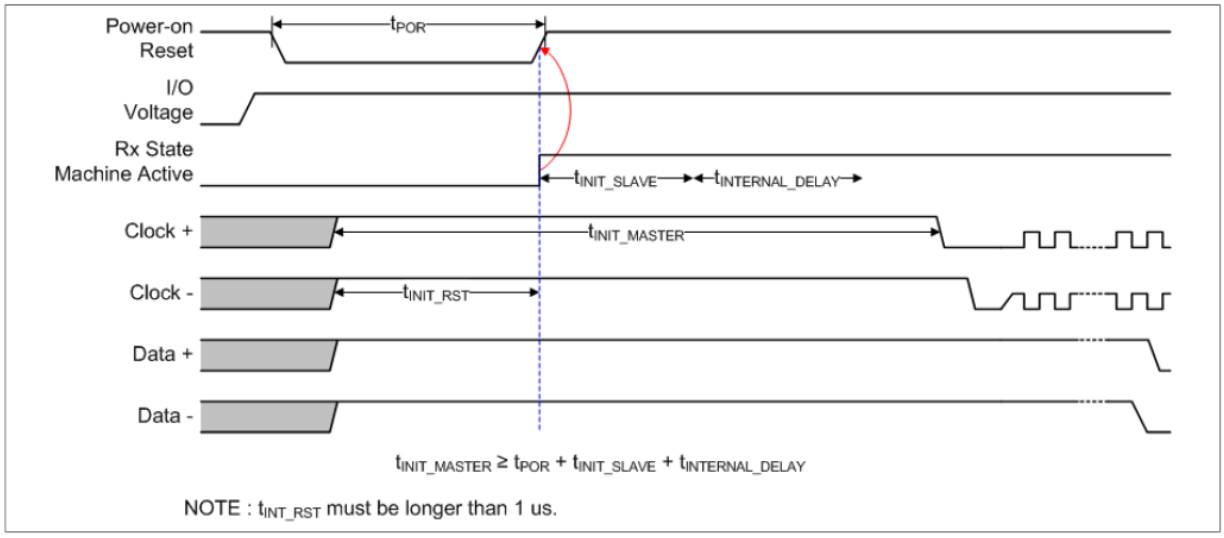


Fig.5 MIPI Peripheral Power-Up sequence

Table.9 Global Operation Timing Parameters

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns	(1) (6)
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52 × UI	-	-		(5)
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	UI	
$T_{CLK-REPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns	
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.	95	-	300		(6)
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	38		
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-		(5)
$T_{CLK-PREPARE}$ $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-		
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	35 ns + 4 × UI		(6)
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.		-	105 ns + n × 12 × UI		(3) (5)

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns	(5)
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4 × UI	-	85 ns + 6 × UI		
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10 × UI	-	-		
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$.	85ns + 6 × UI	-	145 ns + 10 × UI		(6)
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	-	55 ns + 4 × UI		
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max (n × 8 × UI, 60 ns + n × 4 × UI)	-	-		(2) (3) (5)
T_{INIT}		-	-	-		
T_{LPX}	Transmitted length of any Low-Power state period	-	62.5	-	ns	(4) (5)
Ratio T_{LPX}	Ratio of T_{LPX}(MASTER)/T_{LPX}(SLAVE) between Master and Slave side	2/3	-	3/2		
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5 × T_{LPX}			ns	(5)
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	4 × T_{LPX}				
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX	-	2 × T_{LPX}		
T_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1	-	-	ms	

NOTE:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

2. If a > b then max. (a, b) = a otherwise max. (a, b) = b

3. Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode.

4. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

5. Transmitter-specific parameter.

6. Receiver-specific parameter.

(5-4)TE Timing

Parameter	MIN.	TYP.	MAX.	Unit	Remarks
Refresh frame rate operation range	55	58	61	Hz	
Refresh frame rate tolerance	-5	-	+5	%	

TE signal of V-Blanking information only(TEMOD=0)：VFP+VS+VBP-1

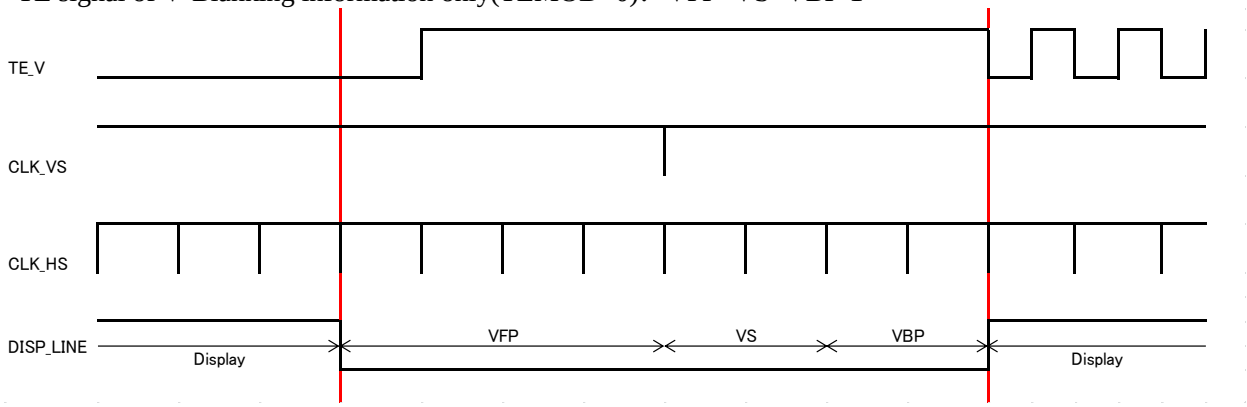


Fig.6 TE signal of V-Blanking information only

Parameter	MIN.	TYP.	MAX.	Unit	Remarks
Refresh frame rate operation range	142.5	150.0	157.5	KHz	
Refresh frame rate tolerance	-5	-	+5	%	

TE signal of V-Blanking and H-Blanking information (TEMOD=1)：1/2 Line（Hsync）

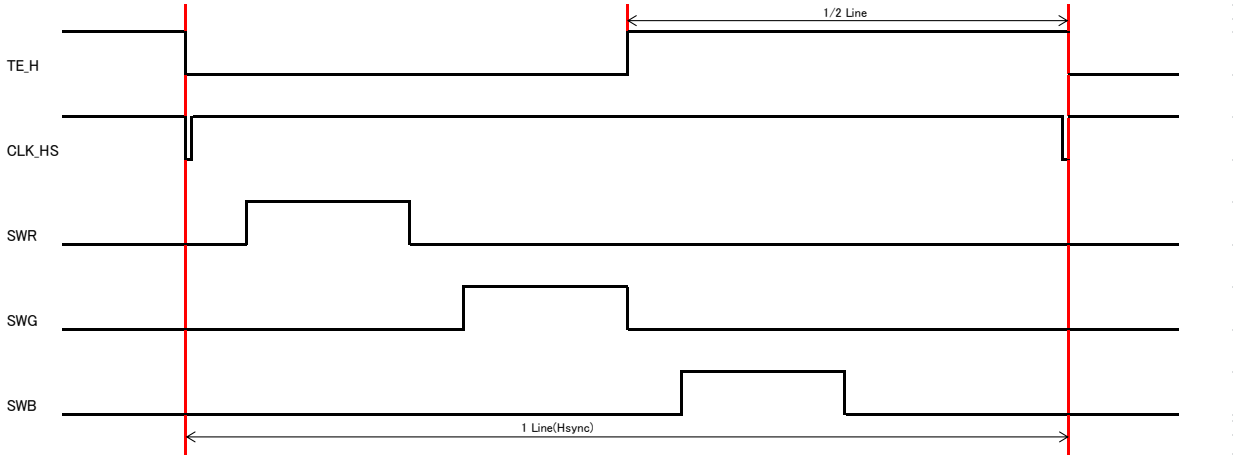


Fig.7 TE signal of V-Blanking and H-Blanking information

(5-5) LED backlight

At main panel the back light uses 16pcs edge light type white LED.

Table.10

Item	Value(1 parallel)			Unit
	Min	Nominal	Max	
Forward current	-	20	-	mA
Forward Voltage	-	24	26.4	V
Number of LED components	16pcs LED(8pcs*2parallel)			

LED lamp:NICHIA (NSSW304D)
Color Rank: Bt07/Bt08/Bt27/Bt28
Luminous Intensity Rank: NW725～
Please consider Allowable Forward Current on used temperature

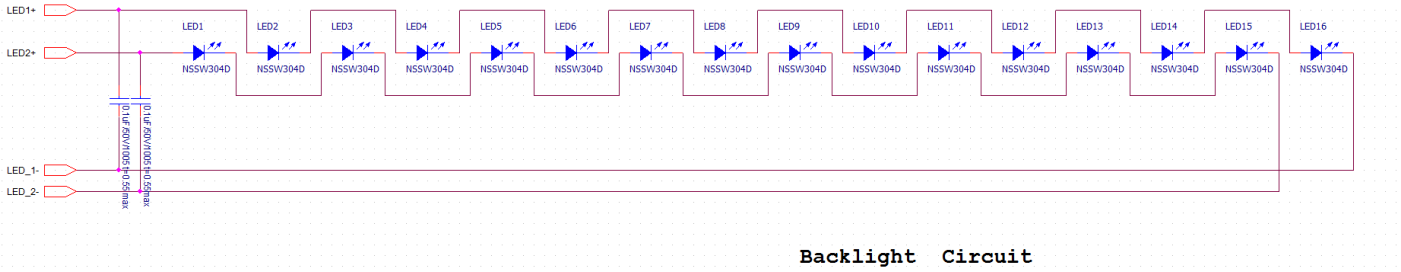


Fig.8 Schematics drawing of lighting

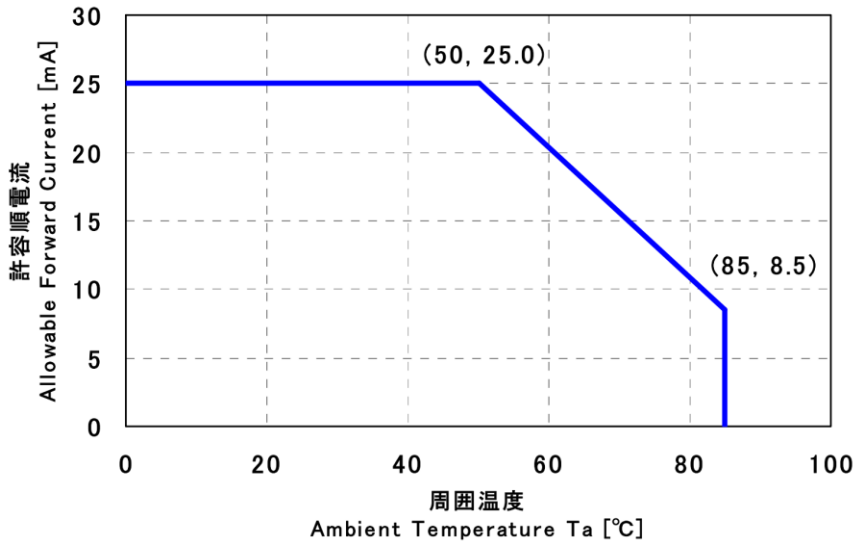


Fig.9 Ambient Temperature VS. Allowable Forword Current

(5-6) Interface signals

Table.11

1	LED1+	Power supply for LED (Anode)	I	
2	GND	GND level pin	-	
3	LED2+	Power supply for LED (Anode)	I	
4	D2_P	MIPI-DSI Data differential input pins.(Data lane2)	I	
5	LED1-	Power supply for LED (Cathode)	I	
6	D2_N	MIPI-DSI Data differential input pins.(Data lane2)	I	
7	LED2-	Power supply for LED (Cathode)	I	
8	GND	GND level pin	-	
9	VDDIO	Power supply for LCD	I	VDDIO=1.8±0.1V
10	D1_P	MIPI-DSI Data differential input pins.(Data lane1)	I	
11	PWM	Backlight brightness control pin	O	
12	D1_N	MIPI-DSI Data differential input pins.(Data lane1)	I	
13	HSYNC	Horizont Scan signal output (use TP control)	O	
14	GND	GND level pin	-	
15	TE	Internal VSYNC output (use TP control)	O	
16	CLK_P	MIPI-DSI Clock differential input pins.	I	
17	GND(TEST)	GND level pin	-	
18	CLK_N	MIPI-DSI Clock differential input pins.	I	
19	RESET	H/W Reset pin	I	
20	GND	GND level pin	-	
21	LCD_ID	Supplier information terminal (VDD level)	O	(SHARP: Connect to VDDIO)
22	D0_P	MIPI-DSI Data differential input/output pins.(Data lane0)	I/O	
23	VGL	IC internal output signal	O	It is opened by the FPC circuit of LCD Module
24	D0_N	MIPI-DSI Data differential input/output pins.(Data lane0)	I/O	
25	VSN	Power supply for LCD	I	VSN= -5.5±0.1V
26	GND	GND level pin	-	
27	VSP	Power supply for LCD	I	VSP= 5.5±0.1V
28	D3_P	MIPI-DSI Data differential input pins.(Data lane3)	I	
29	GND	GND level pin	-	
30	D3_N	MIPI-DSI Data differential input pins.(Data lane3)	I	
31	VGH	IC internal output signal	O	It is opened by the FPC circuit of LCD Module
32	GND	GND level pin	-	

Notes:

The direction is named with respect to the display module, I = from host to module, O = from module to host.

Table.12: Connector description

Assembled on	**Item**	Description
Phone PWB	Connector type	Board to Board
	Pin amount	32
	Manufacturer	JAE
	Part number	WP9-S032VA1-R6000

(5-7) Reset input timing

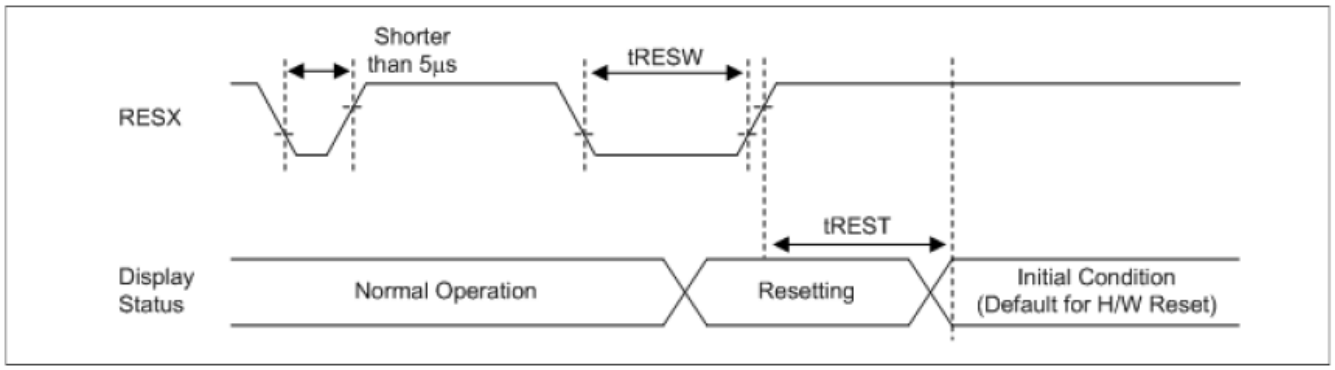


Fig.10 Reset input timing

Table.13

Symbol	Parameter	Pad	Min.	Typ.	Max.	Unit	Note
t_{RESW}	Reset low pulse width	RESX	10	-	-	µs	-
t_{REST}	Reset completion time	RESX	-	-	5	ms	Reset during Sleep In mode
		RESX			120		Reset during Sleep Out mode

NOTE:

1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

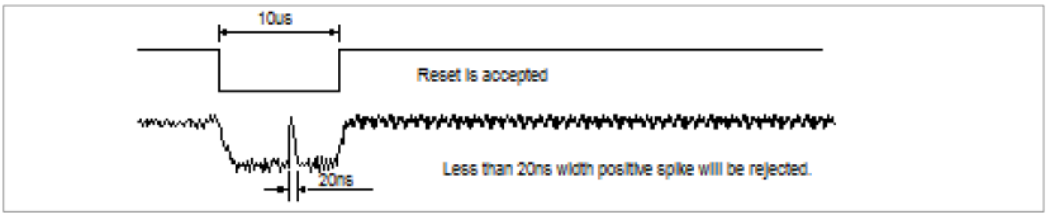
Table.14

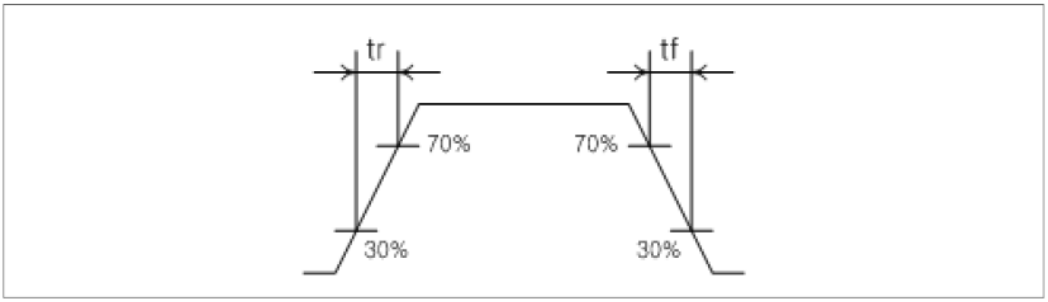
RESX Pulse	Action
Shorter than 5 µs	Reset rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset start

2. During the reset period, the display will be blanked (The display is entering blanking sequence, for which the maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains in the blank state in Sleep In-mode) and then return to Default condition for H/W reset.

3. During Reset Completion Time, ID bytes (or similar) value in NVM will be latched to the internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

4. Spike Rejection also applies during a valid reset pulse as shown below.





5. It is necessary to wait for 5 msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

(5-8) Schematic of LCD module system

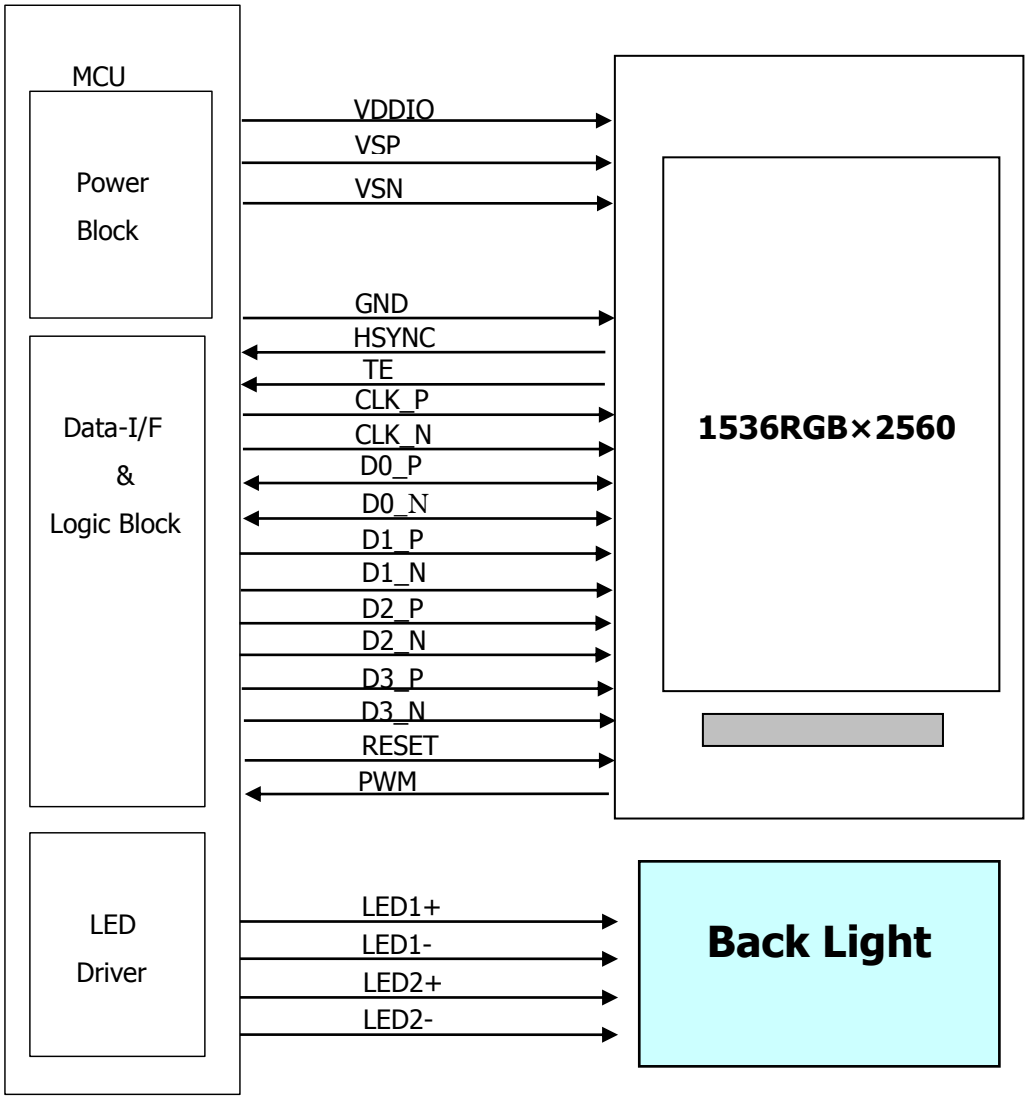


Fig.11 Schematic of LCD module system

(5-9) General Timing Diagram

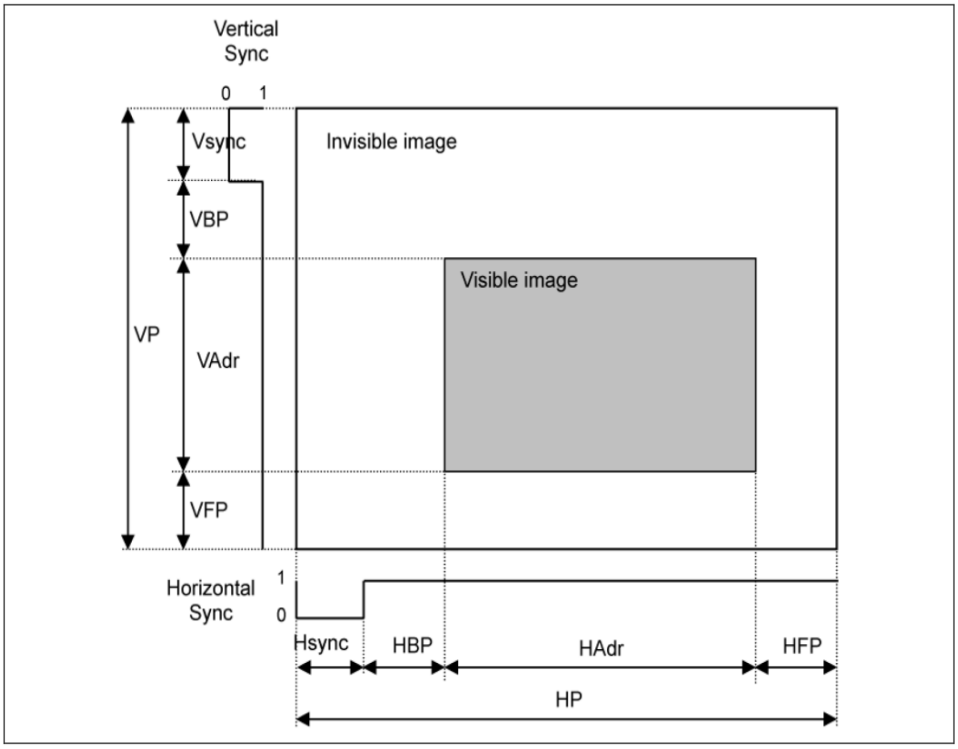


Fig.12 MIPI Interface

(5-10) Video Timing

Table.15：Video Timing

Item	MIN	TYP	MAX	Unit
Horizontal low pulse width(HS)	-	44	-	Line
Horizontal back porch(HBP)		68	-	Line
Horizontal active area (HAdr)	-	768	-	Pixel
Horizontal front porch(HFP)	-	88	-	Line
Vertical low pulse width(VS)	-	2	-	H
Vertical front porch(VFP)	-	4	-	H
Vertical back porch(VBP)	-	2	-	H
Vertical active area (VAdr)	-	2560	-	Pixel
Frame Frequency	55	58	61	Hz
DSI DATA rate	890	930	1000	Mbps/Lane

Ta = -20 - +60°C, VDDIO = 1.8 V, VSP=5.5V, VSN= -5.5V, GND = 0 V

6. Initial Sequence

Table.16: Condition

I/F:MIPI DSI 4lane,Video/Command,1/2 compress
Dots Size:1536xRGBx2560
Power Supply: VDDIO=1.8V,VSP=5.5V,VSN=-5.5V
Color Mode:24 bit
Frame frequency: TYP 58HZ

Table.17: Power ON Sequence(Power ON→Normal)

ITEM	Register Address	Register Data list	REMARK
Reset (RESET="L")			
VDDIO=1.8V			VDDIO power on
WAIT 10ms (min 1.0ms)			Wait to VDDIO=90% (depends on Power Supply Circuit)
VSP=5.5V			VSP power on
WAIT 10ms (min 1.0ms)			
VSN=-5.5V			VSN power on
WAIT 1.0ms (min 10us)			
DSI video mode transfer start			
WAIT 10us (min 1us)			
RSX (RESET="H")			
WAIT 10ms (min 5ms)			[Automatic] Sleep Mode On
SLEEP OUT			
SLPOUT	11h	-	
WAIT Min.120ms			
Password Key enable	F0h	0x5A	
		0x5A	
Password Key enable	F1h	0x5A	
		0x5A	
Password Key enable	FCh	0x5A	
		0x5A	
Interface Setting	B4h	0xE2(VD) 0xE0(CMD)	CMD Mode (1st parameter E0h) Video Mode (1st parameter E2h) Default = E0
		0x08	
		0x00	
G_PARA Set	B0h	0x0B	
PANEL_CTL1	EBh	0x1C	
DDI Guide code	B0h	0x06	
	FEh	0x12	
COLOR ENHANCEMENT			
IMAGE_ON	E8h	0x22	
SMIES	EAh	0x12	
		0x33	
		0x03	
		0x25	
Password Key disable	F0h	0xA5	
		0xA5	
Password Key disable	F1h	0xA5	
		0xA5	

Password Key disable	FCh	0XA5	
		0XA5	
CASET	2Ah	0x00	SC = 00, EC = 1535
		0x00	
		0x05	
		0xFF	
PASET	2Bh	0x00	SP = 00, EP = 2559
		0x00	
		0x09	
		0xFF	
Send display pattern from Host Driver			
RAMWR	2Ch	–	RAM Writing
Image transfer start			
WAIT 50ms			
BackLight ON			
Write_display_brightness	51h	0xFF	
Write_content_adaptive_brightness_control	55h	0x00	00 = CABC OFF 02 = CABC ON
BackLight On-Write Control Display	53h	0x24	LED(PWM) On
Display on			
DISPON	29h	-	
TE ON	35h	0x00	58Hz(typ)
Display pattern			

Table.18: Power OFF Sequence(Normal→Power OFF)

ITEM	Register Address	Register Data list	REMARK
BackLight OFF			
BackLight Off	53h	0x00	LED(PWM) Off
Password Key enable	F0h	0x5A	
		0x5A	
Password Key enable	F1h	0x5A	
		0x5A	
Password Key enable	FCh	0x5A	
		0x5A	
G_PARA Set	B0h	0x0B	
PANEL_CTL1	EBh	0x1C	
All Black Image transfer			
WAIT 20ms MIN 1V(Frame)			
VSN OFF (GND)			VSN power off
WAIT 10ms (min1ms)			
VSP OFF (GND)			VSP power off
WAIT 10ms (min1ms)			
VDDIO OFF (GND)			VDDIO power off

7. Optical Characteristics

Table.19: VDDIO=1.8 V,VSP=5.5V,VSN=-5.5V, ILED=20mA, Ta = 25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remark
Contrast	CR	θ=0°	840	1200	-		Note 1,2, 4
Brightness	L	θ=0°	315	450	-	cd/m2	Note 1, 4
NTSC ratio	S	θ=0°	60	70	-	%	Note 1, 4
Viewing Angle	θ_{11}	CR>10	-	80	-	°(degree)	Note 1, 2,4
	θ_{12}		-	80	-		
	θ_{21}		-	80	-		
	θ_{22}		-	80	-		
Response Time	Tr+Td	θ=0°	-	-	35	ms	Note 1,3,4
White Chromaticity	x	θ=0°	0.278	0.308	0.338	-	Note 1, 4 ※Fig.12
	y		0.297	0.327	0.357		
Red Chromaticity	x	θ=0°	0.613	0.643	0.673	-	Note 1, 4
	y		0.301	0.331	0.361	-	
Green Chromaticity	x	θ=0°	0.275	0.305	0.335	-	Note 1, 4
	y		0.579	0.609	0.639	-	
Blue Chromaticity	x	θ=0°	0.128	0.158	0.188	-	Note 1, 4
	y		0.035	0.065	0.095	-	
Uniformity	-	θ=0°	70	80	-	%	Note1, 5
Crosstalk	-	θ=0°	-	-	6	%	Note1, 7
Flicker	-	θ=0°	-	-	10	%	Note4, 6

*1: Measuring condition

・Temperature = 25℃(±3℃), Frame Frequency =58Hz, LED back-light: ON, CABC/CE OFF, Environment brightness < 150 lx

・Measured sample : New sample before a long term aging.

・Brightness/ Contrast/ Chromaticity/Uniformity/ NTSC ratio Test device: SR3,SR UL-2

Viewing Angle/ Time Test device: DMS

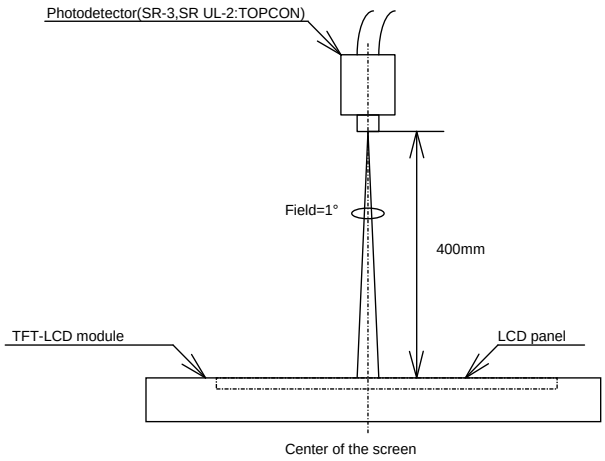


Fig.13 Optical characteristics Test Method(SR3,SR UL-2)

(Note 1) Definition of range of visual angle

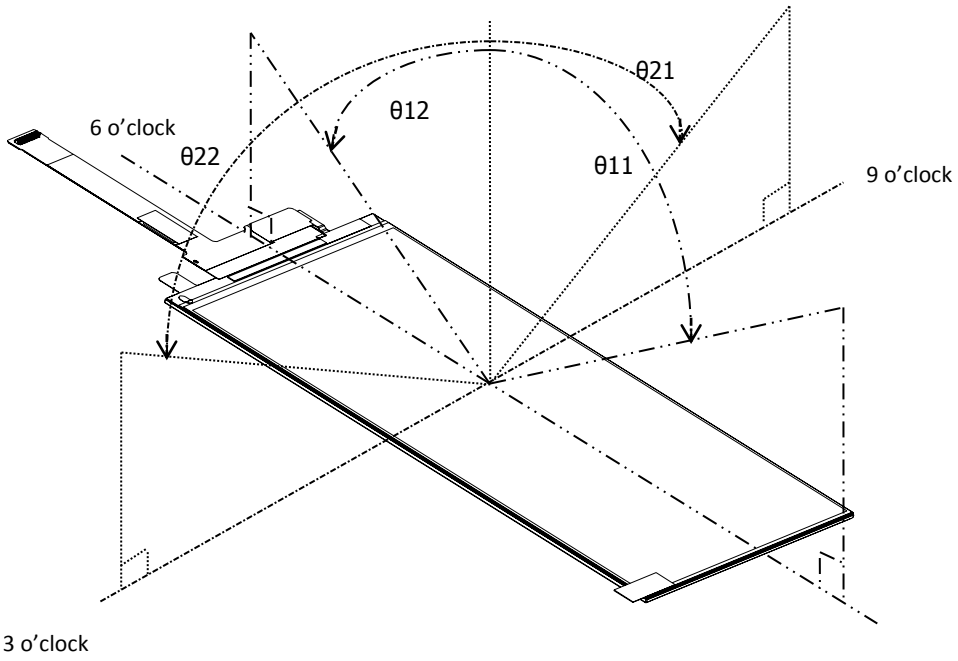


Fig.14 Definition of viewing angle

(Note 2) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixcels "White"}}{\text{Luminance(brightness) all pixcels "Black"}}$$

(Note 3) Response time is defined as follows:

Define response time:

The response time is defined as the following figure and shall be measured by

Switching the input signal for “black” and “white”.

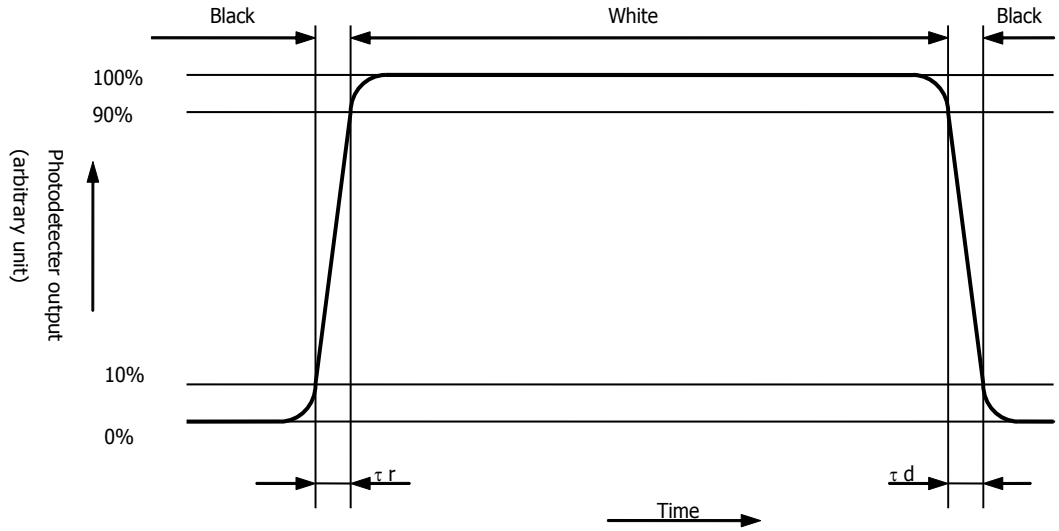


Fig.15 Response time

(Note 4) This shall be measured at center of the screen.

(Note 5) Uniformity is defined as follows:

$$\text{Uniformity} = \frac{\text{Minimum Brightness}}{\text{Maximum Brightness}} \times 100\ [\%]$$

The brightness should be measured on the 9-point as shown in the below figure

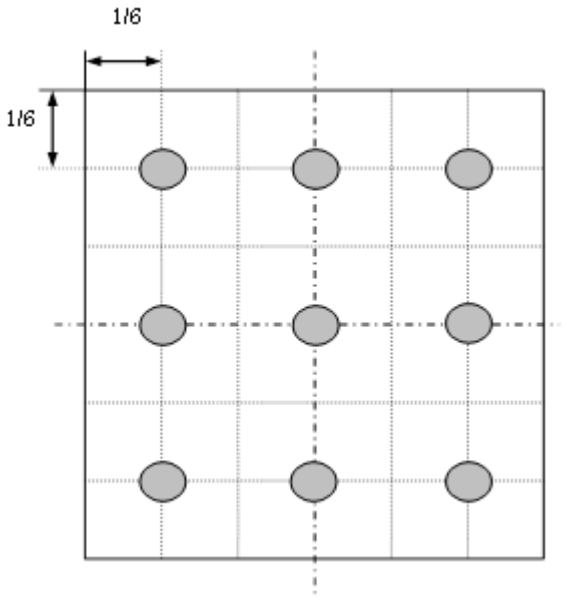
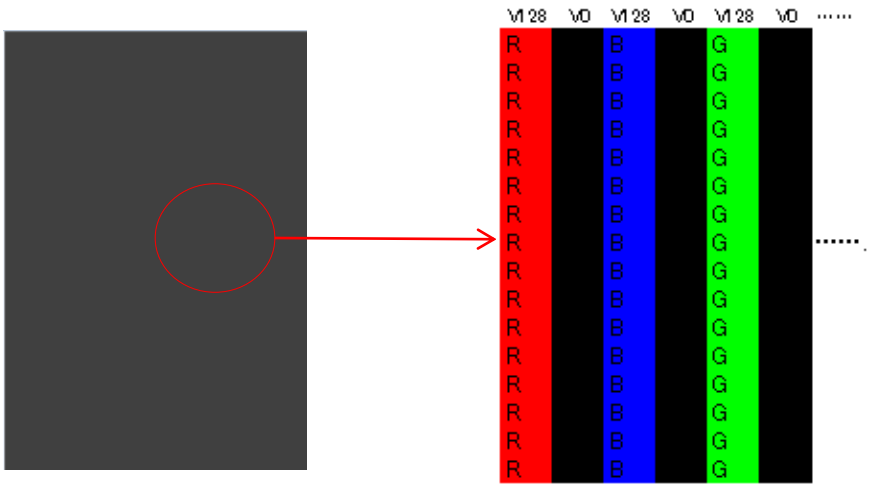


Fig.16 Definition of measurement points

(Note 6) Measuring systems: YOKOGAWA 3298_01 + 3298_11

- Temperature = 25℃(±3℃), Frame Frequency = 58Hz, LED back-light: ON, Environment brightness < 150 lx
- Measured sample : New sample before a long term aging.
- Flicker ratio is very sensitive to measuring condition.
- Measurement point is panel center.
- Conversion of Flicker ratio : Flicker[%] =ACrms/DC×100
- Worst pattern:



(Note 7) Definition of Crosstalk

CT=|Yw(Xi)-YG(Xi)|×100(%)/YG(Xi)　　X=U,D,L,R　　i=gray 127

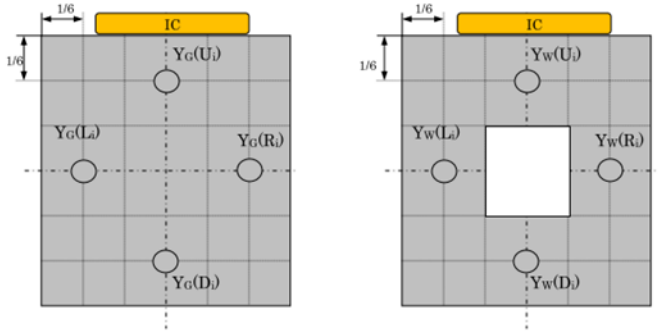


Fig.17　Definition of Crosstalk

8. Reliability test items

Table.20

No.	Test item	Condition
1	High temperature storage test	Ta = 70°C 240h
2	Low temperature storage test	Ta = -30°C 240h
3	High temperature & high humidity operation test 1	Ta = 40°C ; 95%RH 240h
4	High temperature operation test	Ta = 60°C 240h
5	Low temperature operation test	Ta = -20°C 240h
6	Thermal shock test (non-operating)	Ta = -20°C to 70°C / 20 cycles (30 min) (30 min)
7	Electro static discharge test	MM ±200V/200pF(0Ω) to Terminals(Contact) (1 time for each terminals)

Table.21

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

9. Packaging specifications

(9-1) Reliability

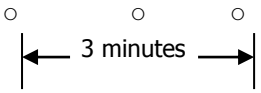
1) Vibration test

Table.22

Item	Test			
Frequency	5 Hz to 50 Hz (3 minutes cycle)			
Direction	Up-Down, Left-Right, Front-Back (3 directions)			
Period	Up-Down	Left-Right	Front-Back	Total
	60min	15min	15min	90min

The frequency should start at 5 Hz and vary continuously.

Total amplitude	20mm	0.2mm	20mm	0.2mm	
Frequency	5 Hz	50 Hz	5 Hz	50 Hz	(For 9.8m/s^2)



2) Drop test

Drop height: 750mm

Number of drop: 10 times (Drop sequence: 1 corner, 3 edges, 6 faces)

(9-2) Packaging quantities

120 modules per master carton

(9-3) Packaging weight

About 8.2kg

(9-4) Packaging outline dimensions

L*W*H=575mm*360mm*225mm

(Packaging materials)

Table.23

	Parts name	CRITERION(after test)
1	Master carton	Corrugate card board
2	Inside sleeve	Corrugate card board
3	Outside sleeve	Corrugate card board
4	Tray for packaging	Polystyrene with anti-static treatment +anti-static polystyrene
5	Protective bag	Polystyrene with anti-static treatment
6	OPP tape	Polypropylene
7	Bar code label	anti-static polystyrene

(9-5) Fig Details of packing

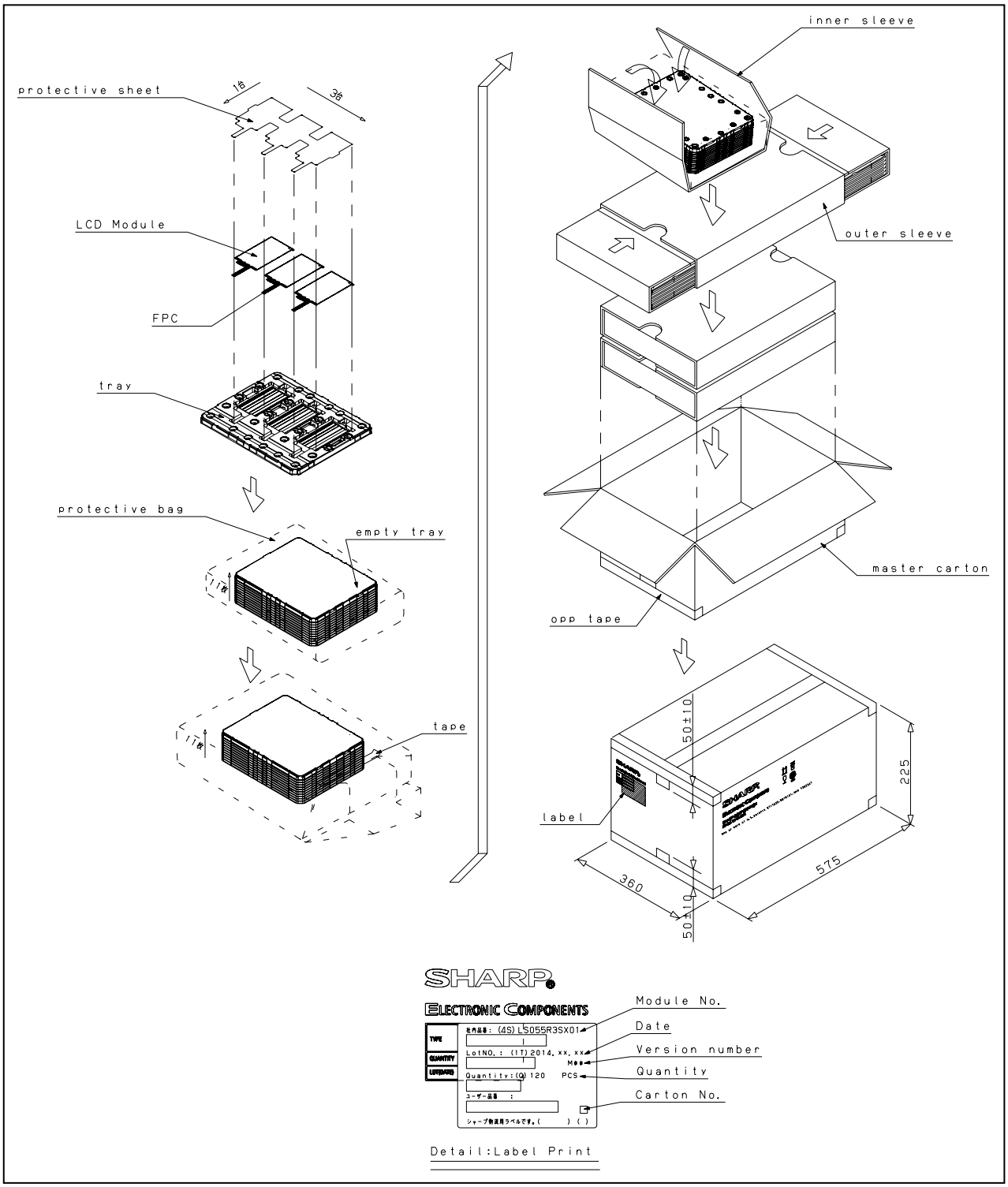


Fig.18 Details of packing

10. Serial Number Label identification

Numbering is specified as follows.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	L	S	0	5	5	R	3	S	X	0	1		Q	
2	4	0	4	8	*	*	*	*	*	1		M	0	2

① First line

1-11: LCM's name

13:Sharp's factory code

Q: The head office plant

X: Xinqu plant

L: Liyuan plant

② Second line

1-2: Vendor and factory code(ID1)

40: The head office plant

41: Xinqu plant

42: Liyuan plant

3-4: Date of production

Year (lower 1 digits)

4: 2014

5: 2015

Month: 1～9

X: October

Y: November

Z: December

5-10: Serial number

12-14: Version

E01=ES01

E02=ES02

M01=MP01

M02=MP02(add conductive adhesive tape.)

11.LCD module Outline dimensions

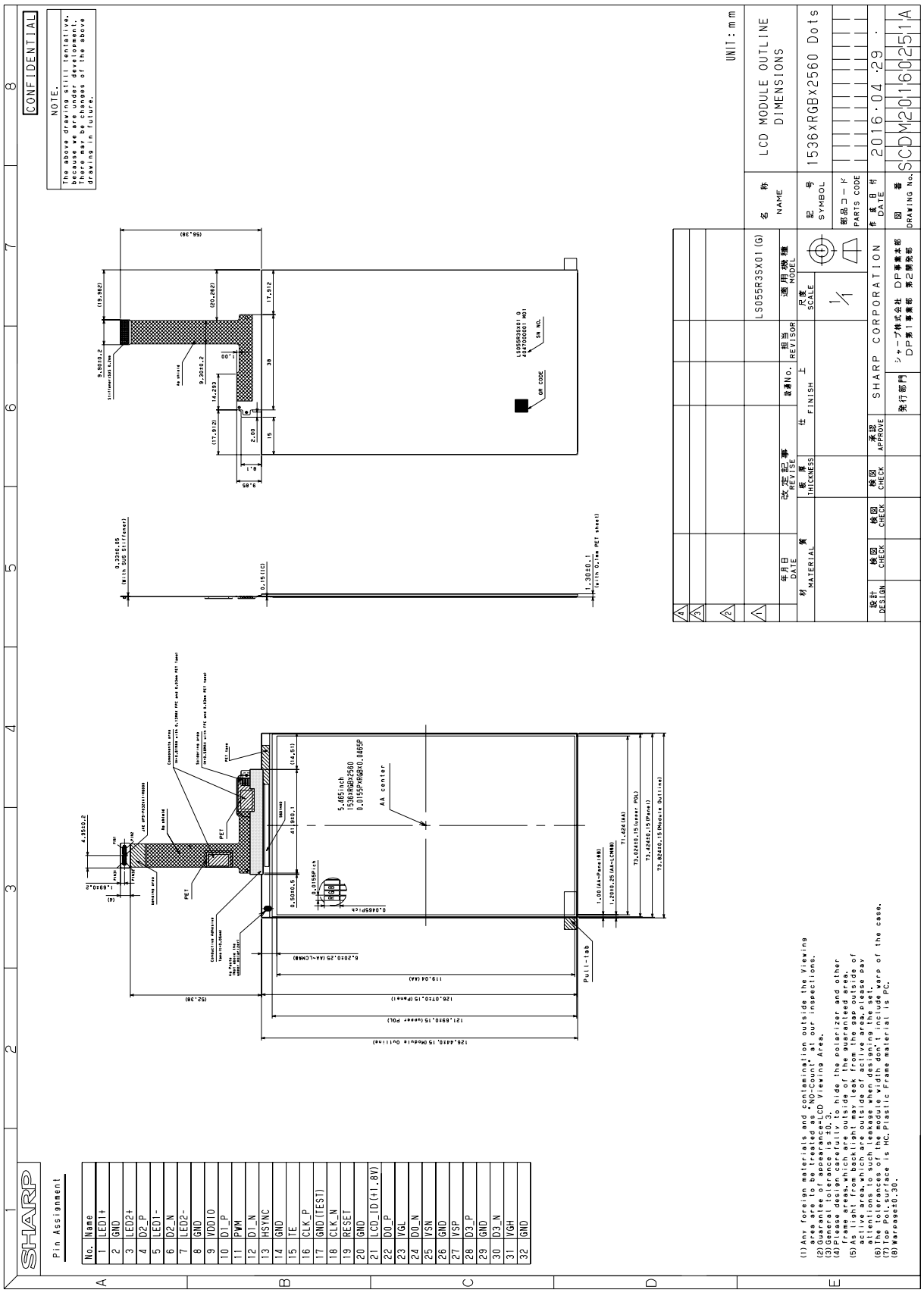


Fig.19 Outline

12. Schematics drawing of FPC

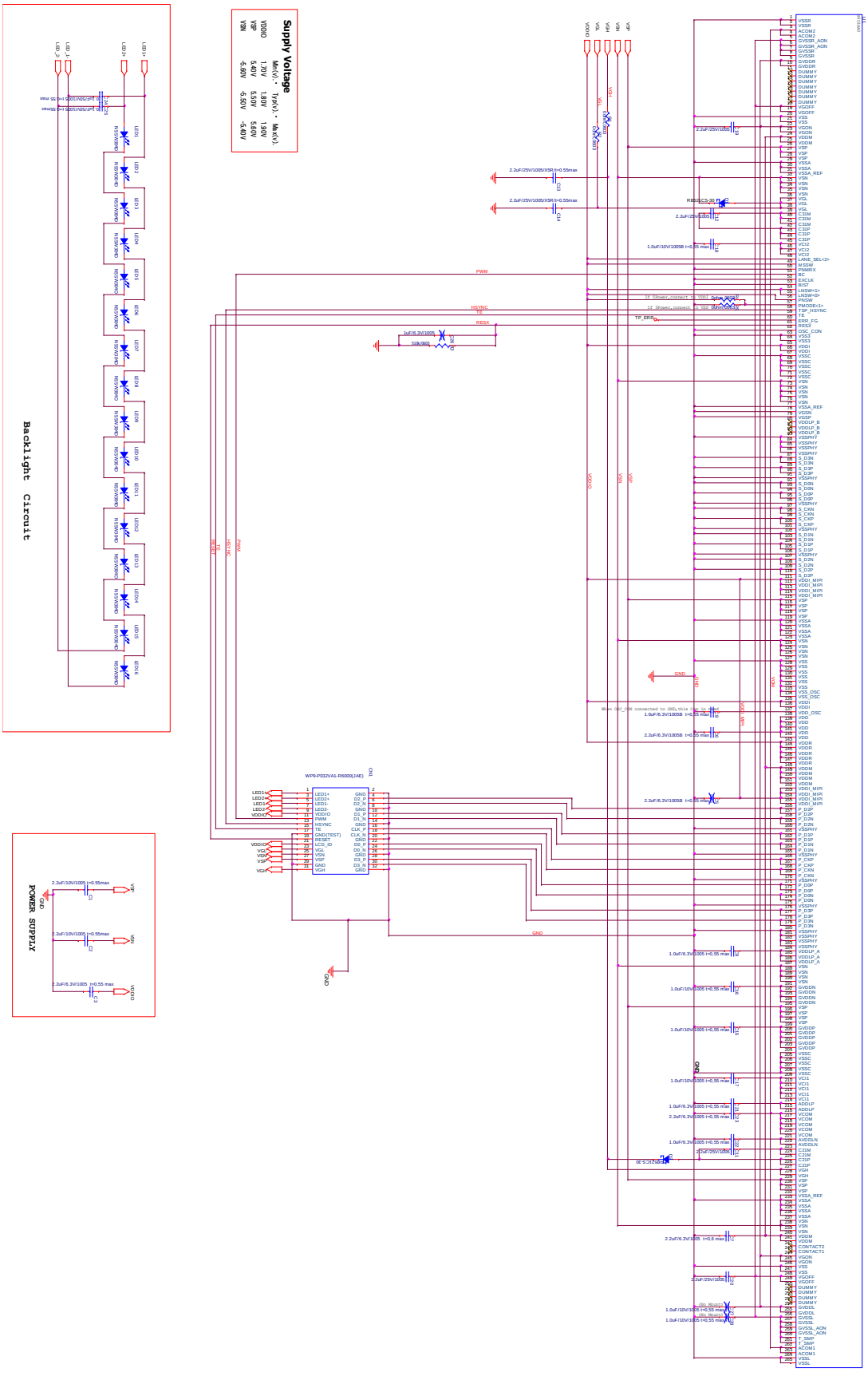


Fig.20 Schematics drawing of FPC

13.FPC part list

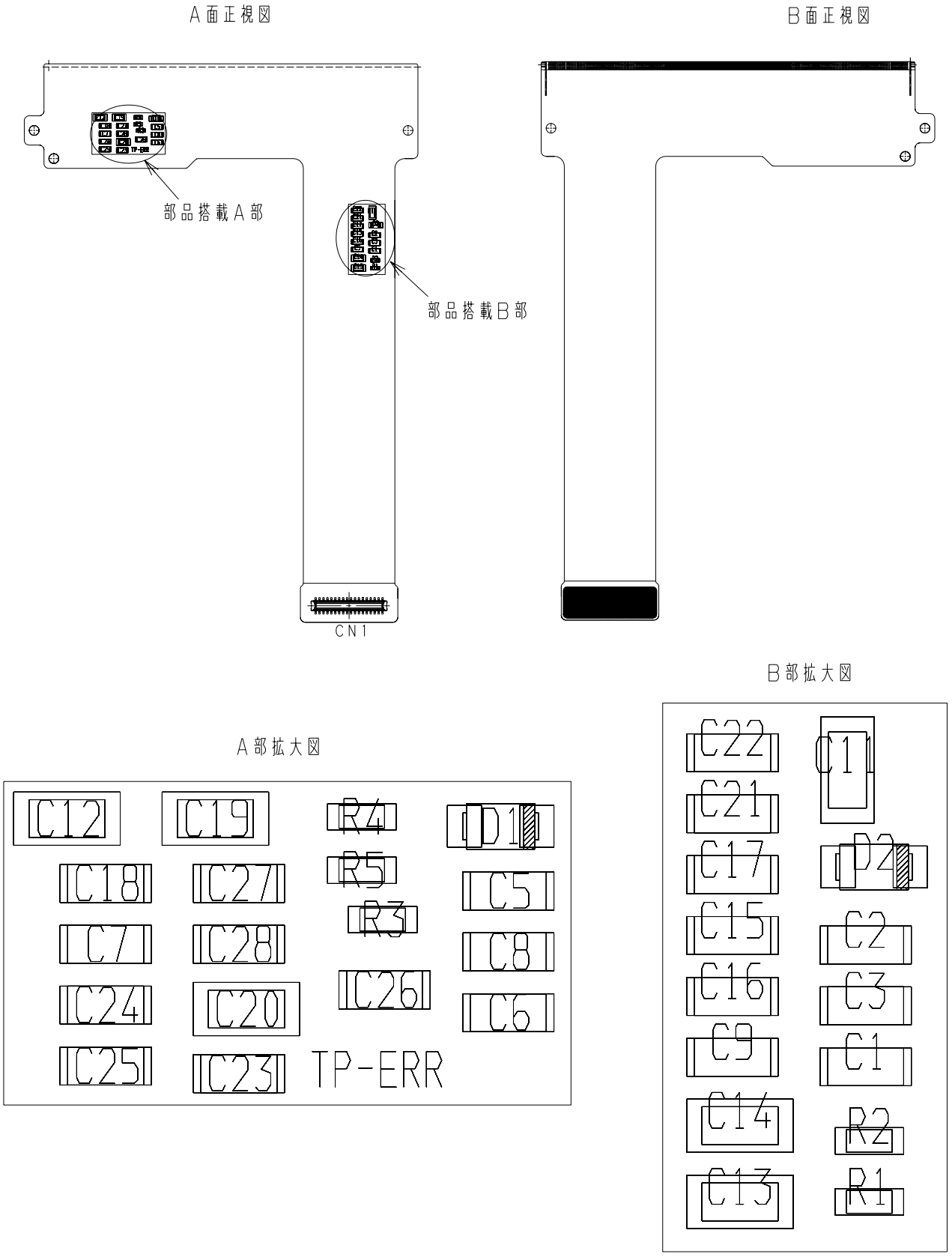


Fig.21 FPC part list layout

Table.24 Part list

Part	Characterisics
C1, C2	2.2uF / 10V / 1005
C11, C12, C13, C14, C19, C20	2.2uF / 25V / 1005
C3, C6, C7, C23	2.2uF / 6.3V / 1005
C8, C9, C21, C22	1uF / 6.3V / 1005
C15, C16, C17, C18	1uF / 10V / 1005
C24, C25	0.1uF / 50V / 1005
R3	510kΩ / J 0603
D1, D2	RB521CS-30GNT2RB / 1006
CN1	WP9-S032VA1-R6000
C5, C26, C27, C28 (No mount)	---
R5	0Ω / J 0603
R1, R2, R4 (No mount)	---

14.LCD-FPC layout pattern

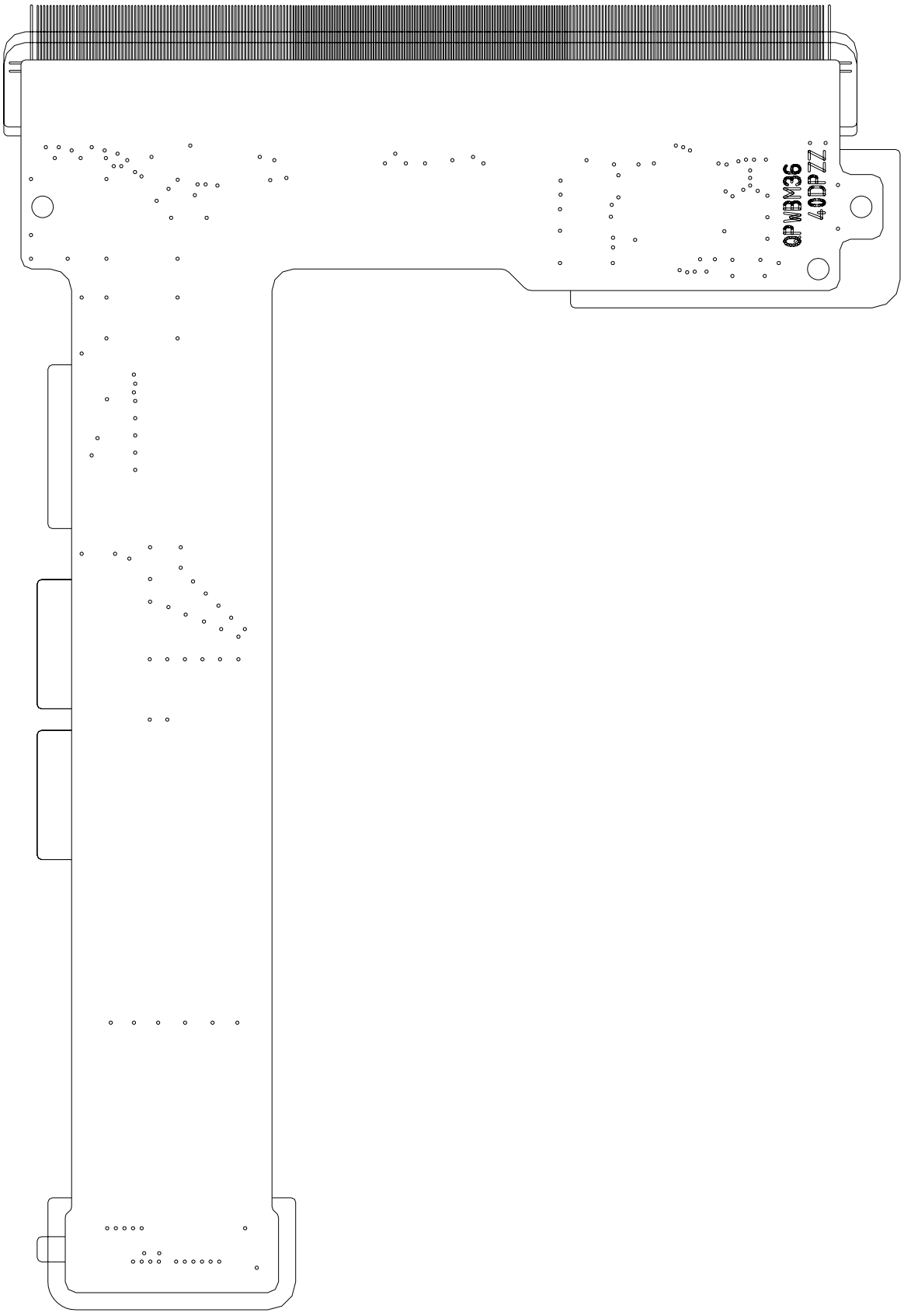


Fig.22 LCD- FPC layout1

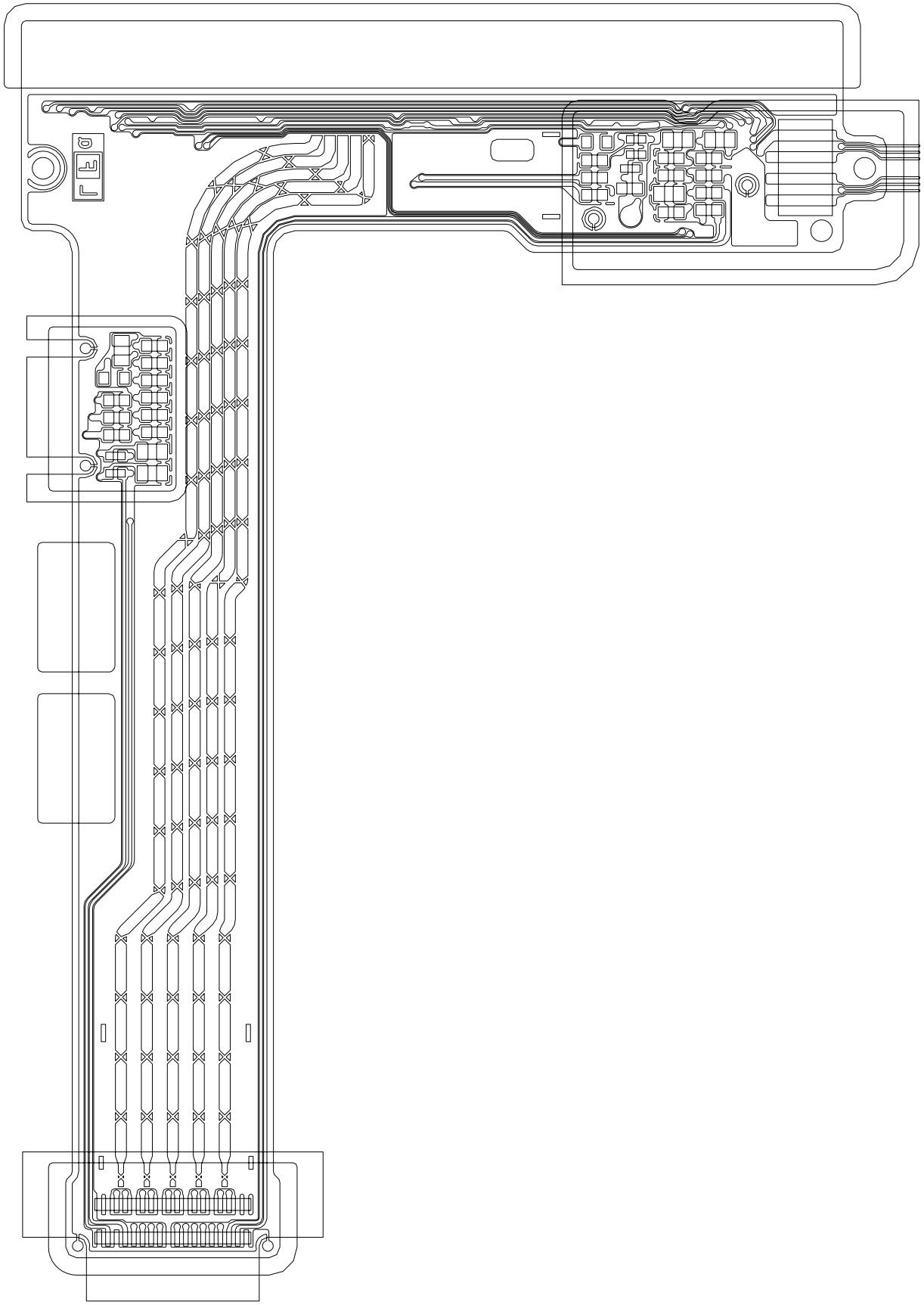


Fig.23 LCD- FPC layout2