SONY

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ACX318ELN

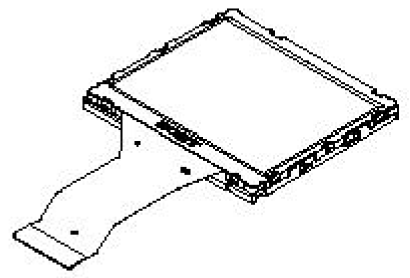
3.86cm (1.5-type) NTSC／PAL Color LCD Panel Module with LED Backlight

Description

The ACX318ELN is an LCD panel module with LED backlight developed exclusively for the ACX318ELN 3.86cm diagonal active matrix TFT-LCD panel Addressed by low temperature polycrystalline silicon transistors with built-in peripheral driving circuitry.

The LCD panel is driven with the reversed COM driving, realizes the lower voltage and the low power consumption.

The module provides full-color representation for NTSC and PAL systems. In addition, RGB dots are arranged in a delta pattern that provides smooth picture quality without fixed color patterns compared to vertical stripe and mosaic patterns.



Features

- Total module thickness : 2.68mm (typ.) ultra-thin, narrow frame type
- Low voltage, low power consumption with reversed COM driving : 8.5V drive , 13mW(panel block, typ.)
- Number of active dots : 118,000 dots, 3.86cm(1.5-type) in diagonal
- Center luminance Standard mode : 280cd/m^2 (backlight 158mW typ.)
  High luminance mode : 350cd/m^2 (backlight 216mW typ.)
- Horizontal resolution : 240 TV lines
- Optical transmittance : 11.0% (typ.)
- High contrast ratio with normally white mode : 200 (typ.)
- Built-in H and V driving circuitry (built-in input level conversion circuit, 3V drive possible)
- Smooth pictures with a RGB delta arrangement
- Supports NTSC/PAL
- Built-in picture quality improvement circuit
- Built-in negative voltage generation circuit
- LR(low reflectance) surface treatment provides an easy-to-see display even outdoors
- Dirt-resistant surface treatment
- Narrow frame

Element Structure

- Active matrix TFT-LCD panel with built-in peripheral driving circuitry using low temperature polycrystalline silicon transistors
- Number of pixels
  - Total number of dots : 494(H)×242(V) = 119,548
  - Number of active dots : 490(H)×240(V) = 117,600
- Module dimensions
  - Package dimensions : 36.96 (W)×32.72 (D)×2.685 (H) (mm)
  - Effective display dimensions : 31.115 (H)×22.860 (V) (mm)

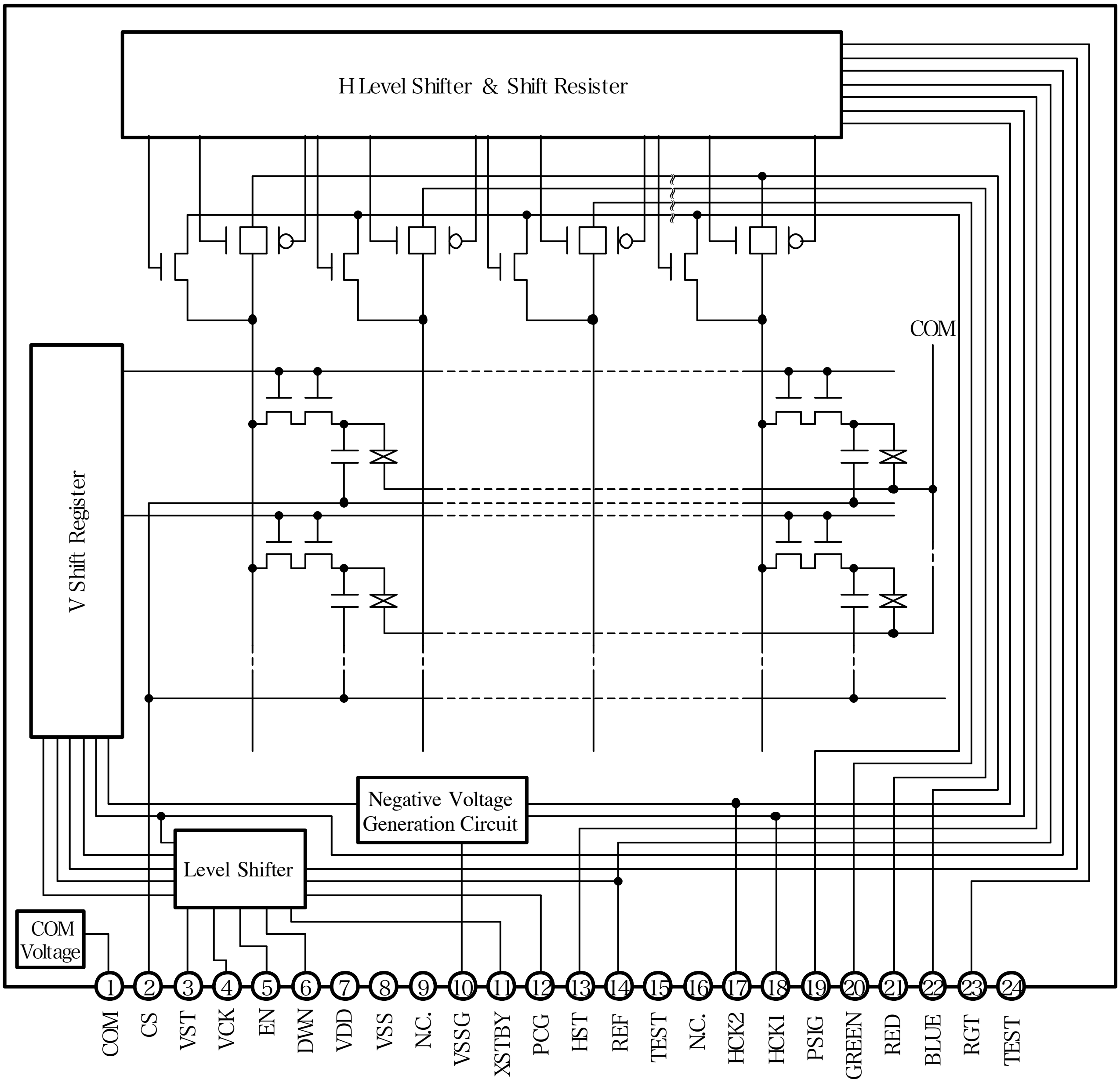
Applications

Compact digital still cameras, compact video cameras, etc.

Module Configuration

Panel Block Diagram

The panel block diagram is shown below.



Absolute Maximum Ratings (Vss=0V)

• H driver supply voltage	VDD	−1.0∼+10	V
• V driver boost supply voltage	VSSG	−7.0∼−1.0	V
• Common voltage of panel	COM	−1.0∼+10	V
• H driver input pin voltage	HST, HCK1, HCK2, PCG	−1.0∼+10	V
• V driver input pin voltage	VST, VCK, EN, REF	−1.0∼+10	V
• Standby input signal voltage	XSTBY	−1.0∼+10	V
• Video signal, uniformity improvement signal input pin voltage	GREEN, RED, BLUE, PSIG	−1.0∼+8.0	V
• Operating temperature	Topr	−10∼+60	℃
• Storage temperature	Tstg	−30∼+85	℃
• LED backlight DC forward voltage	Ifbl	30	mA
• LED backlight reverse withstand voltage	Vrbl	0	V

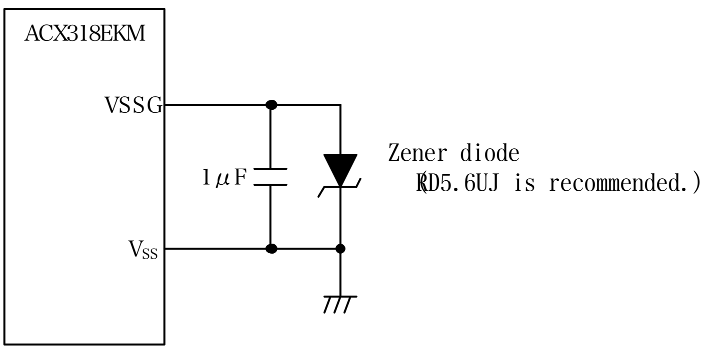
Operating Conditions of Panel Block

1. Input/output supply voltage conditions*1 (Vss=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	8.0	8.5	9.0	V
VSSG output voltage setting*2	VSSG	−6.0	−5.5	−5.0	V

*1 The V_{DD} typical voltage setting is noted as 8.5V in the above table.
*2 For the VSSG, output setting, connect an external smoothing capacitor and a voltage stabilizing Zener diode as shown in the figure below.

Recommended voltage applied example



2. Panel input voltage conditions

Item		Symbol	Min.	Typ.	Max.	Unit
H/V driver input voltage	(Low)	VIL	−0.3	0.0	0.3	V
	(High)	VIH	2.6	3.0	3.5	V
REF input voltage		VREF	VIH/2−0.3	VIH/2	VIH/2+0.3	V
Video signal center voltage		VVC		2.5		V
Video signal input range	Black(Low)	VsigL	0.8	1.0		V
	Black(High)	VsigH		4.0	4.2	V
	White-Black	VsigD		3.0		V
Uniformity improvement signal		Vpsig		2.5		V
Common voltage of panel		VCOMC	VVC-0.65	VVC-0.50	VVC-0.35	V
Common voltage range of panel		VCOMAC		4.0		V

Operating Conditions of Backlight Block

1. Input supply voltage conditions

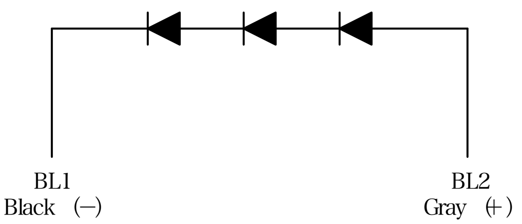
Standard mode : luminance 280cd/m² operation

Item	Symbol	Min.	Typ.	Max.	Unit
Backlight DC forward current	IfBL	—	15	—	mA
Backlight DC forward voltage	$Vfbl_{15}$	8.9	10.5	11.6	V
Backlight power consumption	Pbl_{15}	134	158	174	mW

High luminance mode : luminance 350cd/m² operation

Item	Symbol	Min.	Typ.	Max.	Unit
Backlight DC forward current	IfBL	—	20	—	mA
Backlight DC forward voltage	$Vfbl_{20}$	9.0	10.8	12.0	V
Backlight power consumption	Pbl_{20}	180	216	240	mW

Backlight equivalent circuit



Pin Description of Panel Block

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	COM	Common voltage input of panel	13	HST	Start pulse input for H shift resister drive
2	CS	画素容量共通電極電圧入力端子	14	REF	Level shifter circuit REF voltage input
3	VST	Start pulse input for V shift resister drive	15	TEST1	Panel test output ; no connection
4	VCK	Clock input for V shift resister drive	16	N.C.	No connection inside the panel
5	EN	Gate selection pulse enable input	17	HCK2	Clock input for H shift resister drive
6	DWN	V shift resister drive direction signal input	18	HCK1	Clock input for H shift resister drive
7	VDD	Power supply input for H and V driver	19	PSIG	Uniformity improvement signal input
8	VSS	H and V driver GND	20	GREEN	Video signal (G) input to panel
9	N.C.	No connection inside the panel	21	RED	Video signal (R) input to panel
10	VSSG	Negative power supply setting for V driver	22	BLUE	Video signal (B) input to panel
11	XSTBY	Standby signal input of panel	23	RGT	H shift resister drive direction signal input
12	PCG	Control pulse of uniformity improvement signal	24	TEST2	Panel test output ; no connection

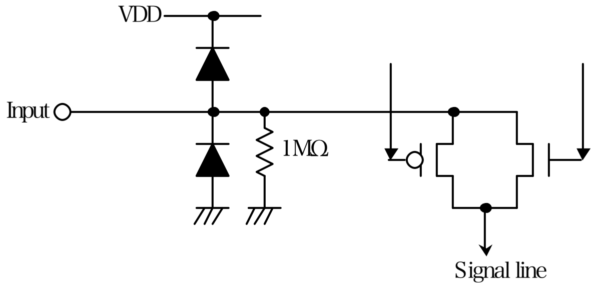
Pin Description of Backlight Block

Pin No.	Symbol	Description
1	BL1	Power supply GND for backlight lighting
2	BL2	Power supply input for backlight lighting

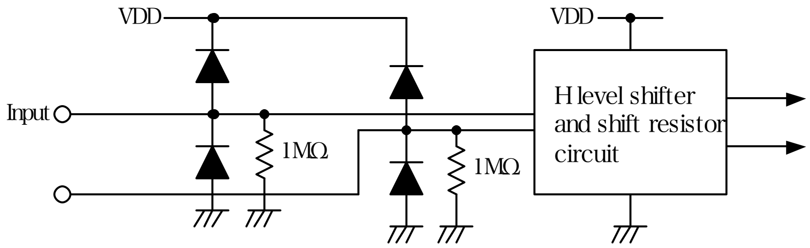
Input Equivalent Circuits of Panel Block

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal input pins. All pins are connected to VSS with a high resistance of 1MΩ (typ.). The equivalent circuit of each input is shown below; (Resistor value : typ.)

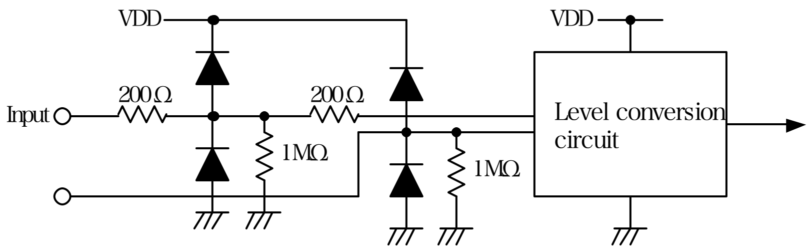
(1) RED, GREEN, BLUE, PSIG



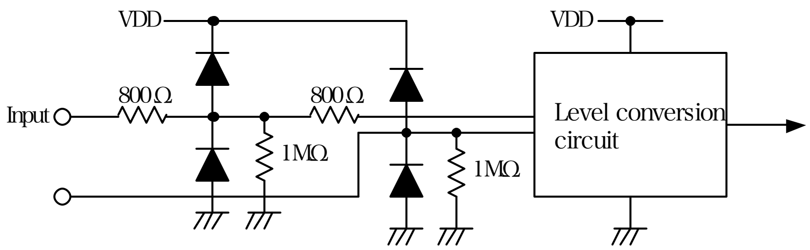
(2) HCK1, HCK2



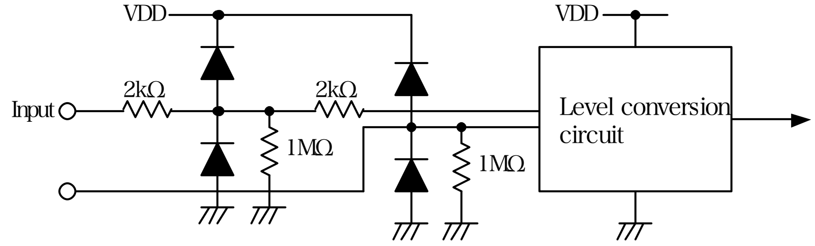
(3) HST, PCG, REF



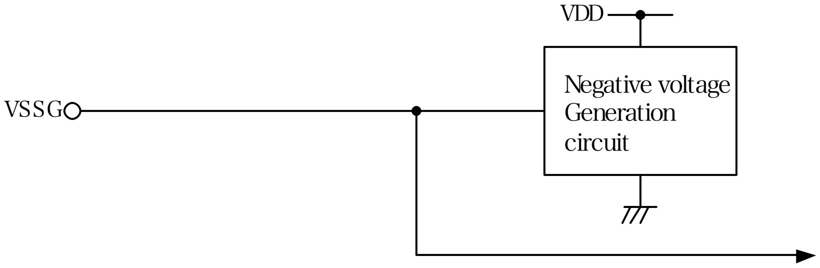
(4) VST, VCK, EN, XSTBY, REF



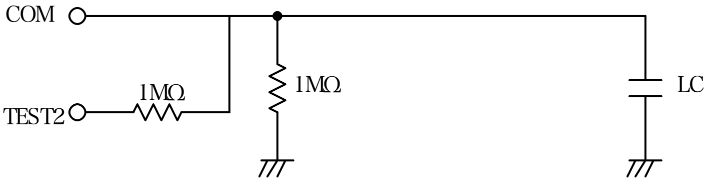
5) RGT, DWN, REF



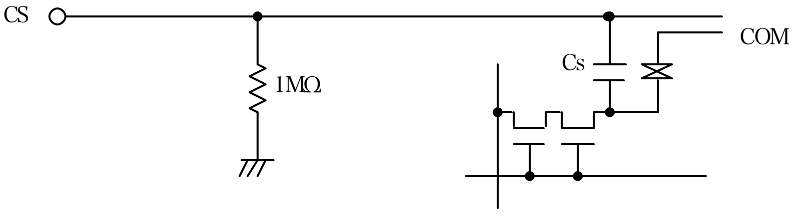
6) VSSG



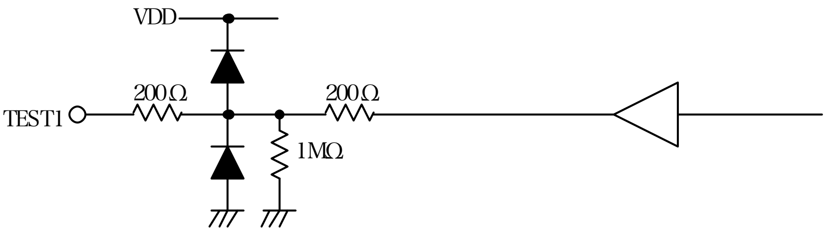
7) COM, TEST2



8) CS



9) TEST1

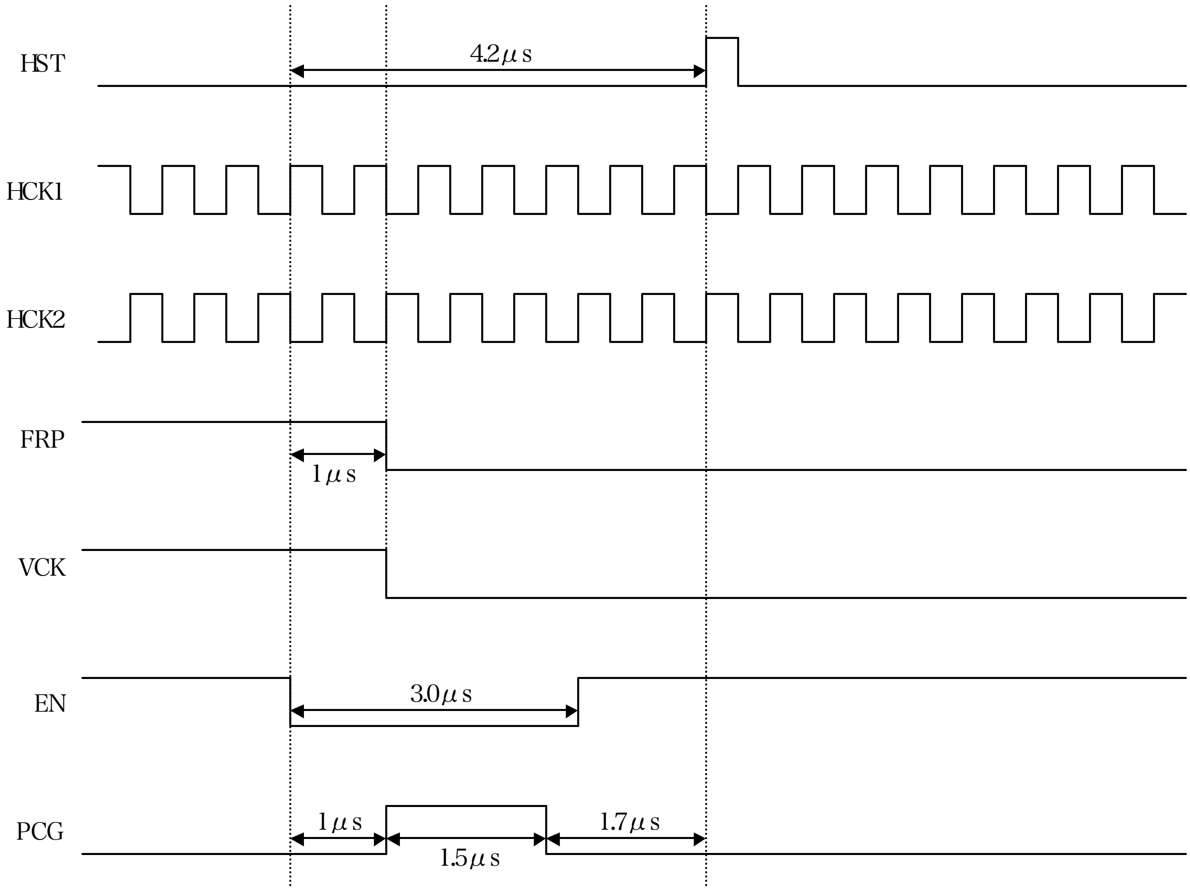


Clock Timing Conditions of Panel Block (VIH=3.0V、VDD=8.5V、Ta=25℃)

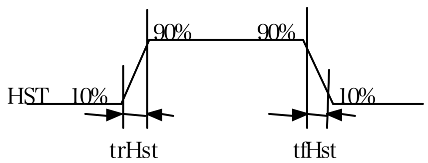
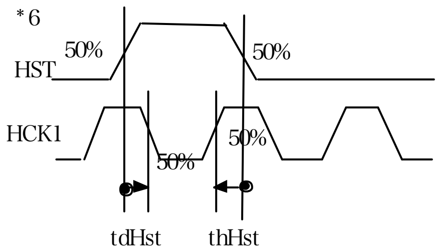
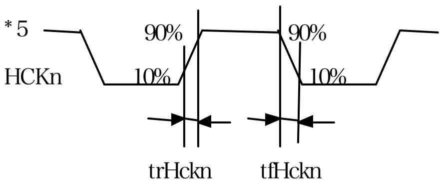
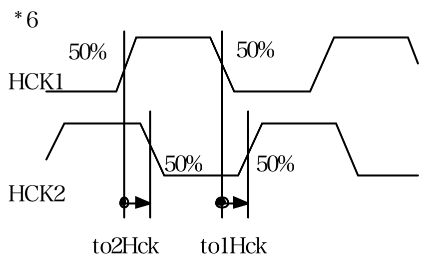
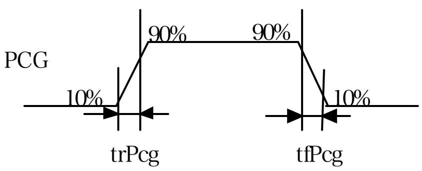
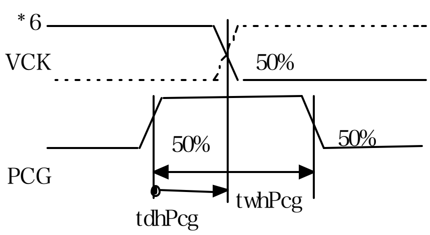
	Item	Symbol	Min.	Typ.	Max.	Unit
HST	HST rise time	trHst	-	-	30	ns
	HST fall time	tfHst	-	-	30	
	HST data setup time	tdHst	- 30	0	30	
	HST data hold time	thHst	- 30	0	30	
HCK	HCKn*5 rise time	trHckn	-	-	30	
	HCKn*5 fall time	tfHckn	-	-	30	
	HCK1 fall to HCK2 rise time	to1Hck	- 15	0	15	
	HCK1 rise to HCK2 fall time	to2Hck	- 15	0	15	
VST	VST rise time	trVst	-	-	100	
	VST fall time	tfVst	-	-	100	
	VST data setup time	tdVst	30	32	34	us
	VST data hold time	thVst	- 34	- 32	- 30	
VCK	VCK rise time	trVck	-	-	100	ns
	VCK fall time	tfVck	-	-	100	
EN	EN rise time	trEn	-	-	100	
	EN fall time	tfEn	-	-	100	
	EN fall to VCK rise/fall time	tdEn	900	1000	1100	
	EN pulse width	twEn	2900	3000	3100	
PCG	PCG rise time	trPcg	-	-	100	
	PCG fall time	tfPcg	-	-	100	
	PCG (H) rise to VCK rise/fall time	tdhPcg	- 0.1	0	0.1	us
	PCG (H) pulse width	twhPcg	1.4	1.5	1.6	

*5 HCKn means HCK1 and HCK2. (fHCKn=1.5MHz)

Horizontal Standard Timing



〈Horizontal Shift Resister Driving Waveforms〉

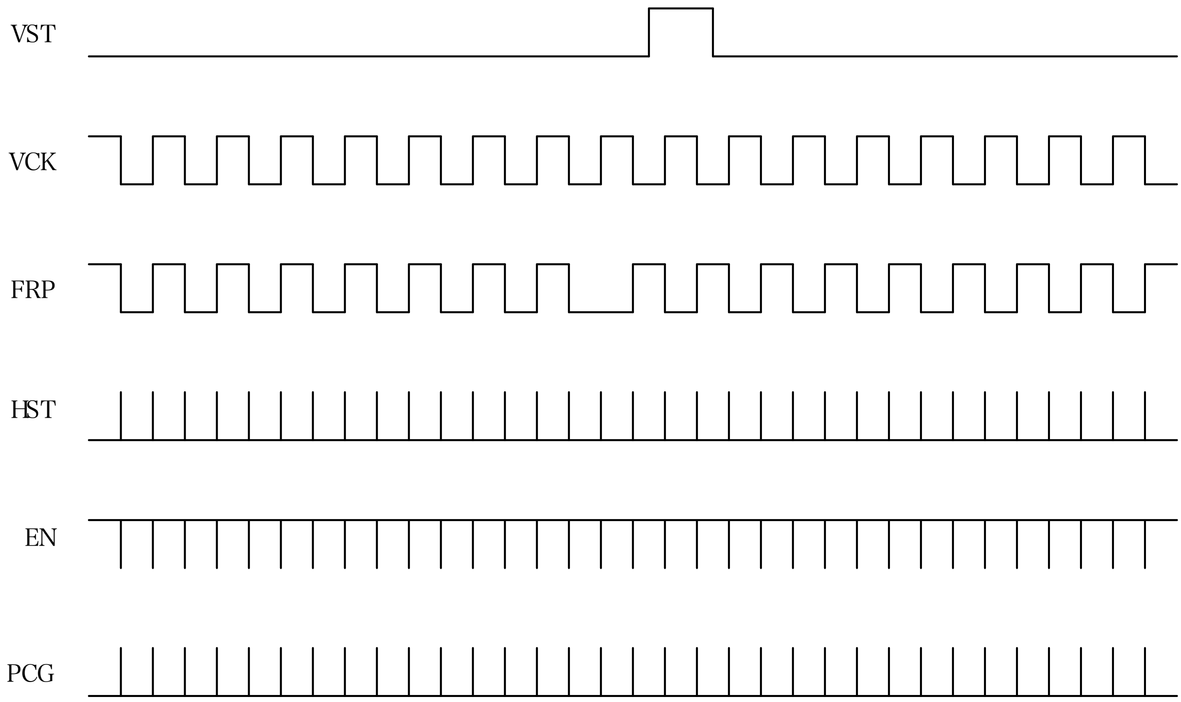
Item		Symbol	波形図	条件
HST	HST rise time	trHst		○ HCKn *5 duty cycle 50% to1Hck=0ns to2Hck=0ns
	HST fall time	tfHst		
	HST data setup time	tdHst		○ HCKn *5 duty cycle 50% to1Hck=0ns to2Hck=0ns
	HST data hold time	thHst		
HCK	HCKn *5 rise time	trHckn		○ HCKn *5 duty cycle 50% to1Hck=0ns to2Hck=0ns tdHst=333ns thHst=0ns
	HCKn *5 fall time	tfHckn		
	HCK1 fall to HCK2 rise time	to1Hck		○ tdHst=333ns thHst=0ns
	HCK1 rise to HCK2 fall time	to2Hck		
*7 PCG	PCG rise time	trPcg		
	PCG fall time	tfPcg		
	PCG rise to VCK rise/fall time	tdhPcg		
	PCG pulse width	twhPcg		

*6 Definitions;

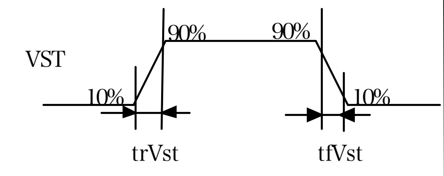
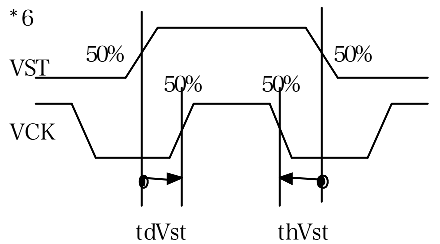
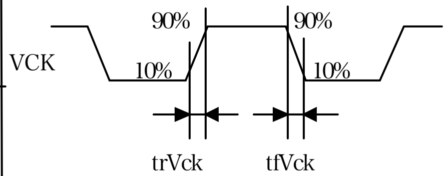
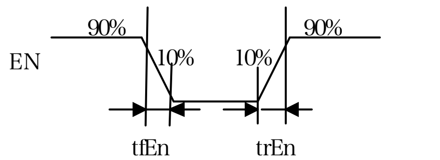
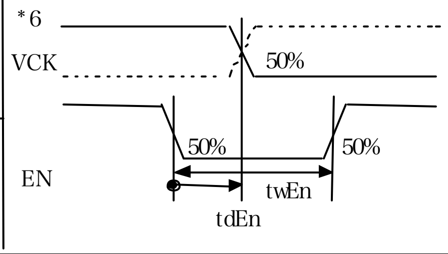
The right-pointing arrow (●→) means +.
The left-pointing arrow (←●) means -.
The black dot at an arrow (●) indicates the start of measurement.

*7 PCG represents every 1H pulse as shown in Horizontal Timing.

Vertical Standard Timing



〈Vertical Shift Resister Driving Waveforms〉

Item		Symbol	Waveform	Conditions
VST	VST rise time	trVst		○ VCK duty cycle 50% to1Vck=0ns to2Vck=0ns
	VST fall time	tfVst		
	VST data setup time	tdVst	＊6 	○ VCK duty cycle 50% to1Vck=0ns to2Vck=0ns
	VST data hold time	thVst		
VCK	VCK rise time	trVck		○ VCK duty cycle 50% to1Vck=0ns to2Vck=0ns tdVst=32μs thVst=32μs
	VCK fall time	tfVck		
EN	EN rise time	trEn		○ VCK duty cycle 50% to1Vck=0ns to2Vck=0ns
	EN fall time	tfEn		
	EN fall to VCK rise/fall time	tdEn	＊6 	
	EN pulse width	twEn		

Electrical Characteristic of Panel Block (Ta＝25℃, VDD＝8.5V, VIH＝3.0V, VREF＝1.5V)

1. Horizontal drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
HCKn input pin capacitance		CHckn	—	50	60	pF	
HST input pin capacitance		CHst	—	25	35	pF	
Video signal input pin capacitance		Csig	—	200	300	pF	
Psig input pin capacitance		Cpsig	—	2.4	3.0	nF	
Input pin current	HCK1	IHck1	−160	−80	—	μA	HCK1 : actual driving
	HCK2	IHck2	−160	−80	—	μA	HCK2 : actual driving
	HST	IHst	−100	−50	—	μA	HST＝GND
	RGT	IRgt	−3	−1	—	μA	RGT＝GND
	XSTBY	IXstby	−60	−30	—	μA	XSTBY＝GND
	REF	IREF	−300	−150	—	μA	REF＝VIH/2

HCKn : HCK1, HCK2 (1.5MHz)

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
VCK input pin capacitance		CVck	—	5	10	pF	
VST input pin capacitance		CVst	—	5	10	pF	
Input pin current	VCK	IVck	−100	−50	—	μA	VCK＝GND
	VST	IVst	−100	−50	—	μA	VST＝GND
	EN	IEn	−100	−50	—	μA	EN＝GND
	DWN	IDwn	−3	−1	—	μA	RGT＝GND
	PCG	IPcg	−100	−50	—	μA	PCG＝GND

3. Common pin capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Each pin－VSS input resistance	Ccom	---	8	12	nF

4. Total power consumption of the panel

Item		Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (NTSC)	(Ta＝25℃)	PWR25	—	15	17	mW
	(Ta＝60℃)	PWR60	—	—	23.5	mW

5 Pin input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
Pin – VSS resistance	Rin	0.5	1	—	MΩ

Electro-optical Characteristics of Module/Panel Block

(Ta=25°C, NTSC mode)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio			CR_{25}	1	150	200	—	—
Panel block optical transmittance[*1]			T	2		11.6	—	%
Center luminance	Iled=15mA		Lm_{15}	2	200	280	—	cd/m²
	Iled=20mA		Lm_{20}		250	350	—	
Chromaticity (Iled=15mA)	W	X	Wx	2	0.286	0.314	0.342	
		Y	Wy		0.284	0.327	0.370	
		Tc	Tcm		5000	6500	9700	K
		⊿uv	duvm		-0.020	0.002	-0.005	
	R	X	Rx	3	0.590	0.620	0.650	
		Y	Ry		0.310	0.340	0.370	
	G	X	Gx		0.300	0.330	0.360	
		Y	Gy		0.470	0.510	0.550	
	B	X	Bx		0.115	0.145	0.175	
		Y	By		0.090	0.140	0.190	
V-T characteristics[*1]	V_{90}	25°C	$V_{90\text{-}25}$	4	1.3	1.6	1.8	V
		60°C	$V_{90\text{-}60}$		1.3	1.5	1.7	
	V_{50}	25°C	$V_{50\text{-}25}$		1.7	1.9	2.1	
		60°C	$V_{50\text{-}60}$		1.5	1.7	1.9	
	V_{10}	25°C	$V_{10\text{-}25}$		2.1	2.3	2.5	
		60°C	$V_{10\text{-}60}$		2.0	2.2	2.4	
Half tone color reproduction range		R-G	V_{50RG}	5	-0.115	-0.080	-0.045	V
		B-G	V_{50BG}		0.00	0.03	0.05	
Response time[*1]	ON time	0°C	Ton0	6	—	70	90	Ms
		25°C	Ton25		—	21	30	
	OFF time	0°C	Toff0		—	120	180	
		25°C	Toff25		—	30	75	
Flicker[*1]		60°C	F	7	—	-60	-30	dB
Image retention time[*1,*2]		60°C, 2h	YT1	8	0	—	—	s
Viewing angle range		CR≧10	θT	9	15	20	—	Degree
			θB		50	60	—	
			θL		35	40	—	
			θR		35	40	—	
Surface reflection ratio		θ=0°	Rf	10	—	0.9	1.5	%
Cross talk[*1]		25°C	CTK	11	—	0.9	1.5	%

*1 Conforms to the measurement results for the discrete panel.
*2 Stress conditions : 60°C, 2h, Checker pattern
Evaluation conditions : After driving in the above conditions, the image retention is not found at the gray raster in 60°C.
(Judgment) In case of finding the image retention, the panel passes when it disappears , while driving in the below conditions.
Easing conditions : RT, 1h leaving → 60°C, 1h, driving at the gray raster

Electro-optical Characteristics of Backlight Block (Ta＝25℃, discrete backlight)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Backlight DC forward voltage	Ifbl＝15mA		$Vfbl_{15}$	—	8.9	10.5	11.6	V
	Ifbl＝20mA		$Vfbl_{20}$		9.0	10.8	12.0	
Backlight power consumption	Ifbl＝15mA		Pbl_{15}	—	134	158	174	mW
	Ifbl＝20mA		Pbl_{20}		180	216	240	
Backlight center luminance	Ifbl＝15mA		Lbl_{15}	—	2000	2800	—	cd/m^2
	Ifbl＝20mA		Lbl_{20}		2500	3500	—	
Backlight center chromaticity	Ifbl＝15mA	X	Xbl	12	0.280	0.295	0.310	
		Y	Ybl		0.260	0.285	0.310	
		Tc	Tcbl		6800	8500	—	K
		⊿uv	Duvbl		-0.005	-0.006	—	
Backlight luminance uniformity	Ifbl＝15mA		BLunif	13	60	—	—	%
Backlight life (Luminance half-life)	Ifbl＝15mA	Ta=less than 55°C	BLl_{1555}	14	5000	—	—	hr
		Ta=55°C to 70°C	BLl_{1570}		1000	—	—	
	Ifbl＝20mA	Ta=less than 40°C	BLl_{2040}		5000	—	—	
		Ta=40°C to 60°C	BLl_{2060}		1000	—	—	

<Panel/Module/Backlight Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage
VDD=8.5V, VIH=3.0V, VREF=1.5V
VVC=2.5V, VCOM=2.0±2.0V, Vpsig=2.5V

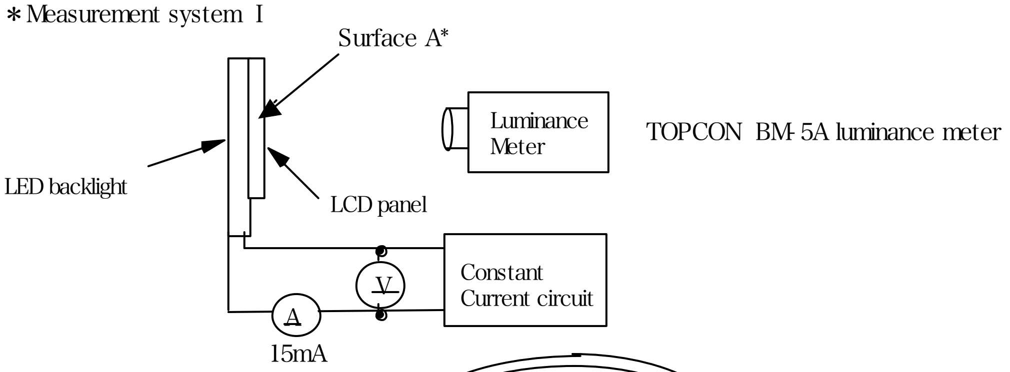
(2) Measurement temperature
25°C unless otherwise specified.

(3) Measurement point
One point in the center of the screen unless otherwise specified.

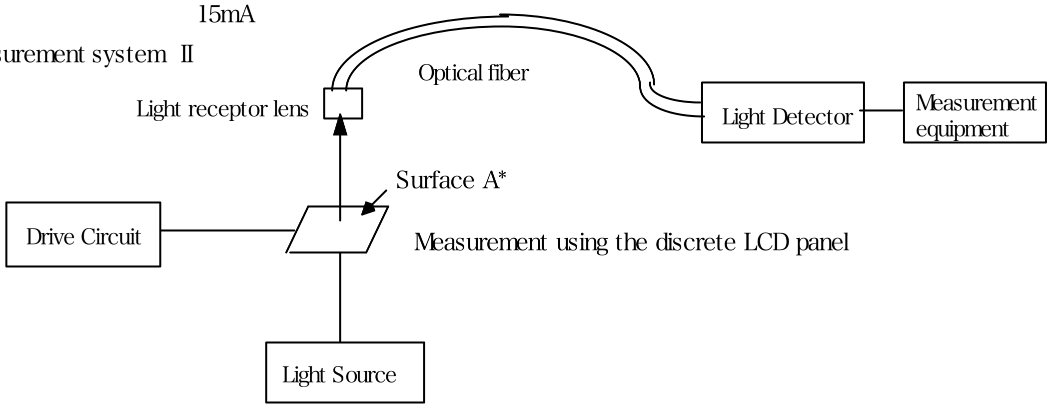
(4) Measurement systems
Three types of measurement systems are used as shown below.

(5) R, G and B input signal voltage Vsig
Vsig=VVC±V_{AC} (V) (V_{AC} : signal amplitude)

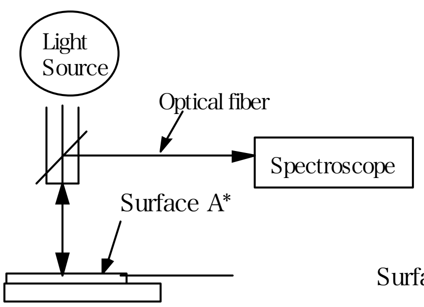
* Measurement system I



* Measurement system II



* Measurement system III



Surface A* : See the Package Outline

1. Contrast Ratio

Contrast ratio (CR) is given by the following formula.

$$CR = \frac{L\ (White)}{L\ (Black)}$$

2. Optical Transmittance of Panel, Center Luminance of Module, Color Temperature

Optical Transmittance (T) is given by the following formula.

$$T = \frac{L(\text{White})}{\text{Luminance of Backlight}} \times 100 \quad (\%)$$

L(White) is the same expression as defined in "Contrast Ratio".

Lm =White luminance at the center of the panel
Tcm=Color temperature at the center of the panel

Measured by System I using the TOPCON BM-5A.

3. Chromaticity

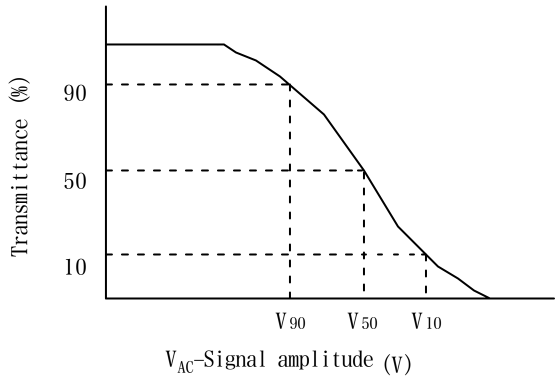
Chromaticity of the panels is measured by System I. Raster modes of each color are defined by the representations at the input signal amplitude conditions shown in the table below. System I uses x and y of the CIE standards as the chromaticity here.

		Signal amplitudes (VVC±Vac) supplied to each input		
		R input	G input	B input
Raster	R	2.5±1.5V	2.5∓1.5V	2.5∓1.5V
	G	2.5∓1.5V	2.5±1.5V	2.5∓1.5V
	B	2.5∓1.5V	2.5∓1.5V	2.5±1.5V
	W	2.5±1.5V	2.5±1.5V	2.5±1.5V

Vcom 2.0±2V (Unit : V)

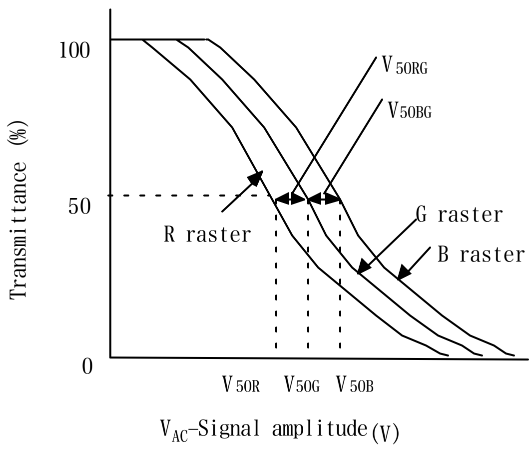
4. V-T Characteristics

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panel, are measured by System II by inputting the same signal amplitude V_{AC} to each input pin. V_{90}, V_{50}, and V_{10} correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.



5. Half Tone Color Reproduction Range

The half tone color reproduction range of LCD panels is characterized by the differences between the V-T characteristics of R, G and B. The differences of these V-T characteristics are measured by System II.
System II defines signal voltages of each R, G and B raster mode which correspond to 50% of transmittance, V_{50R}, V_{50G} and V_{50B}, respectively. V_{50RG} and V_{50BG}, that is to say the differences between V_{50R} and V_{50G} and between V_{50B} and V_{50G}, are given by the following formulas respectively.



$$V_{50RG} = V_{50R} - V_{50G}$$
$$V_{50BG} = V_{50B} - V_{50G}$$

6. Response Time

Response times ton and toff are measured by System II by applying the input signal voltages in the figure to the right to each input pin. These times are defined by the following formulas.

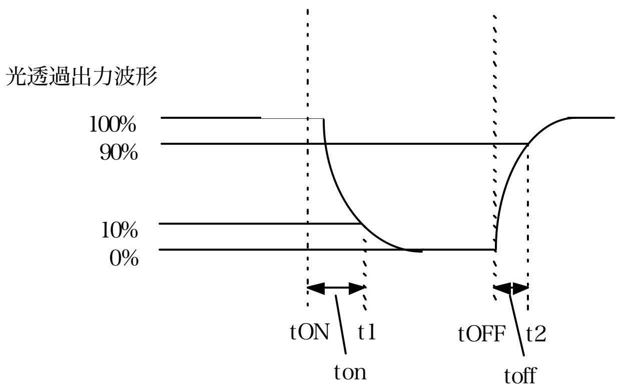
ton = t1 − tON

toff = t2 − tOFF

t1: time which gives 10%transmittance of the panel.
t2: time which gives 90%transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the figure to the right.

Input signal voltage(Waveform applied to measured pixels)



7. Flicker

Flicker(F) is given by the following formula. DC and AC components(NTSC:30Hz, rms; PAL:25Hz, rms) of the panel output signal for gray raster mode are measured by a DC voltmeter and a spectrum analyzer in System II.

$$F\ (dB) = 20\log\left\{\frac{\text{AC component}}{\text{DC component}}\right\}$$

＊R, G, B input signal voltage for gray raster mode is given by V_{sig} Vsig=6.0±V_{50} (V)

where: V50 is the signal amplitude which gives 50%of transmittance in V-T curve.

8. Image Retention Time

Image retention time is given by the following procedures.
Apply the checker pattern to the LCD panel for 2 hours in 60°C and then change to a gray scale signal
Vsig = 6.0±V_{AC} (V_{AC}: 3 ～ 4V)

Judging by sight at the VAC that holds the maximum image retention, measure the time for the residual image to disappear.

Easing conditions :RT, 1h leaving → 60°C, 1h, driving at the gray raster

In case of finding the image retention, the panel passes when it disappears , while driving in the above conditions.

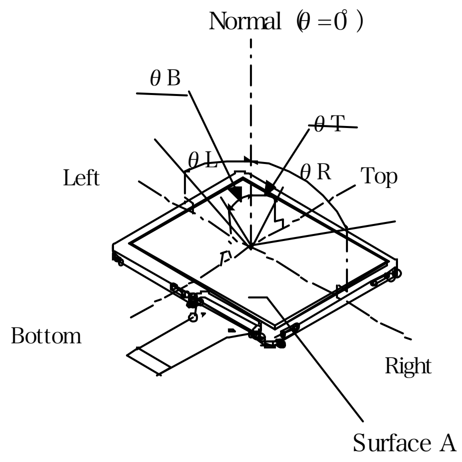
＊Input conditions of the checker pattern
Vsig = 2.5± 1.5 / ∓ 1.5 (V)

VCOM=2.0±2V

9. Definition of Viewing Angle Range

Viewing angle range is measured by System I. The Contrast ratio(CR) is measured at the angles defined in the figure to the right and the range where CR≧10 is taken as the viewing angle range. Measure with surface A* facing upwards.

*Surface A : See the Package Outline.



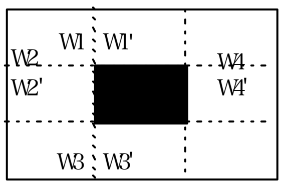
10. Surface Reflection Ratio

Surface reflection ratio(Rf) is given the following formula.

$$Rf = \frac{\text{Reflected optical luminance of the panel surface A*}}{\text{Reflected optical luminance of Al(wafer)}} \times 100 \quad (\%)$$

11. Cross Talk

Cross talk is determined by the luminance differences between adjacent areas represented by Wi' and Wi(i = 1 to 4) around the black window(Vsig = 4.0V/ 1V)



$$\text{Cross talk value CTK=} \left| \frac{Wi' - Wi}{Wi} \right| \text{x100 } (\%)$$

12. Backlight Center Luminance and Chromaticity Measurement Method

1.Environmental conditions

Temperature : 25±5°C

Humidity : 30 to 85%

Start measurement after leaving the module in the above environment for one hour.

Measurement should be performed in a dark room with a luminance of 10 lx or less and which is not subject to the effects of reflective or external light

There should be no heat insulating objects around the module units, and measurement should be performed in a draftless conditions.

2.Luminance and chromaticity measurement method

Measurement equipment : TOPCON BM-5A, viewing angle : 0.2°, distance : 450±50mm

Measure 30s after the backlight is lit.

Using a contrast current circuit, measure the luminance under both conditions of Ifbl = 15mA and 20mA, and measure the chromaticity under only the condition of Ifbl = 15mA.

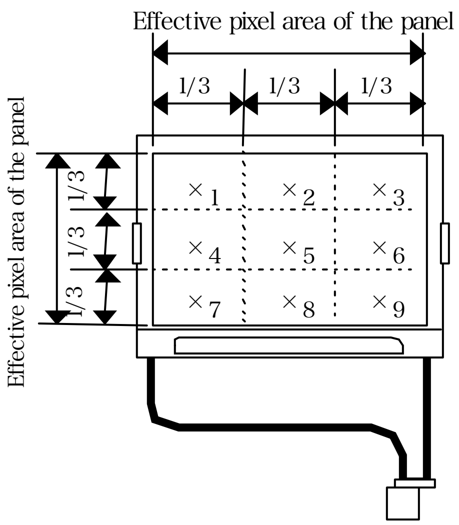
13. Backlight Luminance Uniformity Measurement Method

1.Environmental conditions

Measure under the same conditions as "12.Backlight Center Luminance and Chromaticity Measurement Method" above.

2.Light the backlight at Ifbl = 15mA using a constant current circuit, and start measurement 30s after the backlight is lit.

Backlight luminance uniformity is obtained by dividing the effective pixel area into 9 equal sections as shown below, measuring the luminance at each of the centers 1 to 9, and calculating Min. luminance ÷ Max. luminance x 100 (%).



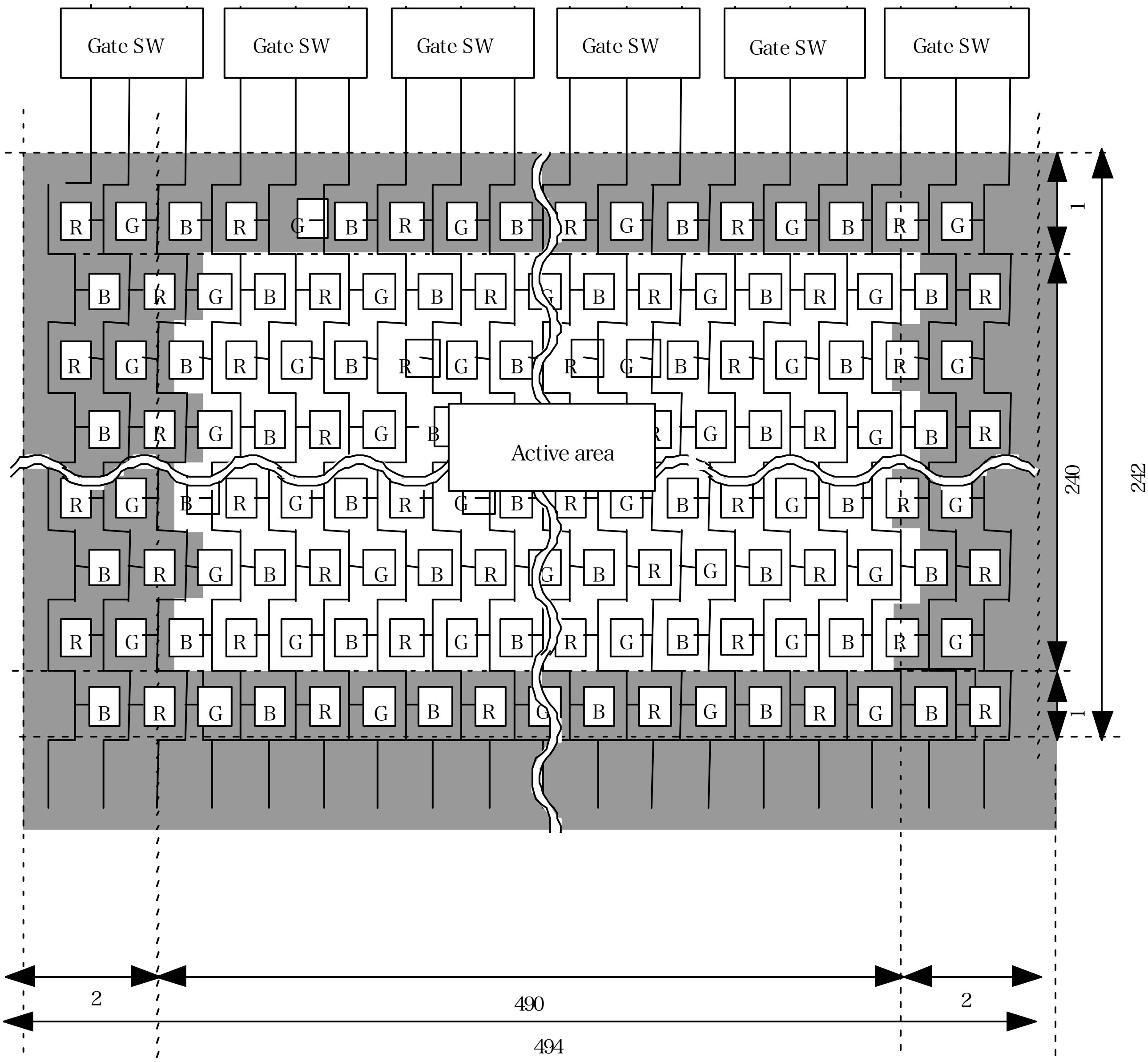
14. Backlight Life

Definition of life : When the backlight center luminance drops to 50% of the initial value.

Description of Panel Block Operation

1. Color Coding

The color filters are coded in a delta arrangement. The shaded area is used for the dark border around the display.



2. Description of LCD Panel Operations

·A vertical driver , which consists of vertical shift registers, enable- gates and buffers, applies a selected pulse to each of 240 line electrodes sequentially one line electrode at a time in a single horizontal scanning period.

·The selected pulse is output when the enable pin goes to high level. PAL signal pulse elimination display is possible by using the enable pin and simultaneously controlling VCK.

·A horizontal driver, which consists of horizontal shift resisters , gates and CMOS sample-and- hold circuitry, applies selected pulses to each of 490 signal electrodes sequentially in a single horizontal scanning period.
These pulses are used to supply the sampled video signal to the low signal lines.

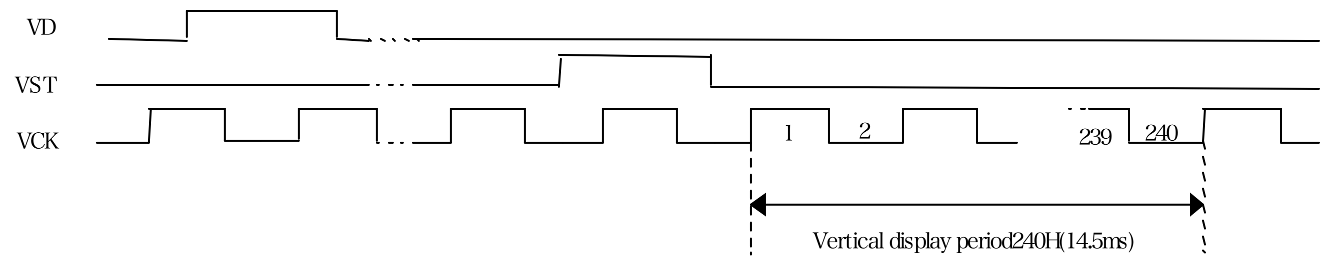
·The vertical and horizontal drivers address one pixel, and then thin film transistors turn on to apply a video signal to the pixel. The same procedures lead to the entire 240 x 490 pixels to display a picture in a vertical scanning period.

·Pixel dots are arranged in a delta pattern, where sets of RGB pixels are positioned shifted by 1.5 dots against adjacent horizontal lines. The horizontal driver output pulse must be shifted by 1.5 dots for each horizontal line against horizontal sync signal to apply a video signal to each pixel properly.

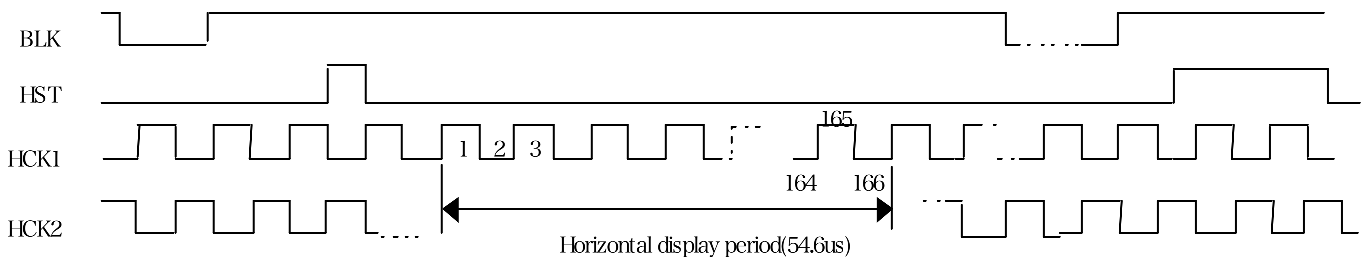
·The video signal should be input with the polarity-inverted every horizontal cycle.

·The relationships between the vertical shift register start pulse VST and the vertical display period, and between the horizontal shift register start pulse HST and the horizontal display period are shown below for top to bottom and left to right scan.

(1) Vertical display period



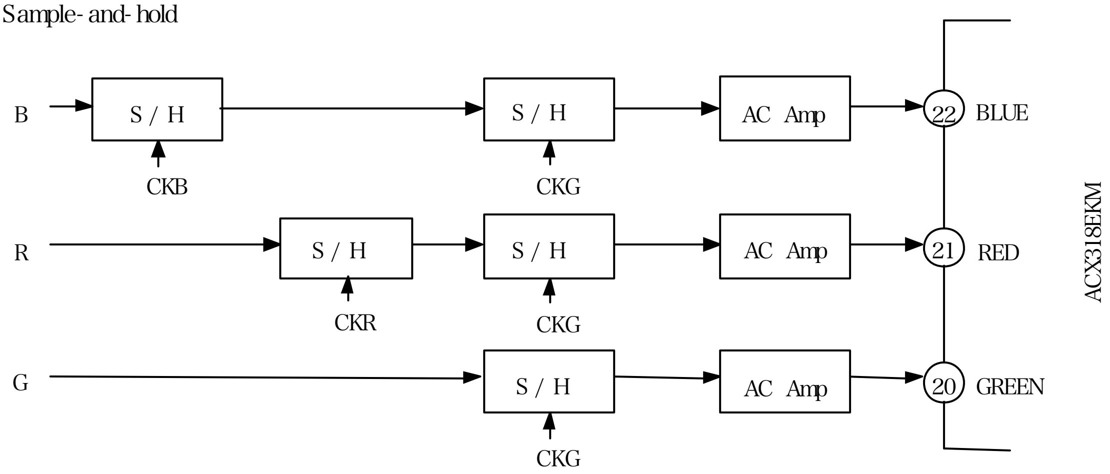
(2) Horizontal display period



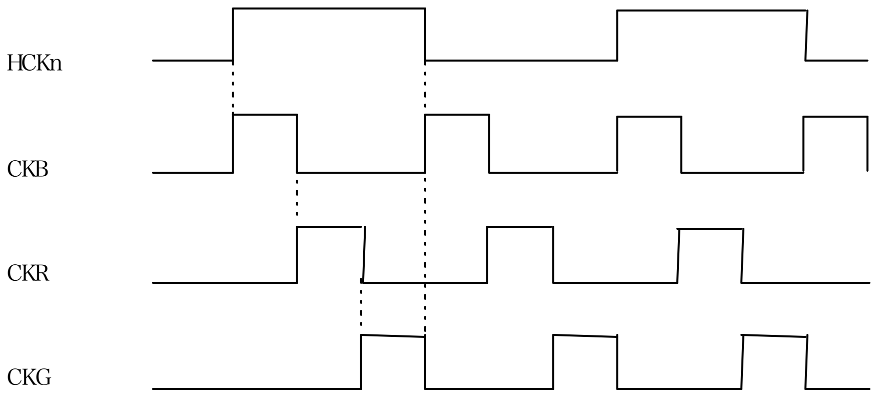
3. RGB Simultaneous Sampling

The horizontal driver samples, R, G and B video signals simultaneously, which requires phase matching between the R, G and B signals to prevent the horizontal resolution from deteriorating. Thus phase matching by an external signal delay circuit is needed before applying the video signal to the LCD panel.
Two methods are applied for the delaying procedure : Sample-and-hold and Delay circuit. These two block diagrams are as follows

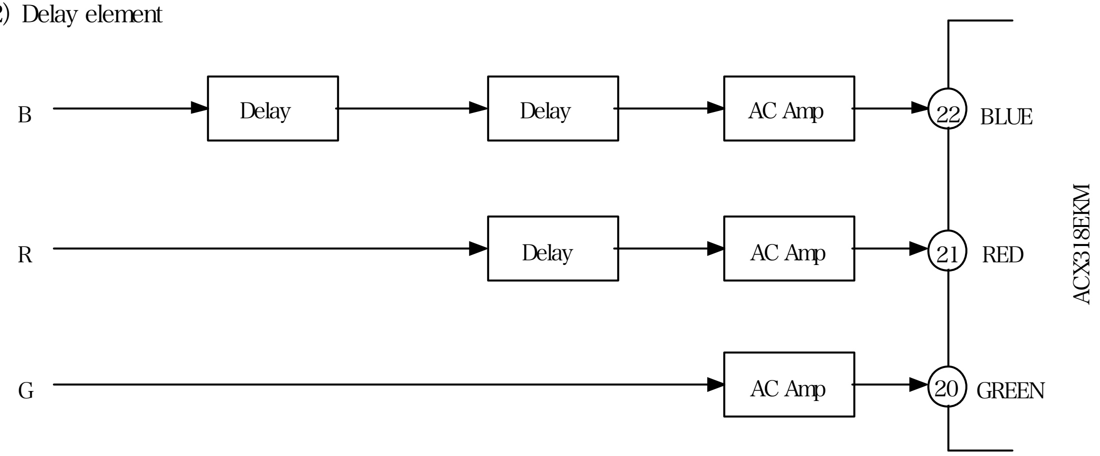
(1) Sample-and-hold



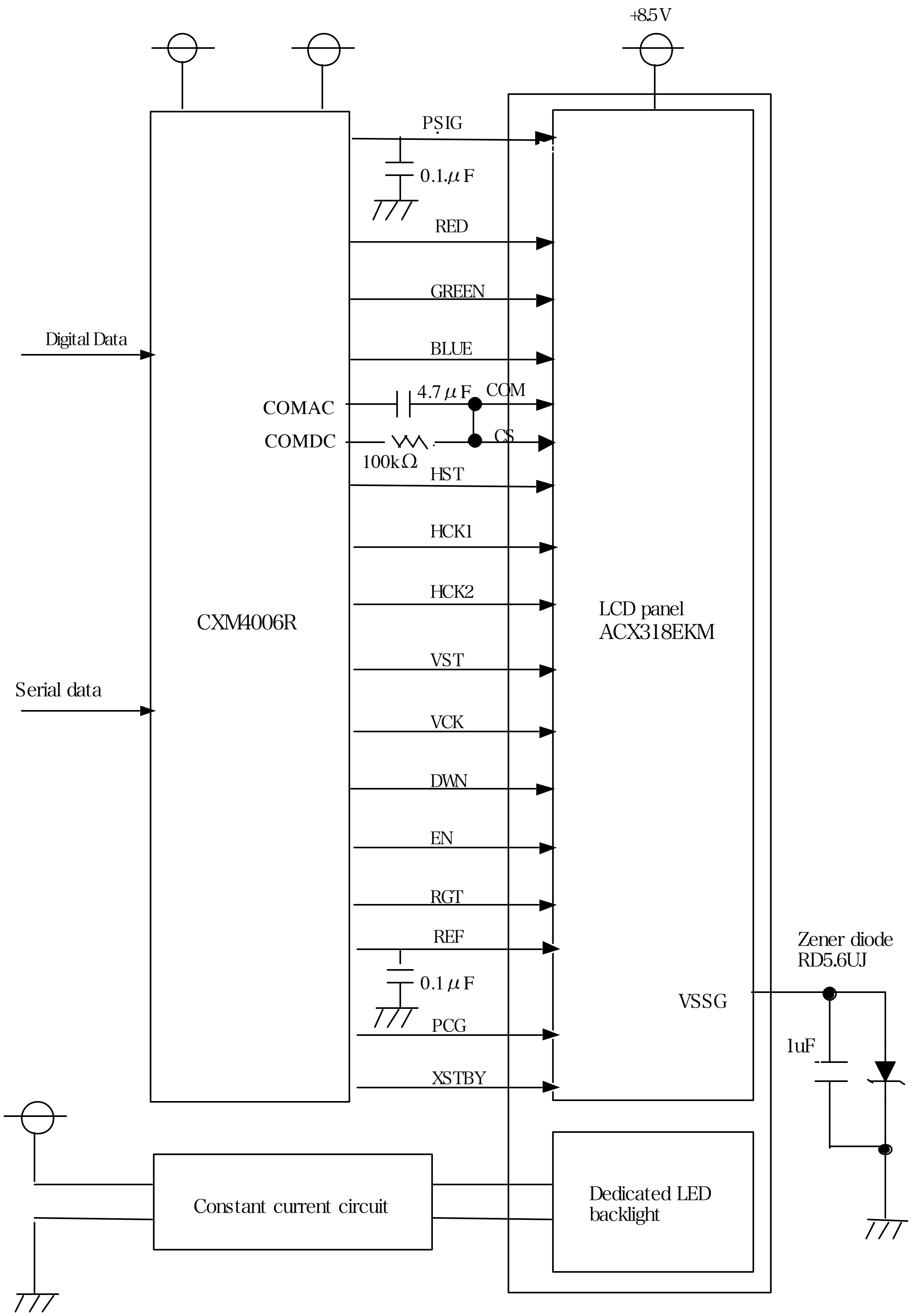
<Phase relationship of delaying sample-and-hold pulses>



(2) Delay element



System Configuration



LCD module with backlight

Notes on Handling

(1) Static charge prevention
Be sure to take the following protective measures. TFT-LCD panels and LED backlights are easily damaged by static charges.
a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install grounded conductive mats on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

(2) Protection from dust and dirt
a) Operate in a clean environment.
b) When delivered, the panel surface (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the panel.
c) Do not touch the polarizer surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
d) Use ionized air to blow dust off the panel.

(3) Module fixing method
a) The following items should be taken into account for the positioning guide design.
·The design reference edges are the upper and left edges of the panel as viewed from the front. Design the guides using the panel frame as the reference and not the backlight.
·Set the guides on the same side of the set as the monitor window frame.
·To prevent LCD image unevenness, the guides should be the maximum package tolerance or more so that a clasping load is not applied to the panel from the x and y directions.
·Make sure the guides do not block the panel FPC outlet and backlight lead wire outlet.
b) The guaranteed area of the polarizer is the outer circumference of 0.7mm of the effective display area(Fig.1). Design the monitor window frame of the set so that it is within this range including variance.
c) Set the holders on the rear of the backlight around the circumference as far from the center of the backlight as possible. Local pressure applied to the center of the rear of the backlight for an extended period may result in uneven luminance, so the holder pressure on the center of the backlight should be 500g/cm^2 or less.
d) Connect the panel or backlight frame to GND.
e) Use a design that does not repeatedly bend or place stress on the backlight lead wires(maximum load in the lead wire pull-out direction: 500g) as this may cause lead wire disconnection at the solder junction on the backlight unit side.(Forced bending of 90° or more is permitted up to 2 times, and repeated bending of 45° up to 8 times.)

(4) Others
a) Do not twist and bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop the panel or backlight.
c) Do not twist and bend the panel, panel frame or backlight.
d) Keep the panel and backlight away from heat sources.
e) Do not dampen the panel or backlight with water or other solvents.
f) Avoid storage or use of the panel at high temperatures or high humidity, as this may result in damage.

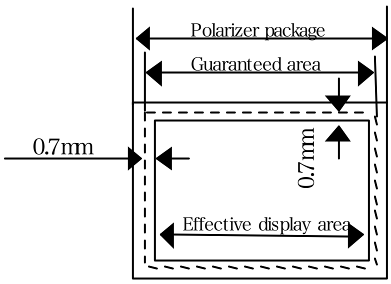


Fig.1