SONY

ACX318ELN

3.86cm (1.5-type) NTSC/PAL Color LCD Panel Module with LED Backlight

Description
The ACX318ELN is an LCD panel module with LED backlight developed exclusively for the ACX318ELN. It features a 3.86cm diagonal active matrix TFT-LCD panel. Addressed by low-temperature polycrystalline silicon thin-film transistors with built-in peripheral driving circuitry, the LCD panel is driven with a reversed COM driving scheme, resulting in lower voltage consumption and low power consumption.

The module provides full-color representation for NTSC and PAL systems. In addition, RGB dots are arranged in a delta pattern that provides smooth picture quality without fixed color patterns compared to vertical stripe and mosaic patterns.

Features
- Total module thickness: 2.68mm (typ.) ultra-thin, narrow frame type
- Low voltage, low power consumption with reversed COM driving: 8.5V drive, 13mW (panel block, typ.)
- Number of active dots: 118,000 dots, 3.86cm (1.5-type) in diagonal
- Center luminance: Standard mode: 280cd/m² (backlight 158mW typ.)
  High luminance mode: 350cd/m² (backlight 216mW typ.)
- Horizontal resolution: 240 TV lines
- Optical transmittance: 11.0% (typ.)
- High contrast ratio with normally white mode: 200 (typ.)
- Built-in H and V driving circuitry (built-in input level conversion circuit, 3V drive possible)
- Smooth pictures with a RGB delta arrangement
- Supports NTSC/PAL
- Built-in picture quality improvement circuit
- Built-in negative voltage generation circuit
- LR (low reflectance) surface treatment provides an easy-to-see display even outdoors
- Dirt-resistant surface treatment
- Narrow frame

Element Structure
- Active matrix TFT-LCD panel with built-in peripheral driving circuitry using low-temperature polycrystalline silicon transistors
- Number of pixels
  - Total number of dots: 494(H) x 242(V) = 119,548
  - Number of active dots: 490(H) x 240(V) = 117,600
- Module dimensions
  - Package dimensions: 36.96(W) x 32.72(D) x 2.685(H) mm
  - Effective display dimensions: 31.115(H) x 22.800(V) mm

Applications
Compact digital still cameras, compact video cameras, etc.

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Module Configuration

Panel Block Diagram

The panel block diagram is shown below.
Absolute Maximum Ratings  \( V_{SS} = 0V \)

- H driver supply voltage  \( VDD \)  \(-1.0 \sim +10 \)  V
- V driver boost supply voltage  \( VSSG \)  \(-7.0 \sim -1.0 \)  V
- Common voltage of panel  COM  \(-1.0 \sim +10 \)  V
- H driver input pin voltage  HST, HCK1, HCK2, PCG  \(-1.0 \sim +10 \)  V
- V driver input pin voltage  VST, VCK, EN, REF  \(-1.0 \sim +10 \)  V
- Standby input signal voltage  XSTBY  \(-1.0 \sim +10 \)  V
- Video signal, uniformity improvement signal input pin voltage  GREEN, RED, BLUE, PSIG  \(-1.0 \sim +8.0 \)  V
- Operating temperature  Topr  \(-10 \sim +60 \)  °C
- Storage temperature  Tstg  \(-30 \sim +85 \)  °C
- LED backlight DC forward voltage  Ifbl  30 mA
- LED backlight reverse withstand voltage  Vrbl  0 V

Operating Conditions of Panel Block

1. Input/output supply voltage conditions*1  \( V_{SS} = 0V \)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>( VDD )</td>
<td>8.0</td>
<td>8.5</td>
<td>9.0</td>
<td>V</td>
</tr>
<tr>
<td>VSSG output voltage setting*2</td>
<td>VSSG</td>
<td>(-6.0 )</td>
<td>(-5.5 )</td>
<td>(-5.0 )</td>
<td>V</td>
</tr>
</tbody>
</table>

*1 The \( VDD \) typical voltage setting is noted as 8.5V in the above table.

*2 For the VSSG, output setting, connect an external smoothing capacitor and a voltage stabilizing Zener diode as shown in the figure below.

Recommended voltage applied example

![Recommended voltage applied example](image_url)
2. Panel input voltage conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>H/V driver input voltage (Low)</td>
<td>VIL</td>
<td>0.3</td>
<td>0.0</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>H/V driver input voltage (High)</td>
<td>VIH</td>
<td>2.6</td>
<td>3.0</td>
<td>3.5</td>
<td>V</td>
</tr>
<tr>
<td>REF input voltage</td>
<td>VREF</td>
<td>VIH/2−0.3</td>
<td>VIH/2</td>
<td>VIH/2+0.3</td>
<td>V</td>
</tr>
<tr>
<td>Video signal center voltage</td>
<td>VVC</td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Video signal input range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Black (Low) VsigL</td>
<td></td>
<td>0.8</td>
<td>1.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Black (High) VsigH</td>
<td></td>
<td>4.0</td>
<td>4.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>White-Black VsigD</td>
<td></td>
<td>3.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Uniformity improvement signal</td>
<td>Vpsig</td>
<td>2.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Common voltage of panel</td>
<td>VCOMC</td>
<td>VVC-0.65</td>
<td></td>
<td>VVC-0.35</td>
<td>V</td>
</tr>
<tr>
<td>Common voltage range of panel</td>
<td>VCOMAC</td>
<td>4.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

Operating Conditions of Backlight Block

1. Input supply voltage conditions

**Standard mode: luminance 280cd/m² operation**

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Backlight DC forward current</td>
<td>ItBL</td>
<td></td>
<td>15</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Backlight DC forward voltage</td>
<td>Vibi15</td>
<td>8.9</td>
<td>10.5</td>
<td>11.6</td>
<td>V</td>
</tr>
<tr>
<td>Backlight power consumption</td>
<td>Plb15</td>
<td>134</td>
<td>158</td>
<td>174</td>
<td>mW</td>
</tr>
</tbody>
</table>

**High luminance mode: luminance 350cd/m² operation**

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Backlight DC forward current</td>
<td>ItBL</td>
<td></td>
<td>20</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Backlight DC forward voltage</td>
<td>Vibi30</td>
<td>9.0</td>
<td>10.8</td>
<td>12.0</td>
<td>V</td>
</tr>
<tr>
<td>Backlight power consumption</td>
<td>Plb30</td>
<td>180</td>
<td>216</td>
<td>240</td>
<td>mW</td>
</tr>
</tbody>
</table>

Backlight equivalent circuit

```
  BL1
Black (−)   BL2
Gray (+)
```
### Pin Description of Panel Block

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>COM</td>
<td>Common voltage input of panel</td>
<td>13</td>
<td>HST</td>
<td>Start pulse input for H shift resister drive</td>
</tr>
<tr>
<td>2</td>
<td>CS</td>
<td>画素容量共通電極電圧入力端子</td>
<td>14</td>
<td>REF</td>
<td>Level shifter circuit REF voltage input</td>
</tr>
<tr>
<td>3</td>
<td>VST</td>
<td>Start pulse input for V shift resister drive</td>
<td>15</td>
<td>TEST1</td>
<td>Panel test output ; no connection</td>
</tr>
<tr>
<td>4</td>
<td>VCK</td>
<td>Clock input for V shift resister drive</td>
<td>16</td>
<td>N.C.</td>
<td>No connection inside the panel</td>
</tr>
<tr>
<td>5</td>
<td>EN</td>
<td>Gate selection pulse enable input</td>
<td>17</td>
<td>HCK2</td>
<td>Clock input for H shift resister drive</td>
</tr>
<tr>
<td>6</td>
<td>DWN</td>
<td>V shift resister drive direction signal input</td>
<td>18</td>
<td>HCK1</td>
<td>Clock input for H shift resister drive</td>
</tr>
<tr>
<td>7</td>
<td>VDD</td>
<td>Power supply input for H and V driver</td>
<td>19</td>
<td>PSIG</td>
<td>Uniformity improvement signal input</td>
</tr>
<tr>
<td>8</td>
<td>VSS</td>
<td>H and V driver GND</td>
<td>20</td>
<td>GREEN</td>
<td>Video signal (G) input to panel</td>
</tr>
<tr>
<td>9</td>
<td>N.C.</td>
<td>No connection inside the panel</td>
<td>21</td>
<td>RED</td>
<td>Video signal (R) input to panel</td>
</tr>
<tr>
<td>10</td>
<td>VSSG</td>
<td>Negative power supply setting for V driver</td>
<td>22</td>
<td>BLUE</td>
<td>Video signal (B) input to panel</td>
</tr>
<tr>
<td>11</td>
<td>XSTBY</td>
<td>Standby signal input of panel</td>
<td>23</td>
<td>RGT</td>
<td>H shift resister drive direction signal input</td>
</tr>
<tr>
<td>12</td>
<td>PCG</td>
<td>Control pulse of uniformity improvement signal</td>
<td>24</td>
<td>TEST2</td>
<td>Panel test output ; no connection</td>
</tr>
</tbody>
</table>

### Pin Description of Backlight Block

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BL1</td>
<td>Power supply GND for backlight lighting</td>
</tr>
<tr>
<td>2</td>
<td>BL2</td>
<td>Power supply input for backlight lighting</td>
</tr>
</tbody>
</table>
Input Equivalent Circuits of Panel Block
To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal input pins. All pins are connected to VSS with a high resistance of 1MΩ (typ.). The equivalent circuit of each input is shown below; (Resistor value : typ.)

1) RED, GREEN, BLUE, PSIG

2) HCK1, HCK2

3) HST, PCG, REF

4) VST, VCK, EN, XSTBY, REF
5) RGT, DWN, REF

6) VSSG

7) COM, TEST2

8) CS

9) TEST1
## Clock Timing Conditions of Panel Block

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HST</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HST rise time</td>
<td>trHst</td>
<td>-</td>
<td>-</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>HST fall time</td>
<td>tfHst</td>
<td>-</td>
<td>-</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>HST data setup time</td>
<td>tdHst</td>
<td>-30</td>
<td>0</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>HST data hold time</td>
<td>thHst</td>
<td>-30</td>
<td>0</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td><strong>HCK</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HCK (n)(^{1/2}) rise time</td>
<td>trHckn</td>
<td>-</td>
<td>-</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>HCK (n)(^{1/2}) fall time</td>
<td>tfHckn</td>
<td>-</td>
<td>-</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>HCK1 rise to HCK2 rise time</td>
<td>to1Hck</td>
<td>-15</td>
<td>0</td>
<td>15</td>
<td>us</td>
</tr>
<tr>
<td>HCK1 fall to HCK2 fall time</td>
<td>to2Hck</td>
<td>-15</td>
<td>0</td>
<td>15</td>
<td>us</td>
</tr>
<tr>
<td><strong>VST</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VST rise time</td>
<td>trVst</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>us</td>
</tr>
<tr>
<td>VST fall time</td>
<td>tfVst</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>us</td>
</tr>
<tr>
<td>VST data setup time</td>
<td>tdVst</td>
<td>30</td>
<td>32</td>
<td>34</td>
<td>us</td>
</tr>
<tr>
<td>VST data hold time</td>
<td>thVst</td>
<td>-34</td>
<td>-32</td>
<td>-30</td>
<td>us</td>
</tr>
<tr>
<td><strong>VCK</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCK rise time</td>
<td>trVck</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>VCK fall time</td>
<td>tfVck</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td><strong>EN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN rise time</td>
<td>trEn</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>EN fall time</td>
<td>tfEn</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>EN fall to VCK rise/fall time</td>
<td>tdEn</td>
<td>900</td>
<td>1000</td>
<td>1100</td>
<td>ns</td>
</tr>
<tr>
<td>EN pulse width</td>
<td>tvEn</td>
<td>2000</td>
<td>3000</td>
<td>3100</td>
<td>us</td>
</tr>
<tr>
<td><strong>PCG</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCG rise time</td>
<td>trPcg</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>us</td>
</tr>
<tr>
<td>PCG fall time</td>
<td>tfPcg</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>us</td>
</tr>
<tr>
<td>PCG (H) rise to VCK rise/fall time</td>
<td>tdiPcg</td>
<td>-0.1</td>
<td>0</td>
<td>0.1</td>
<td>us</td>
</tr>
<tr>
<td>PCG (H) pulse width</td>
<td>tvhPcg</td>
<td>1.4</td>
<td>1.5</td>
<td>1.6</td>
<td>us</td>
</tr>
</tbody>
</table>

*5 HCK\(n\) means HCK1 and HCK2. \(f_{\text{HCKn}}=1.5\text{MHz}\)*
Horizontal Standard Timing

- HST: 42 μs
- HCK1
- HCK2
- FRP: 1 μs
- VCK
- EN: 30 μs
- PCG: 1 μs, 1.5 μs, 1.7 μs
### Horizontal Shift Resister Driving Waveforms

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>波形图</th>
<th>条件</th>
</tr>
</thead>
<tbody>
<tr>
<td>HST rise time</td>
<td>trHst</td>
<td><img src="image" alt="HST rise time waveform" /></td>
<td>$\circ HCKn \ ^\ast \ ^5$ duty cycle 50% toHck=0ns to2Hck=0ns</td>
</tr>
<tr>
<td>HST fall time</td>
<td>tfHst</td>
<td><img src="image" alt="HST fall time waveform" /></td>
<td></td>
</tr>
<tr>
<td>HST data setup time</td>
<td>tdHst</td>
<td><img src="image" alt="HST data setup time waveform" /></td>
<td>$\circ HCKn \ ^\ast \ ^5$ duty cycle 50% toHck=0ns to2Hck=0ns</td>
</tr>
<tr>
<td>HST data hold time</td>
<td>thHst</td>
<td><img src="image" alt="HST data hold time waveform" /></td>
<td></td>
</tr>
<tr>
<td>HCKn $\ ^\ast \ ^5$ rise time</td>
<td>trHckn</td>
<td><img src="image" alt="HCKn rise time waveform" /></td>
<td>$\circ HCKn \ ^\ast \ ^5$ duty cycle 50% toHck=0ns to2Hck=0ns tdHst=333ns thHst=0ns</td>
</tr>
<tr>
<td>HCKn $\ ^\ast \ ^5$ fall time</td>
<td>tfHckn</td>
<td><img src="image" alt="HCKn fall time waveform" /></td>
<td></td>
</tr>
<tr>
<td>HCK1 fall to HCK2 rise time</td>
<td>to1Hck</td>
<td><img src="image" alt="HCK1 fall to HCK2 rise time waveform" /></td>
<td>$\circ$ tdHst=333ns thHst=0ns</td>
</tr>
<tr>
<td>HCK1 rise to HCK2 fall time</td>
<td>to2Hck</td>
<td><img src="image" alt="HCK1 rise to HCK2 fall time waveform" /></td>
<td></td>
</tr>
<tr>
<td>PCG rise time</td>
<td>trPcg</td>
<td><img src="image" alt="PCG rise time waveform" /></td>
<td></td>
</tr>
<tr>
<td>PCG fall time</td>
<td>tfPcg</td>
<td><img src="image" alt="PCG fall time waveform" /></td>
<td></td>
</tr>
<tr>
<td>PCG rise to VCK rise/fall time</td>
<td>tdhPcg</td>
<td><img src="image" alt="PCG rise to VCK rise/fall time waveform" /></td>
<td>$\ast \ ^6$</td>
</tr>
<tr>
<td>PCG pulse width</td>
<td>twhPcg</td>
<td><img src="image" alt="PCG pulse width waveform" /></td>
<td></td>
</tr>
</tbody>
</table>

*6 Definitions:
- The right-pointing arrow $\rightarrow$ means +.
- The left-pointing arrow $\leftarrow$ means -.
- The black dot at an arrow ($\bullet$) indicates the start of measurement.

*7 PCG represents every 1H pulse as shown in Horizontal Timing.
Vertical Standard Timing

VST

VCK

FRP

HST

EN

PCG
# Vertical Shift Resistor Driving Waveforms

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Waveform</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VST rise time</td>
<td>trVst</td>
<td><img src="image1" alt="Waveform" /></td>
<td>○ VCK duty cycle 50% toVcde-0ns toVcde-0ns</td>
</tr>
<tr>
<td>VST fall time</td>
<td>tfVst</td>
<td><img src="image2" alt="Waveform" /></td>
<td>○ VCK duty cycle 50% toVcde-0ns toVcde-0ns</td>
</tr>
<tr>
<td>VST data setup time</td>
<td>tdVst</td>
<td><img src="image3" alt="Waveform" /></td>
<td>○ VCK duty cycle 50% toVcde-0ns toVcde-0ns</td>
</tr>
<tr>
<td>VST data hold time</td>
<td>thVst</td>
<td><img src="image4" alt="Waveform" /></td>
<td>○ VCK duty cycle 50% toVcde-0ns toVcde-0ns</td>
</tr>
<tr>
<td>VCK rise time</td>
<td>trVck</td>
<td><img src="image5" alt="Waveform" /></td>
<td>○ VCK duty cycle 50% toVcde-0ns toVcde-0ns</td>
</tr>
<tr>
<td>VCK fall time</td>
<td>tfVck</td>
<td><img src="image6" alt="Waveform" /></td>
<td>○ VCK duty cycle 50% toVcde-0ns toVcde-0ns</td>
</tr>
<tr>
<td>EN rise time</td>
<td>trEn</td>
<td><img src="image7" alt="Waveform" /></td>
<td>○ VCK duty cycle 50% toVcde-0ns toVcde-0ns</td>
</tr>
<tr>
<td>EN fall time</td>
<td>tfEn</td>
<td><img src="image8" alt="Waveform" /></td>
<td>○ VCK duty cycle 50% toVcde-0ns toVcde-0ns</td>
</tr>
<tr>
<td>EN fall to VCK rise/fall time</td>
<td>tdEn</td>
<td><img src="image9" alt="Waveform" /></td>
<td>○ VCK duty cycle 50% toVcde-0ns toVcde-0ns</td>
</tr>
<tr>
<td>EN pulse width</td>
<td>twEn</td>
<td><img src="image10" alt="Waveform" /></td>
<td>○ VCK duty cycle 50% toVcde-0ns toVcde-0ns</td>
</tr>
</tbody>
</table>
### Electrical Characteristic of Panel Block

Ta=25°C, VDD=8.5V, VIH=3.0V, VREF=1.5V

#### 1. Horizontal drivers

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCKn input pin capacitance</td>
<td>CHckn</td>
<td>–</td>
<td>50</td>
<td>60</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>HST input pin capacitance</td>
<td>CHst</td>
<td>–</td>
<td>25</td>
<td>35</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Video signal input pin capacitance</td>
<td>Csigs</td>
<td>–</td>
<td>200</td>
<td>300</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Psig input pin capacitance</td>
<td>Cpsig</td>
<td>–</td>
<td>2.4</td>
<td>3.0</td>
<td>nF</td>
<td></td>
</tr>
<tr>
<td>Input pin current HCK1</td>
<td>IHck1</td>
<td>–160</td>
<td>–80</td>
<td>–</td>
<td>μA</td>
<td>HCK1 : actual driving</td>
</tr>
<tr>
<td>HCK2</td>
<td>IHck2</td>
<td>–160</td>
<td>–80</td>
<td>–</td>
<td>μA</td>
<td>HCK2 : actual driving</td>
</tr>
<tr>
<td>HST</td>
<td>IHst</td>
<td>–100</td>
<td>–50</td>
<td>–</td>
<td>μA</td>
<td>HST=GND</td>
</tr>
<tr>
<td>RGT</td>
<td>IRgt</td>
<td>–3</td>
<td>–1</td>
<td>–</td>
<td>μA</td>
<td>RGT=GND</td>
</tr>
<tr>
<td>XSTBY</td>
<td>IXstby</td>
<td>–60</td>
<td>–30</td>
<td>–</td>
<td>μA</td>
<td>XSTBY=GND</td>
</tr>
<tr>
<td>REF</td>
<td>IREF</td>
<td>–300</td>
<td>–150</td>
<td>–</td>
<td>μA</td>
<td>REF=VIH/2</td>
</tr>
</tbody>
</table>

HCKn : HCK1, HCK2 (1.5MHz)

#### 2. Vertical drivers

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCK input pin capacitance</td>
<td>CVck</td>
<td>–</td>
<td>5</td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>VST input pin capacitance</td>
<td>CVst</td>
<td>–</td>
<td>5</td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Input pin current VCK</td>
<td>IVck</td>
<td>–100</td>
<td>–50</td>
<td>–</td>
<td>μA</td>
<td>VCK=GND</td>
</tr>
<tr>
<td>VST</td>
<td>IVst</td>
<td>–100</td>
<td>–50</td>
<td>–</td>
<td>μA</td>
<td>VST=GND</td>
</tr>
<tr>
<td>EN</td>
<td>IEn</td>
<td>–100</td>
<td>–50</td>
<td>–</td>
<td>μA</td>
<td>EN=GND</td>
</tr>
<tr>
<td>DWN</td>
<td>IDwn</td>
<td>–3</td>
<td>–1</td>
<td>–</td>
<td>μA</td>
<td>RGT=GND</td>
</tr>
<tr>
<td>PCG</td>
<td>IPCg</td>
<td>–100</td>
<td>–50</td>
<td>–</td>
<td>μA</td>
<td>PCG=GND</td>
</tr>
</tbody>
</table>

#### 3. Common pin capacitance

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Each pin – VSS input resistance</td>
<td>Ccom</td>
<td>---</td>
<td>8</td>
<td>12</td>
<td>nF</td>
</tr>
</tbody>
</table>

#### 4. Total power consumption of the panel

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total power consumption of the panel (NTSC)</td>
<td>PWR25</td>
<td>–</td>
<td>15</td>
<td>17</td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td>PWR60</td>
<td>–</td>
<td>–</td>
<td>23.5</td>
<td>mW</td>
</tr>
</tbody>
</table>

#### 5. Pin input resistance

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin – VSS resistance</td>
<td>Rin</td>
<td>0.5</td>
<td>1</td>
<td>–</td>
<td>MΩ</td>
</tr>
</tbody>
</table>
## Electro-optical Characteristics of Module/Panel Block

*(Ta=25°C, NTSC mode)*

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Measurement method</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contrast ratio</td>
<td>CR&lt;sub&gt;25&lt;/sub&gt;</td>
<td>1</td>
<td>150</td>
<td>200</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Panel block optical transmittance&lt;sup&gt;1&lt;/sup&gt;</td>
<td>T</td>
<td>2</td>
<td>11.6</td>
<td>—</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td>Center luminance</td>
<td>L&lt;sub&gt;m15&lt;/sub&gt;</td>
<td>I&lt;sub&gt;led&lt;/sub&gt;=15mA</td>
<td>2</td>
<td>200</td>
<td>280</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>L&lt;sub&gt;m20&lt;/sub&gt;</td>
<td>I&lt;sub&gt;led&lt;/sub&gt;=20mA</td>
<td>2</td>
<td>250</td>
<td>350</td>
<td>—</td>
</tr>
<tr>
<td>Chromaticity</td>
<td>W</td>
<td>X, X</td>
<td>2</td>
<td>0.286</td>
<td>0.314</td>
<td>0.342</td>
</tr>
<tr>
<td></td>
<td>Y</td>
<td>Y</td>
<td>2</td>
<td>0.284</td>
<td>0.327</td>
<td>0.370</td>
</tr>
<tr>
<td></td>
<td>Tc</td>
<td>Tcm</td>
<td>2</td>
<td>5000</td>
<td>6500</td>
<td>9700</td>
</tr>
<tr>
<td></td>
<td>∆uv</td>
<td>duvm</td>
<td>2</td>
<td>-0.020</td>
<td>0.002</td>
<td>-0.005</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>X, Rx</td>
<td>3</td>
<td>0.590</td>
<td>0.620</td>
<td>0.650</td>
</tr>
<tr>
<td></td>
<td>Y</td>
<td>Ry</td>
<td>3</td>
<td>0.310</td>
<td>0.340</td>
<td>0.370</td>
</tr>
<tr>
<td></td>
<td>G</td>
<td>X, Gx</td>
<td>3</td>
<td>0.300</td>
<td>0.330</td>
<td>0.360</td>
</tr>
<tr>
<td></td>
<td>Y</td>
<td>Gy</td>
<td>3</td>
<td>0.470</td>
<td>0.510</td>
<td>0.550</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>X, Bx</td>
<td>3</td>
<td>0.115</td>
<td>0.145</td>
<td>0.175</td>
</tr>
<tr>
<td></td>
<td>Y</td>
<td>By</td>
<td>3</td>
<td>0.090</td>
<td>0.140</td>
<td>0.190</td>
</tr>
<tr>
<td>V-T characteristics&lt;sup&gt;1&lt;/sup&gt;</td>
<td>V&lt;sub&gt;0&lt;/sub&gt;</td>
<td>25°C</td>
<td>V&lt;sub&gt;0.25&lt;/sub&gt;</td>
<td>4</td>
<td>1.3</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>60°C</td>
<td>V&lt;sub&gt;0.60&lt;/sub&gt;</td>
<td>4</td>
<td>1.3</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;50&lt;/sub&gt;</td>
<td>25°C</td>
<td>V&lt;sub&gt;50.25&lt;/sub&gt;</td>
<td>4</td>
<td>1.7</td>
<td>1.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>60°C</td>
<td>V&lt;sub&gt;50.60&lt;/sub&gt;</td>
<td>4</td>
<td>1.5</td>
<td>1.7</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;10&lt;/sub&gt;</td>
<td>25°C</td>
<td>V&lt;sub&gt;10.25&lt;/sub&gt;</td>
<td>4</td>
<td>2.1</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>60°C</td>
<td>V&lt;sub&gt;10.60&lt;/sub&gt;</td>
<td>4</td>
<td>2.0</td>
<td>2.2</td>
</tr>
<tr>
<td>Half tone color reproduction range</td>
<td>R-G</td>
<td>V&lt;sub&gt;RBG&lt;/sub&gt;</td>
<td>5</td>
<td>-0.115</td>
<td>-0.080</td>
<td>-0.045</td>
</tr>
<tr>
<td></td>
<td>B-G</td>
<td>V&lt;sub&gt;BG&lt;/sub&gt;</td>
<td>5</td>
<td>0.00</td>
<td>0.03</td>
<td>0.05</td>
</tr>
<tr>
<td>Response time&lt;sup&gt;1&lt;/sup&gt;</td>
<td>ON time</td>
<td>0°C</td>
<td>Ton0</td>
<td>6</td>
<td>—</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25°C</td>
<td>Ton25</td>
<td>6</td>
<td>—</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td>OFF time</td>
<td>0°C</td>
<td>Toff0</td>
<td>6</td>
<td>—</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25°C</td>
<td>Toff25</td>
<td>6</td>
<td>—</td>
<td>30</td>
</tr>
<tr>
<td>Flicker&lt;sup&gt;1&lt;/sup&gt;</td>
<td>60°C</td>
<td>F</td>
<td>7</td>
<td>—</td>
<td>-60</td>
<td>-30</td>
</tr>
<tr>
<td>Image retention time&lt;sup&gt;1,2&lt;/sup&gt;</td>
<td>60°C, 2h</td>
<td>YT1</td>
<td>8</td>
<td>0</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Viewing angle range</td>
<td>CR ≥ 10</td>
<td>θ T</td>
<td>9</td>
<td>15</td>
<td>20</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>θ B</td>
<td>9</td>
<td>50</td>
<td>60</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>θ L</td>
<td>9</td>
<td>35</td>
<td>40</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>θ R</td>
<td>9</td>
<td>35</td>
<td>40</td>
<td>—</td>
</tr>
<tr>
<td>Surface reflection ratio</td>
<td>θ = 0°</td>
<td>RF</td>
<td>10</td>
<td>—</td>
<td>0.9</td>
<td>1.5</td>
</tr>
<tr>
<td>Cross talk&lt;sup&gt;1&lt;/sup&gt;</td>
<td>25°C</td>
<td>CTK</td>
<td>11</td>
<td>—</td>
<td>0.9</td>
<td>1.5</td>
</tr>
</tbody>
</table>

<sup>1</sup> Conforms to the measurement results for the discrete panel.

<sup>2</sup> Stress conditions: 60°C, 2h, Checker pattern

---

Evaluation conditions: After driving in the above conditions, the image retention is not found at the gray raster in 60°C.

Judgment: In case of finding the image retention, the panel passes when it disappears, while driving in the below conditions.

Easing conditions: RF, 1h leaving → 60°C, 1h, driving at the gray raster.
<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Measure method</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Backlight DC forward voltage</td>
<td>Ifbl = 15mA</td>
<td>Vfbl₁₅</td>
<td>8.9</td>
<td>10.5</td>
<td>11.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Ifbl = 20mA</td>
<td>Vfbl₂₀</td>
<td>9.0</td>
<td>10.8</td>
<td>12.0</td>
<td>V</td>
</tr>
<tr>
<td>Backlight power consumption</td>
<td>Ifbl = 15mA</td>
<td>Pbl₁₅</td>
<td>134</td>
<td>158</td>
<td>174</td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td>Ifbl = 20mA</td>
<td>Pbl₂₀</td>
<td>180</td>
<td>216</td>
<td>240</td>
<td>mW</td>
</tr>
<tr>
<td>Backlight center luminance</td>
<td>Ifbl = 15mA</td>
<td>Lbl₁₅</td>
<td>2000</td>
<td>2800</td>
<td></td>
<td>cd/m²</td>
</tr>
<tr>
<td></td>
<td>Ifbl = 20mA</td>
<td>Lbl₂₀</td>
<td>2500</td>
<td>3500</td>
<td></td>
<td>cd/m²</td>
</tr>
<tr>
<td>Backlight center chromaticity</td>
<td>Ifbl = 15mA</td>
<td>X</td>
<td>0.280</td>
<td>0.295</td>
<td>0.310</td>
<td>K</td>
</tr>
<tr>
<td></td>
<td>Ifbl = 15mA</td>
<td>Y</td>
<td>0.260</td>
<td>0.285</td>
<td>0.310</td>
<td>K</td>
</tr>
<tr>
<td></td>
<td>Ifbl = 15mA</td>
<td>Tc</td>
<td>6800</td>
<td>8500</td>
<td></td>
<td>K</td>
</tr>
<tr>
<td></td>
<td>Ifbl = 15mA</td>
<td>△uv</td>
<td>-0.005</td>
<td>-0.006</td>
<td></td>
<td>K</td>
</tr>
<tr>
<td>Backlight luminance uniformity</td>
<td>Ifbl = 15mA</td>
<td>BLunif</td>
<td>60</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Backlight life (Luminance half-life)</td>
<td>Ifbl = 15mA</td>
<td>BL₁₅₅₅</td>
<td>5000</td>
<td></td>
<td></td>
<td>hr</td>
</tr>
<tr>
<td></td>
<td>Ifbl = 20mA</td>
<td>BL₁₅₇₀</td>
<td>1000</td>
<td></td>
<td></td>
<td>hr</td>
</tr>
<tr>
<td></td>
<td>Ifbl = 15mA</td>
<td>BL₁₅₉₀</td>
<td>5000</td>
<td></td>
<td></td>
<td>hr</td>
</tr>
<tr>
<td></td>
<td>Ifbl = 20mA</td>
<td>BL₁₆₀₀</td>
<td>1000</td>
<td></td>
<td></td>
<td>hr</td>
</tr>
</tbody>
</table>
<Panel/Module/Backlight Electro-optical Characteristics Measurement>

Basic measurement conditions

1) Driving voltage
   VDD=8.5V, Vih=3.0V, VREF=1.5V
   VVC=2.5V, VCOM=2.0±2.0V, Vpsig=2.5V
2) Measurement temperature
   25°C unless otherwise specified.
3) Measurement point
   One point in the center of the screen unless otherwise specified.
4) Measurement systems
   Three types of measurement systems are used as shown below.
5) R, G and B input signal voltage: Vsig
   Vsig=VVC±V_{AC} \ VAC : signal amplitude

*Measurement system I

LED backlight

Surface A*

Luminance Meter

TOPCON BM-5A luminance meter

Constant Current circuit

15mA

*Measurement system II

Light receptor lens

Optical fiber

Surface A*

Light Detector

Measurement equipment

Drive Circuit

Measurement using the discrete LCD panel

Light Source

*Measurement system III

Light Source

Optical fiber

Surface A*

Spectroscope

Surface A* See the Package Outline

1. Contrast Ratio

Contrast ratio (CR) is given by the following formula.

\[
CR = \frac{L_{\text{White}}}{L_{\text{Black}}}
\]
2. Optical Transmittance of Panel, Center Luminance of Module, Color Temperature

Optical Transmittance (T) is given by the following formula.

\[ T = \frac{L(\text{White})}{\text{Luminance of Backlight}} \times 100 \% \]

L(White) is the same expression as defined in "Contrast Ratio".

Lm = White luminance at the center of the panel
Tcm = Color temperature at the center of the panel

Measured by System I using the TOPCON BM-5A.

3. Chromaticity

Chromaticity of the panels is measured by System I. Raster modes of each color are defined by the representations at the input signal amplitude conditions shown in the table below. System I uses x and y of the CIE standards as the chromaticity here.

<table>
<thead>
<tr>
<th>Raster</th>
<th>Signal amplitudes (Vc±Vac) supplied to each input</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>2.5±1.5V</td>
</tr>
<tr>
<td>G</td>
<td>2.5±1.5V</td>
</tr>
<tr>
<td>B</td>
<td>2.5±1.5V</td>
</tr>
<tr>
<td>W</td>
<td>2.5±1.5V</td>
</tr>
</tbody>
</table>

Vcom 2.0±2V

(Unit: V)

4. V-T Characteristics

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panel, are measured by System II by inputting the same signal amplitude Vm to each input pin. V90, V50, and V10 correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.

5. Half Tone Color Reproduction Range

The half tone color reproduction range of LCD panels is characterized by the differences between the V-T characteristics of R, G, and B. The differences of these V-T characteristics are measured by System II.

System II defines signal voltages of each R, G, and B raster mode which correspond to 50% of transmittance, \( V_{50R}, V_{50G}, \) and \( V_{50B} \), respectively. \( V_{50BG} \) and \( V_{50RB} \) that is to say the differences between \( V_{50R} \) and \( V_{50G} \) and between \( V_{50G} \) and \( V_{50B} \) are given by the following formulas respectively.

\[ V_{50BG} = V_{50R} - V_{50G} \]
\[ V_{50RB} = V_{50G} - V_{50B} \]
6. Response Time
Response times ton and toff are measured by System II by applying the input signal voltages in the figure to the right to each input pin. These times are defined by the following formulas.

\[ \text{ton} = t_1 - t_{ON} \]
\[ \text{toff} = t_2 - t_{OFF} \]

\( t_1 \): time which gives 10% transmittance of the panel.
\( t_2 \): time which gives 90% transmittance of the panel.

The relationships between \( t_1 \), \( t_2 \), \( t_{ON} \) and \( t_{OFF} \) are shown in the figure to the right.

7. Flicker
Flicker (F) is given by the following formula. DC and AC components (NTSC: 30 Hz, rms; PAL: 25 Hz, rms) of the panel output signal for gray raster mode are measured by a DC voltmeter and a spectrum analyzer in System II.

\[ F \ (dB) = 20 \log \left( \frac{\text{AC component}}{\text{DC component}} \right) \]

*R, G, B input signal voltage for gray raster mode is given by \( V_{\text{sig}} \)

\( V_{\text{sig}} = 6.0 \pm V_{50} \) (V)

Where: \( V_{50} \) is the signal amplitude which gives 50% of transmittance in V-T curve.

8. Image Retention Time
Image retention time is given by the following procedures.
Apply the checker pattern to the LCD panel for 2 hours in 60°C and then change to a gray scale signal
\[ V_{\text{sig}} = 6.0 \pm V_{AC} \]
\[ V_{AC} = 3 \sim 4V \]

Judging by sight at the VAC that holds the maximum image retention, measure the time for the residual image to disappear.

Easing conditions: RT, 1h leaving \( 60°C \), 1h, driving at the gray raster

In case of finding the image retention, the panel passes when it disappears, while driving in the above conditions.

*Input conditions of the checker pattern
\( V_{\text{sig}} = 2.5 \pm 1.5 / \mp 1.5 \) (V)

\( V_{\text{COM}} = 2.0 \pm 2V \)
9. Definition of Viewing Angle Range

Viewing angle range is measured by System I. The Contrast ratio (CR) is measured at the angles defined in the figure to the right and the range where CR ≥ 10 is taken as the viewing angle range. Measure with surface A* facing upwards.

*Surface A: See the Package Outline.

10. Surface Reflection Ratio

Surface reflection ratio (Rf) is given the following formula.

\[ Rf = \frac{\text{Reflected optical luminance of the panel surface } A^*}{\text{Reflected optical luminance of Al(Aluminum)}} \times 100 \% \]

11. Cross Talk

Cross talk is determined by the luminance differences between adjacent areas represented by \( W_i \) and \( W_{i+1} \) (1 to 4) around the black window (Vsigt = 4.0V/IV)

Cross talk value \( CTK = \left| \frac{W_i - W_{i+1}}{W_i} \right| \times 100 \% \)
12. Backlight Center Luminance and Chromaticity Measurement Method

1. Environmental conditions
   Temperature: 25±5°C
   Humidity: 30 to 85%

   Start measurement after leaving the module in the above environment for one hour.
   Measurement should be performed in a dark room with a luminance of 10 lx or less and which is not subject to the effects
   of reflective or external light.
   There should be no heat insulating objects around the module units, and measurement should be performed in a draftless conditions.

2. Luminance and chromaticity measurement method
   Measurement equipment: TOPCON BM-5A, viewing angle: 0.2°, distance: 450±50mm
   Measure 30s after the backlight is lit.
   Using a contrast current circuit, measure the luminance under both conditions of lfb = 15mA and 20mA, and measure
   the chromaticity under only the condition of lfb = 15mA.

13. Backlight Luminance Uniformity Measurement Method

1. Environmental conditions
   Measure under the same conditions as “12. Backlight Center Luminance and Chromaticity Measurement Method” above.

2. Light the backlight at lfb = 15mA using a constant current circuit, and start measurement 30s after the backlight is lit.
   Backlight luminance uniformity is obtained by dividing the effective pixel area into 9 equal sections as shown below, measuring
   the luminance at each of the centers 1 to 9, and calculating Min. luminance ÷ Max. luminance x 100%.

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14. Backlight Life

Definition of life: When the backlight center luminance drops to 50% of the initial value.
Description of Panel Block Operation

1. Color Coding

The color filters are coded in a delta arrangement. The shaded area is used for the dark border around the display.
2. Description of LCD Panel Operations

A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to each of 240 line electrodes sequentially one line electrode at a time in a single horizontal scanning period.

The selected pulse is output when the enable pin goes to high level. PAL signal pulse elimination display is possible by using the enable pin and simultaneously controlling VCK.

A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuitry, applies selected pulses to each of 400 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the low signal lines.

The vertical and horizontal drivers address one pixel, and then thin film transistors turn on to apply a video signal to the pixel. The same procedures lead to the entire 240 x 490 pixels to display a picture in a vertical scanning period.

Pixel dots are arranged in a delta pattern, where sets of RGB pixels are positioned shifted by 1.5 dots against adjacent horizontal lines. The horizontal driver output pulse must be shifted by 1.5 dots for each horizontal line against horizontal sync signal to apply a video signal to each pixel properly.

The video signal should be input with the polarity-inverted every horizontal cycle.

The relationships between the vertical shift register start pulse VST and the vertical display period, and between the horizontal shift register start pulse HST and the horizontal display period are shown below for top to bottom and left to right scan.

![Diagram](image-url)

1) Vertical display period

2) Horizontal display period
3.RGB Simultaneous Sampling

The horizontal driver samples, R, G and B video signals simultaneously, which requires phase matching between the R, G and B signals to prevent the horizontal resolution from deteriorating. Thus phase matching by an external signal delay circuit is needed before applying the video signal to the LCD panel.

Two methods are applied for the delaying procedure: Sample-and-hold and Delay circuit. These two block diagrams are as follows:

1) Sample-and-hold

\[ \begin{array}{c}
B & \xrightarrow{\text{S/H}} & \xrightarrow{\text{AC Amp}} & 22 \text{ BLUE} \\
\text{CKB} \\
R & \xrightarrow{\text{S/H}} & \xrightarrow{\text{AC Amp}} & 21 \text{ RED} \\
\text{CKR} \\
G & \xrightarrow{\text{S/H}} & \xrightarrow{\text{AC Amp}} & 20 \text{ GREEN} \\
\text{CKG}
\end{array} \]

<Phase relationship of delaying sample-and-hold pulses>

HCKn

CRB

CKR

CKG

2) Delay element

\[ \begin{array}{c}
B & \xrightarrow{\text{Delay}} & \xrightarrow{\text{Delay}} & \xrightarrow{\text{AC Amp}} & 22 \text{ BLUE} \\
R & \xrightarrow{\text{Delay}} & \xrightarrow{\text{AC Amp}} & 21 \text{ RED} \\
G & \xrightarrow{\text{AC Amp}} & 20 \text{ GREEN}
\end{array} \]
System Configuration

常数电流电路

液晶模块带背光

-85V

Digital Data

Serial data

CXM4006R

COMAC

COMDC

0.1 μF

RED

GREEN

BLUE

4.7 μF

CGM

HST

HCK1

HCK2

VST

VCK

DHM

EN

RGT

REF

0.1 μF

PCG

XSTBY

PSIG

LCD panel

ACX318EKM

VSSG

Zener diode

RD5.6UJ

1uF

Dedicated LED backlight
Notes on Handling

(1) Static charge prevention
   Be sure to take the following protective measures. TFT-LCD panels and LED backlights are easily damaged by static charges.
   a) Use non-chargeable gloves, or simply use bare hands.
   b) Use an earth band when handling.
   c) Do not touch any electrodes of a panel.
   d) Wear non-chargeable clothes and conductive shoes.
   e) Install grounded conductive nuts on the working floor and working table.
   f) Keep panels away from any charged materials.
   g) Use ionized air to discharge the panels.

(2) Protection from dust and dirt
   a) Operate in a clean environment.
   b) When delivered, the panel surface (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the panel.
   c) Do not touch the polarizer surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
   d) Use ionized air to blow dust off the panel.

(3) Module fixing method
   a) The following items should be taken into account for the positioning guide design.
      - The design reference edges are the upper and left edges of the panel as viewed from the front.
      - Design the guides using the panel frame as the reference and not the backlight.
      - Set the guides on the same side of the set as the mirror window frame.
      - To prevent LCD image unevenness, the guides should be the maximum package tolerance or more so that a clamping load is not applied to the panel from the x and y directions.
      - Make sure the guides do not block the panel FPC outlet and backlight lead wire outlet.
   b) The guaranteed area of the polarizer is the outer circumference of 0.7mm of the effective display area (Fig.1).
      - Design the monitor window frame of the set so that it is within this range including variance.
   c) Set the holders on the rear of the backlight around the circumference as far from the center of the backlight as possible. Local pressure applied to the center of the rear of the backlight for an extended period may result in uneven luminance, so the holder pressure on the center of the backlight should be 500g/cm² or less.
   d) Connect the panel or backlight frame to GND.
   e) Use a design that does not repeatedly bend or place stress on the backlight lead wires (maximum load in the lead wire pull-out direction: 500g) as this may cause lead wire disconnection at the solder junction on the backlight unit side. (Forced bending of 90° or more is permitted up to 2 times, and repeated bending of 45° up to 8 times.)

(4) Others
   a) Do not twist and bend the flexible PC board especially at the connecting region because the board is easily deformed.
   b) Do not drop the panel or backlight.
   c) Do not twist and bend the panel, panel frame or backlight.
   d) Keep the panel and backlight away from heat sources.
   e) Do not dampen the panel or backlight with water or other solvents.
   f) Avoid storage or use of the panel at high temperatures or high humidity, as this may result in damage.