To : _____

Date : November 22, 2012

SPECIFICATIONS	
Product Name	**ACX450AKN-7**

Approval Signature

Accepted by : _____

Date : _____

Japan Display Inc.

Proposed by : Yasushi Shimegaichi

Revision History		Product Name	ACX450AKN-7
		Part No.	

Date	Contents of change	Reasons	Remarks
Aug. 8, 2012	Release		Version 1
Aug. 31, 2012	(A) Add Inspection spec.		Version 2
Nov.21 , 2012	(A)Packing Spec. (C)Product Name		Version 3
Nov.27 , 2012	(A)MODULE ID		Version 4

(C): Changed (A): Appended (D): Deleted (F): Filled in

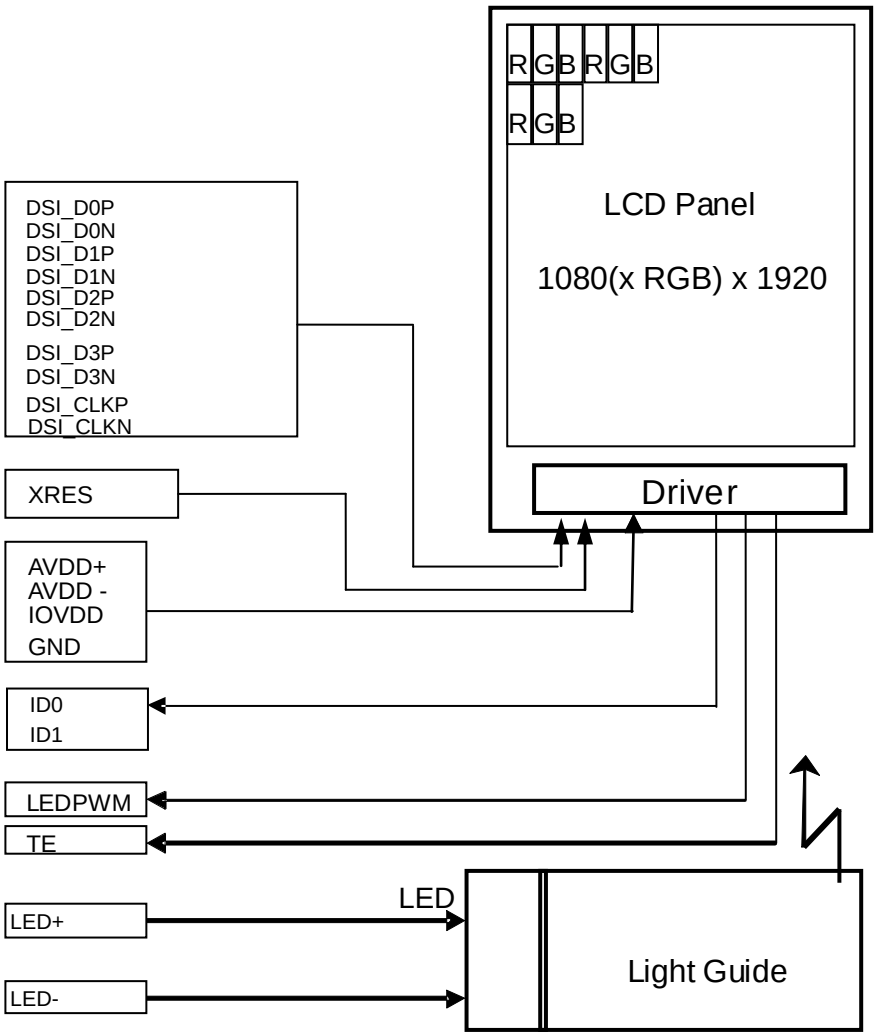
CONTENTS

1. BASIC SPECIFICATIONS

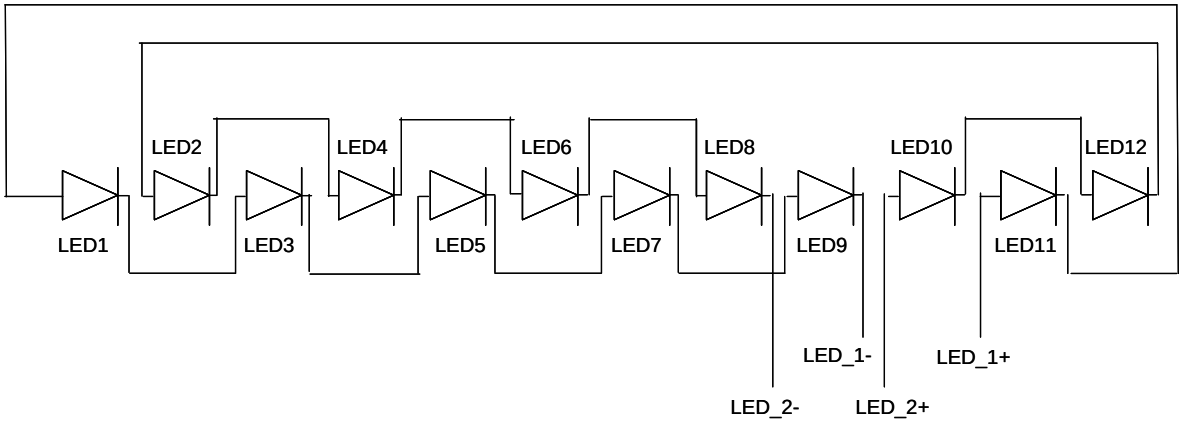
1.1 STRUCTURES

No	Parameter	Specifications
1	LCD Structure	4.97” Low Temperature Poly-Silicon TFT of DC-Vcom driving method with Pixel Column inversion
2	Outward	64.284（W）x 118.8（H）x 1.43（D） [mm] (excluding FPC and parts of protruding)
3	Weight	(21.2) [g]
4	Screen Size	61.884 x 110.016 [mm]
5	Number of Dots	1080 x RGB（W） x 1920（H)
6	Dot Pitch	0.0191（W） x 0.0573（H) [mm]
7	Color Layout	RGB vertical stripe
8	Viewing Direction	Wide viewing angle
9	LCD Optical Mode	Normally Black
10	Polarizer Type	Hard coat treating (3H)
11	Light Source Type	Back light with white LEDs (12chips)
12	Number of Colors	16M (24bits)
13	Frame Rate	55~60Hz(recommend)
14	LCM type	Transmissive
15	Driving Method	DC Vcom
16	Driving inversion	Pixel Column inversion
17	Page orientation	Portrait mode
18	Outline dimension	See 2D drawing
19	System Interface Version	MIPI DSI 4data lanes and 1clock lane MIPI DSI: Version 1.01.00r11 MIPI D-PHY: Version 1.00.00 MIPI DCS: Version 1.01.00

1.2 BLOCK DIAGRAM



LED B/L CIRCUIT



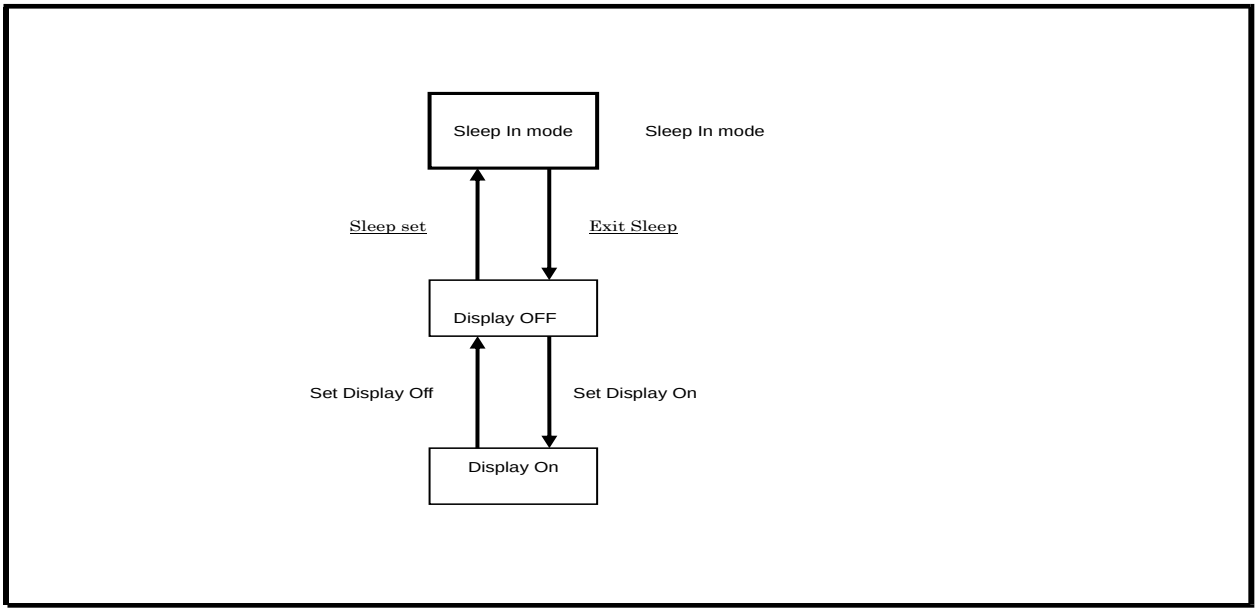
1.3 INTERFACE PINS

Pin No	Symbol	Function	I/O	Remarks
1	LED_1+	LED Power Supply	-	Anode
2	LED_2+	LED Power Supply	-	Anode
3	LED_1-	LED Power Supply		Cathode
4	LED_2-	LED Power Supply		Cathode
5	NC			Not Connected (keep floating)
6	GND	Ground	-	
7	TE	TE signal output from driver IC	O	
8	NC	-	-	Not Connected (keep floating)
9	IOVDD	Power Supply for I/O	-	
10	AVDD+	Power Supply for Analog	-	
11	AVDD-	Power Supply for Analog		
12	LEDPWM	Backlight LED driver PWM	O	
13	XRES	Device Reset Signal	I	
14	ID0	ID0 (100kΩpull-up to IOVDD)	O	ID0=1
15	ID1	ID1 (100kΩpull-up to IOVDD)	O	ID1=1
16	GND	Ground		
17	DSI_D2P	3rd MIPI data positive signal	I	
18	DSI_D2N	3rd MIPI data negative signal	I	
19	GND	Ground		
20	DSI_D1P	2nd Lane MIPI data positive signal	I	
21	DSI_D1N	2nd Lane MIPI data negative signal	I	
22	GND	Ground	-	
23	DSI_CLKP	MIPI Clock positive signal	I	
24	DSI_CLKN	MIPI Clock negative signal	I	
25	GND	Ground		
26	DSI_D0P	1st Lane MIPI data positive signal	I/O	
27	DSI_D0N	1st Lane MIPI data negative signal	I/O	
28	GND	Ground		
29	DSI_D3P	4th Lane MIPI data positive signal	I	
30	DSI_D3N	4th Lane MIPI data negative signal	I	
31	GND	Ground		

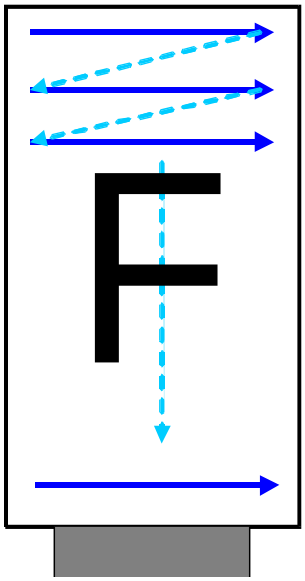
The use of ACX450AKM-7 basically conforms to specifications of LCD driver IC:R63311 (Renesas). It explains typical function in this manual.

1.4 BASIC OPERATION MODE

The basic operation mode of ACX450AKM is illustrated below. When changing from one mode to another, make sure to follow the sequence indicated in the figure.



1.5 INSTRUCTION OF DIFFERENT DIRECTION SCANNING



2. ELECTRICAL SPECIFICATION

2.1 DC SPECIFICATION

GND=0V, Ambient temperature = 25°C unless otherwise specified.

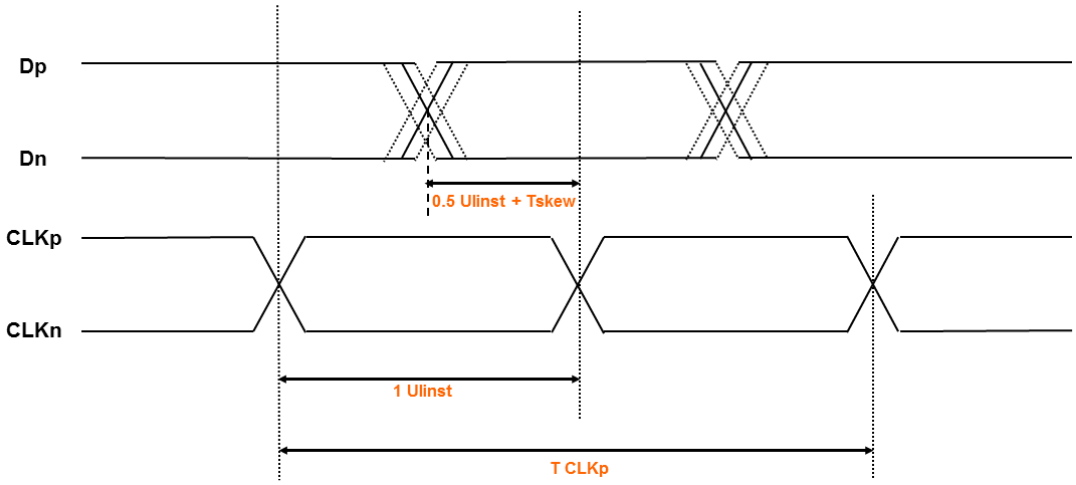
Parameter	Symbol	Condition	Ratings			Unit	Pins (Main FPC)
			Min.	Typ.	Max.		
Power Supply Voltage	AVDD+		4.75	5.0	5.25	V	
	AVDD-		-4.75	-5.0	-5.25	V	
	IOVDD		1.65	1.8	1.95	V	
Low-level input voltage	VIL		GND	-	0.3 x IOVDD	V	13
High-level input voltage	VIH		0.7 x IOVDD	-	IOVDD	V	13
Low-level output voltage	VOL	IOL=+1.0mA	GND	-	0.2 x IOVDD	V	7,8,12
High-level output voltage	VOH	IOH=-1.0mA	0.8 x IOVDD	-	IOVDD	V	7,8,12
Input leak current	ILI				10	µA	
Power supply current (RMS) Note.2, Note.3	IAVDD+	White		10.9	(16.2)	mA	
		Black		8.9	(13.7)	mA	
		Color Bar note5		11.2	(16.1)	mA	
	IAVDD-	White	(-12.7)	-7.4		mA	
		Black	(-10.9)	-6.2		mA	
		Color Bar note5	(-13.2)	-8.2		mA	
	IIOVDD	White		17.2	(23.5)	mA	
		Black		17.1	(23.4)	mA	
		Color Bar note5		18.6	(25.2)	mA	
LED forward current	IF			20	25	mA	
LED VF	VF	1LED, IF=20mA		3.0	3.3	V	

<Note>

1) Rated values indicate operating range of electrical functions.
2) Typ. values are at the condition of power supply voltage is Typ., the ambient temperature is 25°C , still display image. Max. values are at the condition of power supply voltage is in a range of "DC SPECIFICATIONS", ambient temperature is in a range of operating temperature, still display image.
3) The state of MIPI is Video mode and 60Hz frame rate.
4) Power supply current “color bar” is the full screen color bar still display.

2.2 MIPI INTERFACE CHARACTERISTICS

2.2.1 High Speed Data Transmission



Parameter	Symbol	min	typ	max	Units	Notes
UI instantaneous	Ulinst	(1)		5	ns	
Data to Clock Skew [Measured at transmitter]	Tskew[TX]	-0.15		+0.15	Ulinst	

2.3 FRAME RATE SPECIFICATION

In case of video mode, Input Horizontal frequency MUST NOT be over Minimum value including OSC variation.
So please keep input specification as follows;

Item	Column inversion			
	Min.	Typ.	Max.	unit
Horizontal Active Number		1080		dots
Vertical Active Number		1920		lines
Vertical Cycle (VP)		1928		lines
Vertical Blanking(VBL)	8			lines
Vertical front porch(VFP)	3			lines
Vertical Back porch(VBP)	5			lines
Horizontal Frequency (internal timing)			135.8	kHz
Vertical Frequency	55(TBD)		60	Hz

Note: Video Mode Max. 60.0Hz has already considered IC CLK tolerance +/- 5%
VBL=VBP+VFP

2.4 MIPI-DSI INTERFACE

2.4.1 System Interface Configuration

The DSI incorporated in the LCD driver complies with the following standards.

MIPI DSI: Version 1.01.00r11
MIPI D-PHY: Version 1.00.00
MIPI DCS: Version 1.01.00

2.4.2 Introduction

The module DSI interface employs clock and 4 data lanes.
-DSI-D0+,D0-is bi-directional with Low-Power Reverse Escape Mode supporting Low Power Data Transmission.
-DSI-D1+,D1-,D2+,D2- ,D3+,D3- is unidirectional without Turnaround or any kind of Reverse communication functionality.

The DSI interface can communicate in 2 modes, Low Power Data Transmission Mode (LP-Mode) and High Speed Mode (HS-Mode).
In LP-Mode, the differential pair lines are operating in Single End Mode, the differential receiver is disabled and the termination resistor is disconnected from the differential pair lines.
In HS-Mode, the termination resistor is connected and the differential pairs are no longer working in Single End mode.

The lane states are determined by the active Transmitter (Tx). In Normal operation, the lanes are being driven by either a High Speed Transmitter (HS-Tx) or a Low Speed Transmitter (LP-Tx). In HS mode, there are 2 possible lane states and in Low Speed mode, there are 4 possible lanes states defined by the table below:-

State Code	Line Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dx+ line	Dx- line	Burst Mode	Control Mode	Escape Mode
HS-0	HS-Low	HS-High	Differential – 0	Note 1	Note 1
HS-1	HS-High	HS-Low	Differential – 1	Note 1	Note 1
LP-00	LP-Low	LP-Low	N/A	Bridge	Space
LP-01	LP-Low	LP-High	N/A	HS-Request	Mark-0
LP-10	LP-High	LP-Low	N/A	LP-Request	Mark-1
LP-11	LP-High	LP-High	N/A	Stop	Note 2

Notes:-
1. During High Speed Transmission, the Low-Power Receivers constantly check for LP-00 state code.
2. If LP-11 occurs during Escape mode, the Lane will return to Stop State (Control Mode LP-11)

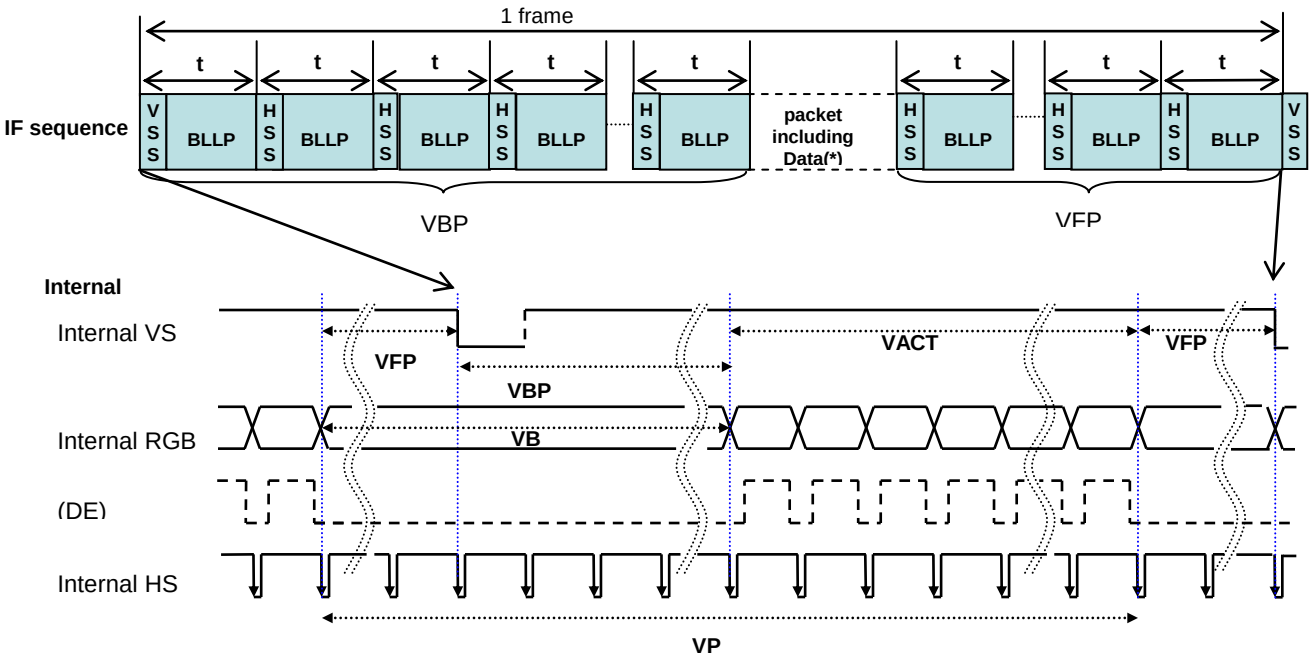
2.4.3 Video mode

ACX450 driver supports only Video Mode. There are thee formats of transmission packet sequences. ACX450 supports two of these formats. See the following formats.

Image Transmission packet sequence	implementation
Video mode (Non-burst mode with sync pulses)	Not supported
Video mode (Non-burst mode with sync events)	Supported
Video mode (Burst mode with sync events)	Supported
Command mode	Not supported

Clock lane should support only continuous clock.

Vertical Video Mode timing (Non-Burst Mode with sync Events / Burst Mode)

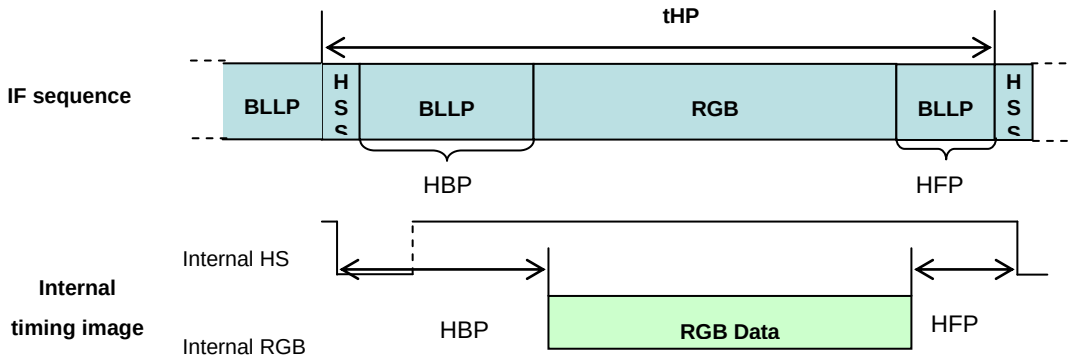


VSS: Vsync Start packet, HSS: Hsync Start packet , BLLP: Blanking packet or Low Power Mode

,

RGB data: Packed pixel stream (RGB data) packet

Horizontal Video mode timing (Non-Burst Mode with sync Events / Burst Mode)



2.4.4 DSI Clock Lanes

The DSI Clock Lanes can operate in different power modes, controlled by the Transmitter (Tx):-

- High Speed Clock Mode (HSCM)

  It is only possible to enter High Speed Clock Mode (HSCM) from Low Power Mode (LPM) by the sequence LPM → LP-01 → LP-00 → HS-0 → HS-0/1 (HSCM).

- Low Power Mode (LPM)

  There are 3 possible methods to enter Low Power mode (LPM).

  1. Power On, Software Reset or Hardware Reset → LPM.
  2. From Ultra Low Power Mode (ULPM) by the sequence ULPM → LP-10 → LP-11 (LPM).
  3. From High Speed Clock Mode (HSCM) by the sequence HSCM → HS-0 → LP-11 (LPM)

- Ultra Low Power Mode. (ULPM)

  It is only possible to enter Ultra Low Power Mode (ULPM) from Low Power Mode (LPM) by the sequence LPM → LP-10 → LP-00 (ULPM).

The protocols for entering/leaving the different power modes can be summarized by the following diagram:-

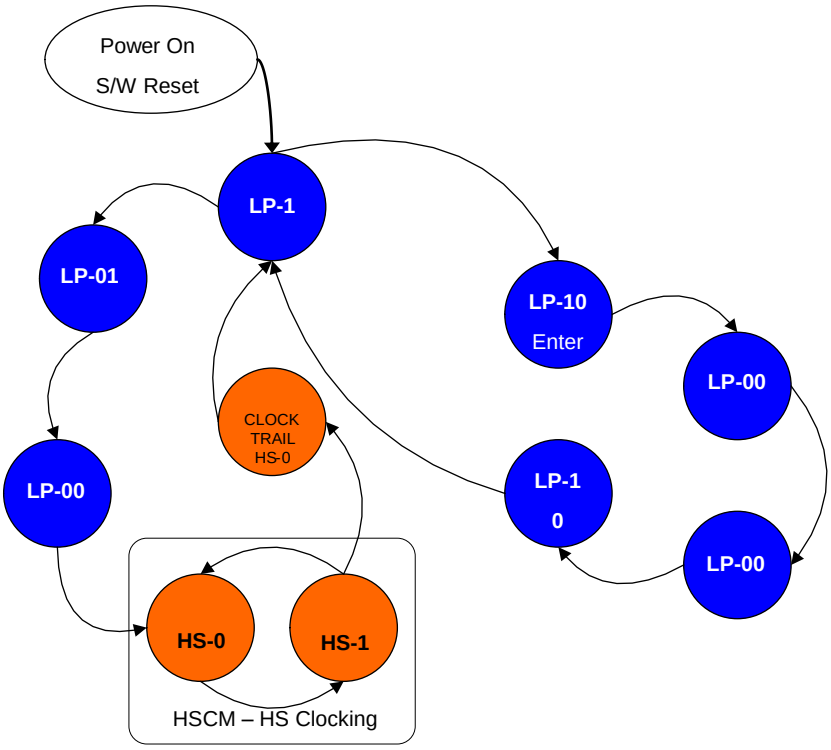


Figure 1 – Clock Lane Power Modes.

For a high speed communication, the DSI CLK+/- lines are always started before high speed data is sent on DSI-D0+/- or DSI D1+/- or DSI D2+/- or DSI D3+/-. The clock lines also continue clocking for a defined period after the data transmission has ended as shown in the diagram below.

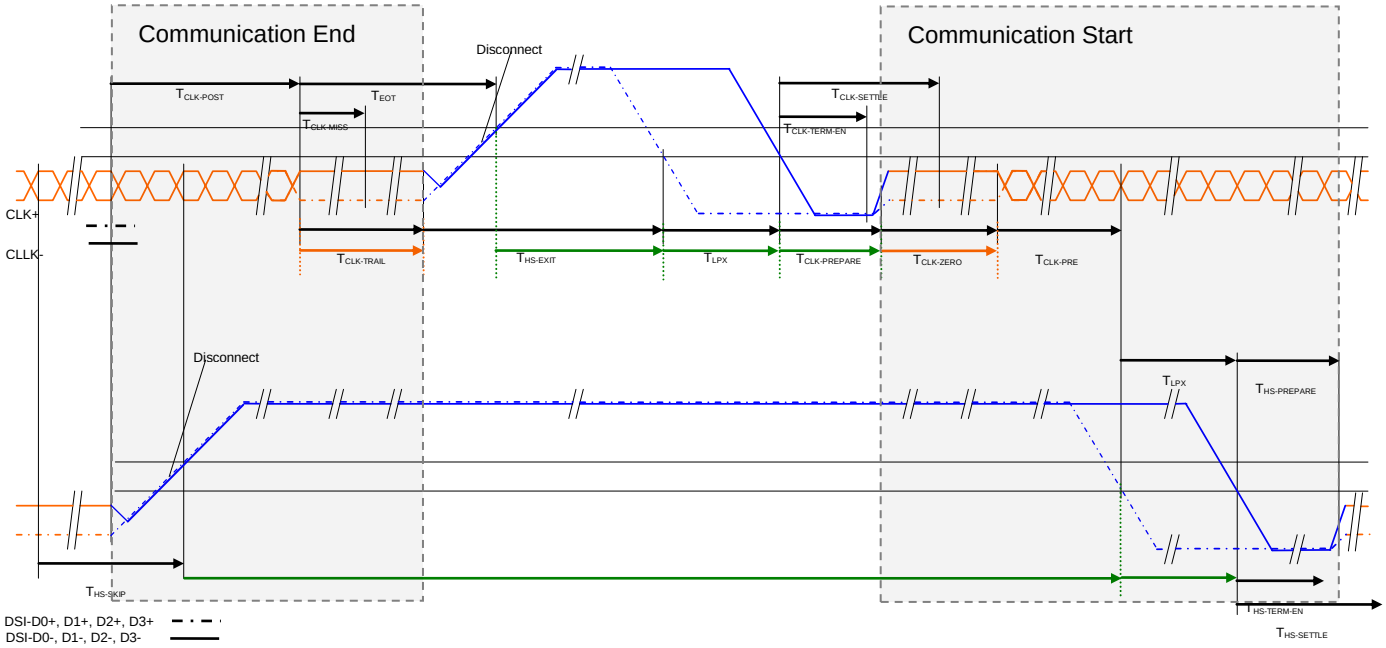


Figure 2 – Clock Lane Power Transitions.

The High Speed Clock burst always starts and ends with state HS-0 so the burst always contains an even number of clock transitions.

2.4.5 DSI Data Lanes.

2.4.5.1 Introduction

The DSI Data Lanes DSI D0+/-, D1+/-, D2+/- and D3+/- can operate in different modes, controlled by the Transmitter (Tx):-

- High Speed Data Transmission (HSDT) where the display is receiving data from the host.

  It is only possible to enter High Speed Data Transmission (HSDT) from Control Mode by the sequence LP-11 → LP-01 → LP-00 → HS-0 → HS-0/1 (HSDT).
- Escape Mode – Applies only to D0+/-.
- Bus Turnaround Mode – Applies only to D0+/-.

  It is only possible to enter Bus Turnaround Mode from Control Mode by the sequence LP-11 → LP-10 → LP-00 → LP-10 → LP-00.

Control Mode is defined as the Data Lane Stop State LP-11.

2.4.5.2 High Speed Data Transmission

All High Speed Data Transmissions start and end with a Stop State (LP-11). The DSI CLK+/- lanes have already entered High Speed Clock Mode before starting High Speed Data Transmission.
A burst of High Speed Data always has an integer number of bytes with a minimum length of one byte.
High Speed Data Transmission can be started and ended independently for any data Lane, however normally the data Lanes will start synchronously but may end at different times if there are an unequal number of transmitted bytes for each Lane.

2.4.5.2.1 HSDT Start of Transmission

The display module DSI D0+/-, D1+/-, D2+/- and D3+/- enter High Speed High Transmission as follows:-

Step	Host	Display module
1	Drives Stop State LP-11	Monitors the Stop State
2	Drives HS-Request state LP-01 for time T_{LPX}.	Monitors the transition from LP-11 to LP-01
3	Drives LP-00 for time $T_{HS\text{-}PREPARE}$.	Monitors the transition from LP-01 to LP-00 and enables the Termination Impedance after time $T_{HS\text{-}TERM\text{-}EN}$.
4	Drives HS-0 for a time $T_{HS\text{-}ZERO}$.	Enables HS-RX and timeout $T_{HS\text{-}SETTLE}$.
5		Monitoring for Leader-Sequence “011101”
6	Inserts the HS Sync-Sequence “00011101” beginning on a clock rising edge.	
7		Synchronises after recognising Leader-Sequence “011101”.
8	Transmit High Speed Data	Receive High Speed data.

The sequence for starting High Speed Data Transmission on the DSI bus is shown in the following figure:-

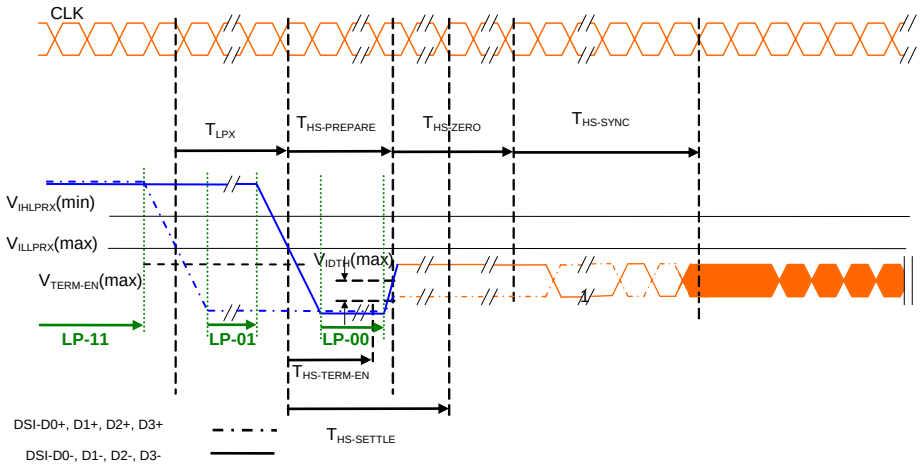


Figure 3 – HSDT Start Sequence.

2.4.5.2.2 HSDT End of Transmission

The display module DSI D0+/-, D1+/-, D2+/- and D3+/- exits High Speed High Transmission as follows:-

Step	Host	Display module
1	End High Speed Data Transmission	Receive the last data
2	Host drives HS-1 for time $T_{HS-TRAIL}$ if the last data bit transmitted was HS-0 Host drives HS-0 for time $T_{HS-TRAIL}$ if the last data bit transmitted was HS-1	
3	Host Drives stop-state LP-11 for a minimum time $T_{HS-EXIT}$.	Monitors the entering stop state LP-11, disables the Termination Impedance and ignores the bits sent during time $T_{HS-SKIP}$.

The sequence for ending High Speed Data Transmission on the DSI bus is shown in the following figure:-

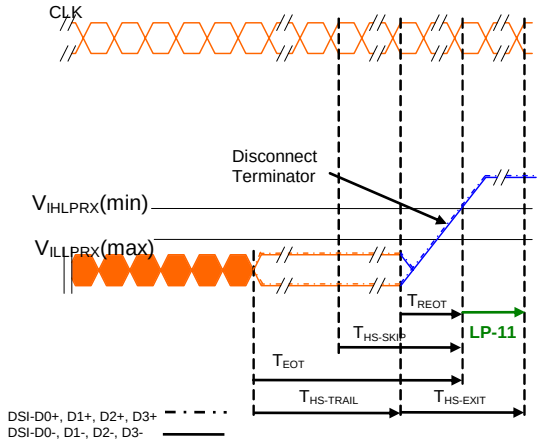


Figure 4 – HSDT End Sequence.

2.4.5.3 Escape Mode

Escape Mode applies only to Data Lane D0+/-. This is a special mode of operation in the Low Power state and is valid in both the forward (Host to Display) and Reverse directions (Display to Host).

The Display module supports the following escape modes:-

Escape Mode Action	Command Type Mode/Trigger	Entry Command Pattern (1^{st} bit to last bit transmitted)	Note
Low Power Data Transmission	Mode	1110 0001 bin	
Ultra Low Power State	Mode	0001 1110 bin	
Remote Application	Trigger	0110 0010 bin	
Acknowledge	Trigger	0010 0001 bin	

It is only possible to enter Escape Mode from Control Mode by the sequence
LP-11 → LP-10 → LP-00 → LP-01 → LP-00.
If LP-11 state is detected before the final bridge state LP-00, then the Escape Mode entry procedure will be aborted and the Display Module will return to the stop state (LP-11).
To exit Escape mode the end sequence LP-10 → LP-00 is applied.

The following example shows the Escape Mode Entry and exit along with Reset-Trigger Escape Command.

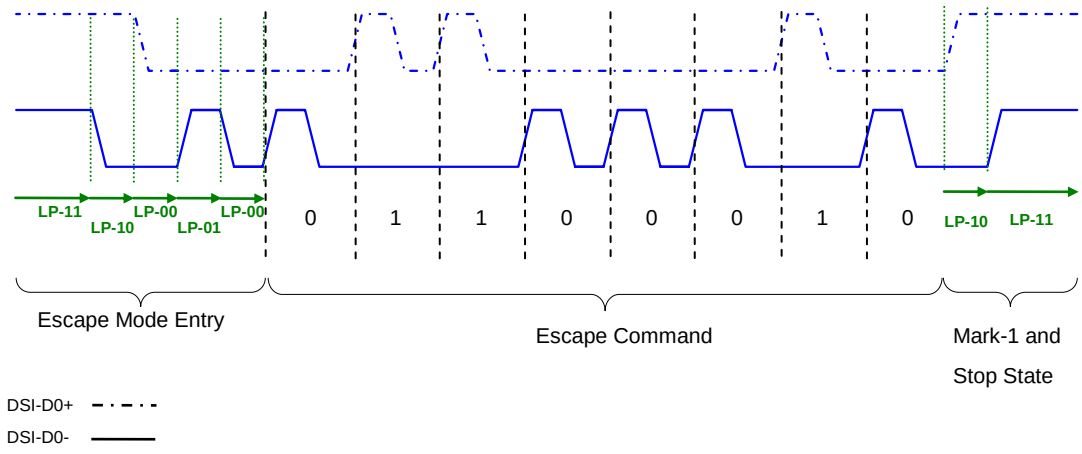


Figure 5 – Escape Mode Sequence.

2.4.5.3.1 Low Power Data Transmission.

Data can be written from the Host to the Display in Low Power Data Transmission. Firstly the Escape Mode Entry Procedure is sent followed by the (LPDT) Escape Command 11100001. Data is encoded by the same Spaced One-Hot code used for Entry Commands and it is possible to add a pause between data bytes by holding both DSI D0+/- lines low as shown in the following example.

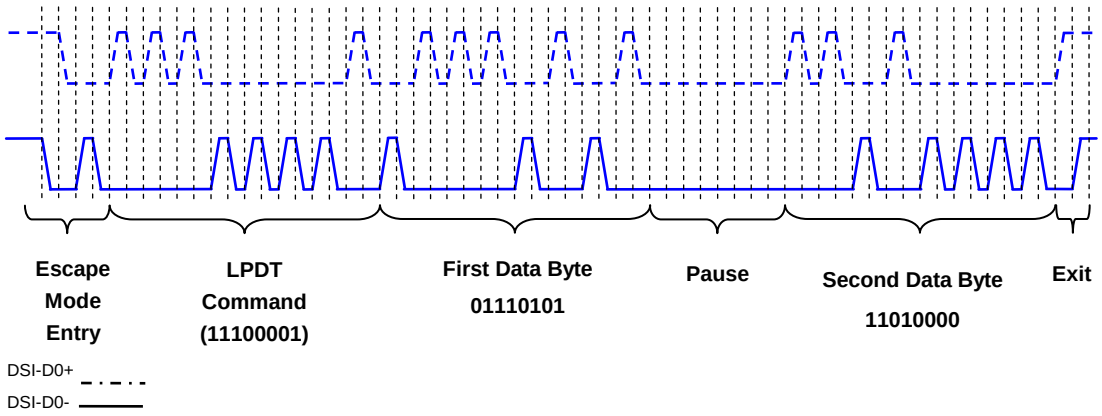


Figure 6 – Low Power Data Transmission Example.

2.4.5.3.2 Ultra Low Power State

The DSI D0+/-, DSI D1+/-, DSI D2+/- and D3+/- data lanes can enter Ultra Low Power State, in this condition both data lines are kept Low by

the Host (LP-00).
To enter Ultra Low Power State, the Escape Command 00011110 is sent after the Escape mode Entry Procedure.
To exit Ultra Low Power State, the Mark01 state (LP-10) should be applied for minimum 1msec followed by the stop state (LP-11).
The following diagram explains Ultra Low Power State entry and exit:-

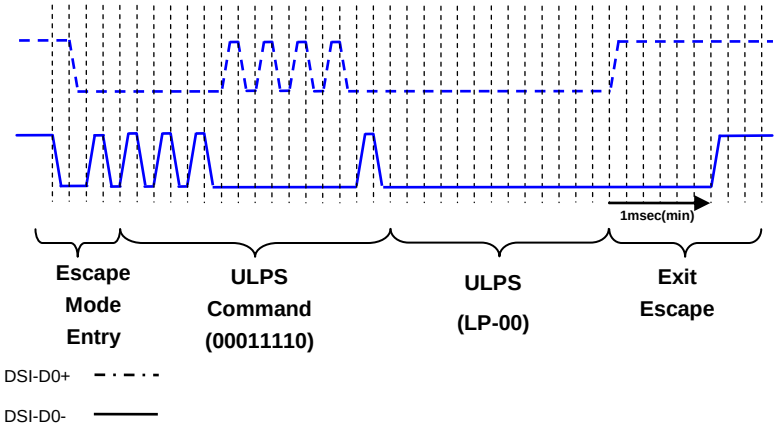


Figure 7 – Ultra Low Power State Example.

2.4.5.3.3 Remote Application Reset

The DSI D0+/-, DSI D1+/- and DSI D2+/- data lanes can enter Remote Application Reset State, in this condition any data bits sent on the data lanes are ignored before the Stop state is received as shown in following example:-

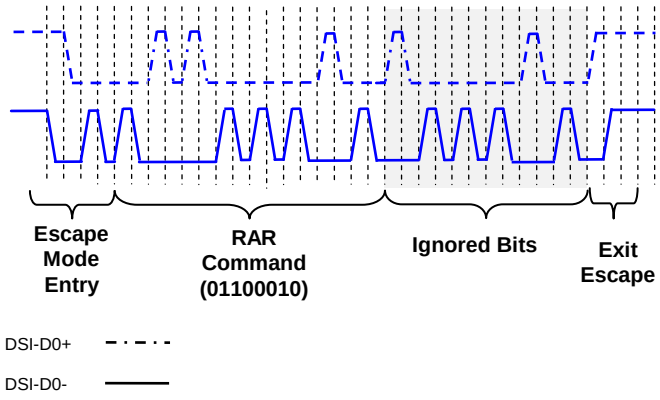


Figure 8 – Remote Application Reset Example.

2.4.5.3.4 Acknowledge Trigger

The Acknowledge Trigger Escape command is used by the host to request an Acknowledge that the preceding command or data sent from the host was successfully received.
To request an Acknowledge, the host will send the Escape Command 00100001 after the Escape Entry Procedure as shown in the following diagram:-

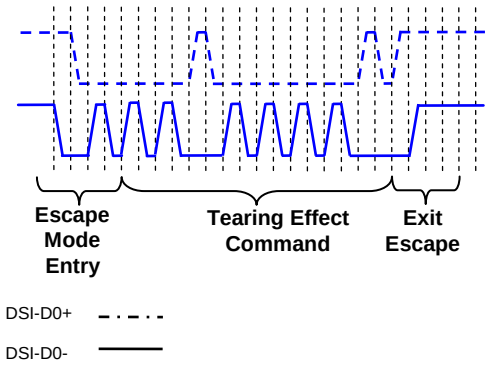


Figure 9 – Acknowledge Trigger.

After sending the Acknowledge Request the host will normally send the Bus Turnaround Command and wait for the Display Module to send the Acknowledge response.

2.4.5.4 Bus Turnaround

The Bus Turnaround procedure can be instigated by either the host or the Display module when they want to receive information from the other device. The same sequence is used regardless of whether the host or the display is performing the turnaround request. The sequence is as follows:-

Step	Initial Tx side => Final Rx Side	Initial Rx side => Final Tx Side
1	Drives Stop State LP-11	Monitors the Stop State
2	Drives LP-Request state LP-10 for time T_{LPX}.	Monitors the transition from LP-11 to LP-10
3	Drives LP-00 for time T_{LPX}.	Monitors the transition from LP-10 to LP-00.
4	Drives LP-10 for a time T_{LPX}.	Monitors the transition from LP-00 to LP-10.
5	Drives LP-00 for a time T_{TA-GO}.	Monitors the transition from LP-10 to LP-00 and waits for a time $T_{TA-SURE}$.
6		Drives LP-00 for a time T_{TA-GET}.
7	Stops driving the DSI Lanes and output drivers become High-Z. Receiver is monitoring for LP-10 state.	
8		Drives LP-10 for a time T_{LPX}.
9	Monitors LP-10 and interprets this as an acknowledgement that the other side has taken over the bus. Waits for Stop state (LP-11) to complete the procedure	
10		Drives LP-11 for a time T_{LPX}.
11	Monitors the transition from LP-10 to LP-11 and interprets this as Turnaround complete. Switched to LP Rx mode and waits for next action from the other side.	

The Bus Turnaround Sequence is as follows:-

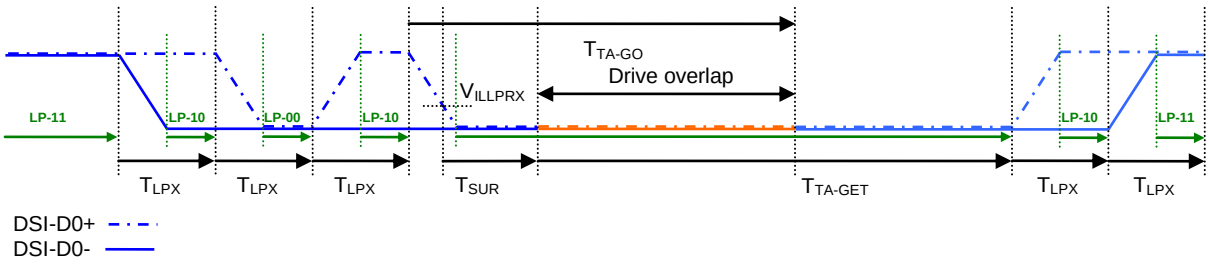


Figure 10 –Bus Turnaround Sequence.

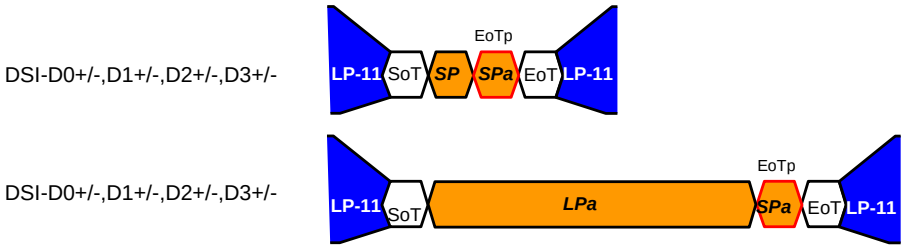
The bus turnaround procedure can be aborted if a Stop state (LP-11) is sent before the bus starts to be driven LP-00 at the beginning of time period T_{SURE} in Fig10. In this event, the lanes will return to the stop state LP-11.
It is not possible to abort the turnaround procedure after LP-00 at the time T_{SURE} has started to be driven.

2.4.6 Packet Level Communication

Data is transferred between host and the display module and vice-versa by means of packet Level communication. Packet communication applies to both Low Power Data Transmission mode (LPDT) and High Speed Data Transmission (HSDT). A Transmission may consist of both Short Packets (SPa) and Long Packets (LPa), it may contain only one packet or multiple packets. Also multiple packets may consist of both Short (SPa) and Long (LPa) packets.

For High Speed Mode, Each Transmission requires Start of Transmission SoT, End of Transmission Packet (which is the last transmitted packet (SPa)) and End of Transmission (EoT).

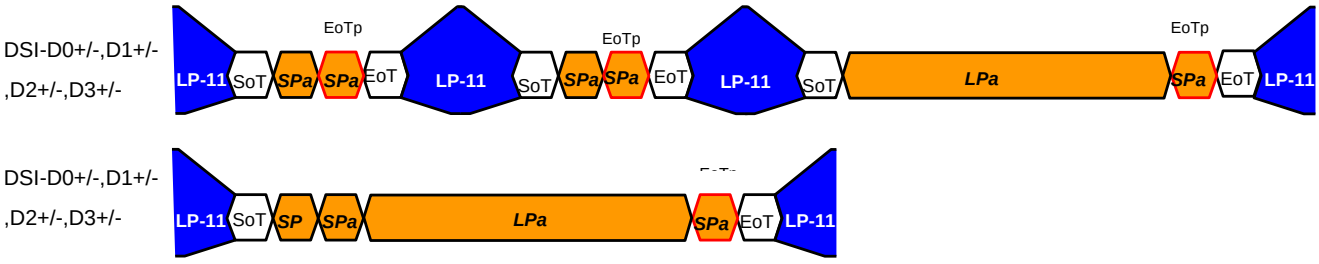
Example of single Short Packet Transmission and single Long Packet Transmission.



Key:
LP-11 – Low Power Mode
SoT – Start of Transmission
SPa – Short Packet
LPa – Long Packet
EoTp – End of Transmission Packet

Figure 11 – Single Packet Transmission.

Example of the same multiple Short and Long Packet Transmissions sent in Separate and Single transmissions.



Key:
LP-11 – Low Power Mode
SoT – Start of Transmission
SPa – Short Packet
LPa – Long Packet
EoTp – End of Transmission Packet

Figure 12 – Multiple Packet Transmission.

2.4.6.1 Data Byte Order in HSDT

When 3 channels are in use, data is always transmitted in the order of the First Byte appears on DSI Lane 0, the second byte on DSI data Lane 1, third on Data Lane 2 , fourth on DSI data lane 0 and so on.
Both DSI-D0+/-, DSI-D1+/-, DSI-D2+/- and DSI-D3+/- will always start data transmission simultaneously with SoT however depending upon the number of bytes being transferred one lane may complete transfer before the other lane.

2.4.6.2 Packet Bit and Byte Order

For each byte in a packet, the bit order is the LSB is sent first and the MSB is sent last. For packets with multiple bytes, the least significant byte is sent first and the most significant byte is sent last.

2.4.6.3 Short Packet Format

Short packets are 4 bytes in length. They are used mainly for sending commands with either none or one parameter. The structure of the packet is as follows, this example is using High Speed Data Transfer, Low Power Data Transfer can also be used.:-

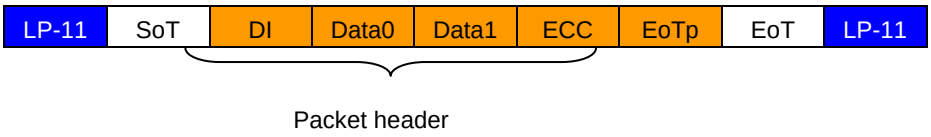


Figure 13 – Short Packet Format.

Where:-

DI = Data Identifier Byte

Contains the Virtual Channel Identifier and the Data Type information.

Data0 = LSB Byte

Data1 = MSB Byte

ECC = Error Correction Code

8-Bit Error Code Correction for the correction of single-bit error and the detection of 2-bit errors.

Bit order on the short packet appears as shown in the following example:-

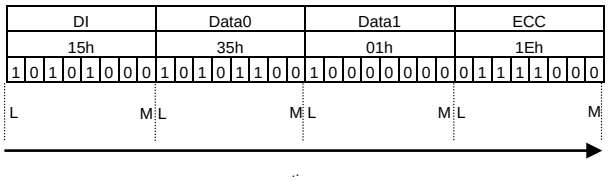


Figure 14 –Short Packet Example.

2.4.6.4 Long Packet Format

Long packets are minimum 6bytes in length and can contain up to a maximum of 65,536 data bytes. The structure of the packet is as follows, this example is using High Speed Data Transfer, Low Power Data Transfer can also be used:-

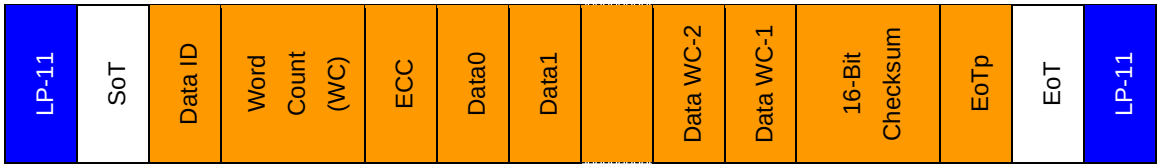


Figure 15 – Long Packet Format.

Where:-

Data ID = Data Identifier Byte

Contains the Virtual Channel Identifier and the Data Type information.

WC = 16-Bit Word Count

The word count informs how many data bytes will be sent in the packet payload from this the Display Module can determine the packet end.

ECC = Error Correction Code

8-Bit Error Code Correction for the correction of single-bit error and the detection of 2-bit errors within the Packet Header.

Data0→Data WC-1 = Packet Data (Payload)

16-Bit Checksum = Checksum for the transmitted packet data payload.

The Display module will calculate the Checksum value from the received data and compare with the transmitted Checksum value from the host. The display module will report an error at the next Bus Turnaround if the values are not equal.

Bit order on the long packet appears as shown in the following example:-

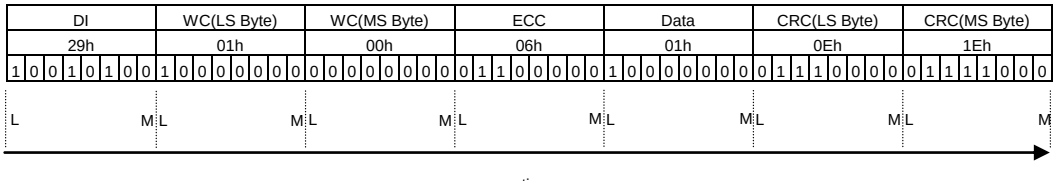


Figure 16 – Long Packet Example.

2.4.6.5 Data Identifier Byte

The Data Identifier Byte serves 2 purposes. One is the Virtual Channel Identification and the other specifies the Data type:-

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Virtual Channel (VC)		Data Type (DT)					

2.4.6.5.1 Virtual Channel Identifier (VC)

The Virtual Channel can allow addressing up to 4 channels, in other words 4 different devices connected to the same receiver.
This display module uses virtual channel 0, i.e. Bits 7 and 6 = '00'.
When the display module sends information back to the host it will also assign Virtual Channel 0 in its packet header.

2.4.6.5.2 Data Type Field (DT)

The Data Type Field informs if the packet is a Short (SPa) or Long Packet (LPa), it also contains information about the type of data transaction from the host to the display module and also from the display module to the host. The supported data transaction types are listed in the following tables:-

Data Types from the Host to the Display Module.

Data Type (Hex)	Data type (binary)						Description	Packet Size	Note
	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0			
01h	0	0	0	0	0	1	Sync Event, V Sync Start	Short	
21h	1	0	0	0	0	1	Sync Event, H Sync Start	Short	
08h	0	0	1	0	0	0	End of Transmission Packet (Note 1).	Short	
22h	0	1	0	0	1	0	Shut Down Peripheral command	Short	
32h	1	1	0	0	1	0	Turn On Peripheral Command	Short	
13h	0	1	0	0	1	1	Generic Short WRITE 1 parameter	Short	1, 2
23h	1	0	0	0	1	1	Generic Short WRITE, 2 parameters	Short	1, 3
29h	1	0	1	0	0	1	Generic Long Write	Long	1
14h	0	1	0	1	0	0	Generic Short READ, 1 parameter	Short	1, 2
24h	1	0	0	1	0	0	Generic Short READ, 2 parameters	Short	1, 3
05h	0	0	0	1	0	1	DCS WRITE with No Parameter.	Short	
15h	0	1	0	1	0	1	DCS WRITE with One Parameter.	Short	
06h	0	0	0	1	1	0	DCS READ with No Parameter.	Short	
37h	1	1	0	1	1	1	Set Maximum Return Packet Size	Short	
09h	0	0	1	0	0	1	Null Packet, No data (Note 2).	Long	
19h	0	1	1	0	0	1	Blanking Packet, no data	Long	
39h	1	1	1	0	0	1	DCS WRITE Long	Long	
2Eh	1	0	1	1	1	0	Loosely Packed Pixel Stream,18bit RGB 6-6-6 Format	Long	
3Eh	1	1	1	1	1	0	Packed Pixel Stream,24bit RGB 8-8-8 Format	Long	
other	x	x	x	x	x	x	DO NOT USE All unspecified codes are reserved		

Notes:
1. The receiver process packets with data type (Generic Write/Read) the same way as data type (DCS Write / Read).
2. Generic Write/Read with 1 parameter: Payload Bytes = Command + 00h.
3. Generic Write/Read with 2 parameter: Payload Bytes = Command + Parameter.
4. The receiver will ignore packets with data type that neither listed in table above nor in MIPI DSI spec.

Data Types from the Display Module to the Host.

Data Type	Data Type (Binary)						Description	Packet Size	Symbol
(Hex)	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0			
02h	0	0	0	0	1	0	Acknowledge with Error Report.	Short	AwER
1Ch	0	1	1	1	0	0	DCS READ Long Response.	Long	DCSRR-L
21h	1	0	0	0	0	1	DCS READ Short Response, 1 Byte Returned.	Short	DCSRR1-S
22h	1	0	0	0	1	0	DCS READ Short Response, 2 Bytes Returned.	Short	DSCRR2-S
1Ah	0	1	1	0	1	0	Generic Read Long Response	Long	GENRR-L
11h	0	1	0	0	0	1	Generic Read Short Response, 1byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Read Short Response, 2byte returned	Short	GENRR2-S

Notes:

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “ Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

2.4.6.6 Packet Data on the Short Packet (SPa)

Packet data is 2 bytes long in a short packet. If the length of data to be sent requires only 1 byte, then the data in the 2nd byte (Data 1) will be set as all zero.

Packet data is always sent in the order Data0 first, followed by Data1as shown in the below example:-

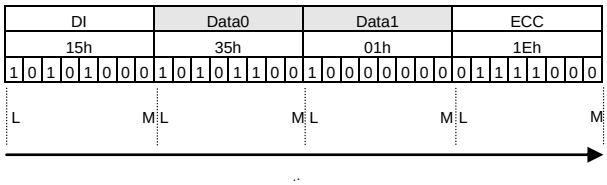


Figure 17 – Data on the Short Packet.

2.4.6.7 Word Count (WC) on the Long Packet.

The word count is used to indicate how many bytes of data will be sent after the Packet header.

The word count is 2 bytes long and can define a minimum of 0 bytes to a maximum of 65,536 bytes to be sent.

The sending order of the 2 word count bytes is the Least Significant Byte is always sent first followed by the most Significant Byte.

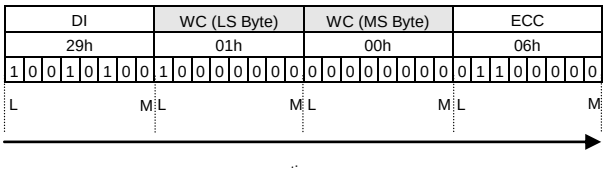


Figure 18 – Word Count on the Long Packet.

2.4.6.8 Error Correction Code (ECC)

The Error Correction Code allows single-bit errors to be corrected and 2 or more-bit errors to be detected in the Packet Header. It is used for both Short (Spa) and Long (Lpa) packets.

When receiving data transmission from the host, the display module will generate ECC byte from the received packet header Data Identifier (DI) and Data0, Data1 bytes in the case of SPa and Data Identifier (DI), WC (LS Byte), WC (MS Byte) in the case of LPa. It will compare this generated ECC byte with that sent on the Packet Header to determine if error has occurred or not.

When sending Data Transmission to the host, the Display Module will generate the ECC byte from the packet data to be sent and appends to the packet header. The ECC byte is always the last transmitted byte on the packet header as highlighted in this example for the Short Packet (SPa):-

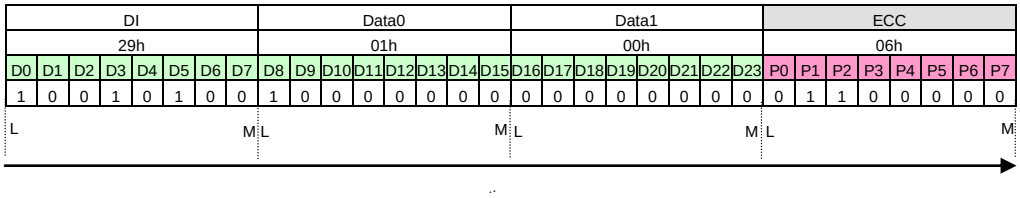


Figure 19 – Error Correction Code on the Short Packet.

The Pink coloured bits are the error correction bits.
The Green coloured bits are the bits that can be corrected by the ECC.

The device transmitting the data sends data D[23..0] and ECC P[7..0]. An 8-bit ECC allows correction for up to 64bits, however in this application only 24bits require to be checked for correction, so bits P7 and P6 are always set to '00' on the ECC.
The remaining bits are generated as follows:-

P7=0
P6=0
P5=D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
P4=D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
P3=D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
P2=D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
P1=D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
P0=D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

where "^" = XOR function.

The receiving device generates the ECC from the received data D[23..0] by the same function as above to generate IECC (internal ECC). The function ECC^IECC is performed and the result OP[7..0]determines if error has occurred or not.

- If the result of ECC^IECC = 00h, then there is no error in the data received.
- If the result of ECC^IECC ≠ 00h and is listed on the table in Fig20, then the error is a single bit error and that corresponding bit can be corrected. Also the "ECC error, single bit (detected and corrected)" bit is flagged.
- If the result of ECC^IECC ≠ 00h and is not listed on the table in Fig20, then the error is in 2bits or more and cannot be corrected, the packet is ignored and the "ECC error, multi-bit (detected, not corrected)" bit is flagged.

Data Bit	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	ECC^IECC
D0	0	0	0	0	0	1	1	1	07h
D1	0	0	0	0	1	0	1	1	0Bh
D2	0	0	0	0	1	1	0	1	0Dh
D3	0	0	0	0	1	1	1	0	0Eh
D4	0	0	0	1	0	0	1	1	13h
D5	0	0	0	1	0	1	0	1	15h
D6	0	0	0	1	0	1	1	0	16h
D7	0	0	0	1	1	0	0	1	19h
D8	0	0	0	1	1	0	1	0	1Ah
D9	0	0	0	1	1	1	0	0	1Ch
D10	0	0	1	0	0	0	1	1	23h
D11	0	0	1	0	0	1	0	1	25h
D12	0	0	1	0	0	1	1	0	26h
D13	0	0	1	0	1	0	0	1	29h
D14	0	0	1	0	1	0	1	0	2Ah
D15	0	0	1	0	1	1	0	0	2Ch
D16	0	0	1	1	0	0	0	1	31h
D17	0	0	1	1	0	0	1	0	32h
D18	0	0	1	1	0	1	0	0	34h
D19	0	0	1	1	1	0	0	0	38h
D20	0	0	0	1	1	1	1	1	1Fh
D21	0	0	1	0	1	1	1	1	2Fh
D22	0	0	1	1	0	1	1	1	37h
D23	0	0	1	1	1	0	1	1	3Bh

Figure 20 – Table of One Bit Error Value for ECC

For example if the value of the function ECC^IECC (OP[7..0]) = 1Fh, then by referring to the above table, this means there has been a one bit error on bit D20. The receiver can correct this error by complementing the bit value of D20 and storing the modified value.

2.4.6.9 Packet Footer on Long Packet (LPa)

To detect errors in transmission of Long Packets, a checksum is calculated over the payload portion of the data packet. Long packets can transmit from 0 to 65,536 bytes, on the special case where there are 0 bytes transmitted, the Checksum value will be fixed to FFFFh.

The checksum can only detect the presence of one or more errors on a transmitted data payload, it cannot make any correction.

The checksum is realised by a 16-bit Cyclic Redundancy Check calculation by the polynomial x^16+x^12+x^5+x^0

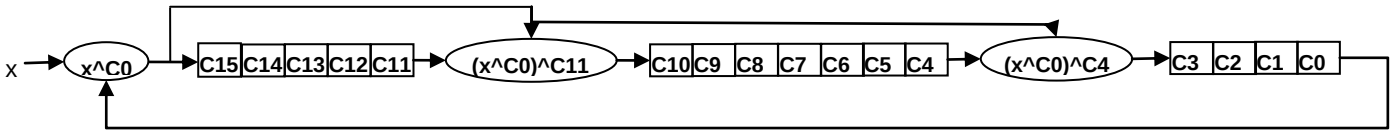


Figure 21 – 16-Bit Cyclic Redundancy Check Calculation

In the transmitting device, before Packet Data transmission starts, the CRC shift register is initialized to FFFFh, then packet data (excluding the Packet Header) enters as a bitwise stream at “x” in above figure from the Least Significant Bit first.
After all the Bytes in the packet payload have passed through the CRC shift register, then the shift register contains the Checksum Value C[15..0]. This is appended to the data stream and passed to the receiver.
The receiver will calculate Checksum by the same method and compare its calculated value versus the transmitted value. If an error is detected, then the “Checksum Error” bit is flagged.

2.4.7 Host to Display Module Packet Transmissions.

2.4.7.1 Display Command Set (DCS)

The Display Command Set is described in Section 0, it is used for sending commands from the Host to the Display Module. The Command is always set on Data0 and parameters are set on the following bytes.
In the case of Short Packet Transfer (SPa), if the command has no parameter, then the second byte (Data1) is set to 00h.
If the command requires more than one parameter, then the Long Packet Transfer (LPa) is used.

The following transfer types are supported; please refer to the table in Section 2.4.6.5.2 for the various Data Field Type Code

2.4.7.2 DCS Command WRITE with No Parameter, (DT=05h).

DCS Command WRITE with No Parameter is used for writing a command which has no parameter to the Display Module, always using Short Packet (SPa). The following commands can be sent by this method:-

Example of sending Sleep In (10h) command:-

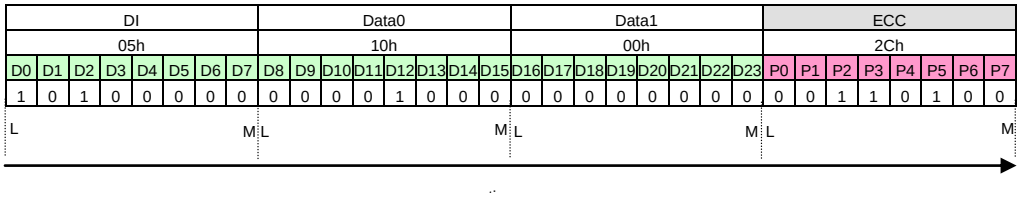


Figure 22 – DCS Command WRITE with No Parameter.

2.4.7.3 DCS Command Write with 1 Parameter, (DT=15h).

DCS Command WRITE with 1 Parameter is used for writing a command which has 1 parameter to the Display Module, always using Short Packet (SPa).

Example of sending Gamma Set (26h) command:-

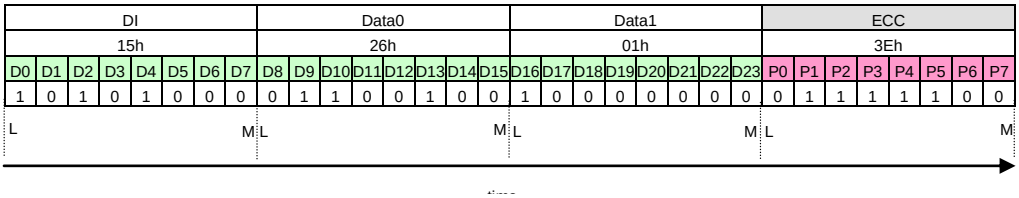


Figure 23 – DCS Command WRITE with No Parameter.

2.4.7.4 DCS Command Read with No Parameter, (DT=06h) & Set Maximum Return Size (DT=37h).

DCS Command Read with no Parameter is used to request data from the Display Module, always using Short Packet (SPa). Before sending this Data Type, the host has to define to the Display Module what is the maximum size of the return packet. This is defined by Data Type Set Maximum Return Size (DT=37h). Following this read request, the Bus Turnaround shall be performed so the Display Module can send back the requested data. The following read commands can be requested by this method:-

Example of requesting Read ID1 (DAh) command:-

Firstly send the maximum return size (DT=37h) then Read Command with no parameter (DT=06h).

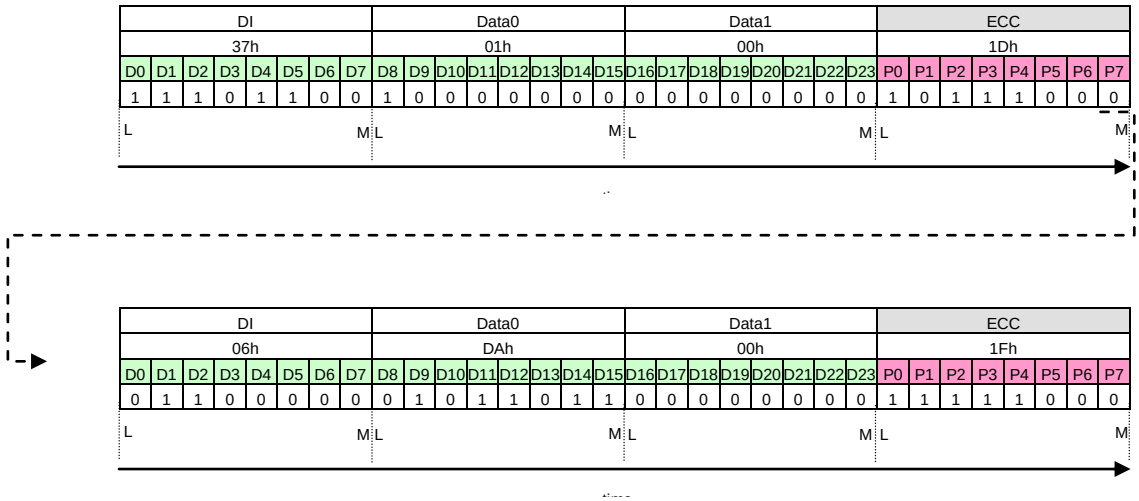


Figure 24 – DCS Command Read.

After sending the Bus Turnaround Command, the Display Module will reply with either of the following:-

1. An acknowledge with Error Report (AwER) in a short packet if there is an error to report. See Section 2.4.9.1
2. Read data for the requested read command in Short (SPa) or Long (LPa) packets.

Note:

The Default value of the Maximum Return Size (DT=37h) after Power On, Hardware or Software Reset is 1.

2.4.7.5 Null Packet, No data, (DT=09h)

The purpose of this command is to keep the Data Lanes in High Speed Mode if required. The format of this packet is Long Packet (LPa). Any data included in a Null Packet is completely ignored by the Display Module.

Example of Sending a Null Packet of 5 bytes in length:-

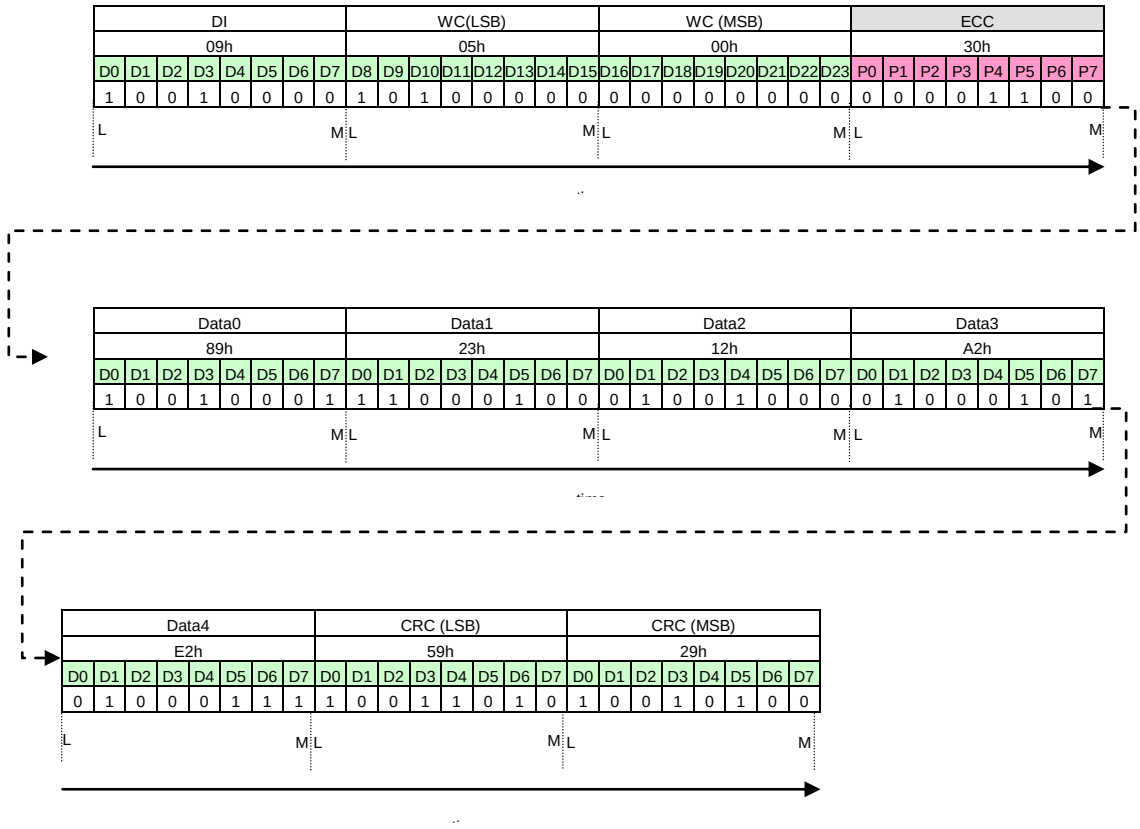


Figure 25 – Null Packet, No Data.

2.4.7.6 DCS WRITE Long (DT=39h).

DCS WRITE Long is used for writing commands both with and without parameter types to the Display Module, always using Long Packet (LPa). The following commands can be sent by this method:-

Example 1 - Sending Sleep In (10h) command (DCS Command with no Parameter):-

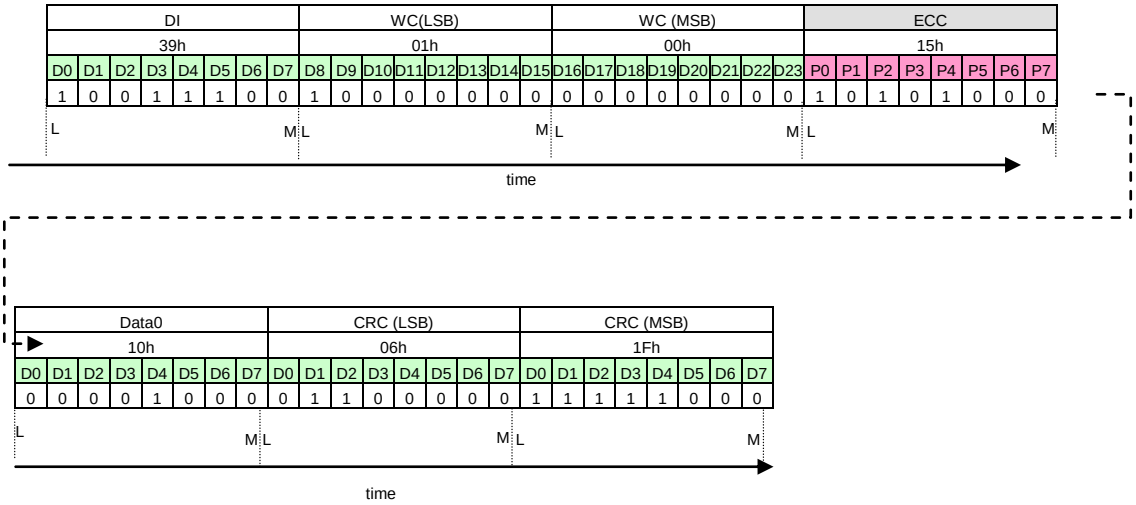


Figure 26 – Long Packet Example 1.

Example 2 - Sending Gamma Set (26h) command (DCS Command with one Parameter):-

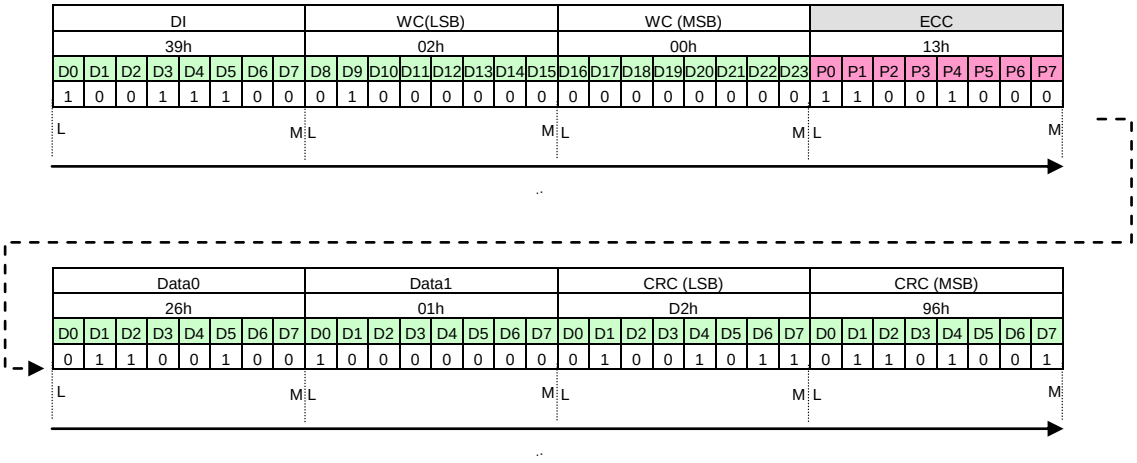


Figure 27 – Long Packet Example 2.

Example 3 - Sending Column Address Set (2Ah) command (DCS Command with four Parameters):-

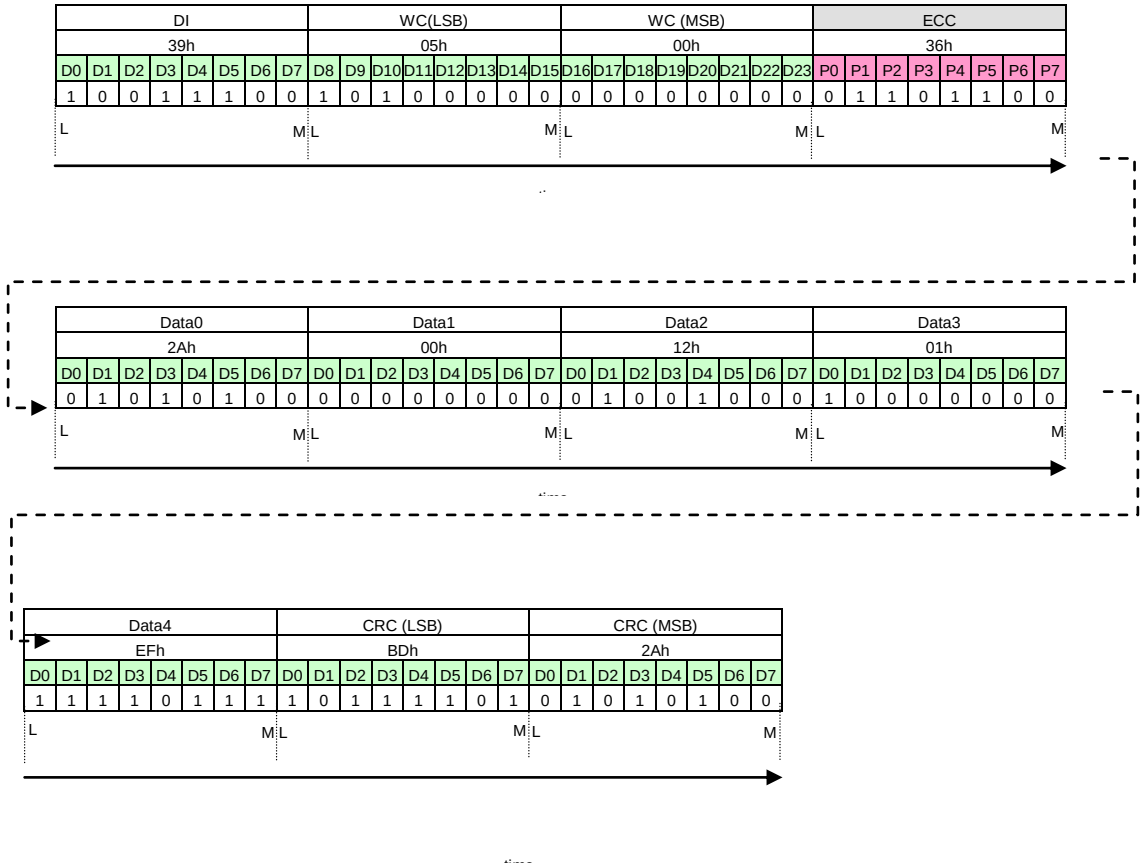


Figure 28 – Long Packet Example 3.

2.4.7.7 End of Transmission Packet (DT=08h)

The purpose of the End of Transmission Packet (EoTp) is to indicate to the Display module that the host intends to terminate High Speed Data Transmission. It is always using Short Packet (SPa). This packet is always added after the last payload data and before the End of Transmission Sequence.
It is possible that the EoTp is sent in Low Power Mode, in such case there is no influence to the display module.

Example of End of Transmission Packet:-

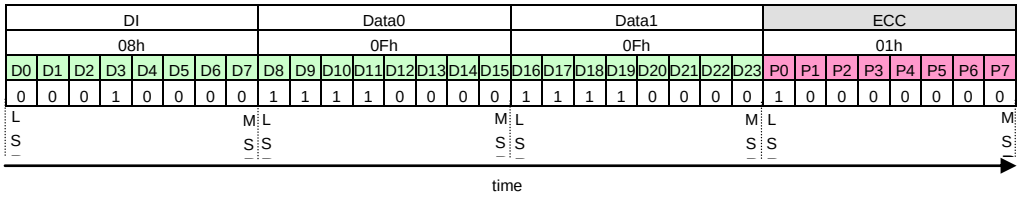


Figure 29 – End of Transmission Packet.

2.4.7.8 Generic Short WRITE Packet with 1, or 2 parameters (DT=13h or 23h)

Generic Short WRITE command is a Short packet type for sending generic command and data to the LCD.
The complete packet shall be four bytes in length including an ECC byte. The two Data Type MSBs, bits [5:4], indicate the number of valid parameters (1, or 2). For single-byte parameters, the parameter shall be sent in the first data byte following the DI byte and the second data byte shall be set to 0x00.

2.4.7.9 Generic Short Read Packet with 1, or 2 parameters (DT=14h or 24h)

Generic READ request is a Short packet requesting data from the LCD.
Returned data may be of Short or Long packet format. Note the Set Max Return Packet Size command limits the size of returning packets so that the host processor can prevent buffer overflow conditions when receiving data from the peripheral. If the returning block of data is larger than the maximum return packet size specified, the read response will require more than one transmission. The host processor shall send multiple Generic READ requests in separate transmissions if the requested data block is larger than the maximum packet size.

2.4.7.10 Generic Long Write (DT=29h)

Generic Long Write Packet is used to transmit arbitrary blocks of data from a host processor to a peripheral in a Long packet. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum as DCS Long Write.

2.4.8 Host to Display Module Packet Transmissions for Video mode operation

2.4.8.1 Sync Event (V Start, H Start) (DT=01h , 21h)

Sync Events are Short packets to represent timing information as accurately as possible a V sync and H Sync Start event. Timing position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the LCD. See section for timing details of interlaced video formats. Sync events may be concatenated with blanking packets to transport inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however.

2.4.8.2 Blanking Packet (Long) (DT=19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload.

2.4.8.3 Loosely Packed Pixel Stream (Long) (DT=2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits, but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte as shown in Figure 27. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

Figure 30 – 18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet

2.4.8.4 Packed Pixel Stream , 24bit RGB 8-8-8 Format (Long) (DT=3Eh)

Packed Pixel Stream 24-Bit Format shown in Figure 28 is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

Figure 30– 24-bit per Pixel – RGB Color Format, Long Packet

2.4.8.5 Shutdown Peripheral Command (DT=22h)

Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode display module for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up, command.

2.4.8.6 Turn On Peripheral Command (DT=32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode display module for normal display operation.

2.4.9 Display Module to Host Packet LP Transmissions.

2.4.9.1 Acknowledge and Error Report (DT=02h)

The purpose of the Acknowledge and Error Report is to feedback to the Host if any errors occurred in data transmissions from the Host to the Display Module since the previous communication from the Display Module to the Host. It is always using Short Packet (SPa).

Example of Acknowledge and Error Report:-

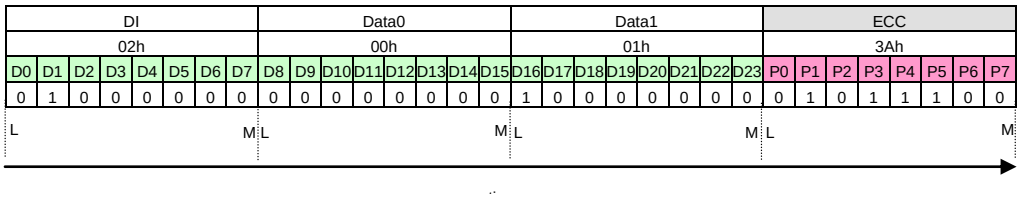


Figure 32 – End of Transmission Packet.

In general, after there has been communication from the Host to the Display Module followed by a Bus Turnaround BTA, the Display Module will respond with either an Acknowledge if there have been no recorded error or an “Acknowledge and Error Report” Packet if there are errors to report.
The following table provides a list of the bit assignments for the “Acknowledge and Error Report” packet:-

Bit	Description	Implementation
0	SoT Error	No
1	SoT Sync Error	No
2	EoT Sync Error	No
3	Escape Mode Entry Command Error	Yes
4	Low-Power Transmit Sync Error	Yes
5	Any Protocol Timer Time-Out	No
6	False Control Error	No
7	Reserved	-
8	ECC Error, single-bit (detected and corrected)	Yes
9	ECC Error, multi-bit (detected, not corrected)	Yes
10	Checksum Error (Long Packet only)	Yes
11	DSI Data Type Not Recognized	Yes
12	DSI Virtual Channel (VC) ID Invalid	Yes
13	Invalid Transmission Length	No
14	Reserved	-
15	DSI Protocol Violation.	No

2.4.9.2 DCS Read Long Response (DT=1Ch)

DCS Read Long Response is used for sending requested read data from the Display Module back to the Host. The format is the same as Long Packet (LPa) writing from the Host to the Display Module i.e. It has a packet header containing the Data Identifier, two byte Word Count and an ECC byte.

Example – Sending 5 bytes of data:-

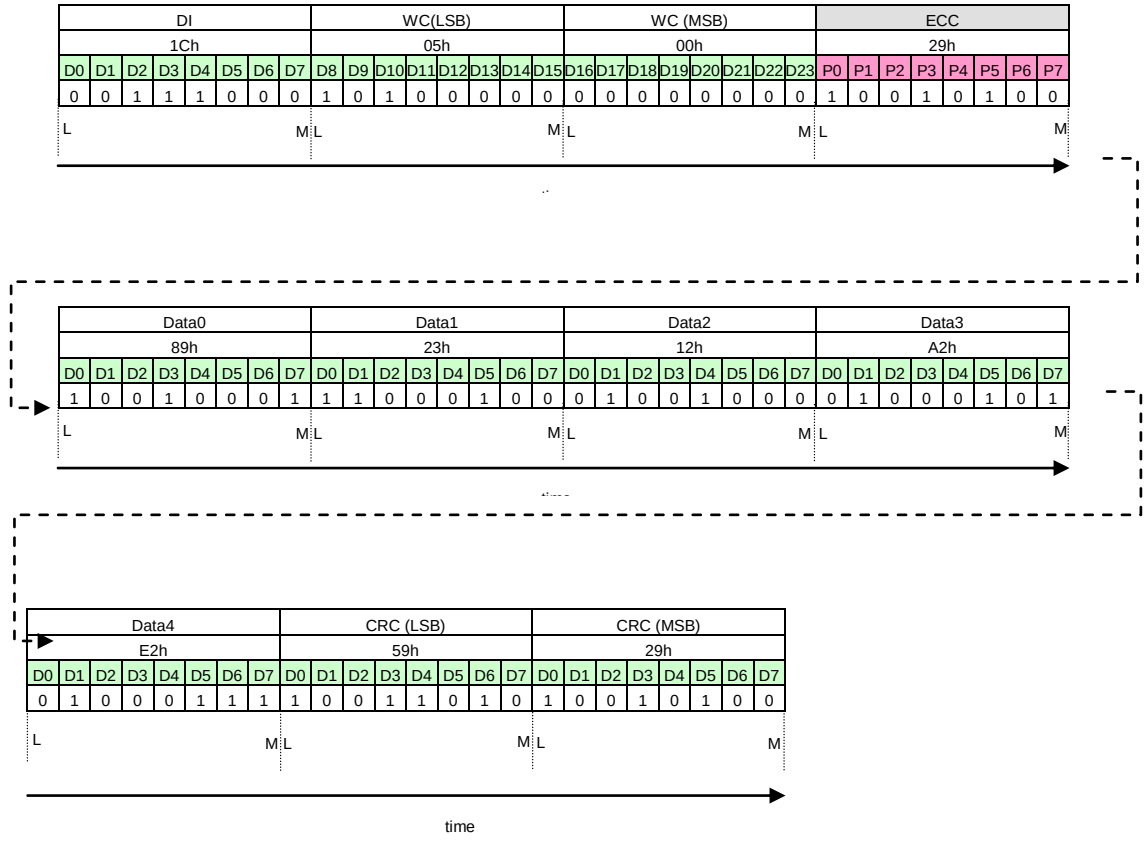


Figure 30 – DCS Read Long Response.

2.4.9.3 DCS Read Short Response, 1 Byte Returned (DT=21h)

DCS Read Short Response with 1 byte Returned is used for sending requested read data of 1 byte in length, always using Short Packet (SPa).

Example of sending DCS Read Short Response with 1 byte Returned:-

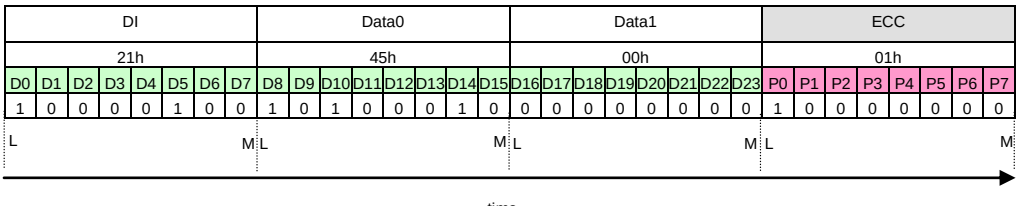


Figure 31 – DCS Read Short Response, 1 byte Returned.

2.4.9.4 DCS Read Short Response, 2 Byte Returned (DT=22h)

DCS Read Short Response with 2 bytes Returned is used for sending requested read data of 2 bytes in length, always using Short Packet (SPa).

Example of sending DCS Read Short Response with 2 bytes Returned:-

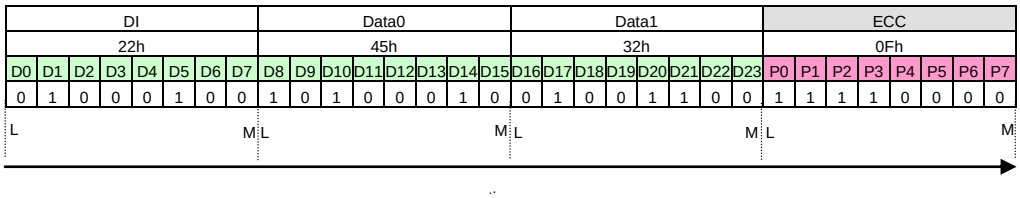
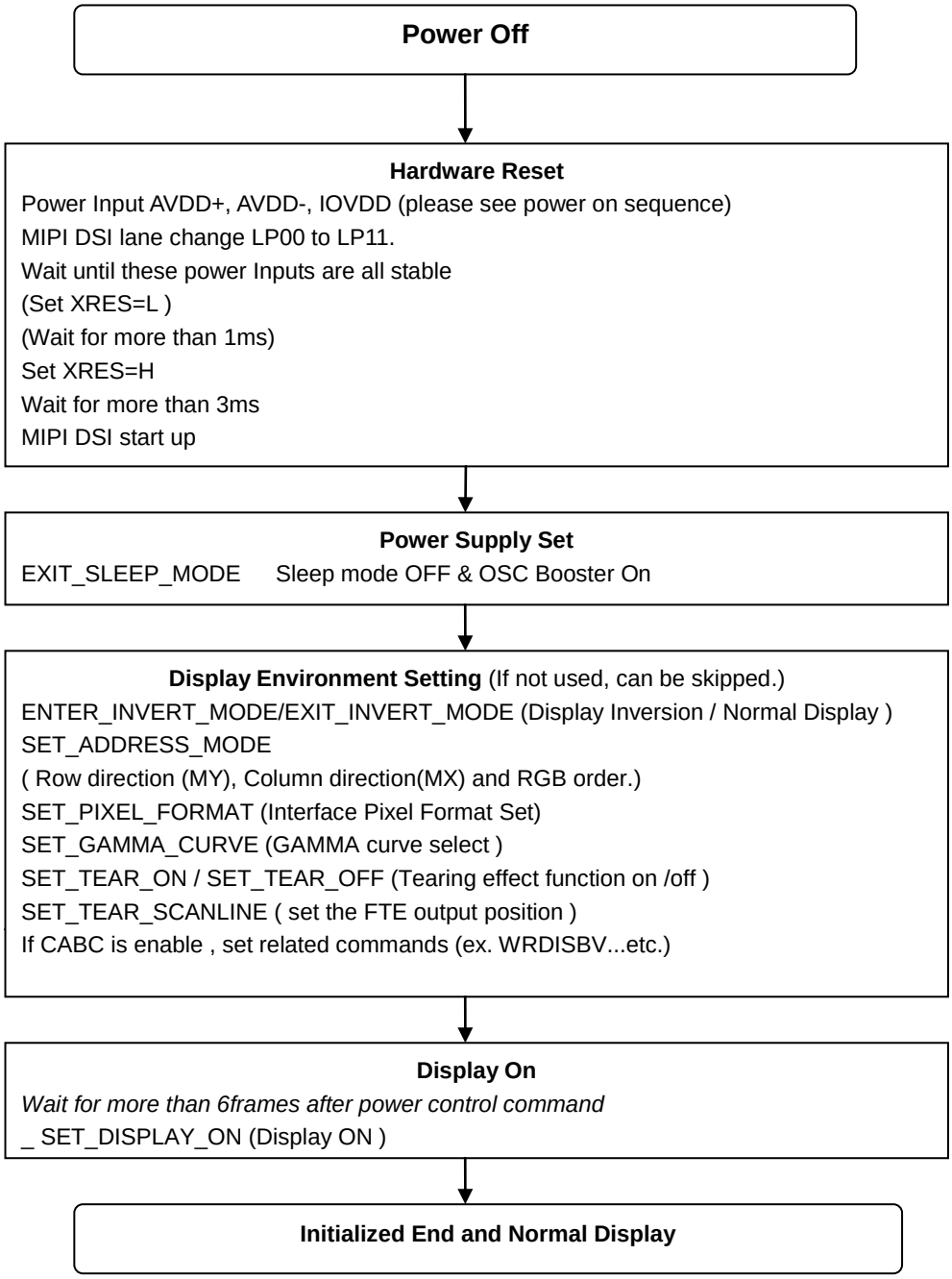


Figure 32 – DCS Read Short Response, 2 bytes Returned.

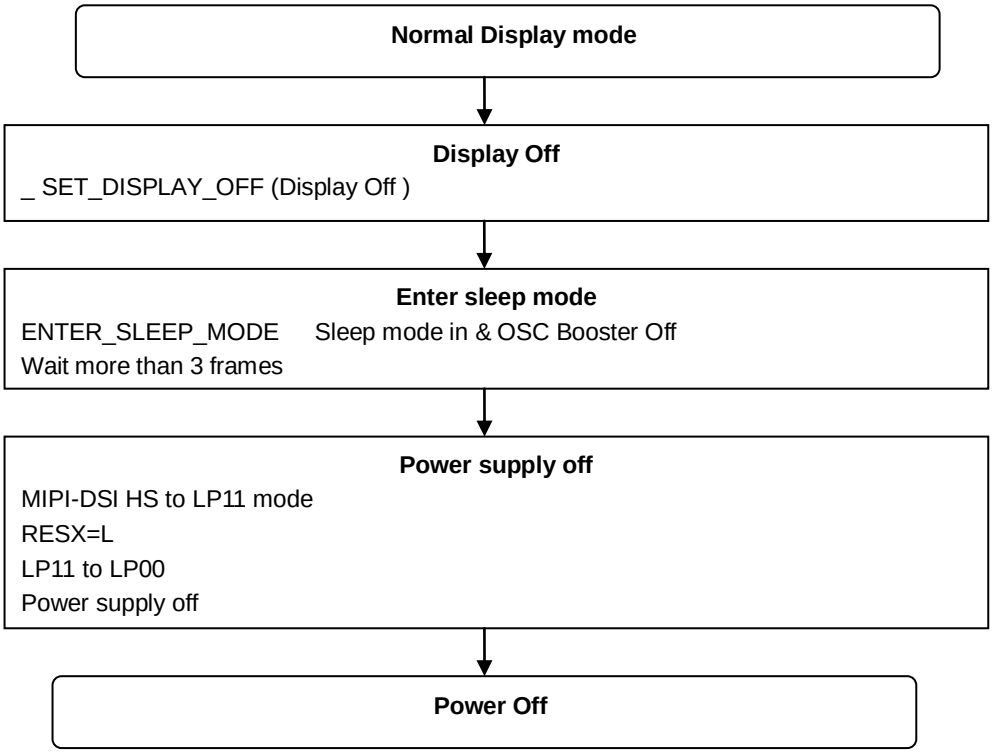
2.5 POWER SUPPLY SETTING SEQUENCE

The power supply ON/OFF setting for Display ON/OFF, Sleep Set/Exit sequences is illustrated in figure below. When setting instruction to the R63311, the sequences shown in below figures must be followed to complete the instruction setting.

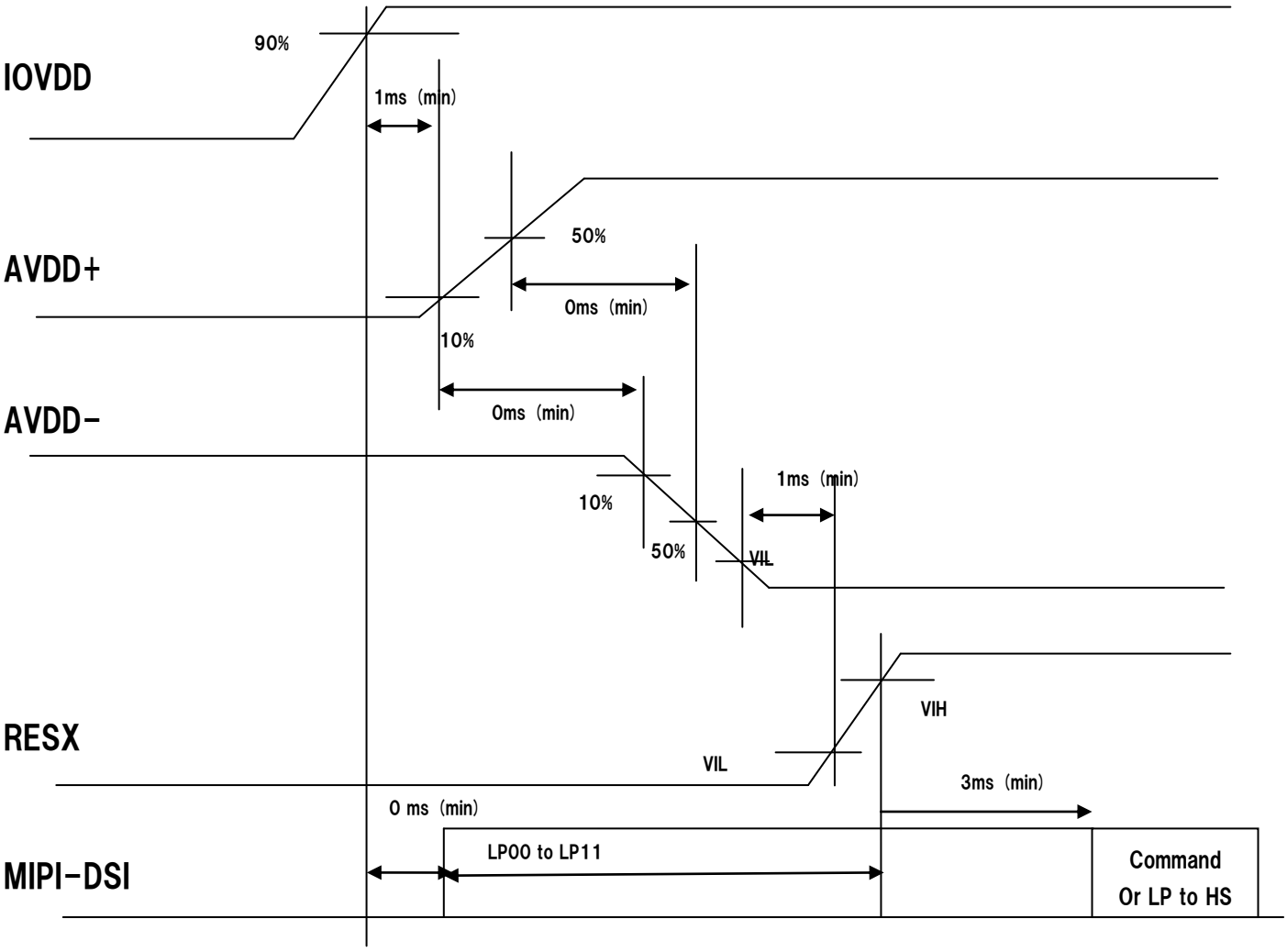
2.5.1 Power and Display on sequence.



2.5.2 Power and Display off sequence.

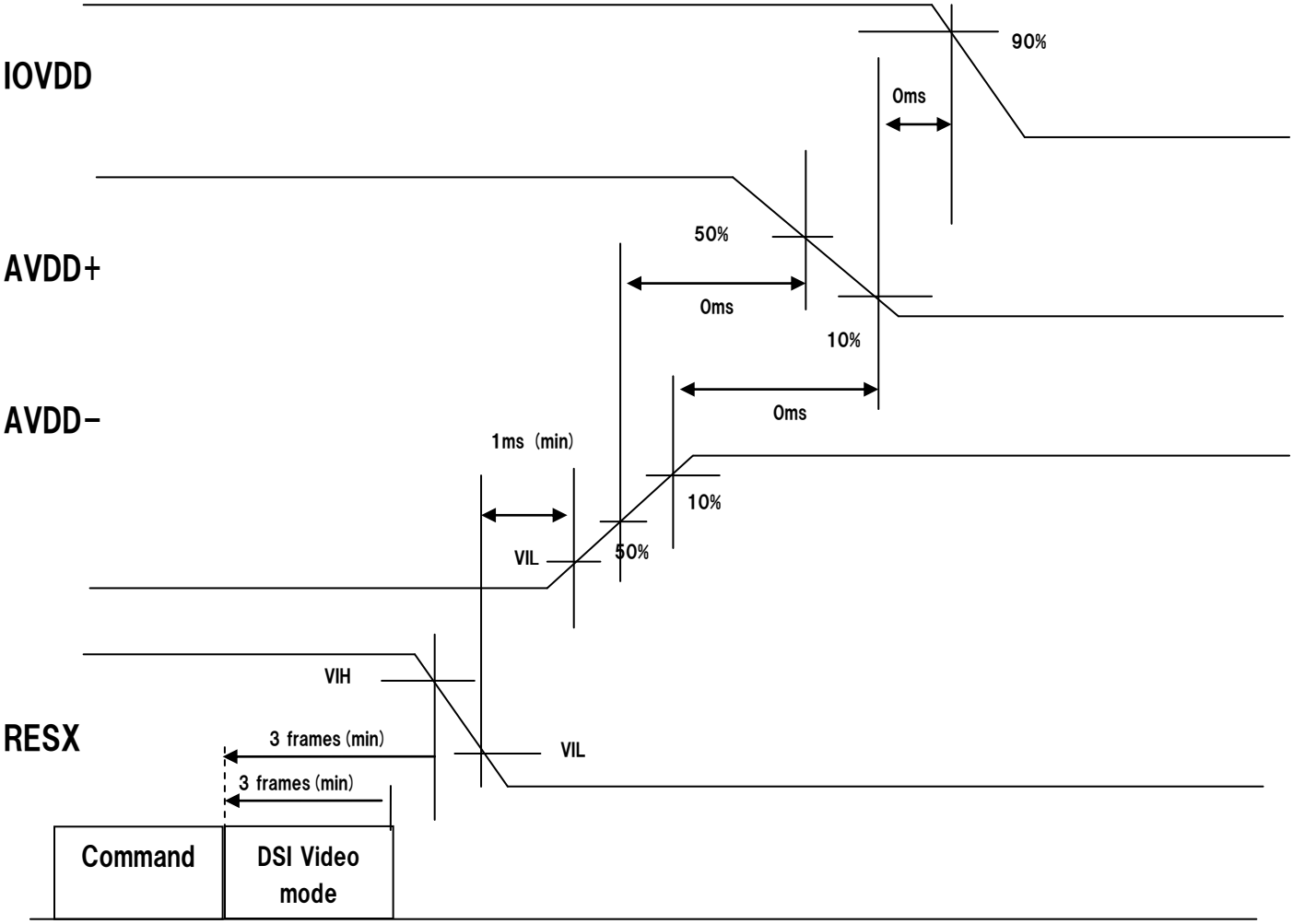


2.5.3 The waveform imaging of power on



Note: If the restriction of above power on sequence will not obeyed, there is possibility that the driver IC may be destroyed

2.5.4 The waveform image of power off sequence



If last command is “Sleep in” command(10h),DSI video mode signal should be kept output more than 3frame length.

Note: If the restriction of above power off sequence will not obeyed, there is possibility that the driver IC may be destroyed

2.6 COMMAND TABLE

Command Table 1

Address [Hex]	Parameter	Instruction	D7	D6	D5	D4	D3	D2	D1	D0
00h		NOP	No Argument							
01h		SOFT_REST	No Argument							
04h	1st Parameter	RDIDIF	ID1[15]	ID1[14]	ID1[13]	ID1[12]	ID1[11]	ID1[10]	ID1[9]	ID1[8]
	2nd Parameter		ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]
	3rd Parameter		ID2[15]	ID2[14]	ID2[13]	ID2[12]	ID2[11]	ID2[10]	ID2[9]	ID2[8]
	4th Parameter		ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]
	5th Parameter		ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]
	6th Parameter		ID4[7]	ID4[6]	ID4[5]	ID4[4]	ID4[3]	ID4[2]	ID4[1]	ID4[0]
	7th Parameter		0	IFID[6]	IFID[5]	IFID[4]	IFID[3]	IFID[2]	IFID[1]	IFID[0]
	8th~15th Parameter		0	0	0	0	0	0	0	0
	16th Parameter		1	1	1	1	1	1	1	1
05h	1st Parameter	RDNUMED	D7	D6	D5	D4	D3	D2	D1	D0
06h	1st Parameter	GET_RED_CHANNEL	R7	R6	R5	R4	R3	R2	R1	R0
07h	1st Parameter	GET_GREEN_CHANNEL	G7	G6	G5	G4	G3	G2	G1	G0
08h	1st Parameter	GET_BLUE_CHANNEL	B7	B6	B5	B4	B3	B2	B1	B0
0Ah	1st Parameter	GET_POWER_MODE	0	0	0	D4	1	D2	0	0
0Bh	1st Parameter	GET_ADDRESS_MODE	D7	D6	0	0	D3	0	0	0
0Ch	1st Parameter	GET_PIXEL_FORMAT	0	D6	D5	D4	0	0	0	0
0Dh	1st Parameter	GET_DISPLAY_MODE	0	0	D5	0	0	D2	D1	D0
0Eh	1st Parameter	GET_SIGNAL_MODE	D7	D6	0	0	0	0	0	D0
0Fh	1st Parameter	RDDSDR	0	D6	0	0	0	0	0	0
10h		ENTER_SLEEP_MODE	No Argument							
11h		EXIT_SLEEP_MODE	No Argument							
26h	1st Parameter	GAMSET	0	D6	0	0	GC3	GC2	GC1	GC0
28h		SET_DISPLAY_OFF	No Argument							
29h		SET_DISPLAY_ON	No Argument							
34h	-	SET_TEAR_OFF	No Argument							
35h	1st Parameter	SET_TEAR_ON	0	0	0	0	0	0	0	M
36h	1st Parameter	SET_ADDRESS_MODE	MY	MX	0	0	RGB	0	0	0
3Ah	1st Parameter	SET_PIXEL_FORMAT	0	VIPF2	VIPF1	VIPF0	0	0	0	0
44h	1st Parameter	SET_TEAR_SCANLINE	0	0	0	0	0	N10	N9	N8
	2nd Parameter		N7	N6	N5	N4	N3	N2	N1	N0
4Fh	1st Parameter	ENTER_DSTB_MODE	0	0	0	0	0	0	0	DSTB
51h	1st Parameter	WRDISBV	0	0	0	0	DBV11	DBV10	DBV9	DBV8
	2nd Parameter	WRDISBV	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

52h	1st Parameter	RDDISBV	0	0	0	0	DBV11	DBV10	DBV9	DBV8
	2nd Parameter	RDDISBV	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
53h	1st Parameter	WRCTRLD	0	0	BCTRL	0	DD	BL	0	0
54h	1st Parameter	RDCTRLD	0	0	BCTRL	0	DD	BL	0	0
55h	1st Parameter	WRPWRSAVE	0	0	0	0	0	0	C1	C0
56h	1st Parameter	RDPWRSAVE	0	0	0	0	0	0	C1	C0
5Eh	1st Parameter	WRPWRSAVE	0	0	0	0	CMB[11]	CMB[10]	CMB[9]	CMB[8]
	2nd Parameter		CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]
5Eh	1st Parameter	RDPWRSAVE	0	0	0	0	CMB[11]	CMB[10]	CMB[9]	CMB[8]
	2nd Parameter		CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]
68h	1st Parameter	RDBCSDR	0	D6	0	0	0	0	0	0
A1h	1st Parameter	RDDB_START	ID1[15]	ID1[14]	ID1[13]	ID1[12]	ID1[11]	ID1[10]	ID1[9]	ID1[8]
	2nd Parameter		ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]
	3rd Parameter		ID2[15]	ID2[14]	ID2[13]	ID2[12]	ID2[11]	ID2[10]	ID2[9]	ID2[8]
	4th Parameter		ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]
	5th Parameter		ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]
	6th Parameter		ID4[7]	ID4[6]	ID4[5]	ID4[4]	ID4[3]	ID4[2]	ID4[1]	ID4[0]
	7th Parameter		0	IFID[6]	IFID[5]	IFID[4]	IFID[3]	IFID[2]	IFID[1]	IFID[0]
	8th~15th Parameter		0	0	0	0	0	0	0	0
	16th Parameter		1	1	1	1	1	1	1	1
A8h	1st Parameter	RDDB_CONTINUE	ID1[15]	ID1[14]	ID1[13]	ID1[12]	ID1[11]	ID1[10]	ID1[9]	ID1[8]
	2nd Parameter		ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]
	3rd Parameter		ID2[15]	ID2[14]	ID2[13]	ID2[12]	ID2[11]	ID2[10]	ID2[9]	ID2[8]
	4th Parameter		ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]
	5th Parameter		ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]
	6th Parameter		ID4[7]	ID4[6]	ID4[5]	ID4[4]	ID4[3]	ID4[2]	ID4[1]	ID4[0]
	7th Parameter		0	IFID[6]	IFID[5]	IFID[4]	IFID[3]	IFID[2]	IFID[1]	IFID[0]
	8th~15th Parameter		0	0	0	0	0	0	0	0
	16th Parameter		1	1	1	1	1	1	1	1
DAh	1st Parameter	RDID1	RDID1 [7]	RDID1 [6]	RDID1 [5]	RDID1 [4]	RDID1 [3]	RDID1 [2]	RDID1 [1]	RDID1 [0]
DBh	1st Parameter	RDID2	RDID2 [7]	RDID2 [6]	RDID2 [5]	RDID2 [4]	RDID2 [3]	RDID2 [2]	RDID2 [1]	RDID2 [0]
DCh	1st Parameter	RDID3	RDID3 [7]	RDID3 [6]	RDID3 [5]	RDID3 [4]	RDID3 [3]	RDID3 [2]	RDID3 [1]	RDID3 [0]

2.7 LED CHRACTERISTICS

Parameter	Symbol	Ratings			Unit	Remark
		Min.	Typ.	Max.		
PWM Frequency Range		0.428		109.803	kHz	109.803kHz/(1+n) n=0~255 set by register
PWM Frequency tolerance		-5		5	%	Full operating temperature range
PWM On Duty cycle		0		100	%	
PWM Duty cycle tolerance		-5		5	%	Full operating temperature range
LED Forward Voltage	Vf		3.0	3.3	V	@ 500nits, LED forward current= 20mA
LED Reverse current				50	uA	@25degC

2.8 MISCELLANEOUS

2.8.1 Audio Noise

Test distance is 1cm

Test position is Center 1 point

Test frequency range is from 1kHz to20kHz

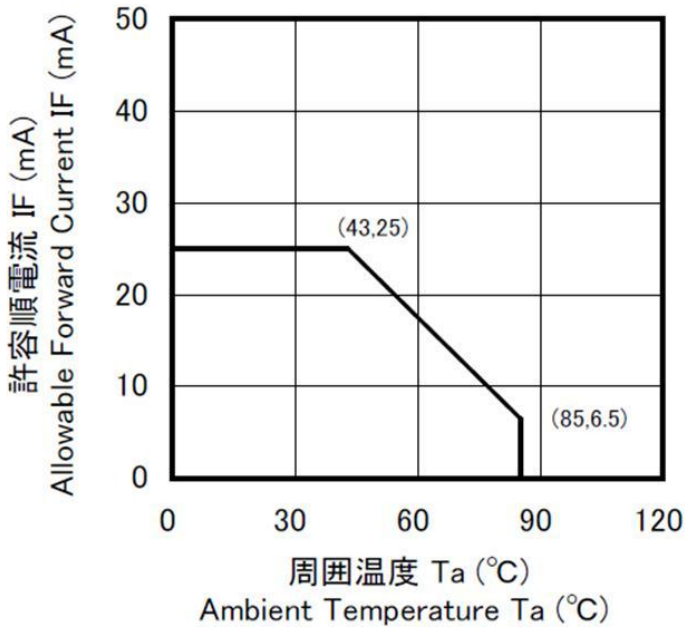
Criteria is less than 10dB

3. ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Ratings	Unit	Remarks
Power supply voltage	AVDD+	-0.3 ~ +6.5	V	
Power supply voltage	AVDD-	+0.3 ~ -6.5	V	
Power supply voltage	IOVDD	-0.3 ~ +4.6	V	
LED forward current	IF	Typ 20, Max 25	mA	Ta=25 ºC
Operating temperature range (environmental)	TOP	-20 to 60	ºC	no condensation
Storage temperature range (environmental)	TST	-30 to 70	ºC	no condensation

1) The rating of maximum LED forward current is decreased along the ambient temperature as the following schema.



Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

4. OPTICAL CHARACTERISTICS

Values in “OPTICAL Specifications“ are provided under the following conditions.

* Frame Rate : 58 (typical)Hz

* IOVDD : 1.8V

* AVDD : +5V -5V Optical characteristics

4.1 OPTICAL CHARACTERISTICS

Item		Symbol	Temp. (°C)	Rating			Unit	Optical System	Definition (Condition)	Remarks
				Min.	Typ.	Max.				
Contrast			25	700	1000		-	1	1 (3)	
Response		tr+tf	25	-	-	35	ms	1	2 (1)	
Color coordinates	R-x	Rx	25	0.61	0.64	0.67	-	1	3 (1)	
	R-y	Ry		0.30	0.33	0.36				
	G-x	Gx		0.27	0.30	0.33				
	G-y	Gy		0.57	0.60	0.63				
	B-x	Bx		0.12	0.15	0.18				
	B-y	By		0.03	0.06	0.09				
	W-x	Wx		0.275	0.310	0.345				
	W-y	Wy		0.285	0.320	0.355				
Brightness		B	25	340	485	-	cd/m^2	1	4 (1)	If = 20mA/chip by 12 LED
Brightness uniformity		δB	25	80	90	-	%	1	4 (2)	
Viewing angle	ϕ=0	-	25	80	-	-	Deg.	2	5 (3)	CR>100:1
	ϕ=90			80	-	-				
	ϕ=180			80	-	-				
	ϕ=270			80	-	-				
NTSC ratio			25	60.8	70.8		%	1	6 (3)	
Gamma			25	-	2.2	-		1	7(1)	
Flicker			25-			-25	dB		(5)	
Cross-talk			25-			5	%	1	8	

4.2 DEFINITIONS AND MEASUREMENT CONDITIONS

4.2.1 Definitions of optical characteristics

Definition 1

Contrast ratio "CR" is defined as:

$$CR = \frac{\text{Brightness at White}}{\text{Brightness at Black}}$$

The contrast ratio should be measured at the center of the nine points (point 5 shown on “Figure A”)

Definition 2

tf: This is a time that increases to 90% of total change of the screen surface brightness from the point of 10%, after data signal is switched from black-raster to white-raster.

tr: This is a time that decreases to 10% of total change of the screen surface brightness from the point of 90%, after data signal is switched from white-raster to black-raster.

Definition 3

This is the x-y coordinate of Red, Green, Blue and White colors specified on the CIE1931 chromaticity diagram.

Definition 4

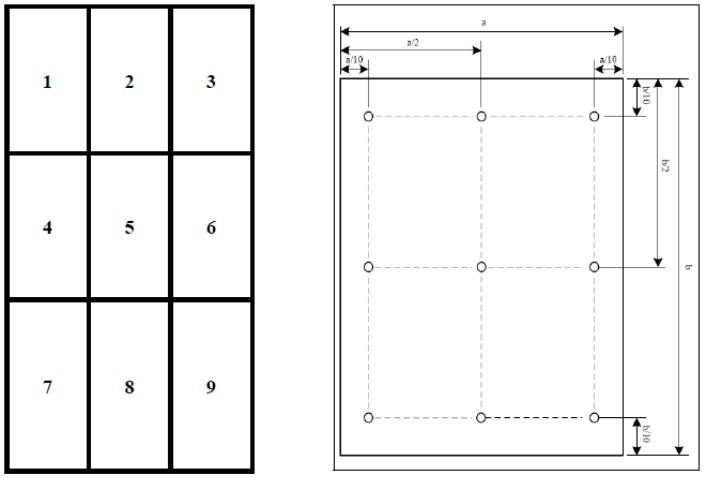


Figure A

< Brightness >

Brightness of each 9 point average value

< Brightness uniformity >

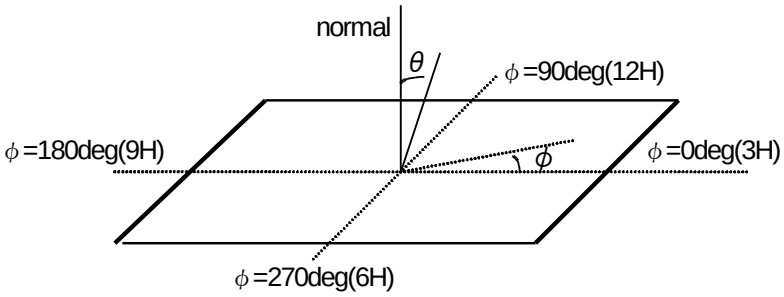
The brightness uniformity "δB" is defined as:

$$SB = \frac{\text{Minimum brightness of the nine points}}{\text{Maximum brightness of the nine points}} \times 100(\%)$$

Definition 5

This is a maximum angle θ from the normal direction that keeps having the contrast more than 10.

The angle on surface ϕ is defined respectively.



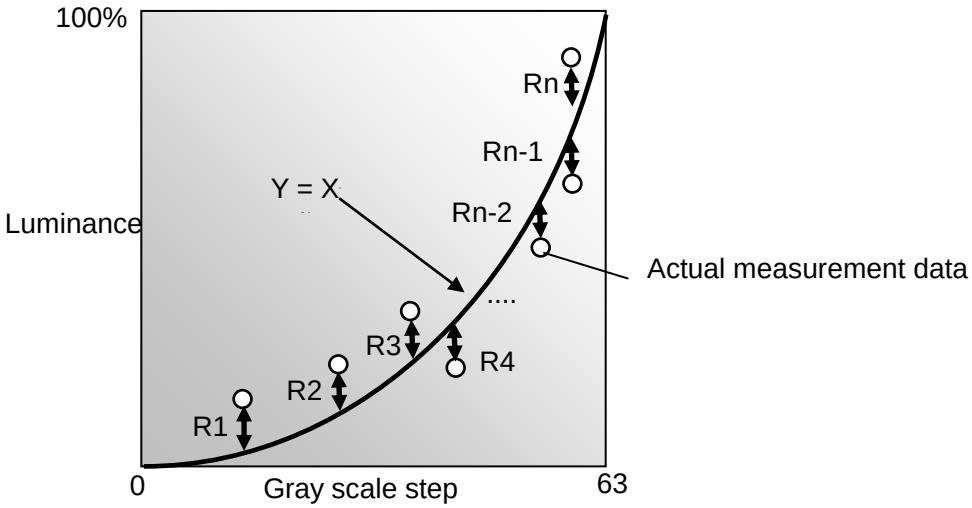
Definition 6

NTSC ratio: The ratio of the color triangle area and NTSC color standards.

(NTSC：National Television Standards Committee)

Definition 7

Gamma: Finding γ0 to meet the curve of theoretical gamma with a method of fitting the quadratic curve which has the least-squares.

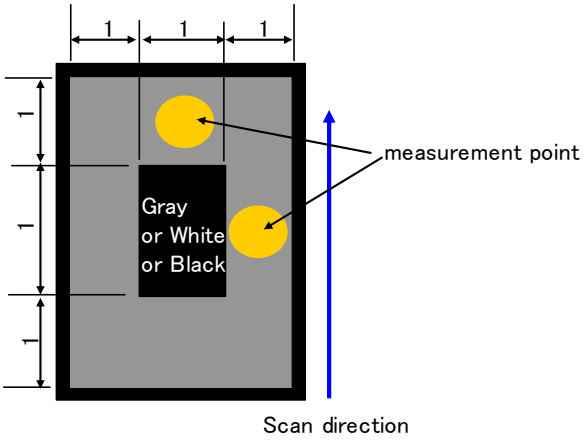


Definition 8

The cross talk(CT) is defined as:

$$CT(Normal\ Black) = \frac{|Y_B(x) - Y_G(x)|}{Y_G(x)}$$

$$CT(Normal\ White) = \frac{|Y_W(x) - Y_G(x)|}{Y_G(x)}$$



4.2.2 Measurement Conditions of Optical Characteristics

[Electrical inputs and adjustments]

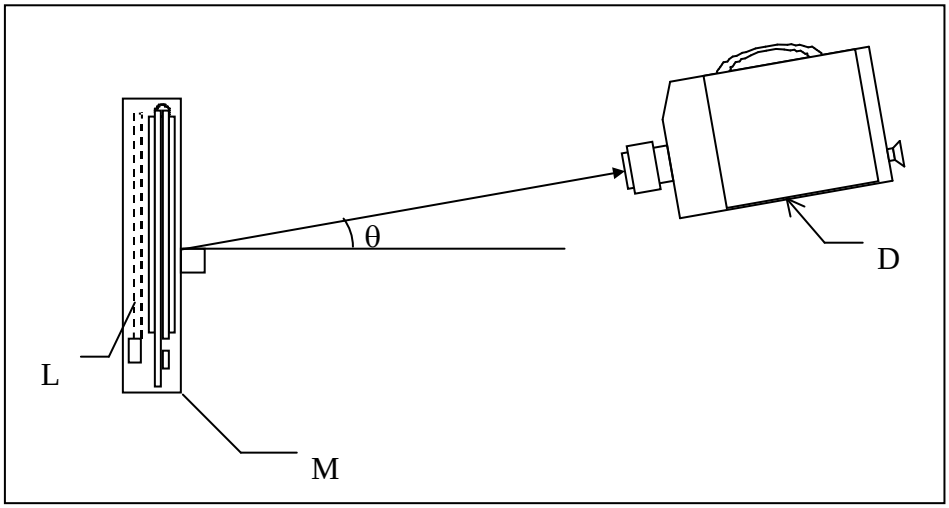
Black raster display R[ ] = G[ ] = B[ ] = 0

White raster display R[ ] = G[ ] = B[ ] = 63

Saturate color raster display R[ ], G[ ], B[ ] (one color only) = 63, otherwise = 0

Color bar display Vertical color bars with pure colors and complementary colors

[Optical system 1]

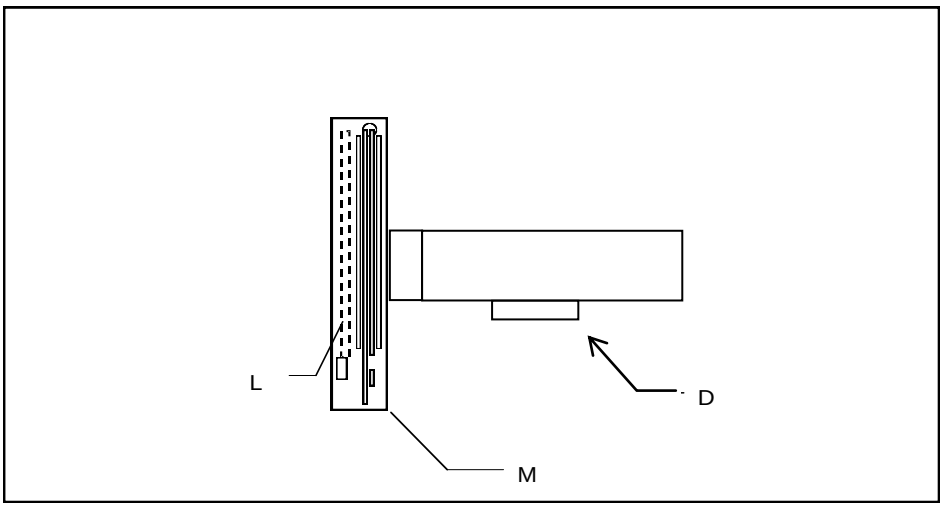


L : Light source mounted to the LCD module (LED Back Light)

M : LCD module

D : Measurement instruments: MCPD7000 (OTSUKA ELECTRONICS) or equivalents

[Optical system 2]



L : Light source mounted to the LCD module (LED Back Light)

M : LCD module

D : Measurement instruments: EZContrast160R (ELDIM) or equivalents

Condition 1

Measurement distance : 400±50mm
Measurement field angle : 1.0 degrees
Measurement point : the center of the active area
Measurement angle θ : 0 degrees

Condition 2

Measurement distance : 400±50mm
Measurement field angle : 1.0 degrees
Measurement point : each 9 points in Figure A
Measurement angle θ : 0 degrees

Condition 3

Measurement distance : 400±50mm
Measurement field angle : 1.0 degrees
Measurement point : the center of the active area

Condition 4

Measurement distance : 400±50mm
Measurement field angle : 1.0 degrees
Measurement point : each points in Figure B (Definition 5)

Condition 5

Measurement pattern : TBD

5. INSPECTION STANDARD

5.1 STANDARDS

The standards are the quality level used to judge whether or not products lots pass during acceptance inspections of products delivered to your company.

The standards are shown below.

* Inspection method: Compliant with ANSI/ ASQC Z1.4-1993, ordinary inspection level II, inspection by one time sampling.

* AQL

Defect type	AQL	Definition
Major defects	0.40%	accompanied with functional abnormalities
Minor defects	0.65%	out of the range of “General Appearance Specifications”, but no functional abnormalities

5.2 LOT

Lot means the unit includes all products delivered to your company at one time.

5.3 INSPECTION CONDITION

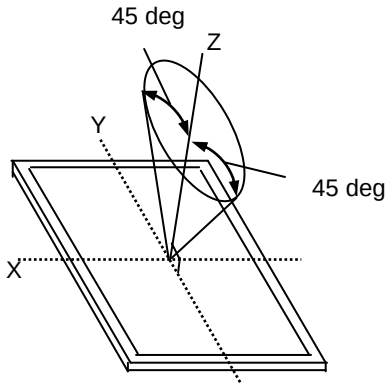
1) Environmental conditions:

1. Temperature/humidity condition: Normal temperature (25 ± 5 ºC)
   Normal humidity (60 ± 20% RH)
2. Luminance environment:
   Not lighted appearance 1000~ 1300 lx
   Lighted appearance: Transmissive type 100~ 400 lx
   Semi-Transmissive 800~ 2000 lx
   *Some specified patterns: 50 lx or the less

2) Inspection method: Inspection by naked eye

Inspect the screen by naked eye from a distance of about 30 cm and the angle shall be 45 degrees from the vertical direction to the product.

Viewing angle is 45 degrees from the vertical direction as shown in the picture below.



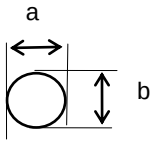
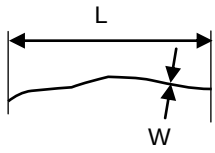
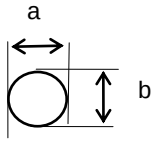
3) Drive condition: It is done pursuant to product specification.

5.4 APPEARANCE STANDARD

5.4.1 Application scope

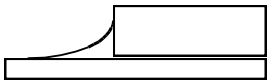
The application scope is limited to the viewing area.
The product should be judged non-defective if all defects are outside of the viewing area and do not interfere with product quality or the assembly process.
If any item is defined with a boundary sample, the boundary sample takes precedence.

5.4.2 Display appearance standard

<table>
<tr><th>6 No</th><th>Items</th><th>Judgment criteria</th><th>Class</th></tr>
<tr><td>1</td><td>Abnormal display</td><td>Must not be abnormal function such as not function or not to get normal pattern for input signal, etc.</td><td>Major</td></tr>
<tr><td>2</td><td>Line defect
(Open, Short)</td><td>No line defect</td><td>Major</td></tr>
<tr><td>3</td><td>Dot defect
(Dot failure)</td><td>bright dot≦2 , dark dot≦4, total dot defect≦6
Single dark dot is not counted
allow 2 horizontal or vertical adjacent dark dots is counted as one dark dot
allow 3 horizontal dark dot is counted as one dark dot
allow 4 horizontal dark dot is counted as one dark dot
Bright dot Limit sample pattern : (R,G,B) = (206,188,230) ; Total : 256 level
Less than bright dot limit pattern is not counted.</td><td>Minor</td></tr>
<tr><td>4</td><td>Dot type defect
d = (a + b) / 2</td><td><table><tr><th>Size d (mm)</th><th>Tolerance</th></tr><tr><td>d<=0.1</td><td>Disregard</td></tr><tr><td>0.1<d<=0.2</td><td>2</td></tr><tr><td>0.2<d<=0.3</td><td>1</td></tr><tr><td>0.3<d</td><td>0</td></tr></table> 
</td><td>Minor</td></tr>
<tr><td>5</td><td>Line type defect
(Black/ White)</td><td><table><tr><th>Width W (mm)</th><th>Length L(mm)</th><th>Tolerance</th></tr><tr><td>W<=0.02</td><td colspan="2">Disregard</td></tr><tr><td>0.02<W<=0.03</td><td>L<=2.0</td><td>2</td></tr><tr><td>0.03<W<=0.05</td><td>L<=2.0</td><td>1</td></tr><tr><td>0.05<W</td><td colspan="2">Dot type Criteria</td></tr></table> 
</td><td>Minor</td></tr>
<tr><td>6</td><td>Unevenness display</td><td>Should not be remarkable.
If necessary, boundary samples should be provided.</td><td>Minor</td></tr>
<tr><td>7</td><td>Bubble in polarizer
d = (a + b) / 2</td><td><table><tr><th>Size d (mm)</th><th>Tolerance</th></tr><tr><td>d<=0.10</td><td>Disregard</td></tr><tr><td>0.10<d<=0.20</td><td>3</td></tr><tr><td>0.20<d<=0.30</td><td>2</td></tr><tr><td>0.30<d<=0.40</td><td>1</td></tr><tr><td>0.40<d</td><td>0</td></tr></table> 
</td><td>Minor</td></tr>
</table>

Total accepted defect number; n=< 4

5.5 GENERAL APPEARANCE SPECIFICATIONS

No	Parameter	Criteria	Class
1	Different specifications	Not permitted.	Major
2	Damaged resist on FPC	Copper patterns on FPC must not be visible.	Minor
3	Circuit pattern	Must not be peeled or separated from FPC.	Major
4	Conductive refuses	No solder refuses or solder balls easily moving. Fixed particle which has no functional affect can be ignored.	Minor
5	Dirt	Should not be prominent. Dirt on backside is permitted.	Minor
6	I/F terminal scratch/ dirt	Should not be prominent.	Minor
7	Plating	Must not be peeled, no rust and no discoloration.	Minor
8	Soldering defect	Solder omissions is not permitted Solder bridges is not permitted.	Major Major Minor
9	Parts soldering	There must be fillet. 	Minor
10	Metal frame scratch/ discoloration	Scratch out of viewing area and discoloration shall be ignored.	Minor

6. WARRANTY

Japan Display Inc. warrants this product from the date of delivery for certain timeframe which will be discussed with the customer and Japan Display. Inc..

We replace or compensate for the defective product which is judged as our responsibility within the term of warranty.

7. RELIABILITY

7.1 TEST CONDITION

No	Parameter	Condition	Ratings	Remark
1	High-temperature storage	70 ºC ± 2 ºC	240 h	
2	High-temperature operation	60 ºC ± 2 ºC	240 h	*1)
3	Low-temperature storage	-30 ºC ± 2 ºC	240 h	*3)
4	Low-temperature operation	-20 ºC ± 2 ºC	240 h	*1)
5	High-temperature, high-humidity storage	60 ºC 90%RH	240 h	*2)
6	High-temperature, high-humidity operation	40 ºC 95%RH	240h	*1) *2)
7	Thermal Shock Test (Non-OP)	-30 ºC ⇔ 70 ºC (30min) (30min)	50 cycles	*2) *3)
8	Low Pressure storage	40,000ft	48 h	-
9	Static Electricity Characteristics (On to panel/Air discharge)		Contact:4kV Air:8kV	

1) Operation test conditions are as follows.
   - IOVDD : 1.8V
   - AVDD+ : 5V
   - AVDD- : -5V
2) Any polarizer's deteriorations are permitted in the case of dew condition.
3) Bubbles of LC material are permitted if mechanical stress is given to the LCD panel at low temperature.

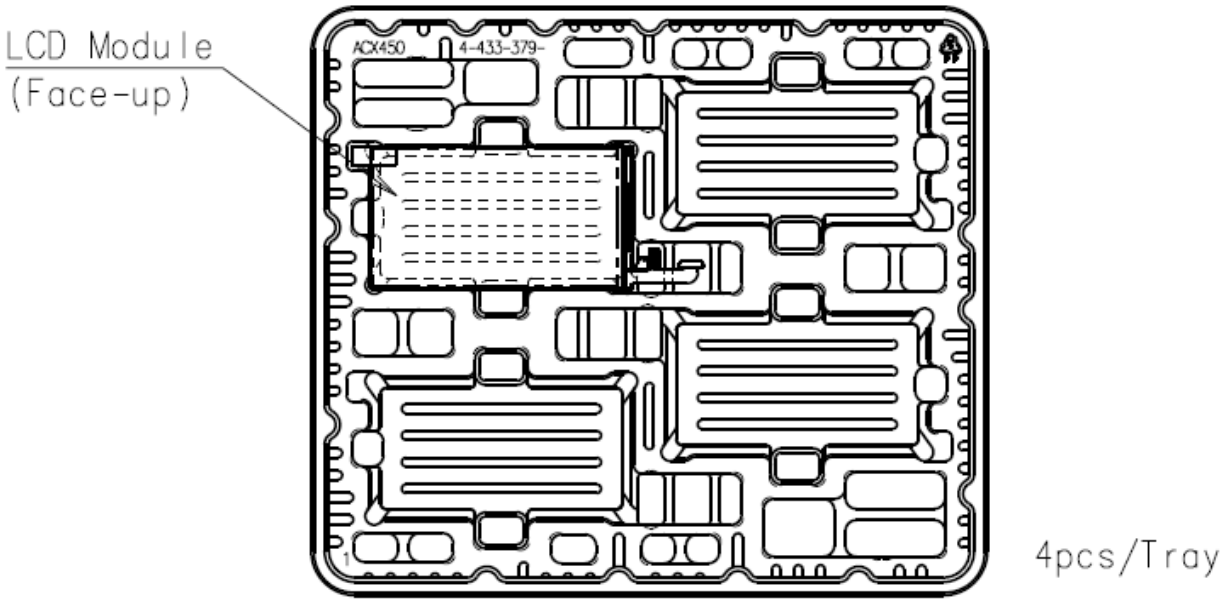
7.2 FALUT JUDGEMENT CRITERIA

After the test, leave the sample under room temperature (25 ºC, 40%RH) for 2 hours elapsed at least.

1) There are not function-related abnormalities.
2) There are not clearly visible defects or deterioration of display quality allowed.
3) Current consumption must not exceed 2 times of initial value.
4) Contrast ratio should be at least 50% of initial value.
5) NTSC ration should be at least 50% of initial value.

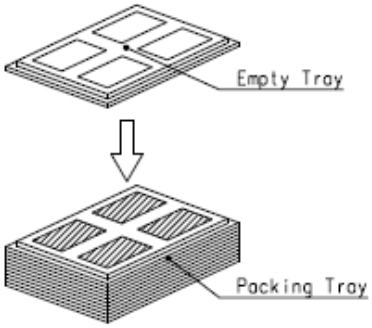
8. PACKING SPECIFICATIONS

8.1 LCM TRAY



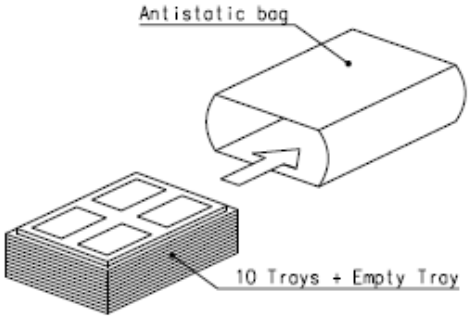
8.2 CARTON

(1)



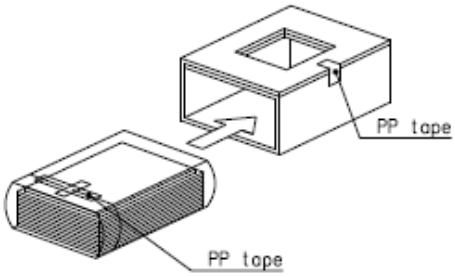
※ 4 pcs each in one tray

(2)

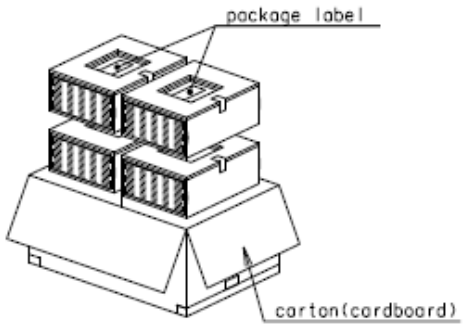


※ 40 pcs each in one inner package

(3)

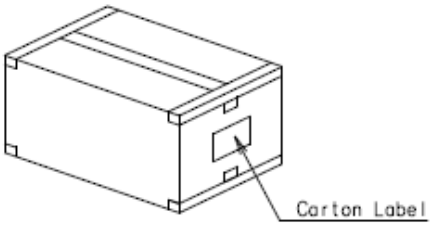


(4)



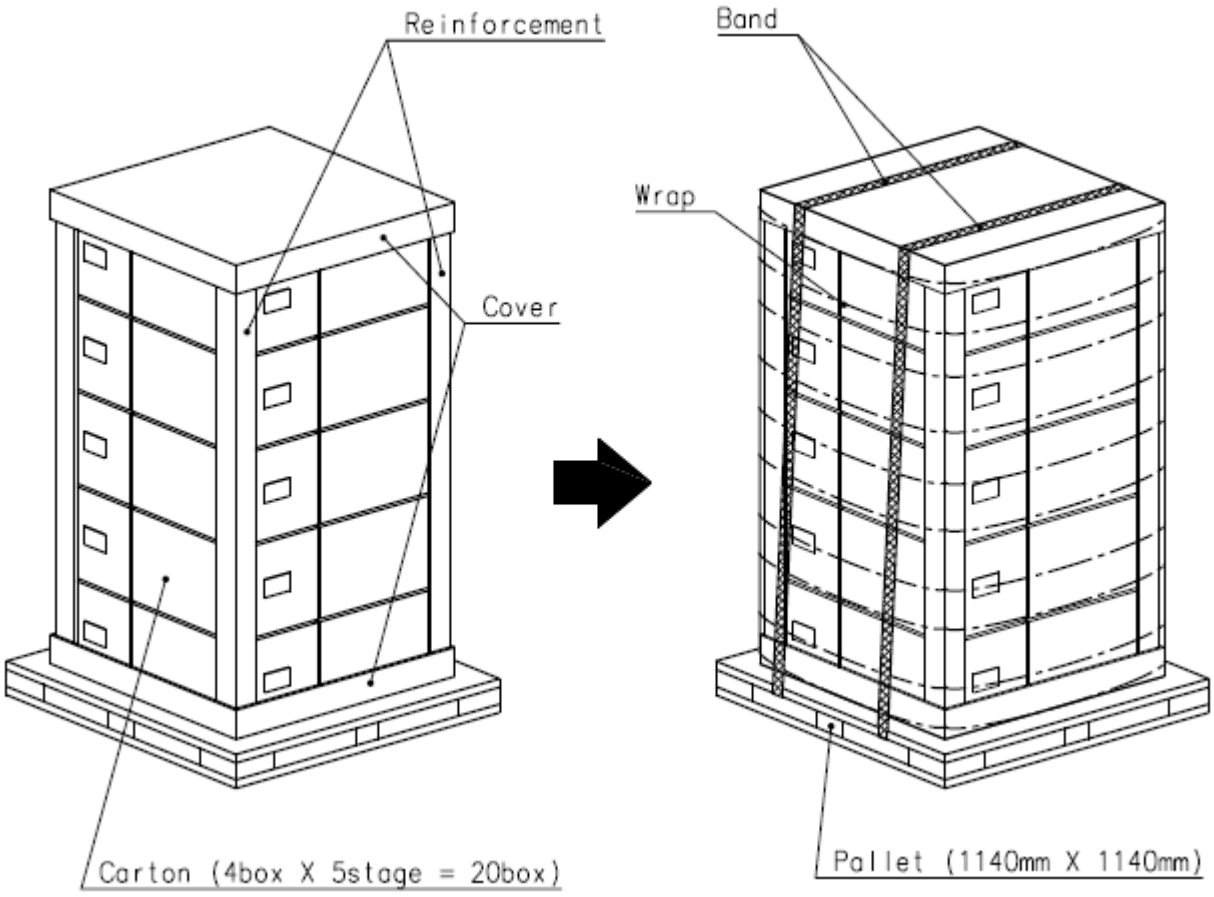
※ 160 pcs each in one carton

(5)



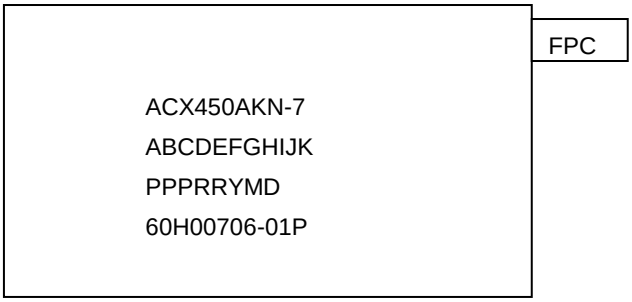
・Place the product on the packing tray.(4pcs / Tray)
・10 stacked tray that contains the product, put an empty tray as a lid on the top.
・Taped to the anti-static bag into 10+1 tray.
・Taped to the sleeve into the anti-static bag put the product.
・Affix the package label to the antistatic bag as shown in the figure.
・Put four sleeve packed in carton as shown in the figure.(160pcs / Carton)
・Seal the carton, affix the carton label to the carton as shown in the figure.

8.3 PALLET



・Place the Lower Cover on the pallet, the carton 20boxes(4box X 5 stage) stacked in it.
・Put a reinforcing structure to the four corners of the carton, cover the Upper Cover.
・Secured by band(2 pieces) ,after wrapped around the Wrap.

8.4 MODULE ID (module back side)



> ACX450AKN-7 : JDI Product Name 1

> ABCDEFGHIJK : JDI control ID

>

PPPRR:JDI control ID

YMD : Year , Month , Day

Year : the last digit of the year

Month:

Month	1	2	3	4	5	6	7	8	9	10	11	12
code	1	2	3	4	5	6	7	8	9	A	B	C

Day :

Day	Code	Day	Code	Day	Code
1	1	11	B	21	M
2	2	12	C	22	N
3	3	13	D	23	P
4	4	14	E	24	R
5	5	15	F	25	S
6	6	16	G	26	T
7	7	17	H	27	V
8	8	18	J	28	W
9	9	19	K	29	X
10	A	20	L	30	Y
				31	Z

> 60H00706-01P : JDI Product Name 2

9. LCD MODULE USAGE AND PRECAUTION

9.1 DESIGN OF APPLICATION

1) To prevent damage to the module, design applications in consideration of the following.
   - The absolute maximum ratings represent the rated values which the LCD module must not exceed. When modules are used beyond this rating, the operating characteristics may be irreversibly affected.
   - It is recommended that power supply lines [AVDD, IOVDD] include current surge protection (fuses, etc.). Without such protection, foreign material or isolated circuit failures can cause overheating or smoke emission, resulting in injury.
   - When logic circuit power is off, do not apply any signals to the input terminals.
   - Potentially irreversible abnormality may occur with forcible disconnection of LCD module power supply, such as removing the device battery.
   - Employ designs that avoid direct contact with the IC. In the event there is a chance of contact, please contact Japan Display Inc. regarding precautions.
2) To prevent erroneous operation, design applications in consideration of the following:
   - To prevent the occurrence of erroneous operation caused by noise, pay special attention to satisfying specified operating conditions. This includes precautionary measures, like using short signal cables.
   - Note that peripheral devices can cause mutual noise interference with LCD modules. In particular, input devices such as touch panels may emit operational level noise as radiation, even when these devices are not in operation. Provisions for, and evaluation of, performance under actual usage conditions with the system are highly recommended.
   - The driver IC used by the LCD module is easily affected by light exposure because it is mounted as a bare chip on the module. To avoid increased current consumption and accompanied shut-down of power supply, give consideration to taking light-shielding countermeasures, and evaluating performance in the system.
   - Just as with general electronic components, ESD may cause LCD modules to malfunction. ESD countermeasures should be considered around components surrounding the LCD module, especially the driver IC and power IC. When an LCD module is mounted near the outer surface of a product, take extra care that components such as these cannot act as conductive paths for ESD.
   - By command, LCD module operation status and display data is saved, but that data can easily be altered by external noise. Noise should be minimized, or its effect avoided, at the device or system level.
   - As unexpected noise may occur, periodic refresh operations, such as resetting commands or resending display data, are highly recommended as part of the software routine.
   - As display problems can occur when signals are fed to the input/output cable NC terminals, system designs should keep them open.
3) System designs should consider the following:
   - Design applications so that excessive force will not be applied to the surface, perimeter or adjoining areas of LCD modules, as this may cause display panel color tone to vary.
   - Be sure that the LCD module is free from twisting, warping, or distortion as any stress can have great influence on the display quality. Ensure sufficient stiffness of the system's outer case or frame. Also, exercise caution when handling.
   - Use the backlight frame section to set and fix the LCD module position inside the system. Using other components to fix the LCD module position may sever circuits on the FPC.
   - As part of the construction of the LCD module, the FPC board with on-board electronic components is only partly fixed to the case, in consideration of reworking. Potentially, the FPC may curve under the weight of individual

components, and they may protrude beyond the outline of the case. As such, preventive measures should be taken to prevent any electrical contact between the LCD module components and other circuits inside the system.

- The viewing angle of the LCD module and that of the system should match.
- If a display frame or printed frame is provided, place it inside the viewing area and outside the active area for a good appearance.

4) Liquid crystal display elements are temperature dependent. Be sure to use the LCD modules within the specified operating temperature range, as recognition of the display becomes difficult when the LCD module is used outside its range. Also, keep in mind that the supply voltage necessary for clear image display will vary according to temperature.
5) To avoid EMI, preventive measures should be implemented in the system.
6) Note that sudden powering-up sends excessive inrush current to the LCD module, and can affect the entire system.

9.2 ASSEMBLY PRECAUTIONS

1) Static electricity can destroy LCD module elements, so carefully observe the following during assembly:
   - Be sure to ground your body when handling the LCD module.
   - Make sure that solder guns and all other tools required for assembly have been grounded.
   - The use of anti-static mats (0.5kÙ – 1MÙ) on the workbench for grounding is recommended.
   - To reduce occurrence of static electricity, avoid using this product in dry environments, (less than 50%RH).
   - To eliminate static electricity, the use of an ionizer (anti-static air blower) is recommended.
   - A protective film has been attached to the surface of the LCD panel. When peeling off the protective film, do so carefully near an ionizer.
   - To guard against performance degradation of the LCD module caused by destructive forces such as static electricity, etc., avoid direct contact to the terminal electrodes of connectors and FPC circuit pattern when handling.
2) In the inspection process, design and assemble structures that ensure sufficient light-shielding measures for the LCD driver.
3) The LCD Panel surface is protected by a protective film, which must be removed before system installation. Units having been in prolonged storage may have some adhesive residue left on the display panel. In such cases, please remove the contaminant according to the procedure in item 5) under "9.3 Handling Precautions" below.
4) As removing the LCD module's protective film makes the polarizer susceptible to the adhesion of foreign material, do so immediately prior to assembly.
5) Exercise caution when applying adhesive to the LCD module as it is difficult to remove.
6) Do not touch or handle the LCD module directly with bare hands as residue of dirt, oil or water can cause corrosion. Be sure to wear finger stalls or gloves when handling LCD modules. (CAUTION: The following applies to bare panel modules) When holding an LCD module, carefully hold the panel by the edges of the glass plate.
7) Handle LCD modules by their edges. Handling the screen directly can cause display problems or cracks in the panel.
8) When installing the LCD module, don't forcibly bend or stretch the input/output cable. Bending or twisting the FPC section may damage circuit patterns. Applying any excessive stress to the LCD module can damage it.
9) Do not apply pressure to the LSI chip or surrounding mold area as it can cause damage.
10) Do not use sharp, pointy or rigid tools when handing LCD panels. These objects can scratch or nick the glass panel, which can cause it to crack.
11) Perform the LCD module power on/off of the system assembly inspection according to the procedure in the specification document.
12) Do not allow non-atmospheric, specialty gases to contact with the LCD module. Check plastic or rubber materials to be used in the system beforehand as gas they produce can cause functional degradation of internal components like the LCD panel polarizer.
13) Trays are used to package LCD modules for shipment. If LCD modules scratch the tray during shipment, tray material may be left on LCD modules. In such case, it may be necessary to air-clean the LCD modules, but take care not to use excess air pressure or apply air flow in the same area for too long as this can peel off attached tape.

9.3 HANDLING PRECAUTIONS

1) The display panel is made of glass. Do not subject it to mechanical shock such as dropping it from a high position, etc.
2) If the display panel is damaged and internal liquid crystal substance leaks out, be sure not to inhale or consume it. Direct contact with skin should also be avoided. Should contact with the internal liquid crystal substance occur, promptly apply the following responses:
   - Contact with clothing: Remove affected items
   - Contact with skin: Wash off using soap and running water
   - Contact with eyes: Wash out for 15 min. or longer with clean water then consult a physician
   - Ingestion: Induce vomiting with water and consult a physician
3) Take precautions in handling the LCD module because the glass plate has very keen edges. Should it break, take extra care to avoid injury from chips, shards and flying glass.
4) The polarizer covering the display panel surface of the LCD module is soft and can be easily scratched. Handle this polarizer carefully, avoiding contact with sharp, pointy instruments or stiff cloth.
5) If the polarizer surface becomes contaminated, use the following recommended or equivalent adhesive tape for contaminants removal:
   - Scotch-brand mending tape (No. 810)
6) Do not breathe on the display surface or use ethyl alcohol solvent for contaminant removal. This can cause cloudiness in the polarizer surface. Furthermore, do not use the following as they can damage the polarizer:
   - Water
   - Ketones
   - Aromatic solvents
7) Avoid using the LCD module under condensation or high-humidity environments as this may cause polarizer or other functional degradation.
8) After being in a high-humidity or condensation environment, keep the LCD module at room temperature more than 30 minutes before using.
9) Current flow in a condensation or high-humidity environment can cause corrosion of electrodes. Also, take precautions against water getting inside the LCD module as it can cause damage.
10) Liquid crystal freezes when stored below the storage temperature range and such freezing may cause orientation defects or bubbles (black or white) to appear in the LCD panel. Bubbles may also occur if the panel receives an impact in a low-temperature environment.
11) If the LCD module is left operating for a long time with the same display showing, the displayed pattern may leave traces on the screen or the contrast may become inconsistent.
12) As optimal operating voltage of the LCD module depends on the surrounding temperature, operation in a high-temperature environment may cause slight flickering.
13) When reading a label, Barcode reader “SYMBOL LS2208” is recommended.

9.4 DISASSEMBLY AND MODIFICATION

Do not attempt to disassemble or modify the LCD module. The internal construction of the LCD module is susceptible to shock, and foreign material or damage can cause screen loss. Japan Display Inc. . shall not be responsible in the event that a customer attempts to disassemble or modify the LCD module.

9.5 STORAGE

14) When storing LCD modules, avoid the following conditions or environments:
   - Exposure to direct sunlight or fluorescent lighting.
   - High-temperature/high-humidity or very low-temperature (below 0°C) environments.
   - Exposure to water droplets, condensation, etc.

15) Furthermore, keep LCD modules in anti-static bags to prevent static electricity charge ups. Whenever possible, LCD modules should be stored in the same conditions in which they were shipped from Japan Display Inc.. When doing so, ensure there are no water droplets, or condensation.
16) Take precaution to minimize corrosion of electrodes. Corrosion of electrodes is accelerated by moisture, condensation or a current flow in a high-humidity environment.
17) Recommended storage conditions:
    - Storage environment : +15 ºC to 35 ºC, less than 65%RH
    - Duration: up to 2 months after shipping date
18) The shipping cartons must not be stacked up over 1.8m in height.

9.6 DISPOSAL

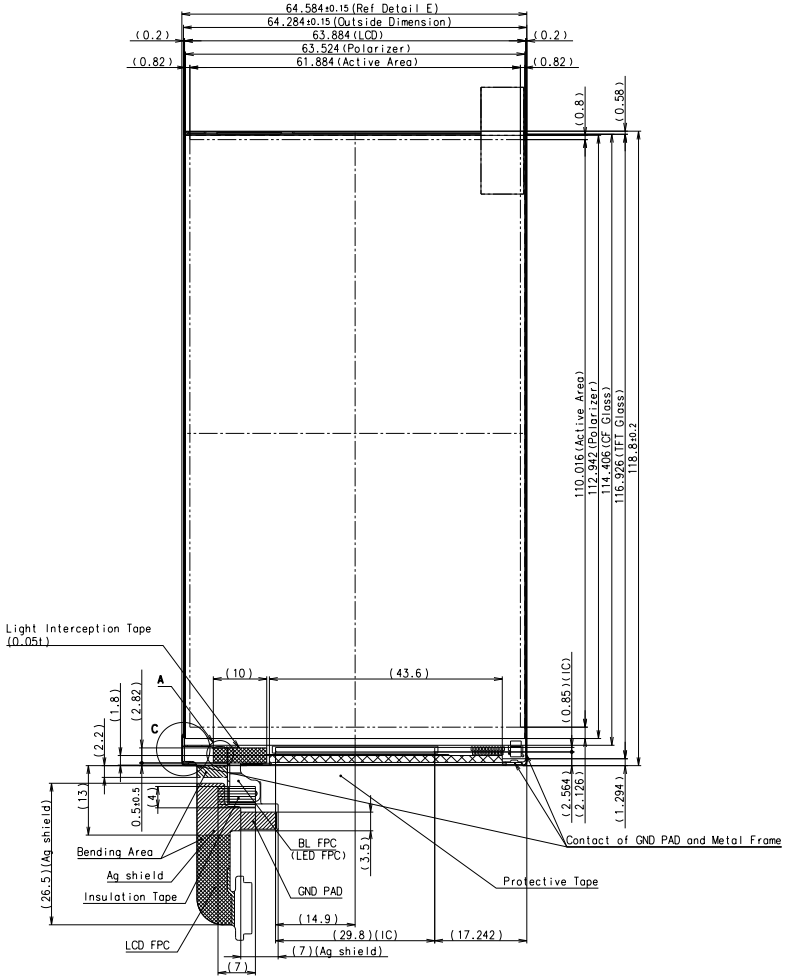
When disposing of LCD modules, consult companies authorized to handle industrial waste treatment. When incineration is the method of LCD module disposal, relevant environmental legislation must be observed.

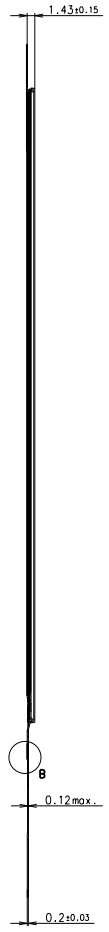
9.7 OTHERS

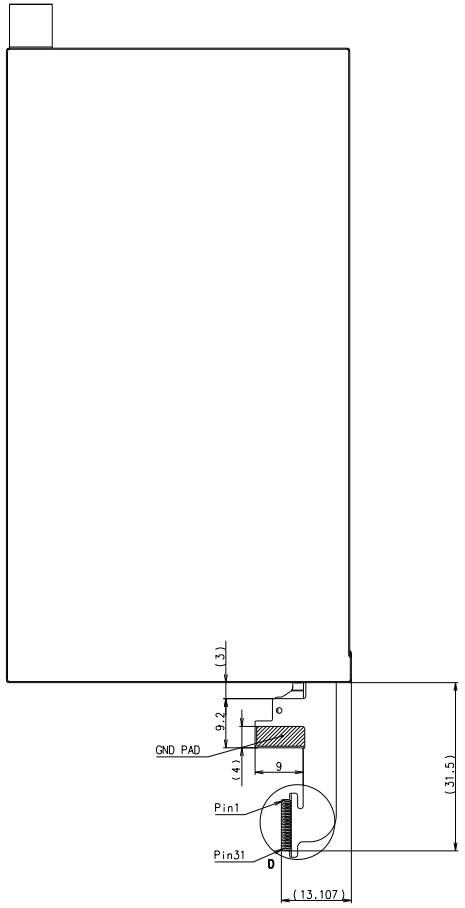
1) This product is designed to be used in general electronic devices (such as office equipment, telecommunications equipment, home electronics, or video game devices). Do not use this product in applications that require an extremely high level of reliability and safety, especially in devices that may cause direct bodily damage to end users (such as equipment for aerospace, traffic control, nuclear, medical, life-support, or safety use).
2) Japan Display Inc.. shall not be responsible for defects that occur in this product or in equipment connected to this product if the product is used in an environment that exceeds the ranges specified in this document, or in an environment not described in this document.
3) Use this product within the scope of conditions and precautions set forth in this document. Even when used according to guidelines ensure sufficient safety at a system and design level to avoid the operation of this product becoming the cause of personal injury, fire or wider damage.

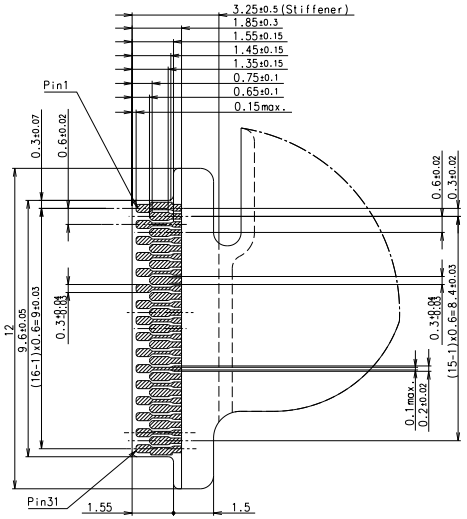
10. CHANGES

When making any changes in manufacturing site, manufacturing methods, manufacturing conditions, specified components, design, dies, molds, or package, the Quality Assurance Division of Japan Display Inc. . will make contact in advance to obtain your approval.
Changes to content described in this document shall be implemented only after mutual agreement between the customer and Japan Display Inc. .



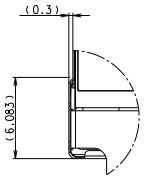




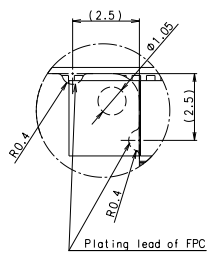


FPC end spec. is for AYF333135(Panasonic).

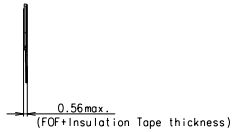
D(10:1)



C(5:1)



A(10:1)



B(5:1)

UNIT: mm / ANGLE	TOLERANCE: ±0.2	USED ON	RANK			
SCALE: 2:1			FAMILY			
MATERIAL(COLOR)		FINISH(COLOR)	ORIGINAL MODEL			
TITLE/DESCRIPTION: ja: LCD Module(5.0" FHD) / en: LCD Module(5.0" FHD)						
DRAWN BY: 12.08.08	PLANNED BY: 12.08.08	CHECKED BY	APPROVED BY	MODEL: ACX450X03	PART NO.	SHEET 1/1
				TENTATIVE PART NO.: ADL450X03-01		

issued 12.08.08

F spec - D12

A1
12.4