SONY

Distribution Restraint	Internal	Outside
	Prohibited	Prohibited

7.96cm 320 × 480 16,777,216 colors HVGA Transflective color LCD Module

ACX567AKM-7

Description

This display is a 7.96cm diagonal active matrix transflective color LCD module based on Low temperature polycrystalline silicon TFT technology. This LCD has 320 × 480 pixels and integrated driver which provides a symmetric module with narrow edge frame. This module includes a LED backlight and a memory integrated one chip driver IC with Low power consumption. The driver IC contains FL3G/SPI and RGB interface circuit, partial memory, CABC function and DC-DC converter.
(Application: Smartphone)

Features

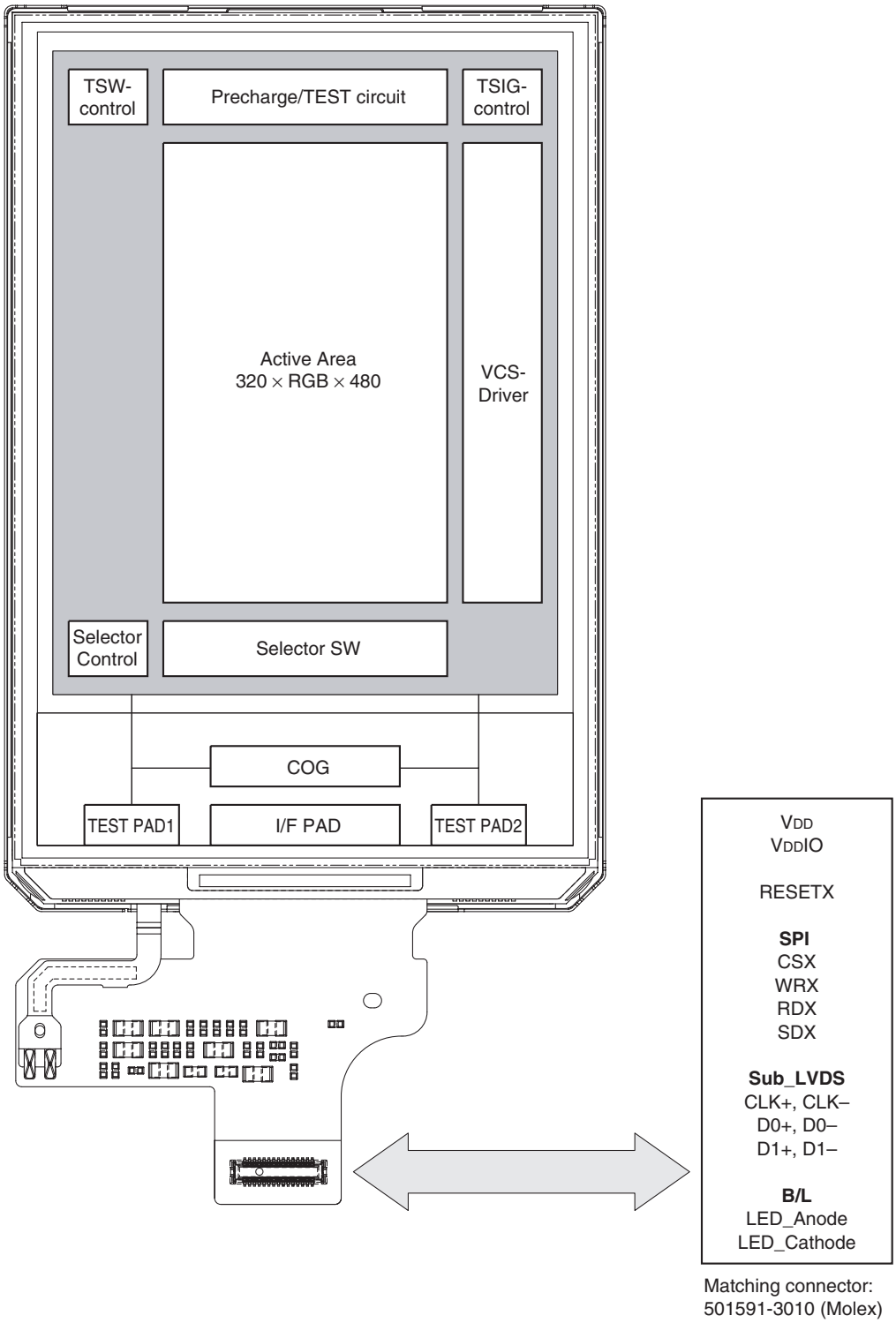
◆ LCD type	: Transflective Symmetric and narrow frame edge module
◆ Dot layout	: RGB stripe
◆ Number of dots	: 320 × RGB × 480 / Portrait type
◆ Dot size	: 0.046mm × 0.138mm (184ppi)
◆ Number of colors	: 16,777,216 (R,G, B each 8bit)
◆ Interface	: 8bit FL3G/SPI or RGB
◆ Partial RAM size	: 320 × 120 × 3bit
◆ Supply voltage	: V_{DD}_18 1.8V ± 5% V_{DD} (V_{BATT}) 3.0V ± 3%
◆ Low power consumption	: 32mW (max.) (Vertical B/W worst image @V_{BATT} = 3.7V) 100μW (max.) (Standby mode)
◆ High reflectivity	: 1.7% (@Diffusion)
◆ High contrast ratio	: 700:1 (typ.) (LED backlight on)
◆ Luminance (LED backlight on)	: 400cd/m^2 (typ.)
◆ Built-in DC-DC converter	
◆ Weight	: 15g

Element Structure

- ◆ Active matrix TFT-LCD panel with built-in peripheral driving circuitry using Low temperature polycrystalline silicon transistors.
- ◆ Driver IC mounted on TFT glass as COG
- ◆ 5 LEDs backlight
- ◆ Hardcoated surface polarizer
- ◆ Number of active dots: 320 (H) × 3 × 480 (V) = 460,800
- ◆ Dimensions
  - ◆ Module dimensions: 49.86mm (W) × 75.19mm (H) × 1.64mm (t)
  - ◆ Thickness: from top polarizer to FPC surface
- ◆ Effective display dimensions (Active area): 44.16mm (H) × 66.24mm (V)

Block Diagram

The panel block diagram is shown below.



Matching connector:
501591-3010 (Molex)

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Rating	Unit
Power supply voltage 1	V_{BATT}	–0.3 to +5.5	V
Power supply voltage 2	V_{DD}_18	–0.3 to +3.0	V
Logic signal input voltage 1 (*1)	V_{I1}	–0.5 to V_{DD}_18 + 0.5	V
Logic signal output voltage (*2)	V_O	–0.5 to V_{DD}_18 + 0.5	V
Operation temperature	Topr	–10 to +60	℃
Storage temperature	Tstr	–30 to +70	℃

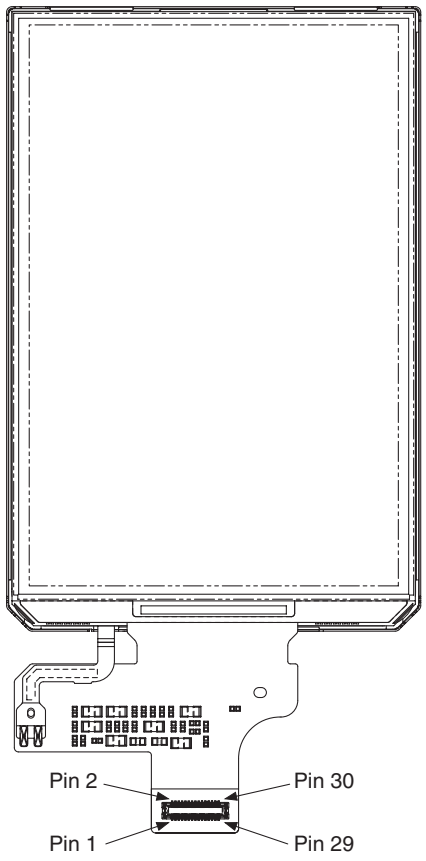
Note) Ta = –30 to +70℃ (no damage at –40 to +85℃)

*1 SPI_CS, SPI_DI, SPI_CLK, RESETX

*2 SPI_DO, PWM_LCD

Pin Location

The pin assignment is described in the next page. The location of Pad is shown below.



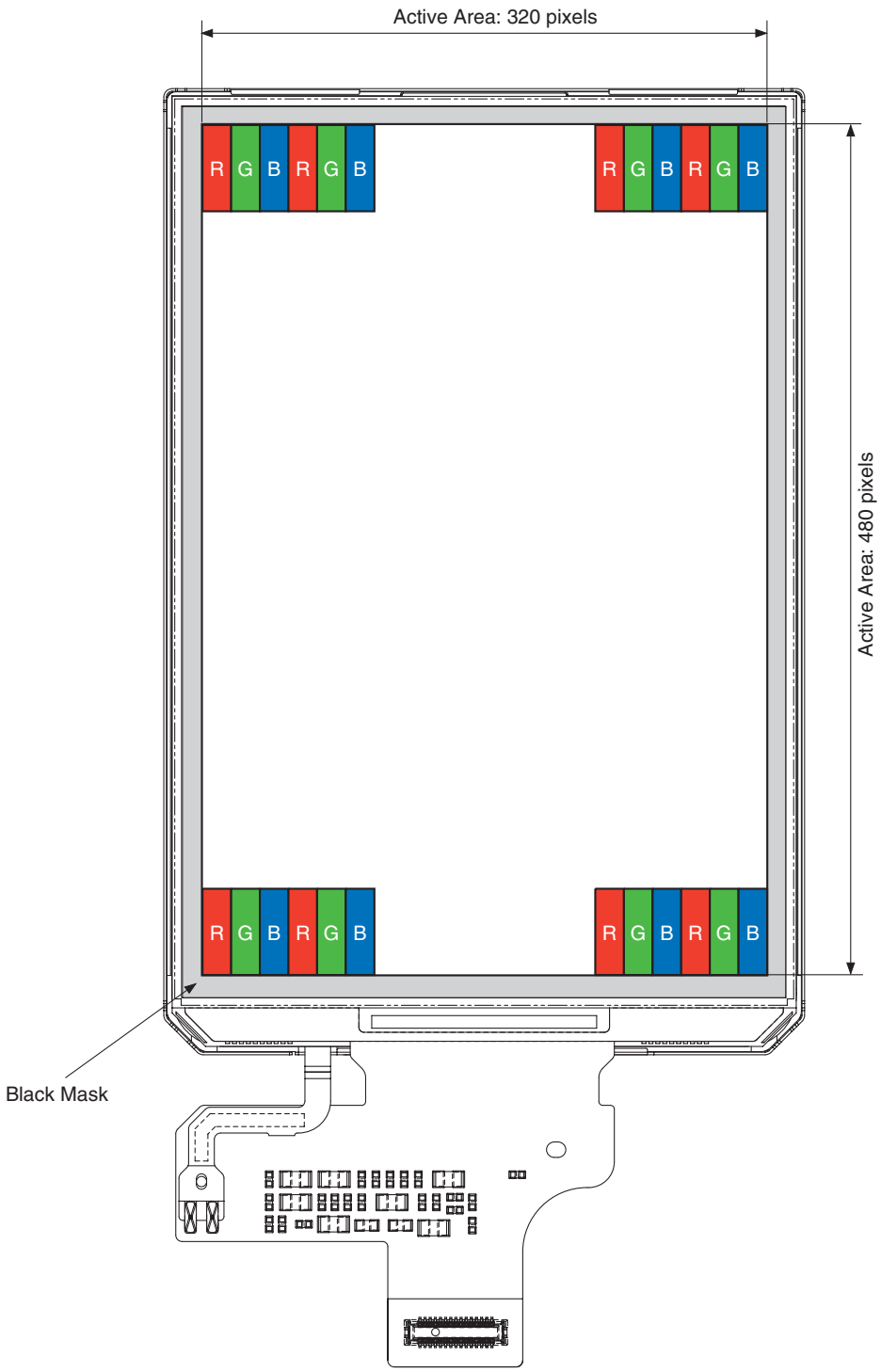
Pin Description

Pin No.	Symbol	I/O	Description
1	N.C.		Non connect. For customer, this pin should be open.
2	BL LED ANODE		Common anode for LED's
3	BL LED CATHODE		Common cathode for LED's
4	SPI_CS	I	Serial interface CHIP SET input
5	PWM_LCD	O	PWM signal output for LCD
6	SPI_DI/DO	I/O	Serial interface DATA input/output
7	N.C.		Non connect. For customer, this pin should be open.
8	GND		Ground
9	N.C.		Non connect. For customer, this pin should be open.
10	GND		Ground
11	GND		Ground
12	FL3G D0–	I	Negative polarity signal of High-speed data channel 0
13	SPI_CLK	I	Serial interface clock input
14	FL3G D0+	I	Positive polarity signal of High-speed data channel 0
15	GND		Ground
16	GND		Ground
17	RESETX	I	Hard reset input. (Active-Low)
18	FL3G CK–	I	Negative polarity signal of High-speed clock channel
19	GND		Ground
20	FL3G CK+	I	Positive polarity signal of High-speed clock channel
21	V_{BATT}	P	Positive power supply 3.0V
22	GND		Ground
23	V_{BATT}	P	Positive power supply 3.0V
24	FL3G D1–	I	Negative polarity signal of High-speed data channel 1
25	V_{DD}_18	P	Positive power supply 1.8V
26	FL3G D1+	I	Positive polarity signal of High-speed data channel 1
27	V_{DD}_18	P	Positive power supply 1.8V
28	GND		Ground
29	NVM		Non connect. For customer, this pin should be open. Using SONY's manufactory only.
30	N.C.		Non connect. For customer, this pin should be open.

Color Table

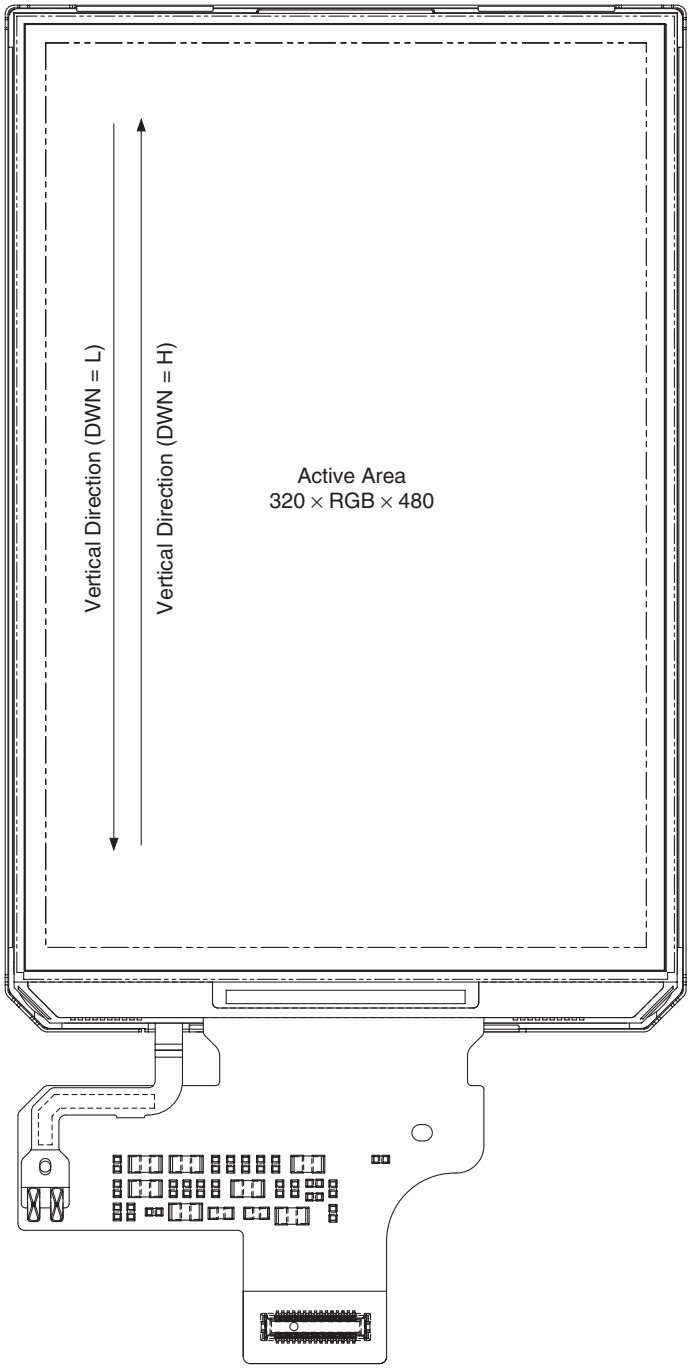
Color & gray scale	Gray scale level	Data signal																							
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Black	—	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Blue	—	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
Green	—	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
Cyan	—	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
Red	—	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Magenta	—	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
Yellow	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
White	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
Black	GS0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
↑	GS1	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Darker	GS2	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
↑	—																								
↓	—																								
Brighter	GS253	H	L	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
↓	GS254	L	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Red	GS255	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Black	GS0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
↑	GS1	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Darker	GS2	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
↑	—																								
↓	—																								
Brighter	GS253	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	L	L	L	L	L	L	L	L
↓	GS254	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
Green	GS255	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
Black	GS0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
↑	GS1	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
Darker	GS2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
↑	—																								
↓	—																								
Brighter	GS253	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H
↓	GS254	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H
Blue	GS255	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H

Color Coding



Scanning Direction

The scanning direction for the vertical period are A as shown below.
This scanning directions is from a front view.



Electrical Characteristics

DC Characteristics

(V_{BATT} = 3.0V ± 3%, V_{DD}_18 = 1.8V ± 5%, Ta = –30 to +70℃ (no damage at –40 to +85℃))

Item	Symbol	Application pins	Condition	Min.	Typ.	Max.	Unit
Power supply voltage 1	V_{BATT}	V_{BATT}		–3%	3.0	3%	V
Power supply voltage 2	V_{DD}_18	V_{DD}_18		–5%	1.80	5%	V
Power supply voltage noise	V_{DD_NOISE}	V_{DD}_18	*1	—	—	100	mVp-p
	V_{BATT_NOISE}	V_{BATT}		—	—	300	mVp-p

*1 This value is not symmetric amplitude which center point is V_{DD}_18. The value of V_{DD}_18 is an average value. See example below. These values are valid up to 100MHz.

(V_{BATT} = 3.0V ± 3%, V_{DD}_18 = 1.8V ± 5%, Ta = –30 to +70℃ (no damage at –40 to +85℃))

Item	Symbol	Application pins	Condition	Min.	Typ.	Max.	Unit
Logic High level input voltage 1	V_{IH1}	SPI_CS, SPI_DI, SPI_CLK, RESETX,		0.7 × V_{DD}_18	—	V_{DD}_18	V
Logic Low level input voltage 1	V_{IL1}			V_{SS}	—	0.3 × V_{DD}_18	V
Logic OUT High level output voltage	V_{DOH}	PWM_LCD	I_{OUT} = –1mA	0.8 × V_{DD}_18	—	V_{DD}_18	V
Logic OUT Low level output voltage	V_{DOL}		I_{OUT} = +1mA	V_{SS}	—	0.2 × V_{DD}_18	V

PWM Outputs

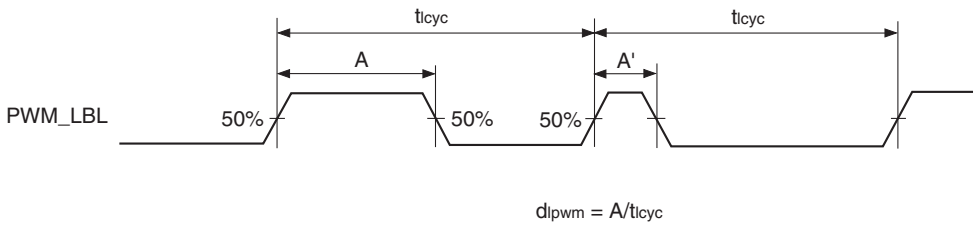
(V_{BATT} = 3.0V ± 3%, V_{DD}_18 = 1.8V ± 5%, Ta = –30 to +70℃ (no damage at –40 to +85℃))

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
				500		Hz
PWM_LBL duty	d_{lpwm}	LBV[7:0] = 00h to FFh No Load Note2	0	—	100	%

Note 1: The PWM frequency for LCD B/L is adjustable by internal 8bits register that is programmed to NVM in Sony's factory.

Note 2: User can adjust PWM Duty for LCD B/L by register (WRLBV / 51h).

PWM Output for LCD



$d_{lpwm} = A/t_{lcyc}$

Input Timing

FlatLink3G Interface

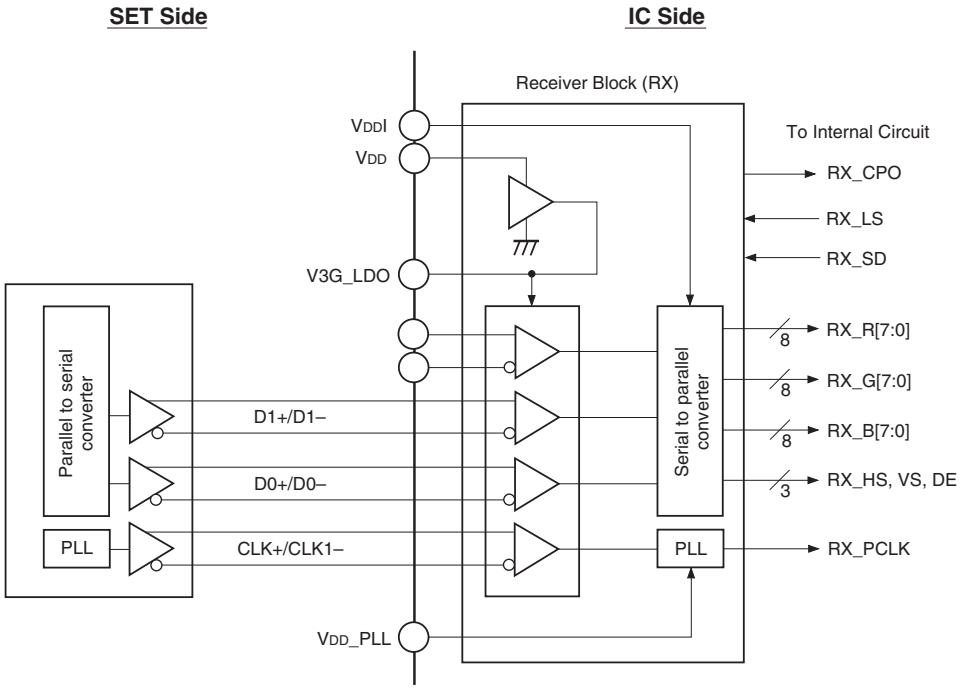
Introduction

The number of data channels between TX and RX is programmable from 1 to 2 depending on bandwidth needed. The data link speed is defined according to pixel clock (PCLK) of RGB I/F and the number of data channels. FlatLink3G has 2 different power modes; shutdown and active. In shutdown mode, FlatLink3G is totally inactive and assumed to consume least power (order of μA). In active mode, FlatLink3G works as a High-speed data link as defined.
TX adds odd parity bit in every data frame and RX checks the pixel data according to the sent parity.

System Block Diagram and Link Protocol

System Block Diagram of FlatLink3G

FlatLink3G consists of three parts; TX, RX and High-speed signaling channels, as shown below.



VDDI is a link power and logic level supply and GND is a ground level of all circuits from a system power supply.
TX_R[7:0], TX_G[7:0], TX_B[7:0], TX_VS, TX_HS, TX_DE and TX_PCLK are RGB I/F parallel CMOS signals provided for TX. PLL of TX provides necessary multiplied clock internally based on TX_PCLK. TX serializes TX_R[7:0], TX_G[7:0], TX_B[7:0], TX_VS, TX_HS and TX_DE into High-speed data channels, D0+/D0–, D1+/D1–, D2+/D2–, based on the multiplied clock. TX transfers TX_PLCK into a High-speed clock channel, CLK+/CLK–, with its original rate. The number of data channels is programmed by TX_LS and RX_LS.
PLL of RX provides necessary multiplied clock internally based on the High-speed clock channel inputs. RX desterilizes the High-speed data channel inputs into RX_R[7:0], RX_G[7:0], RX_B[7:0], RX_VS, RX_HS and RX_DE based on the multiplied clock. TX transfers the High-speed clock channel into RX_PCLK. RX_R[7:0], RX_G[7:0], RX_B[7:0], RX_VS, RX_HS, RX_DE and RX_PCLK construct RGB I/F parallel CMOS signals as output.
RX_XSD are CMOS signals for shutdown of TX and RX.

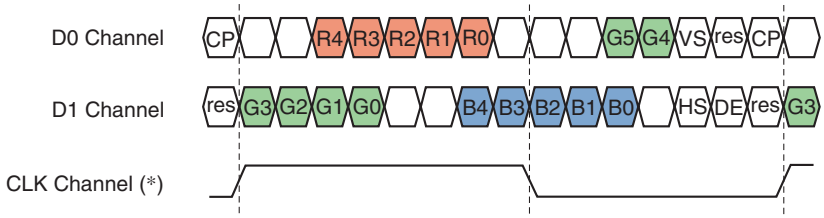
Link Programmability

The number of High-speed data channels is programmed in NVM by CM[2:0].
Table 1 shows the relation among CM, the number of High-speed data channels, the supported RX_PCLK range and the guaranteed data bandwidth per channel.

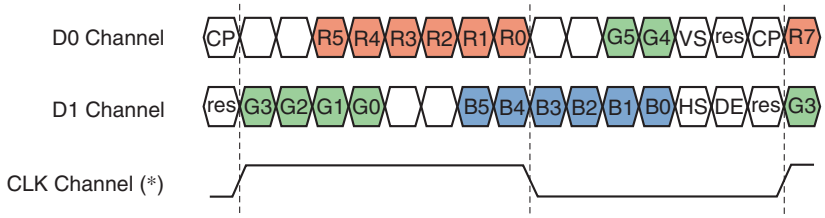
Table 1. Link programmability

CM[2:0]	The number of High-speed data channels	Supported RX_PCLK range [MHz]	Supported guaranteed data bandwidth per channel [Mbits/sec]
(0, 0, 1)	2	8.0 - 30.0	120 - 450

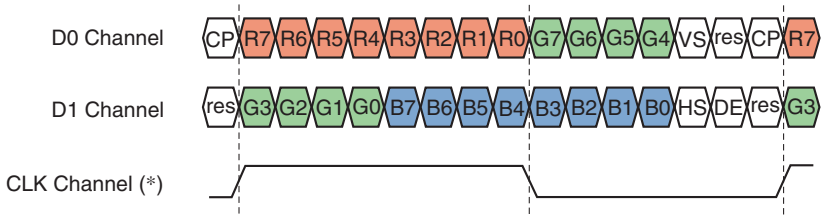
Option 1: The number of High-speed data channels is 2;



Protocol for 2-channel deta (16-bit Mode)



Protocol for 2-channel deta (18-bit Mode)



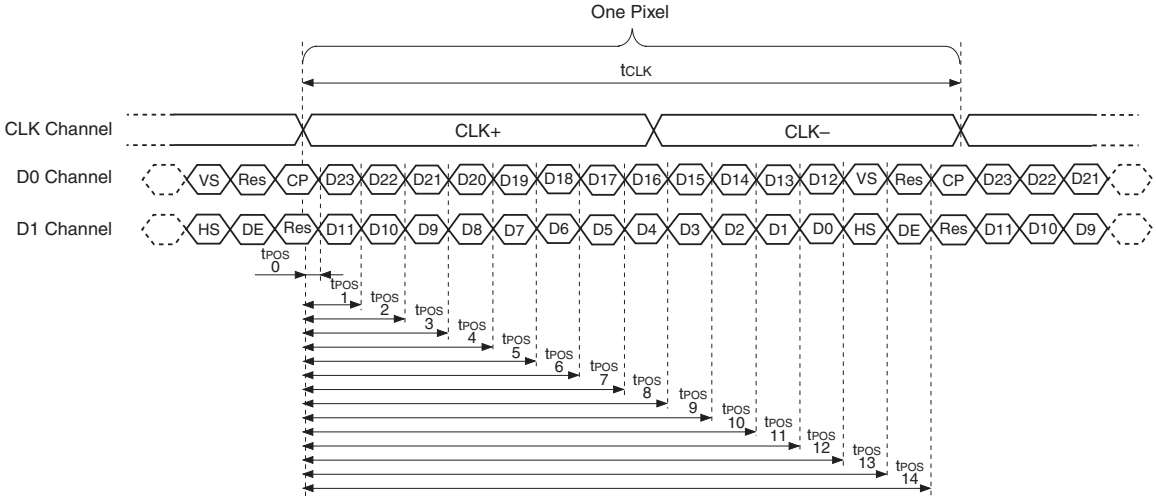
Protocol for 2-channel deta (24-bit Mode)

Two Data Channel Case

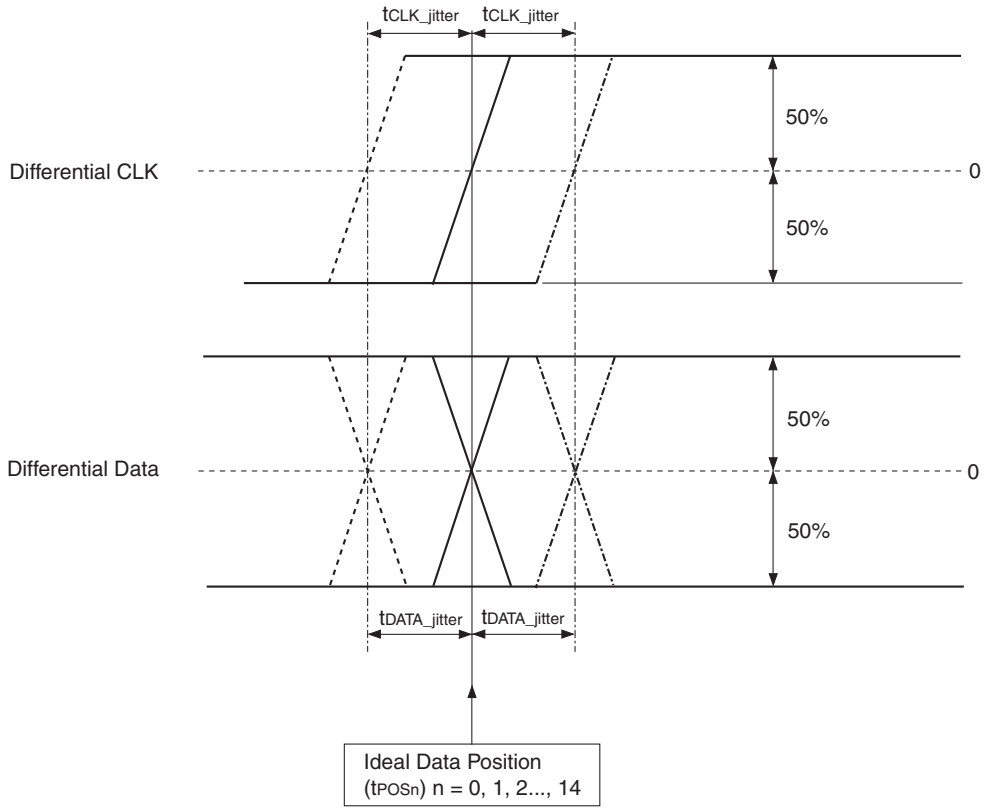
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Pixel clock frequency	P_{CLK}		8.0	—	30.0	MHz
Pixel clock cycle	t_{CLK}	Ideal t_{CLK}	60	—	125	ns
Clock-to-clock position jitter	$t_{CLKjitter}$		0	—	300	ps
Clock-to-data posittion jitter	$t_{DATAjitter}$		0	—	330	ps
Ideal tpos0 position	tpos0	Note 2	0	0	0	ns
Ideal tpos1 position	tpos1	Note 2	(1/15) × t_{CLK}	(1/15) × t_{CLK}	(1/15) × t_{CLK}	ns
Ideal tpos2 position	tpos2	Note 2	(2/15) × t_{CLK}	(2/15) × t_{CLK}	(2/15) × t_{CLK}	ns
Ideal tpos3 position	tpos3	Note 2	(3/15) × t_{CLK}	(3/15) × t_{CLK}	(3/15) × t_{CLK}	ns
Ideal tpos4 position	tpos4	Note 2	(4/15) × t_{CLK}	(4/15) × t_{CLK}	(4/15) × t_{CLK}	ns
Ideal tpos5 position	tpos5	Note 2	(5/15) × t_{CLK}	(5/15) × t_{CLK}	(5/15) × t_{CLK}	ns
Ideal tpos6 position	tpos6	Note 2	(6/15) × t_{CLK}	(6/15) × t_{CLK}	(6/15) × t_{CLK}	ns
Ideal tpos7 position	tpos7	Note 2	(7/15) × t_{CLK}	(7/15) × t_{CLK}	(7/15) × t_{CLK}	ns
Ideal tpos8 position	tpos8	Note 2	(8/15) × t_{CLK}	(8/15) × t_{CLK}	(8/15) × t_{CLK}	ns
Ideal tpos9 position	tpos9	Note 2	(9/15) × t_{CLK}	(9/15) × t_{CLK}	(9/15) × t_{CLK}	ns
Ideal tpos10 position	tpos10	Note 2	(10/15) × t_{CLK}	(10/15) × t_{CLK}	(10/15) × t_{CLK}	ns
Ideal tpos11 position	tpos11	Note 2	(11/15) × t_{CLK}	(11/15) × t_{CLK}	(11/15) × t_{CLK}	ns
Ideal tpos12 position	tpos12	Note 2	(12/15) × t_{CLK}	(12/15) × t_{CLK}	(12/15) × t_{CLK}	ns
Ideal tpos13 position	tpos13	Note 2	(13/15) × t_{CLK}	(13/15) × t_{CLK}	(13/15) × t_{CLK}	ns
Ideal tpos14 position	tpos14	Note 2	(14/15) × t_{CLK}	(14/15) × t_{CLK}	(14/15) × t_{CLK}	ns

Note 1: Ta = –30 to +70°C (to +85°C no damage), V_{DD}I = 1.65 to 1.95V, V_{SS} (DGND) = 0V

Note 2: The reference point is when the CLK channel is changing from logical “0” to logical “1” at the 50% level. This reference point is used to defined ideal t_{POS}n (n = 0, 1, 2, 3, ... ,14) positions.

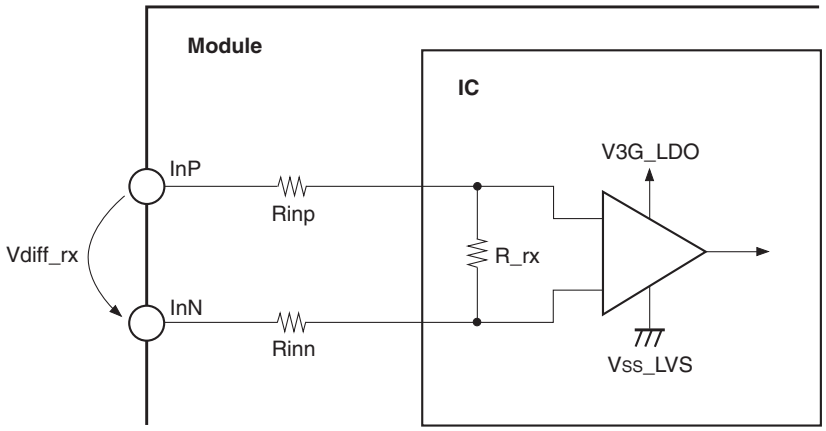


Data Position - Two Data Channel Case



Clock and Data Jitters - Two Data Channel Case

DC Characteristics for FlatLink3G



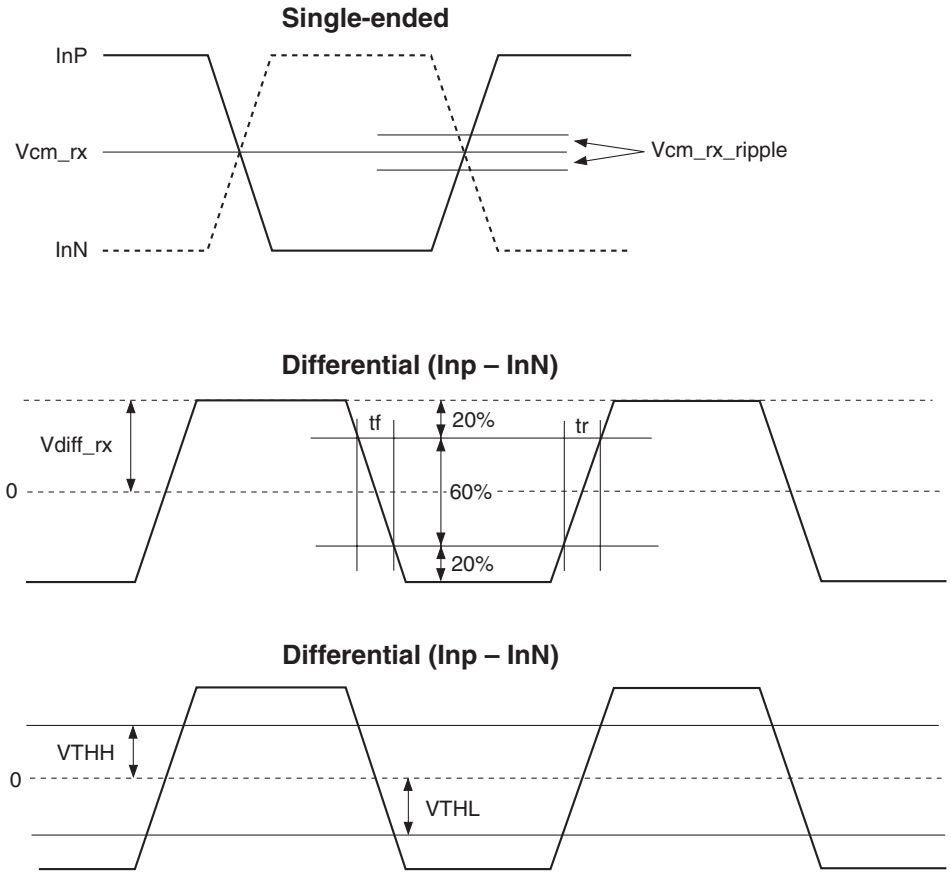
SubLVDS Receiver

SubLVDS Receiver Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input differential voltage range *1	Vdiff_rx		70	—	200	mVp-p
Input Low level threshold voltage *1	VTHL		–40	—	—	mV
Input High level threshold voltage *1	VTHH		—	—	40	mV
Input common mode voltage range *1	Vcm_rx		0.6	0.9	1.2	V
Common mode ripple *1	Vcm_rx_ripple		–75	—	75	mV
Differential termination resistor	R_rx	Rinp: 2 (min), 3 (typ), 7.5 (max) Ω Rinn: 2 (min), 3 (typ), 7.5 (max) Ω	80	100	120	Ω
Self bias resistor	R_self		—	—	500	kΩ
Vdiff_rx rise time (20-80%) *1	tr		—	—	800	ps
Vdiff_rx fall time (20-80%) *1	tf		—	—	800	ps
Operating frequency			—	—	225	MHz
Amplitude mismatch (ΔVdiff _tx/Vdiff_tx) *2			–10	—	10	%
Common mode mismatch (ΔVcm _tx) *3			–0.1	—	0.1	V
Rise time difference *4			–100	—	100	ps
Fall time difference *4			–100	—	100	ps
Input leakage current +/–	IIN+/–		—	—	90	μA
Output leakage current +/–	IOUT+/–	Note	—	—	3.0	μA

Note) This current is what the host can supply when its differential outputs are in Hi-Z state.

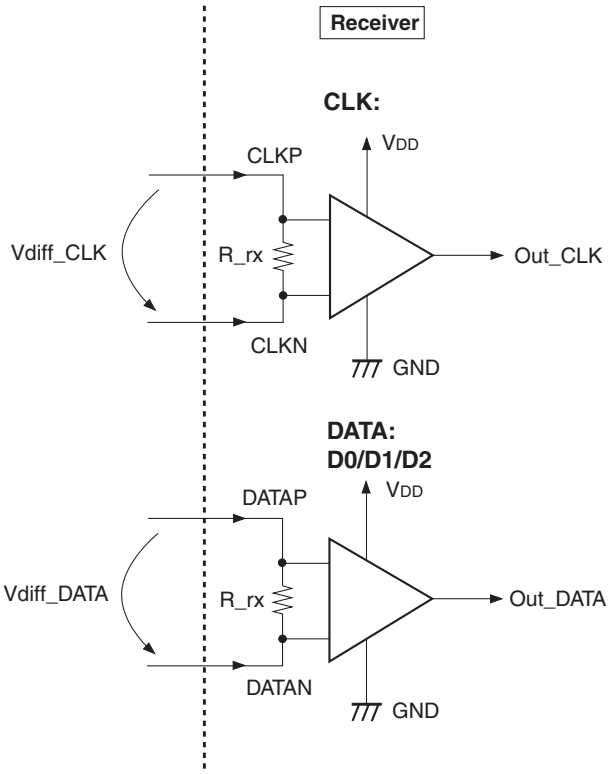
*1



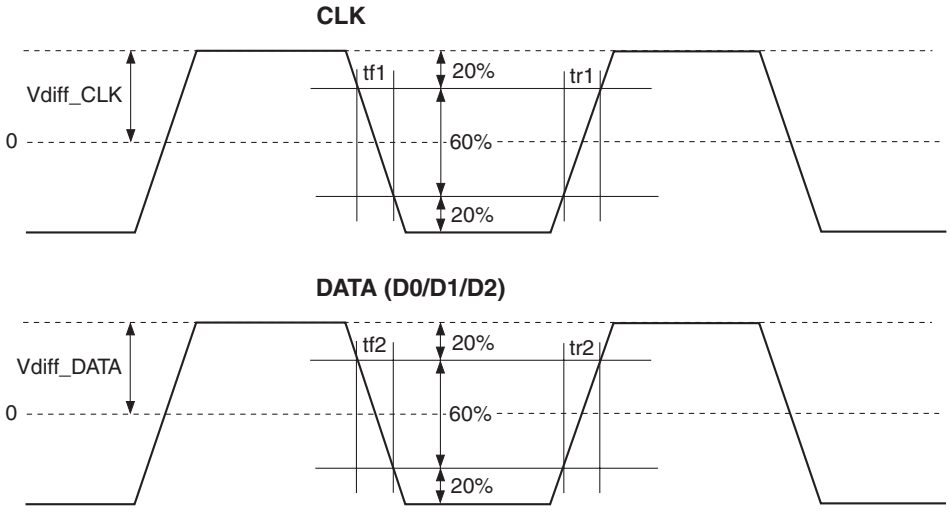
Mismatch is Signal Properties at TX Output Causes Same Mismatches to RX Input

*2 ΔVdiff_tx = Vdiff_CLK – Vdiff_DATA

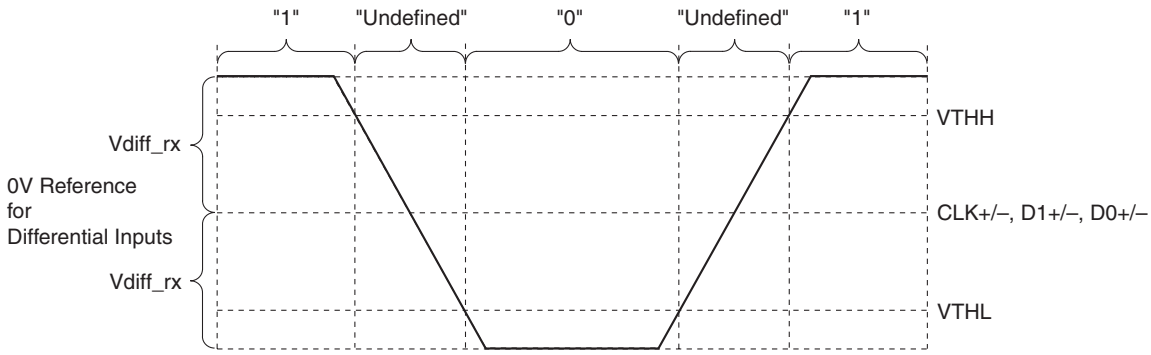
*3 ΔVcm_tx = Vcm_CLK – Vcm_DATA



*4 Rise time difference = tr1 – tr2, Fall time difference = tf1 – tf2

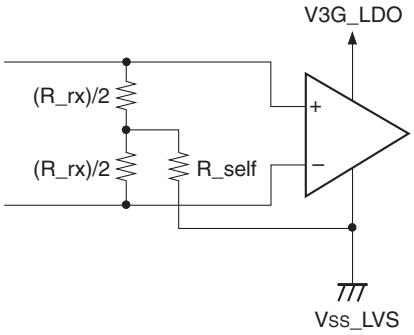


The FlatLink3G receiver is understanding that there is logical “1” when a differential voltage is more than VTHH and the FlatLink3G receiver is understanding that there is logical “0” when a differential voltage is more than VTHH. There is undefined state if the differential voltage is less than VTHH and less than VTHH. A reference figure is below.



Differential Inputs Logical “0”s and “1”s, Threshold High/Low, Differential Voltage Range

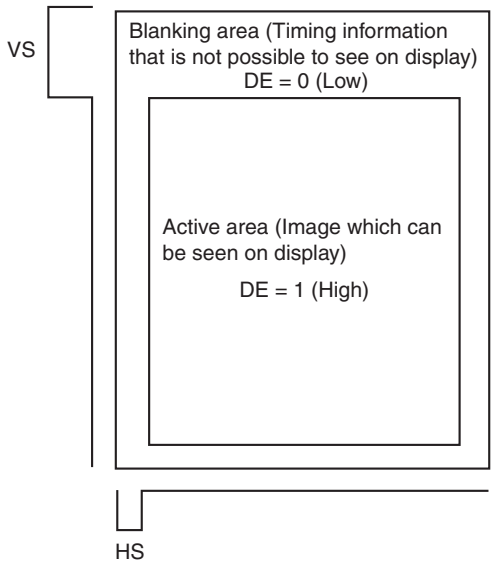
The FlatLink3G transmitter can be driven to Hi-Z on the host side, when the FlatLink3G interface is not used. Therefore, there is implemented pull-down or pull-up resistor(s) (RSELFBIAS) to avoid e.g. unstable situations for differential inputs of the FlatLink3G receiver.
Therefore, those two examples, which are shown below, are only for reference purposes, when there is defined an implementation of the pull-up or pull-down resistor(s) (RSELFBIAS).



Note) 1. R_self is used if a transmitter is not driven Clock (CLK+/–) or Data (D1+/–, D0+/–) channels.
2. R_self can be implemented as pull-up or pull-down.

RGB Interface

General Timing Diagram



Note)

The horizontal and vertical blanking number (also sync widths, front and back poach number) are unsettled value in this system, therefore internal synchronization is operated by only DE pulse, HS and VS are only used reset for H system and V system.

General Timing Diagram

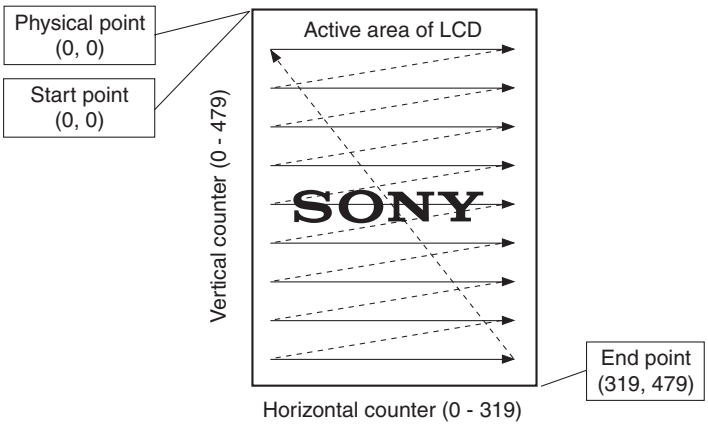
The image information must be correct on the display, when the timings are in range on the interface.

However, the image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range interface timings.

Updating Order on Display Active Area (Normal Display Mode On + Sleep Out)

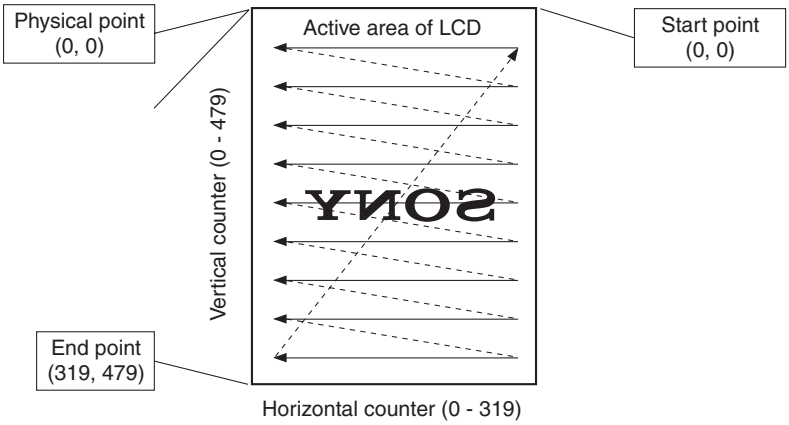
There is defined different kind of updating orders for Display. These updating orders are controlled by bits.

Normal Scan Direction Mode



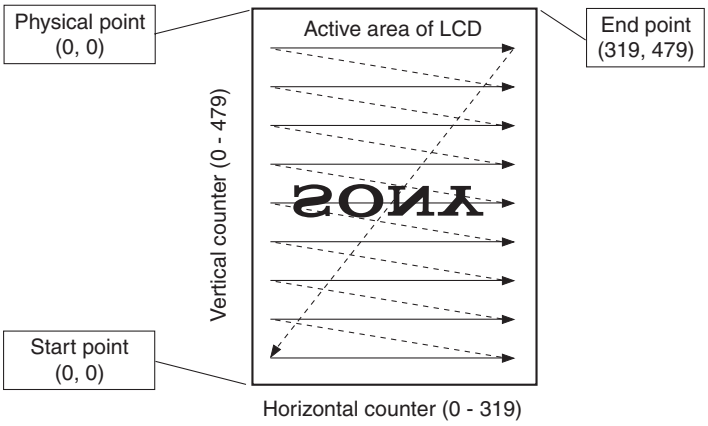
Updating order when MADCTL's B7 = 0 and B6 = 0

Left/Right Inversion Scan Direction Mode



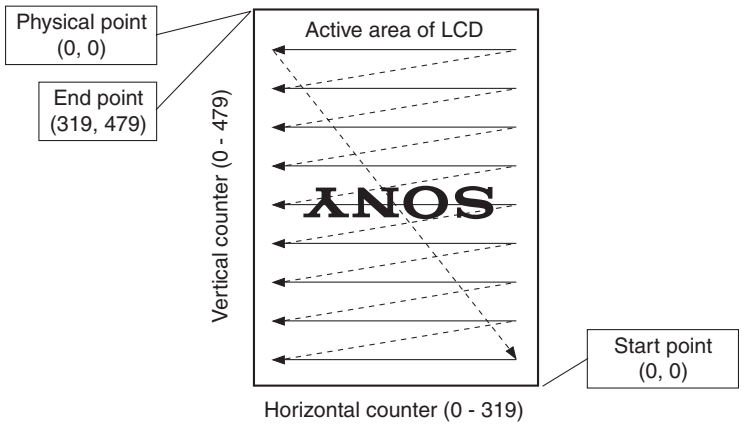
Updating order when MADCTL's B7 = 0 and B6 = 1

Up/Down Inversion Scan Direction Mode



Updating order when MADCTL's B7 = 1 and B6 = 0

Up/Down and Left/Right Inversion Scan Direction Mode



Updating order when MADCTL's B7 = 1 and B6 = 1

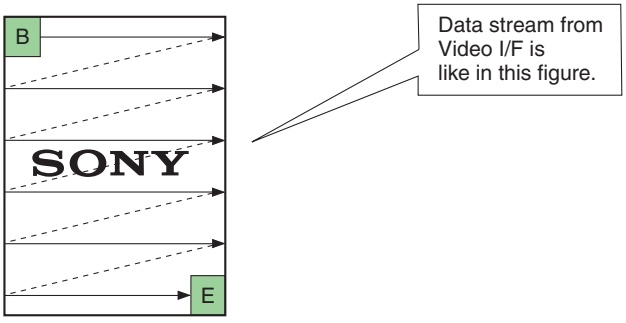
Rules for Updating the Display

Condition	Horizontal counter	Vertical counter
An active VS signal is received	Return to 0	Return to 0
Single pixel information of active area is received	Increment by 1	No change
An active HS signal is received after a falling edge of DE signal	Return to 0	Increment by 1

Rules for Updating Order

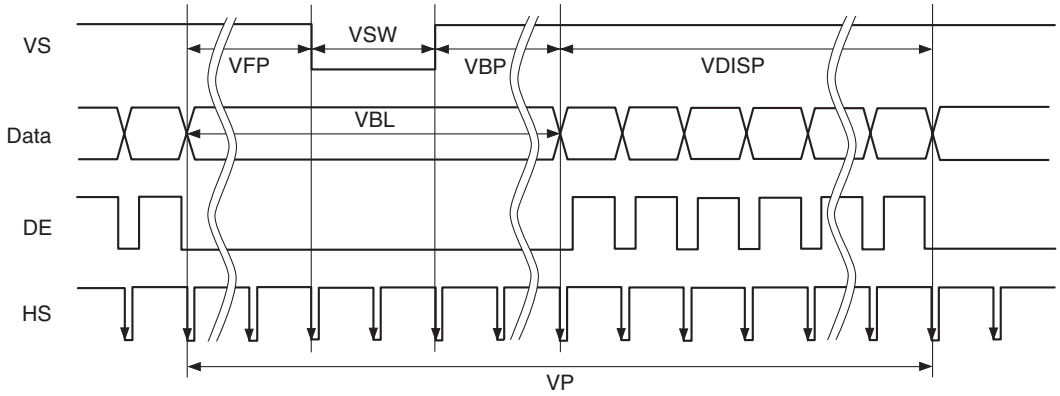
Condition	Horizontal counter	Vertical counter
An active VS signal is received	Return to 0	Return to 0
Single pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than 319 and the vertical counter value is larger than 479 (In case of 320 × 480 mode)	Return to 0	Return to 0

Note) 1. Pixel order is RGB on the display.
2. Data streaming direction from the host to the display is described in the following figure.



Data streaming order from RGB I/F

Vertical Timing of RGB Interface (RGB I/F / FlatLink3G)



Vertical Timing Diagram of RGB Interface (RGB I/F)

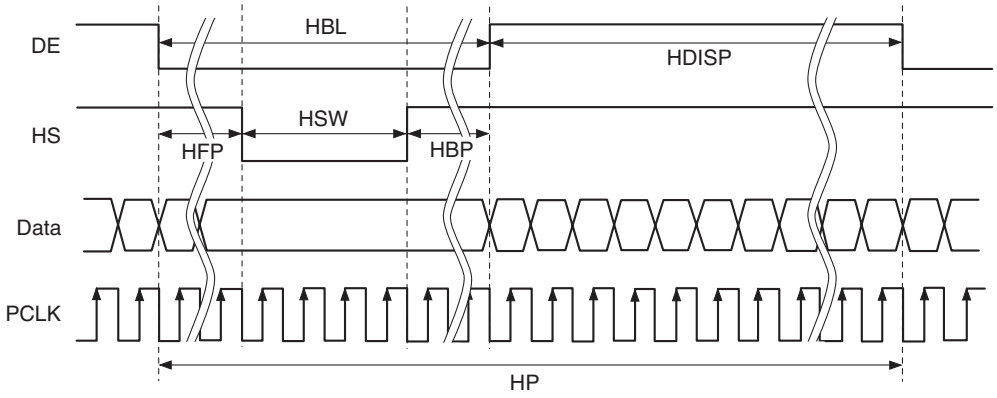
Vertical Timing of RGB Interface (320 × 480 Mode)

(Ta = –30 to +70°C, $V_{DD}I$ = 1.65 to 1.95V, V_{DD} = 2.3 to 4.3V, V_{SS} = 0V)

320 × 480 Mode						
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	Normal Mode	486	488	490	lines
Vertical Low pulse width	VSW	Normal Mode	2	2	4	lines
Vertical front porch	VFP	Normal Mode	2	3	4	lines
Vertical back porch	VBP	Normal Mode	2	3	4	lines
Vertical blanking period	VBL	Normal Mode	6	8	10	lines
Vertical active area	VDSIP	Normal Mode	—	480	—	lines
Vertical frequency		Normal Mode	50	60	65	Hz

Note) 1. Signal rise and fall times are equal or less than 20ns.
2. Measuring of input signals are using 0.30 × $V_{DD}I$ for Low state and 0.70 × $V_{DD}I$ for High state.
3. Data lines can be set to “High” or “Low” during blanking time — Don’t care.

Horizontal Timing of RGB Interface (RGB I/F / FlatLink3G)



Horizontal Timing Diagram of RGB Interface

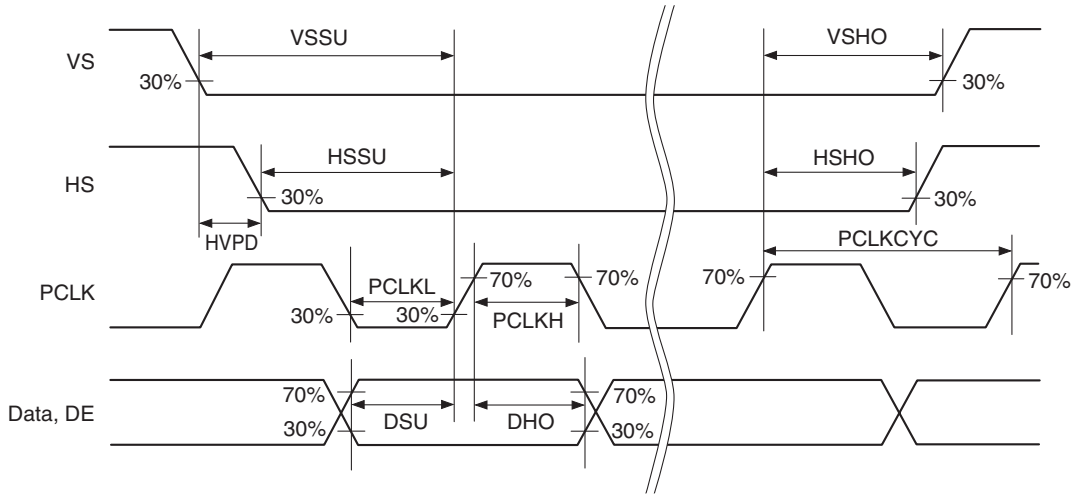
Horizontal Timing of RGB Interface (320 × 480 Mode)

(Ta = –30 to +70°C, $V_{DD}I$ = 1.65 to 1.95V, V_{DD} = 2.3 to 2.9V, V_{SS} = 0V)

320 × 480 Mode						
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Horizontal cycle	HP	Normal Mode	344	352	376	dots
Horizontal Low pulse width	HSW	Normal Mode	2	4	52	dots
Horizontal front porch	HFP	Normal Mode	2	16	52	dots
Horizontal back porch	HBP	Normal Mode	2	12	52	dots
Horizontal blanking period	HBL	Normal Mode	24	32	56	dots
Horizontal active area	HDISP	Normal Mode	—	320	—	dots
Pixel clock frequency	PCLK	Normal Mode	8.36	10.31	11.98	MHz

Note) 1. Signal rise and fall times are equal or less than 20ns.
2. Measuring of input signals are using 0.30 × $V_{DD}I$ for Low state and 0.70 × $V_{DD}I$ for High state.
3. HP is multiples of eight PCLK.
4. Data lines can be set to “High” or “Low” during blanking time — Don’t care.

General Timing Diagram of RGB Interface



General Timing Diagram of RGB Interface

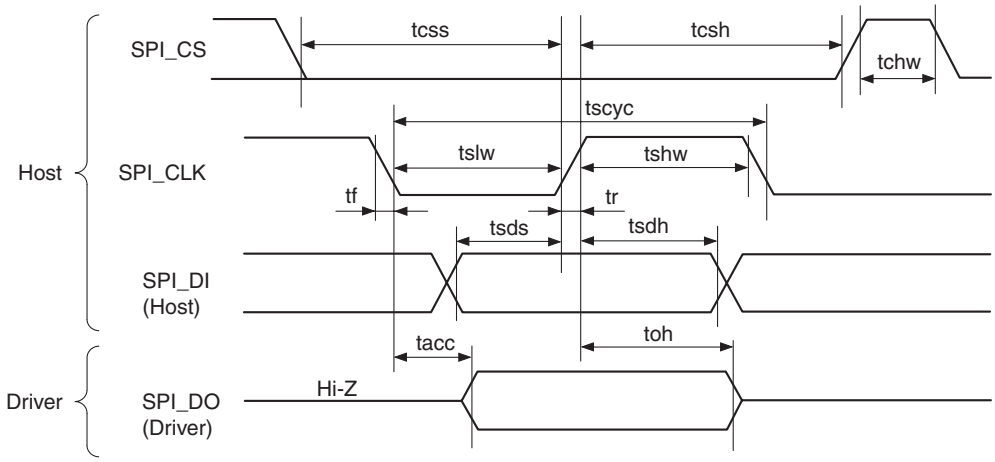
General Timing of RGB Interface

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VS setup time	VSSU		5	—	—	ns
VS hold time	VSHO		5	—	—	ns
HS setup time	HSSU		5	—	—	ns
HS hold time	HSHO		5	—	—	ns
Phase difference of sync. signal falling edge	HVPD		—	0	—	ns
Pixel clock Low time	PCLKL		15	—	—	ns
Pixel clock High time	PCLKH		15	—	—	ns
Data setup time	DSU		5	—	—	ns
Data hold time	DHO		5	—	—	ns

Note) 1. Signal rise and fall times are equal or less than 20ns.
2. Measuring of input signals are using 0.30 × V_{DD}I for low state and 0.70 × V_{DD}I for High state.

Serial Interface

Timing of Serial Interface



Timing Diagram of Serial Interface

Timing of Serial Interface

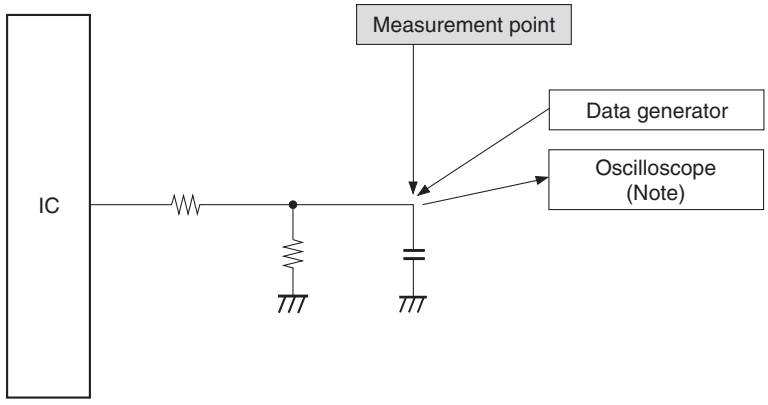
(Ta = –30 to +70°C, $V_{DD}I$ = 1.65 to 1.95V, V_{DD} = 2.3 to 2.9V, V_{SS} = 0V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Write mode	Serial clock cycle	tscyc	SPI_CLK	100	—	—	ns
	SCL High pulse width	tshw	SPI_CLK	35	—	—	ns
	SCL Low pulse width	tslw	SPI_CLK	30	—	—	ns
	Data setup time (write)	tsds	SPI_DI	20	—	—	ns
	Data hold time	tsdh	SPI_DI	20	—	—	ns
Read mode	Serial clock cycle	tscyc	SPI_CLK	150	—	—	ns
	SCL High pulse width	tshw	SPI_CLK	60	—	—	ns
	SCL Low pulse width	tslw	SPI_CLK	60	—	—	ns
	Access time (Note 1)	tacc	SPI_DO	10	—	50	ns
	Output disable time (Note 1)	toh	SPI_DO	15	—	50	ns
XSC High pulse width		tchw	SPI_CS	40	—	—	ns
XSC - SCL time		tcss	SPI_CS	30	—	—	ns
		tcsh	SPI_CS	35	—	—	ns

Note) 1. The output signal's rise and fall times are to be stipulated maximum 15ns.
2. The input signal's rise and fall times are equal or less than 15ns.
3. Logic High and Low levels of input signals are specified as 0.3 × $V_{DD}I$ for Low state and 0.7 × $V_{DD}I$ for High state.
4. SPI_CLK can be High or Low during off state.

t_{ACC} and t_{OH} Measurement Condition for Serial Interface

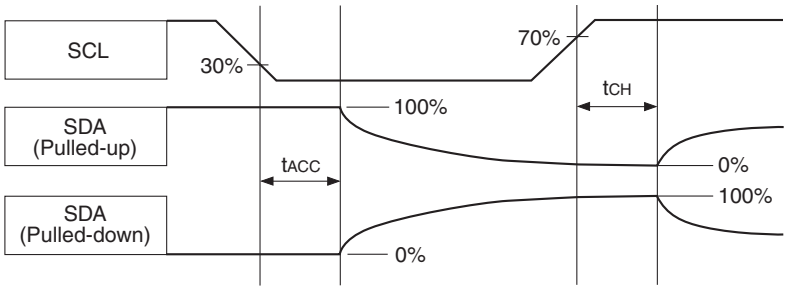
Measurement Condition and Setup



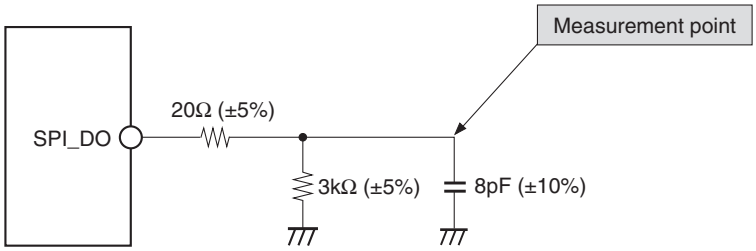
Measurement Condition and Setup

Note) Capacitances and resistances of the oscilloscope's probe must be included in external components in these measurements.

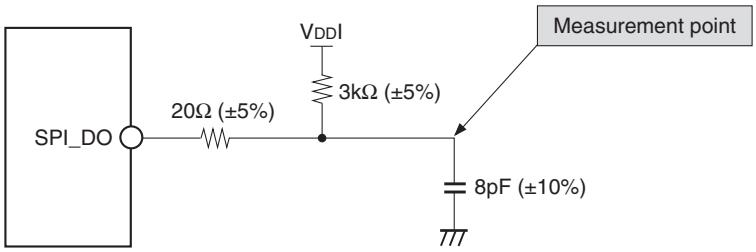
Minimum Measurement



Minimum Measurement Timing

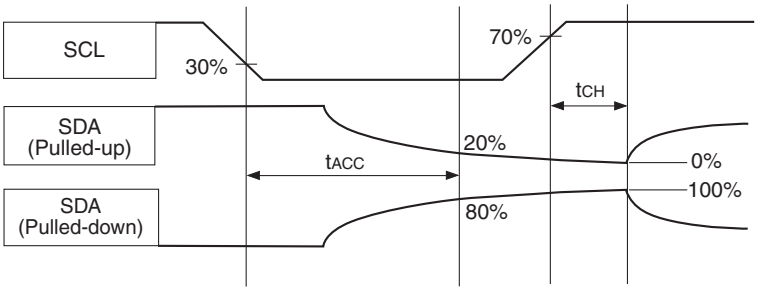


Measurement Circuit (Pull-down Resistor)

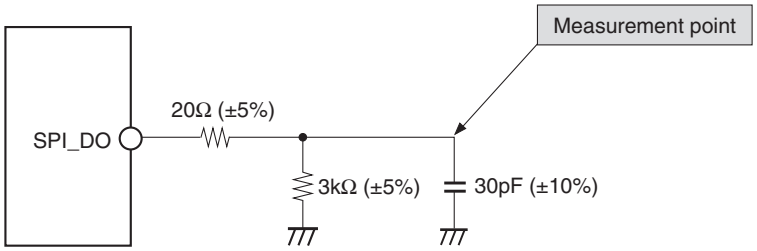


Measurement Circuit (Pull-up Resistor)

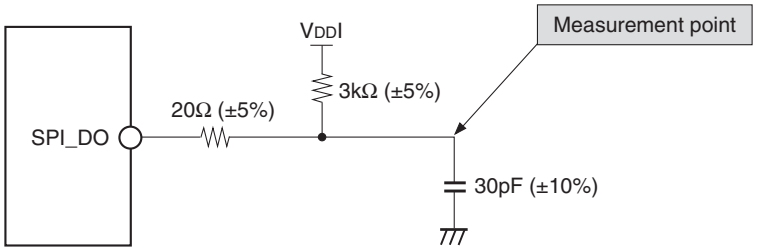
Maximum Measurement



Maximum Measurement Timing



Measurement Circuit (Pull-down Resistor)



Measurement Circuit (Pull-up Resistor)

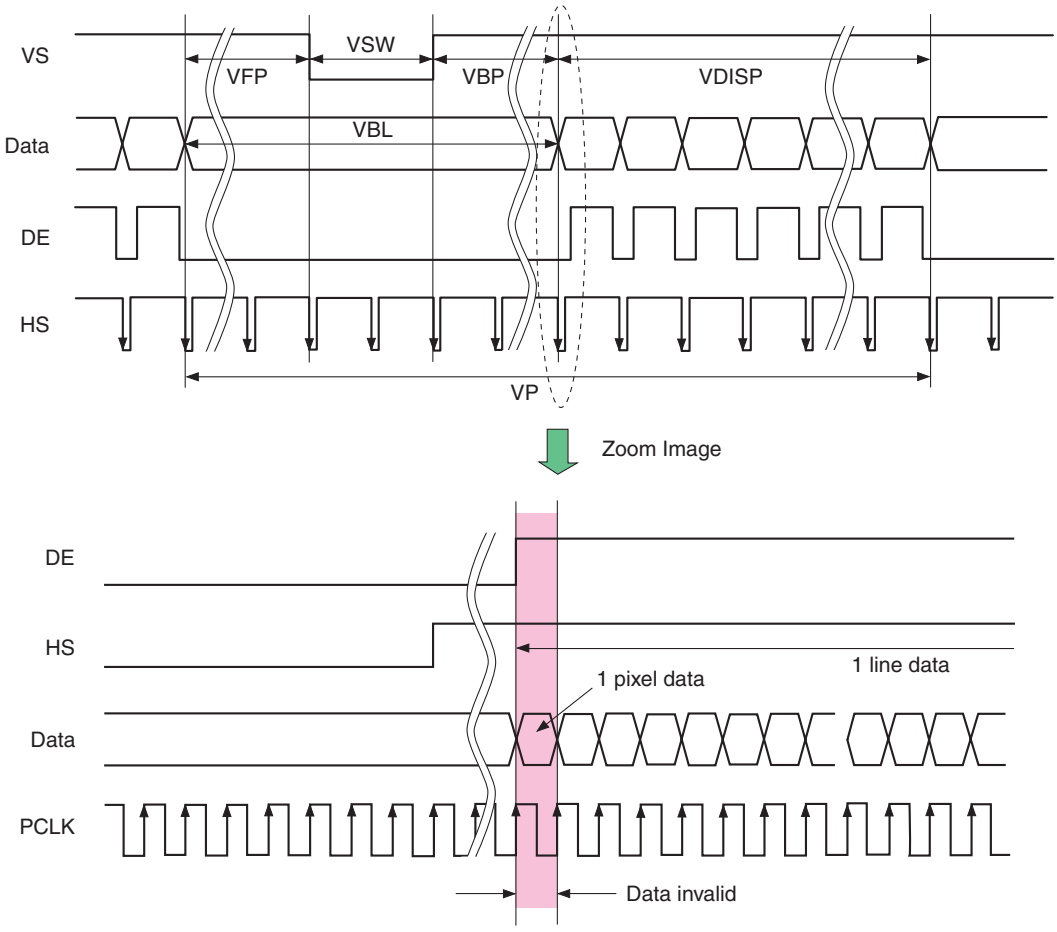
One Pixel Data Memory

The display module includes one pixel (24 bit: 8 bits for R, G and B). This memory includes information of the first active pixel on the frame (pixel: 0, 0 = first active line and pixel on the display) from RGB I/F.

The purpose of this memory is that there is possible the check that D[23:0]-lines are working correctly. The information of this memory is read via serial interface.

There will not be any abnormal visible effect on the display when there is written RGB information to this memory or read RGB information via the serial interface from this memory at the same time.

Note) Data read from the one pixel memory not guaranteed if read during the period when first pixel is being written to the display from the FlatLink3G /RGB interface as indicated below: -



Note) There will be no abnormal visible effects on the display when RGB data is written to the one pixel memory or when data is read from the one pixel memory via the read registers.

Serial Interface (SPI)

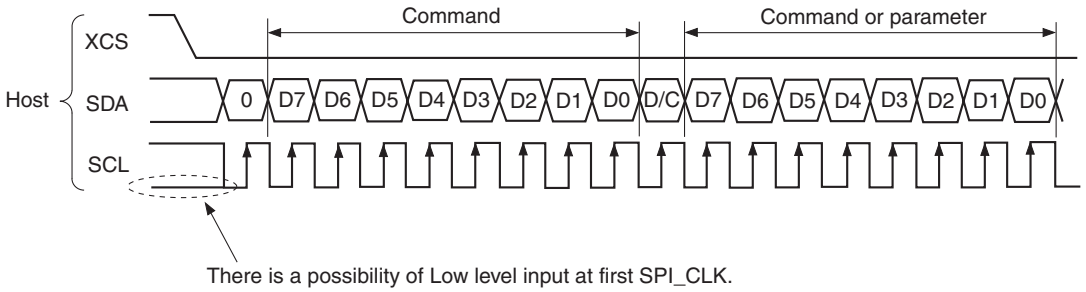
General Description

The Module uses a 3-wire 9-bit serial interface. The chip-select SPI_CS (active Low) enables and disables the serial interface. RESETX (active Low) is an external reset signal.
SPI_CLK is the serial data clock and SPI_DI/DO is serial data.

Serial data must be input to SPI_DI/DO in the sequence D/CX, D7 to D0. The Graphics Controller Chip reads the data at the rising edge of SPI_CLK signal. The first bit of serial data D/CX is data/command flag. When D/CX = “1”, D7 to D0 bits are display RAM data or command parameters. When D/CX = “0” D7 to D0 bits are commands.

Command Write

The host CPU drives the SPI_CS pin Low and starts by setting the D/CX-bit on SPI_DI/DO. The bit is read by the display on the first rising edge of SPI_CLK. On the next falling edge of SPI_CLK the MSB data bit (D7) is set on SPI_DI by the CPU. On the next falling edge of SPI_CLK the next bit (D6) is set on SPI_DI. This continues until all 8 Data bits have been transmitted as shown below.

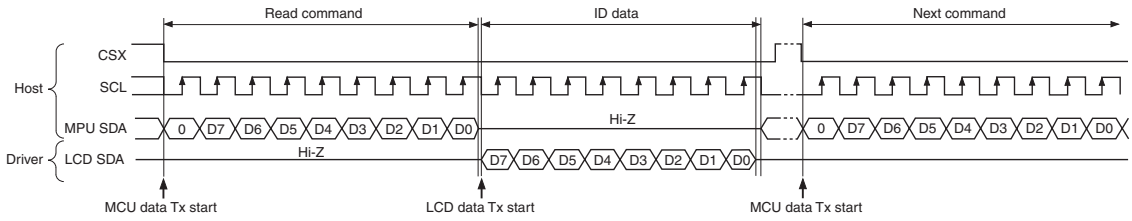


Command Write

Read Functions

The host read mode means that the host reads information from the display module (display driver) via the serial interface. The display driver sends data to the host on a falling edge of SCL and the host reads data on a rising edge of SCL. After reading operation there is a XCS High pulse before next command is sent.

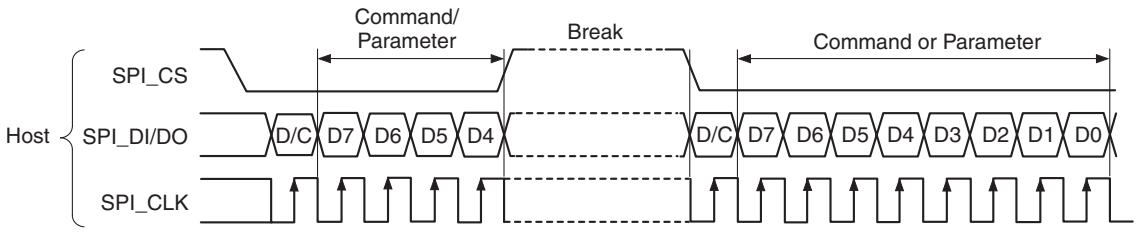
Reading Commands 05h, 06h, 07h, 08h, DAh, DBh, DCh



8-bit Reading Function without Dummy Clock Cycle

Display Module Data Transfer Recovery

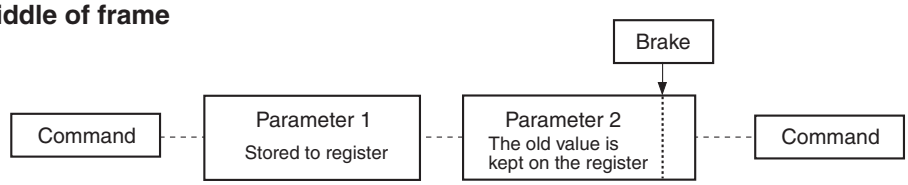
If there is a break in data transmission while transferring command, Frame Memory Data or Multiple Parameter command Data, before a whole byte has been completed, then the Display Module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (SPI_CS) is next activated.
See the following example:



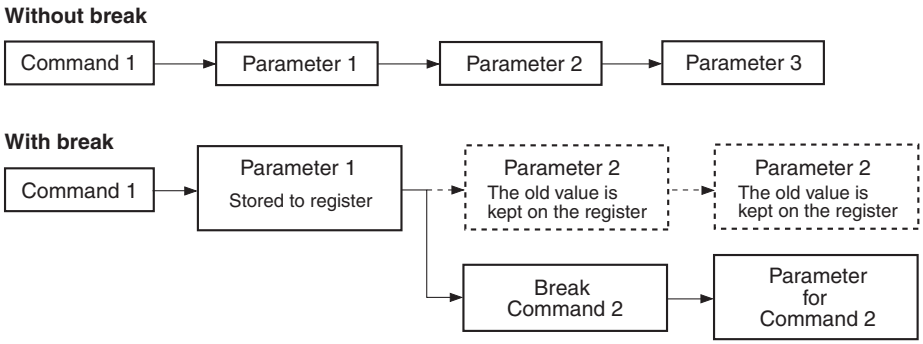
Serial Interface Break

If a 1 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below:

1. Middle of frame



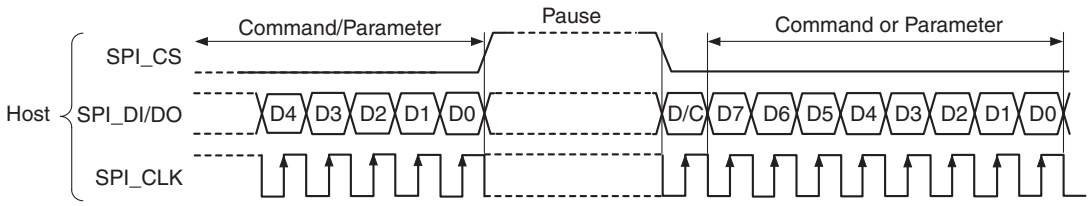
2. Bitween frames



Serial Interface Break During Parameter

Display Module Data Transfer Pause

It will be possible when transferring Frame Memory Data, Command or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of Frame Memory Data, Command or Multiple Parameter Data has been completed, then the Display Module will wait and continue the Frame Memory Data, Command or Parameter Data Transmission from the point where it was paused as shown below:



Serial Interface Pause

There are 4 cases when this kind of pause is possible:

(1) Command - Pause - Command
(2) Command - Pause - Parameter
(3) Parameter - Pause - Command
(4) Parameter - Pause - Parameter

Display Module Data Transfer Modes

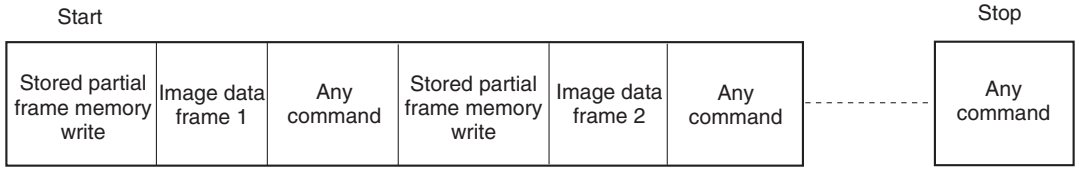
The Module has one color mode for transferring data to the display RAM. This is 3-bit color per pixel. The data format is described for the interface. Data can be downloaded to the Frame Memory by 2 methods.

Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note) These apply to Data Transfer Color mode on the Serial interface.

Power Functions

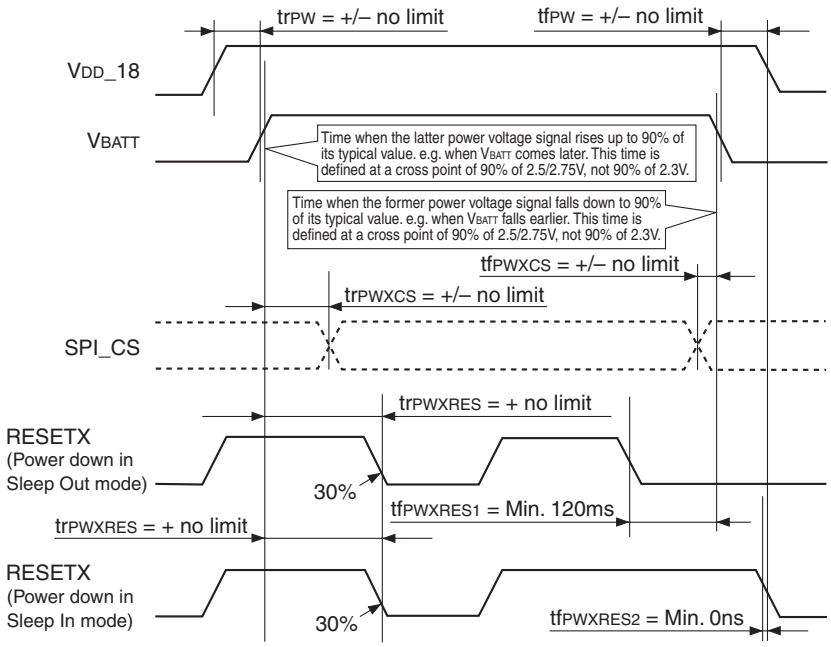
Power ON and OFF Sequences

V_{DD}_18 and V_{BATT} can be applied in any order.
V_{BATT} and V_{DD}_18 can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, V_{BATT} and V_{DD}_18 must be powered down minimum 120ms after RESETX has been released.
During power off, if LCD is in the Sleep In mode, V_{DD}_18 or V_{BATT} can be powered down minimum 0ms after RESETX has been released.
SPI_CS can be applied at any timing or can be permanently grounded. RESETX has priority over SPI_CS.

Note)
1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESETX line is not held stable by host during Power On Sequence as defined in Sections P.35 and P.36, then it will be necessary to apply a Hardware Reset (RESETX) after Host Power On Sequence is complete to ensure correct operation.
   Otherwise function is not guaranteed.

Case-1. RESETX line is held High or unstable by host at power on

If RESETX line is held High or unstable by the host during power on, hardware reset will be applied after both V_{BATT} and V_{DD}_18 have been applied - otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



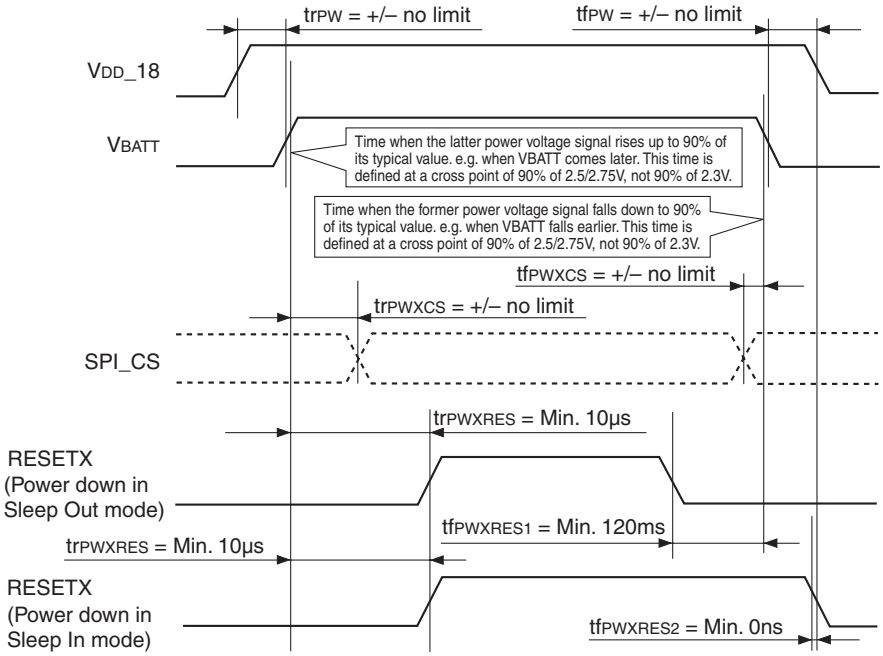
tfPWXRES1 is applied to RESETX falling in Sleep Out mode.
tfPWXRES2 is applied to RESETX falling in Sleep In mode.

Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Power ON/OFF Sequence in Case 1

Case-2. RESETX line is held Low by host at power on

If RESETX line is held Low (and stable) by the host during power on, then the RESETX must be held Low for minimum 10μs after both V_{BATT} and V_{DD}_18 have been applied.

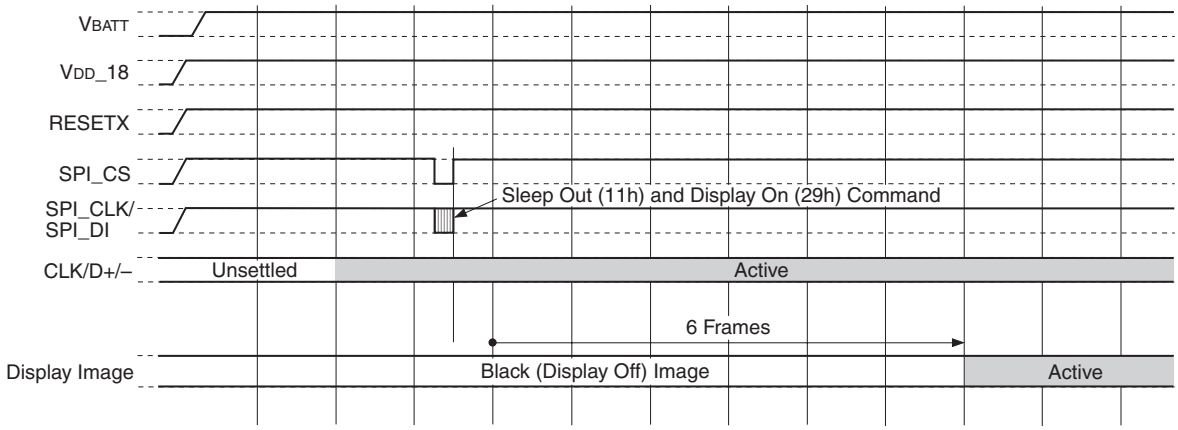


tfPWXRES1 is applied to RESETX falling in Sleep Out mode.
tfPWXRES2 is applied to RESETX falling in Sleep In mode.

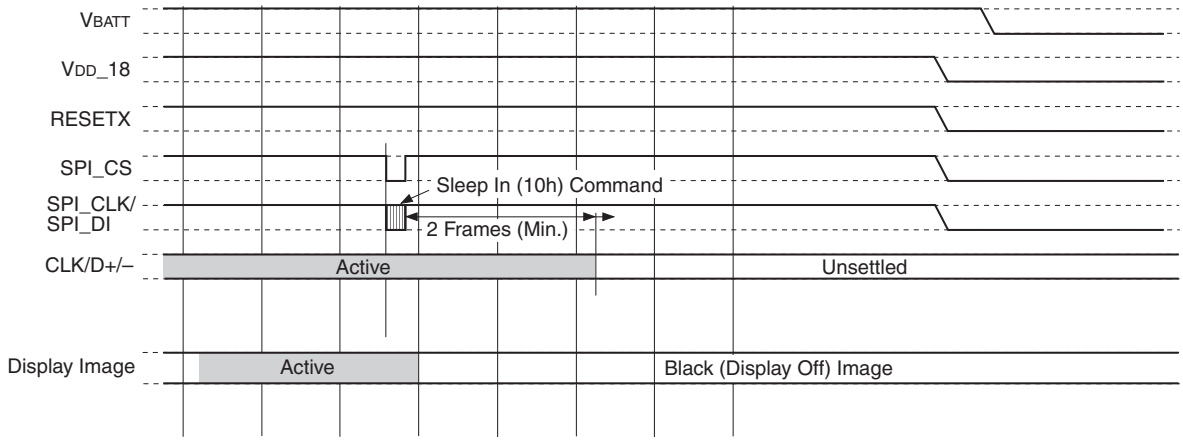
Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Power ON/OFF Sequence in Case 2

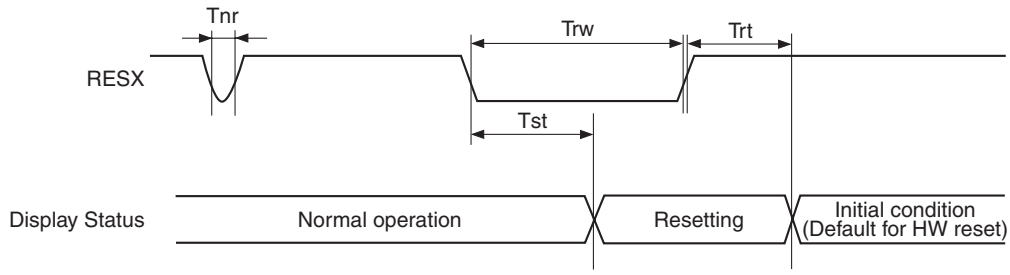
Sleep Out Sequence 1 (I/F: FlatLink3G, Sleep Mode → Normal Mode)



Sleep In Sequence 1 (I/F: FlatLink3G, Normal Mode → Sleep Mode)



Reset Timing

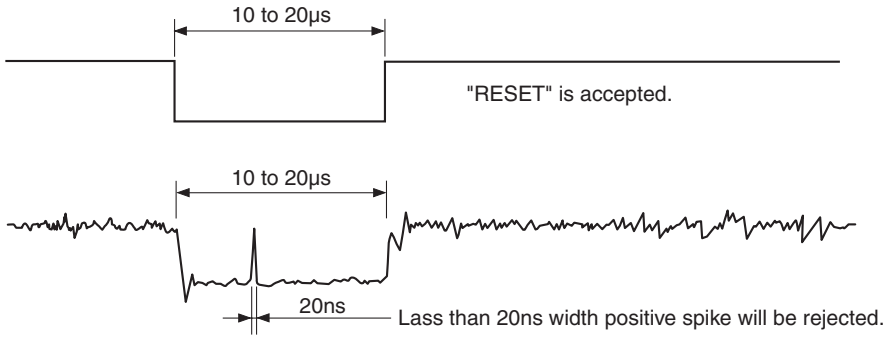


Reset Timing

Reset Timings

Symbol	Item	Min.	Typ.	Max.	Unit
Tnr	Negative noise pulse	—	—	< 5	μs
Trw	Reset pulse width	10	—	—	μs
Trt	Reset cancel time	—	—	< 5 (Note 1)	ms
		—	—	120 (Note 2, 3)	ms
Tst	Reset start time	5	—	10	μs

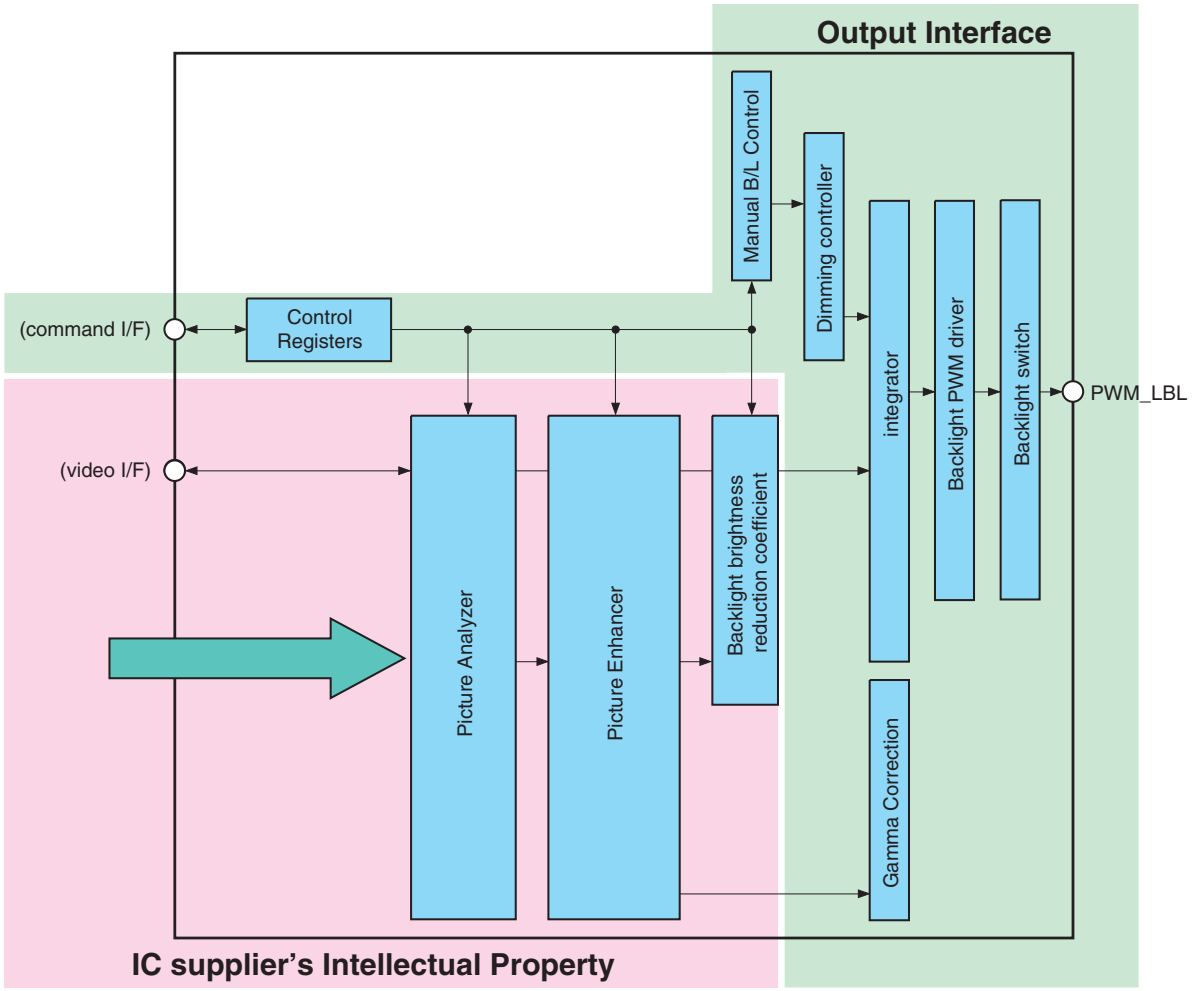
Note) 1. When reset applied during Sleep in mode.
2. When reset applied during Sleep out mode.
3. It is necessary to wait 5ms after releasing XRES before sending commands.
Also Sleep out command cannot be sent for 120ms.
4. The reset cancel time includes also required time for loading ID bytes (or similar) from NVM to ID (or similar) registers.
This loading is done every time within 5ms when HW reset is applied.
5. During the resetting period (at the end of Tst period), the display will be blanked immediately and then return to default condition for hardware reset.
6. Spike rejection also applies during a valid reset pulse as shown below:



Positive Noise Spike During Reset

In-Panel Photo Sensing Device Controller

Block Diagram (Signal Flow Chart)



Interface

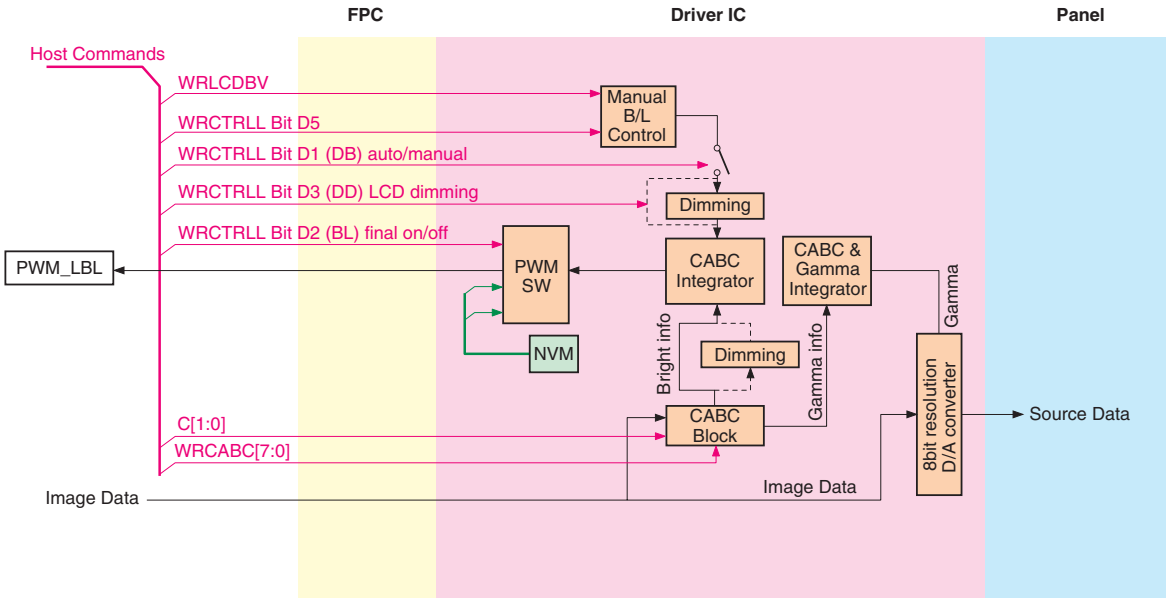
Software Interface

The In-panel Light Sensor has some optional function provided by register setting. Some of the resister is public and open to LCD module interface.

Register name	Size of registers	Function	Default	Access
LBV[7:0]	8bit	Write LCD brightness	00h	0x51 (Write) 0x52 (Read)
BCTRL	1bit	Control display	0b	0x53 (Write) 0x54 (Read)
LD	1bit	Control display	0b	
BL	1bit	Control display	0b	
LB	1bit	Control display	0b	
CM[1:0]	2bits	Content auto backlight control	00b	0x55 (Write) 0x56 (Read)
CMB[7:0]	8bit	CABC minimum brightness	00h	0x5E (Write) 0x5F (Read)

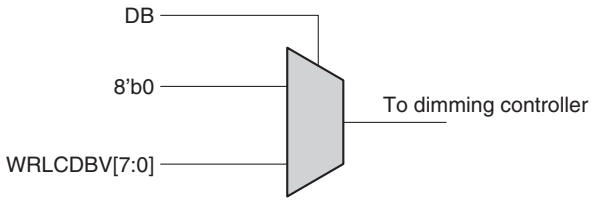
Register Connection Overview

Public/Private Control registers are connected to each blocks as shown below.



Backlight Brightness Selector

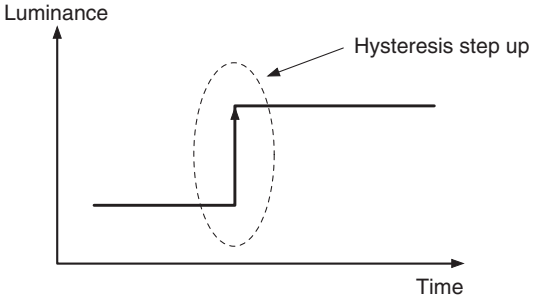
User can select to use either manual B/L values (WRLCDBV[7:0]) or 8'b0.
Manual B/L values (WRLCDBV[7:0]) can set between 0 (minimum) and 255 (maximum).
In case of using external ALS, user should be set DB = "0".



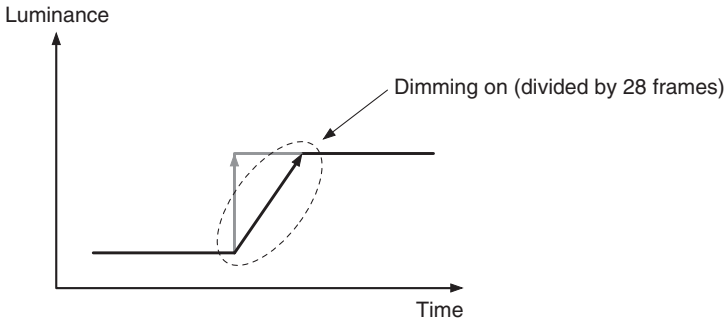
Dimming Controller

A dimming function is used when changing form one brightness level to another.
Dimming function is control 0x53 register for display and 0x63 register for keyboard respectively.

Dimming Off



Dimming On



Contents Auto Backlight Function

Contents Adaptive Function is provided by IC vender's IP.
Use can control only CM[1:0] setting defined by 0x55 register.
CM[1:0] is defined by below table.

CM1	CM0	Function	Reduction ratio
0	0	CABC off	0
0	1	Desk top mode	< 10%
1	0	Still image mode	> 30%
1	1	Moving image mode	> 30%

Definition of mode:

- ◆ CM[1:0] = 00 (Off mode): Content Auto Backlight control is totally off.
- ◆ CM[1:0] = 01 (Desk top mode): Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio 10% or less.
- ◆ CM[1:0] = 10 (Still image mode): Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio more than 30%.
- ◆ CM[1:0] = 11 (Moving image mode): Optimized for moving image. If is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio more than 30%.

LCD Backlight Control Integrator

Configuration

When CM[1:0] is 00, Contents adaptive function is turned off and minimum brightness limitation; CMB[7:0] must not applied to the result.

When CM[1:0] is not 00, Contents adaptive function is turned on and calculated CABC and LABC must not be smaller than CMB[7:0].

		C[1:0] > 0	C[1:0] = 0
CABC × WRLCDBV < WRCABC	WRLCDBV < WRCABC	WRLCDBV	WRLCDBV
	WRLCDBV ≥ WRCABC	WRCABC	WRLCDBV
CABC × WRLCDBV ≥ WRCABC	WRLCDBV < WRCABC	—	—
	WRLCDBV ≥ WRCABC	WRLCDBV × CABC	WRLCDBV

Commands for Serial Interface

Command Set

Operational code [HEX]	Function	Number of parameter bytes	Parameters
0	No operation	0	—
1	Software reset	0	—
5	Read number of parity errors	1	—
6	Read red color	1	Red information from one pixel memory
7	Read green color	1	Green information from one pixel memory
8	Read blue color	1	Blue information from one pixel memory
10	Sleep in	0	—
11	Sleep out	0	—
28	Display off	0	—
29	Display on	0	—
36	Memory access control	1	1 byte for memory access definition
3A	Interface color format	1	1 byte for color format
51	Write LCD brightness	1	
52	Read LCD brightness	1	
53	Write CTRL LCD	1	
54	Read CTRL LCD	1	
55	Write content auto backlight control	1	
56	Read content auto backlight control	1	
5E	Write CABC minimum brightness	1	
5F	Read CABC minimum brightness	1	
DA	Read ID1	1	Fixed value (10h)
DB	Read ID2	1	Module version
DC	Read ID3	1	Module ID (XXh)

Note) 1. Undefined commands are working as a NOP (00h) command.

2. B0h to D9h and DEh to FFh are for factory use (Display manufacturer area).
   After shipping these commands are acting as same as NOP (00h) commands for end customer.

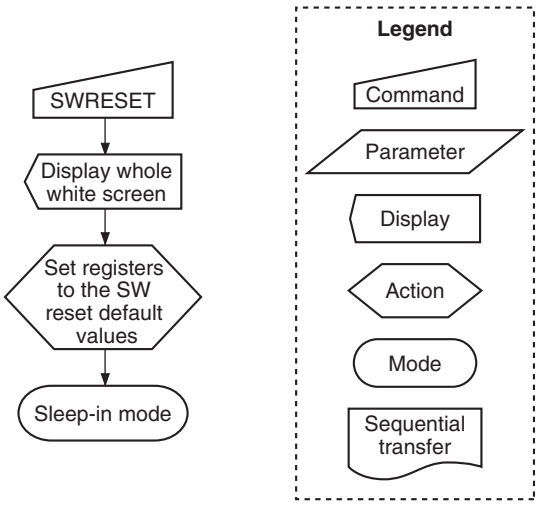
3. Commands 10h, 28h, 29h, and 36h (Bits: B4, only) are updated during V-sync when the display module is in Sleep Out mode to avoid abnormal visual effects.
   During Sleep In mode, these commands are updated immediately.

Command Description

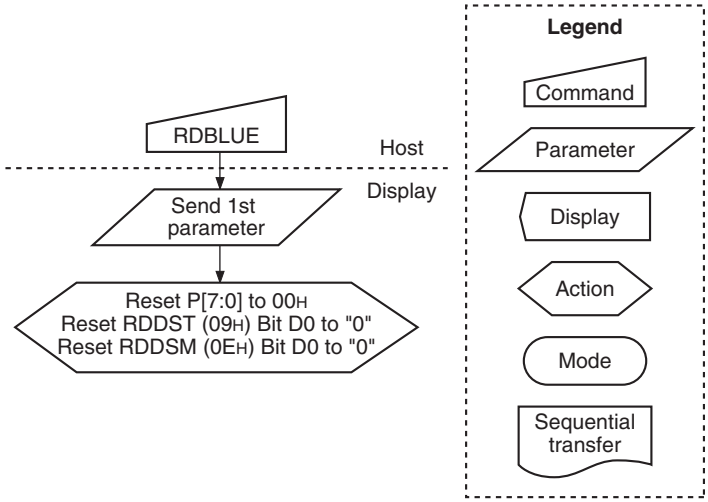
NOP (00h)

<table>
<tr><td rowspan="2">00H</td><td colspan="10">NOP (No operation)</td></tr>
<tr><td>D/CX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Parameter</td><td colspan="10">No parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command is an empty command. It does not have any effect on the display module.</td></tr>
<tr><td>Restrictions</td><td colspan="10"></td></tr>
<tr><td>Register availability</td><td colspan="10"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal mode, Sleep out</td><td>Yes</td></tr><tr><td>Partial mode, Sleep out</td><td>Yes</td></tr><tr><td>Sleep in</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><td>Status</td><td>Default value</td></tr><tr><td>Power on sequence</td><td>N/A</td></tr><tr><td>SW reset</td><td>N/A</td></tr><tr><td>HW reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow chart</td><td colspan="10"></td></tr>
</table>

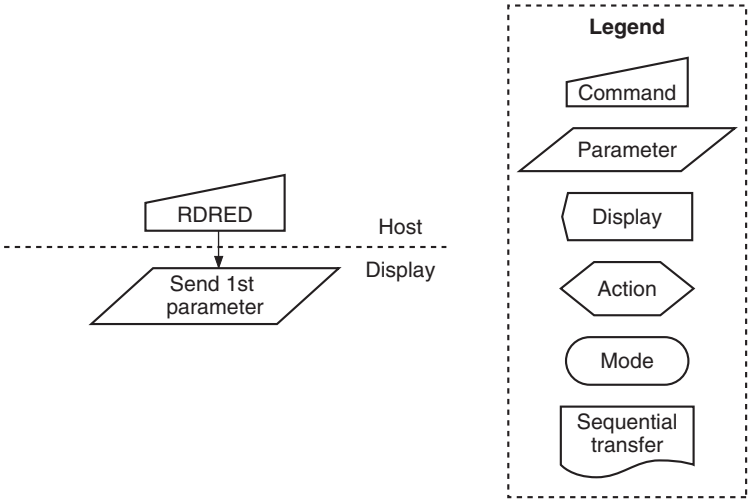
Software Reset (01h)

<table>
<tr><td>01H</td><td colspan="10">SWRESET (Software reset)</td></tr>
<tr><td></td><td>D/CX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01</td></tr>
<tr><td>Parameter</td><td colspan="10">No parameter</td></tr>
<tr><td>Description</td><td colspan="10">When software reset command is applied, it causes software reset. It resets the commands and parameters to their SW reset default values. (See default tables in each command description.) The display is blank (white in case of normally white display, black in case of normally black display) immediately.
Note) The single pixel memory content is unaffected by this command.</td></tr>
<tr><td>Restrictions</td><td colspan="10">It is necessary to wait 5ms before sending new command following software reset.
If SW reset is applied during Sleep out mode, it is necessary to wait 120ms before sending Sleep out command. Factory default settings are loaded from NVM during the first 5ms after S/W reset command is sent.
SW reset command cannot be sent during Sleep out sequence.</td></tr>
<tr><td>Register availability</td><td colspan="10"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal mode, Sleep out</td><td>Yes</td></tr><tr><td>Partial mode, Sleep out</td><td>Yes</td></tr><tr><td>Sleep in</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><td>Status</td><td>Default value</td></tr><tr><td>Power on sequence</td><td>N/A</td></tr><tr><td>SW reset</td><td>N/A</td></tr><tr><td>HW reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow chart</td><td colspan="10"> 
</td></tr>
</table>

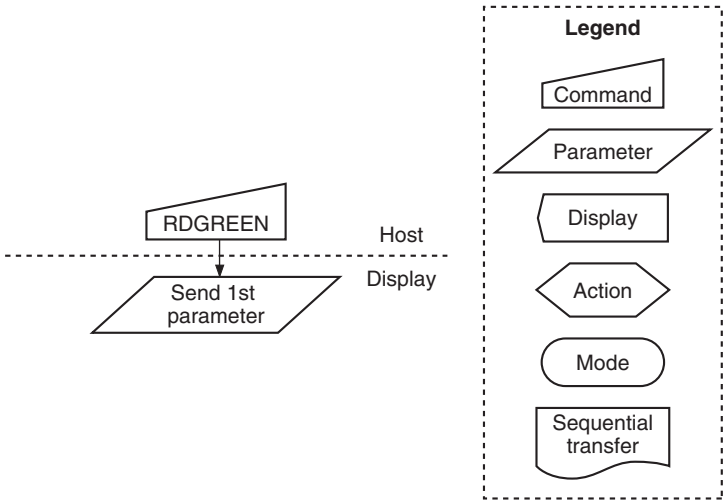
Read Number of Parity Errors (05h)

<table>
<tr><td>05H</td><td colspan="9">RDNUMPE (Read Number of Parity Errors)</td></tr>
<tr><td></td><td>D/CX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>05</td></tr>
<tr><td>1st parameter</td><td>—</td><td>P7</td><td>P6</td><td>P5</td><td>P4</td><td>P3</td><td>P2</td><td>P1</td><td>P0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="9">The first parameter returns the number of detected errors on the FlatLink3G interface: -
Bits P[6:0] indicate the number of parity errors.
Bit P7 indicate there is an overflow in bits P[6:0].</td></tr>
<tr><td>Restrictions</td><td colspan="9"></td></tr>
<tr><td>Register availability</td><td colspan="9"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal mode, Sleep out</td><td>Yes</td></tr><tr><td>Partial mode, Sleep out</td><td>Yes</td></tr><tr><td>Sleep in</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="9"><table><tr><td>Status</td><td>Default value</td></tr><tr><td>Power on sequence</td><td>00h</td></tr><tr><td>SW reset</td><td>00h</td></tr><tr><td>HW reset</td><td>00h</td></tr></table></td></tr>
<tr><td>Flow chart</td><td colspan="9"> 
</td></tr>
</table>

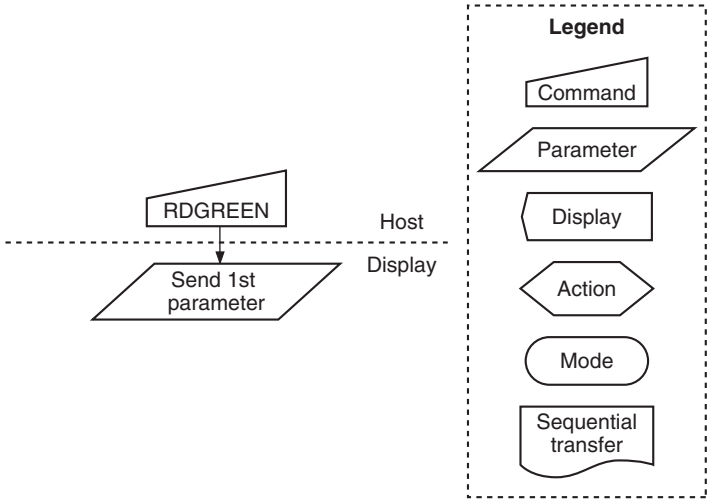
Read Red Color (06h)

06H	RDRED (Read red color)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	0	1	1	0	06
1st parameter	—	R7	R6	R5	R4	R3	R2	R1	R0	xx
Description	The first parameter is telling red color value of the first pixel of the frame when there is used RGB I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to “0”. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to “0”. 24 bit format: R7 is MSB and R0 is LSB. See: P.29									
Restrictions										
Register availability	Status: Normal mode, Sleep out — Availability: Yes Status: Partial mode, Sleep out — Availability: Yes Status: Sleep in — Availability: Yes									
Default	Status: Power on sequence — Default value: 00h Status: SW reset — Default value: 00h Status: HW reset — Default value: 00h									
Flow chart										

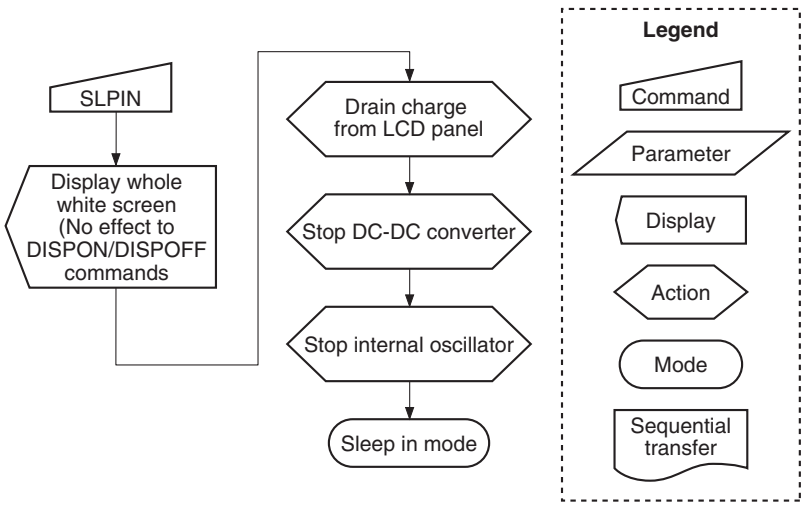
Read Green Color (07h)

07H	RDGREEN (Read green color)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	0	1	1	1	07
1st parameter	—	G7	G6	G5	G4	G3	G2	G1	G0	xx
Description	The first parameter is telling green color value of the first pixel of the frame when there is used RGB I/F. 16 and 18 bit formats: G5 is MSB and G0 is LSB. G7 and G6 are set to “0”. 24 bit format: G7 is MSB and G0 is LSB. See: P.29									
Restrictions										
Register availability	Status: Normal mode, Sleep out — Availability: Yes Status: Partial mode, Sleep out — Availability: Yes Status: Sleep in — Availability: Yes									
Default	Status: Power on sequence — Default value: 00h Status: SW reset — Default value: 00h Status: HW reset — Default value: 00h									
Flow chart										

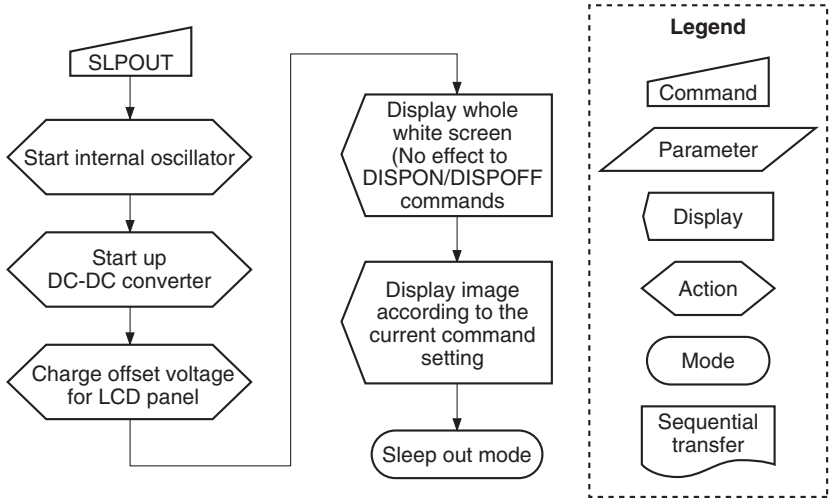
Read Blue Color (08h)

08H	RDBLUE (Read blue color)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	0	0	1	0	0	0	08
1st parameter	—	B7	B6	B5	B4	B3	B2	B1	B0	xx
Description	The first parameter is telling blue color value of the first pixel of the frame when there is used RGB I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to “0”. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to “0”. 24 bit format: B7 is MSB and B0 is LSB. See: P.29									
Restrictions										
Register availability	Status: Normal mode, Sleep out — Availability: Yes Status: Partial mode, Sleep out — Availability: Yes Status: Sleep in — Availability: Yes									
Default	Status: Power on sequence — Default value: 00h Status: SW reset — Default value: 00h Status: HW reset — Default value: 00h									
Flow chart										

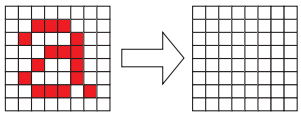
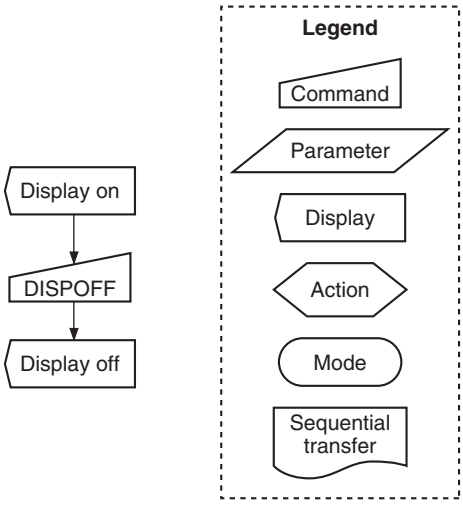
Sleep In (10h)

<table>
<tr><td>10H</td><td colspan="10">SLPIN (Sleep in)</td></tr>
<tr><td></td><td>D/CX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>Parameter</td><td colspan="10">No parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped and panel scanning is stopped. SPI and RGB I/F as well as Single Pixel Memory and Frame Memory are still working and the memory keeps its contents. The FlatLink3G receiver is Low power mode. MCU will send PCLK, HS and VS information on FlatLink3G (if FlatLink3G mode is used) or RGB I/F (if RGB I/F Mode is used) for Blank display after Sleep In command and this information is valid during 2 frames after Sleep In command if there is used Normal Display Mode On in Sleep Out -mode. The FlatLink3G receiver is powered down after these 2 frames if FlatLink3G mode is used.
There is used an internal oscillator for blank display in Partial Mode On.</td></tr>
<tr><td>Restrictions</td><td colspan="10">This command has no effect when module is already in Sleep in mode. Sleep in mode can only be exit by the Sleep out command (11h). It is necessary to wait 5ms before sending next command, this is to allow time for supply voltages and clock circuit to stabilize. It is necessary to wait 120ms after sending Sleep out command (when in Sleep in mode) before Sleep in command can be sent.</td></tr>
<tr><td>Register availability</td><td colspan="10"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal mode, Sleep out</td><td>Yes</td></tr><tr><td>Partial mode, Sleep out</td><td>Yes</td></tr><tr><td>Sleep in</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><td>Status</td><td>Default value</td></tr><tr><td>Power on sequence</td><td>Sleep in mode</td></tr><tr><td>SW reset</td><td>Sleep in mode</td></tr><tr><td>HW reset</td><td>Sleep in mode</td></tr></table></td></tr>
<tr><td>Flow chart</td><td colspan="10"> 
</td></tr>
</table>

Sleep Out (11h)

<table>
<tr><td>11H</td><td colspan="10">SLPOUT (Sleep out)</td></tr>
<tr><td></td><td>D/CX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11</td></tr>
<tr><td>Parameter</td><td colspan="10">No parameter</td></tr>
<tr><td>Description</td><td colspan="10">This command turns off Sleep mode. In this mode the DC/DC converter is enabled and panel scanning is started. MCU will start to send PCLK, HS and VS information on FlatLink3G (if FlatLink3G mode is used) or RGB I/F (if RGB I/F mode is used) before Sleep Out command and this information is valid at least 2 frames before Sleep Out command, if there is left Sleep In -mode to Sleep Out -mode in Normal Display Mode On. The FlatLink3G receiver is High power mode and stabilized within 2 image frames (2 VS) after this command, if there is left Sleep In -mode to Sleep Out -mode in Normal Display Mode On and FlatLink3G mode is used.
There is used an internal oscillator for blank display in Partial Mode On.</td></tr>
<tr><td>Restrictions</td><td colspan="10">This command has no effect when module is already in Sleep out mode. Sleep out mode can only be exit by the Sleep in command (10h). It is necessary to wait 5ms before sending next command, this is to allow time for supply voltages and clock circuit to stabilize. It is necessary to wait 120ms after sending Sleep In command (when in Sleep out mode) before Sleep out command can be sent.</td></tr>
<tr><td>Register availability</td><td colspan="10"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal mode, Sleep out</td><td>Yes</td></tr><tr><td>Partial mode, Sleep out</td><td>Yes</td></tr><tr><td>Sleep in</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><td>Status</td><td>Default value</td></tr><tr><td>Power on sequence</td><td>Sleep in mode</td></tr><tr><td>SW reset</td><td>Sleep in mode</td></tr><tr><td>HW reset</td><td>Sleep in mode</td></tr></table></td></tr>
<tr><td>Flow chart</td><td colspan="10"> 
</td></tr>
</table>

Display Off (28h)

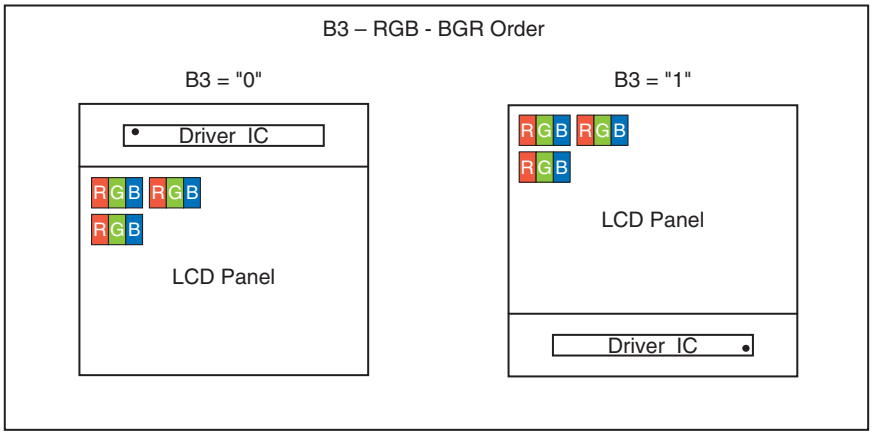
28H	DISPOFF (Display off)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	0	1	0	1	0	0	0	28
Parameter	No parameter									
Description	This command is used for entering into Display off mode. In this mode the output from RGB I/F is disabled and white page inserted. Also the output of partial frame memory is disabled. This command does not change contents of RGB I/F nor partial frame memory. This command does not change any other status. There will be no abnormal visible effect on the display when Display off command is sent. Exit from this command by Display on (29h). **Example:** RGB interface/ Partial framememory → Display 									
Restrictions	This command has no effect when module is already in display off mode.									
Register availability	Status: Normal mode, Sleep out — Availability: Yes Status: Partial mode, Sleep out — Availability: Yes Status: Sleep in — Availability: Yes									
Default	Status: Power on sequence — Default value: Display off Status: SW reset — Default value: Display off Status: HW reset — Default value: Display off									
Flow chart										

Memory Access Control (36h)

<table>
<tr><td>36H</td><td colspan="10">MADCTL (Memory access control)</td></tr>
<tr><td></td><td>D/CX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36</td></tr>
<tr><td>Parameter</td><td>1</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>00</td><td>00</td><td>00</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="10">This command defines the updating order of panel in the normal mode, updating order of partial frame memory and scanning order in partial mode. This command makes no change on the other driver status.

<table>
<tr><td>Bit</td><td>Name</td><td>Default value</td></tr>
<tr><td>B7</td><td>Page address order</td><td rowspan="3">B7, B6 and B5 control writing direction to partial frame memory. B7 and B6 control the updating order of the panel in normal mode.</td></tr>
<tr><td>B6</td><td>Column address order</td></tr>
<tr><td>B5</td><td>Page (colmun selection)</td></tr>
<tr><td>B4</td><td>Vertical order</td><td>B4 controls vertical refresh direction in partial mode.</td></tr>
<tr><td>B3</td><td>RGB/BGR order</td><td>Color selector switch control.
(0 = RGB color filter panel, 1 = BGR color filter panel)</td></tr>
</table>

All five bits (B7 - B3) affects to partial mode. The description of B3 is below.
Only bits B7, B6 and B3 affect to normal mode. Behavior of B7 and B6 in normal mode is explained in P.20 and 21. The description of B3 is below.

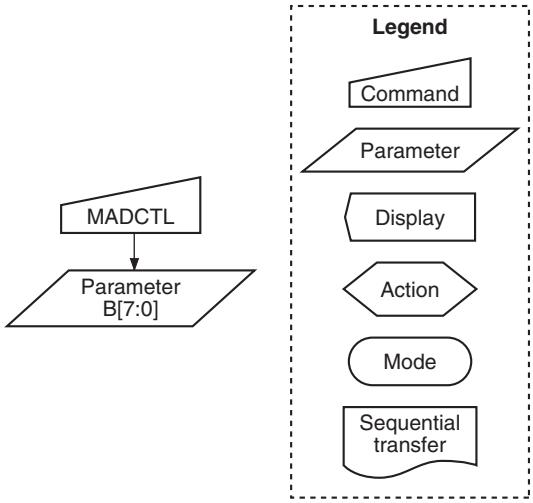


</td></tr>
<tr><td>Restrictions</td><td colspan="10">D2, D1 and D0 are set to “000” internally.</td></tr>
<tr><td>Register availability</td><td colspan="10">
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal mode, Sleep out</td><td>Yes</td></tr>
<tr><td>Partial mode, Sleep out</td><td>Yes</td></tr>
<tr><td>Sleep in</td><td>Yes</td></tr>
</table>

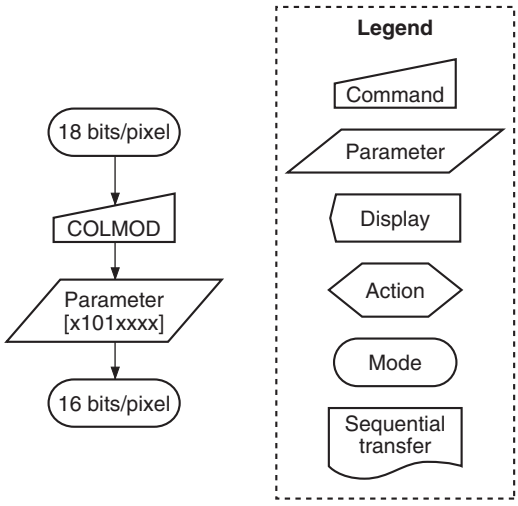
MADCTL command affects the display module according to the current mode of operation. The table below summaries the action of MADCTL for each mode: -

<table>
<tr><td>Bit</td><td>Normal Mode On</td><td>Partial Mode On</td></tr>
<tr><td>B7</td><td rowspan="2">Panel Scan Direction</td><td rowspan="2">Partial Frame Memory Pointer Control</td></tr>
<tr><td>B6</td></tr>
<tr><td>B5</td><td rowspan="2">Updates Road Register 09h Bits D28, D27 and 0Bh Bits D5, D4 only</td><td rowspan="2">Frame Memory Read and
Panel Scanning Direction Control</td></tr>
<tr><td>B4</td></tr>
<tr><td>B3</td><td colspan="2">Update Read Register 09h Bit D26 and 0Bh Bit D3 only</td></tr>
</table>

In both modes, the status register 09h and 0Bh are always updated immediately.</td></tr>
</table>

<table>
<tr><td>36H</td><td>MADCTL (Memory access control)</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default value</th></tr>
<tr><td>Power on sequence</td><td>B7 = 0, B6 = 0, B5 = 0, B4 = 0, B3 = 0, B2 = 0, B1 = 0, B0 = 0</td></tr>
<tr><td>SW reset</td><td>No change</td></tr>
<tr><td>HW reset</td><td>B7 = 0, B6 = 0, B5 = 0, B4 = 0, B3 = 0, B2 = 0, B1 = 0, B0 = 0</td></tr>
</table>
</td></tr>
<tr><td>Flow chart</td><td> 
</td></tr>
</table>

Interface Color Format (3Ah)

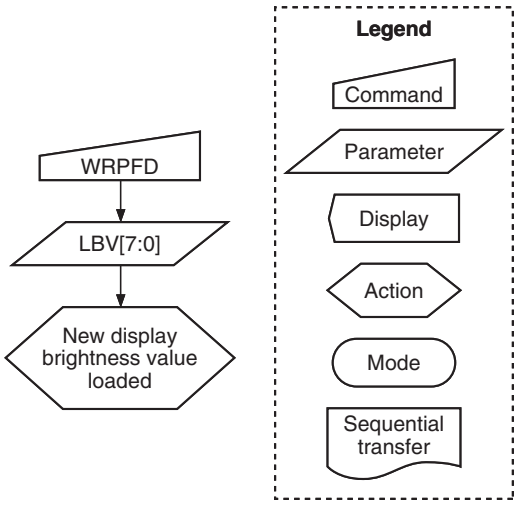
<table>
<tr><td>3AH</td><td colspan="10">COLMOD (Interface color format)</td></tr>
<tr><td></td><td>D/CX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3A</td></tr>
<tr><td>Parameter</td><td>1</td><td>xx</td><td>D6</td><td>D5</td><td>D4</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="10">This command defines the format of FlatLink3G /RGB I/F image data, which is transferred via interface. The formats are shown in the table below.
<table><tr><td>Interface format</td><td>D6</td><td>D5</td><td>D4</td></tr><tr><td>Not defined</td><td>0</td><td>0</td><td>0</td></tr><tr><td>Not defined</td><td>0</td><td>0</td><td>1</td></tr><tr><td>Not defined</td><td>0</td><td>1</td><td>0</td></tr><tr><td>Not defined</td><td>0</td><td>1</td><td>1</td></tr><tr><td>Not defined</td><td>1</td><td>0</td><td>0</td></tr><tr><td>16 bits/pixel</td><td>1</td><td>0</td><td>1</td></tr><tr><td>18 bits/pixel</td><td>1</td><td>1</td><td>0</td></tr><tr><td>24 bits/pixel</td><td>1</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>Restrictions</td><td colspan="10">Not defined in the table above are invalid and will not change the current interface color format until valid value is received.</td></tr>
<tr><td>Register availability</td><td colspan="10"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal mode, Sleep out</td><td>Yes</td></tr><tr><td>Partial mode, Sleep out</td><td>Yes</td></tr><tr><td>Sleep in</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><td>Status</td><td>Default value</td></tr><tr><td>Power on sequence</td><td>24 bits/pixel</td></tr><tr><td>SW reset</td><td>No change</td></tr><tr><td>HW reset</td><td>24 bits/pixel</td></tr></table></td></tr>
<tr><td>Flow chart</td><td colspan="10"> 
</td></tr>
</table>

Write LCD Brightness (51h)

51H	WRLCDBV (Write LCD Brightness)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	0	0	0	1	51
Parameter	1	LBV7	LBV6	LBV5	LBV4	LBV3	LBV2	LBV1	LBV0	00..FF
Description	This command is used to adjust the brightness value of the display when in Manual Brightness Mode. (When WRCTLL (53H) Bits D5 (BCTRL) = “1” and D1 (DB) = “0” The relationship between this value and output brightness of the display in luminance terms is defined in the Display Module Specification. Principally LBV[7:0] = 00H means minimum brightness, LBV[7:0] = FFH means maximum brightness. X = Don’t care									
Restrictions										
Register availability										
Default										
Flow chart										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default value
Power on sequence	00h
SW reset	00h
HW reset	00h

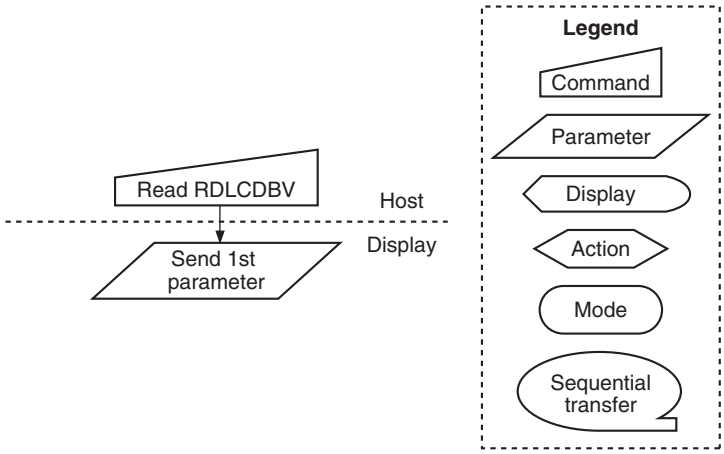


Read LCD Brightness Value (52h)

52H	RDLCDBV (Read LCD Brightness Value)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	0	0	1	0	52
Parameter	1	LBV7	LBV6	LBV5	LBV4	LBV3	LBV2	LBV1	LBV0	xx
Description	This command returns the brightness value of the LCD. The relationship between this value and output brightness of the LCD in luminance terms is defined in the LCD Module Specification. Principally LBV[7:0] = 00H means minimum brightness, LBV[7:0] = FFH means maximum brightness. When WRCTRLL (53H) Bits D5 (BCTRL) = “1” and D1 (DB) = “0” (Manual Brightness Mode), then RDLCDBV LBV[7:0] returns the value of WRLCDBV (51H) LBV[7:0]. When WRCTRLL (53H) Bits D5 (BCTRL) = “1”, D4 (A) = “1” and D1 (LB) = “1” (Automatic Brightness Mode), then RDLCDBV LBV[7:0] returns the current value of LCD Brightness after the dimming function. When WRCTRLL (53H) Bits D5 (BCTRL) = “1” and D4 (A) = “0” and DB = “1”, then RDLCDBV LBV[7:0] returns then RDLCDBV LBV[7:0] returns the current value of LCD Brightness after the dimming function. When WRCTRLL (53H) Bit D5 (BCTRL) = “0” then RDLCDBV LBV[7:0] returns 00H. When in Sleep In Mode, RDLCDBV LBV[7:0] returns 00H. X = Don’t care									
Restrictions										
Register availability										
Default										
Flow Chart										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default value
Power on sequence	00h
SW reset	00h
HW reset	00h



Write CTRL LCD (53h)

53H	WRCTRLL (Write CTRL LCD)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	0	0	1	1	53
Parameter	1	X	X	BCTRL	X	LD	BL	X	X	00..FF

Description

This command is used to control ambient light and brightness.

Bit D5 - BCTRL (Brightness Control Block On/Off)
"0" = Off (Brightness registers RDLCDBV (52H) LBV[7:0] = 00H PWM outputs PWM_LBL is Low).
"1" = On (Brightness registers RDLCDBV (52H)

Bit D3 - LD (LCD Dimming)
"0" = LCD Dimming is Off
"1" = LCD Dimming is On

Bit D2 - BL (Backlight On/Off)
"0" = Off (Completely turn off backlight circuit. Control Lines PWM_LBL must be Low).
"1" = On

- If Bit D5 (BCTRL) is changed while Bit D3 (DD) = "1" (Dimming On), then dimming will be applied to PWM_LBL and the read register values for RDLCDBV (52H).
- When Bit D1 (LB) is changed from 1 → 0 (On → Off), the backlight is turned off without any dimming, even if Bit D3(LD) is set to "1" (Dimming On).

Restriction

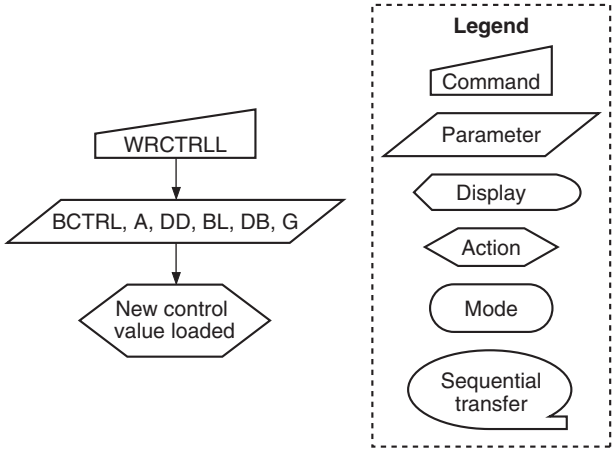
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power on sequence	00h
SW reset	00h
HW reset	00h

Flow Chart



Read CTRL Value LCD (54h)

54H	RDCTRLL (Read CTRL Value LCD)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	0	1	0	0	54
Parameter	1	0	0	BCTRL	0	LD	BL	0	0	xx

Description

This command is used to control ambient light and brightness settings.

Bit D6 - ACS (Checksum Function On/Off)
"0" = Off
"1" = On

Bit D5 - BCTRL (Brightness Control Block On/Off)
"0" = Off
"1" = On

Bit D3 - LD (LCD Dimming)
"0" = LCD Dimming is Off
"1" = LCD Dimming is On

Bit D2 - BL (Backlight On/Off)
"0" = Off
"1" = On

Restrictions

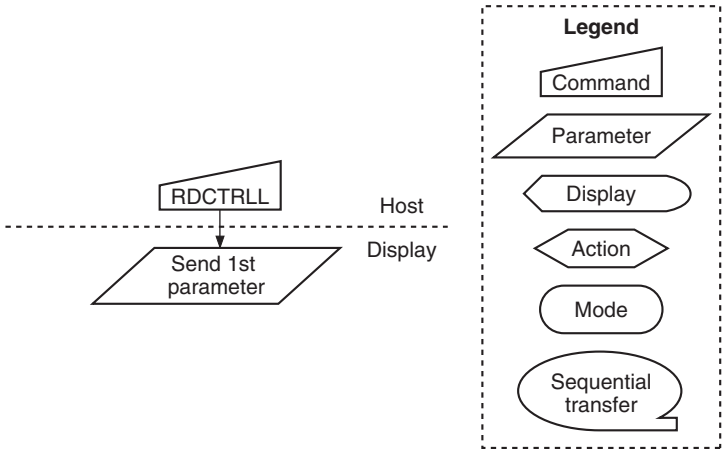
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

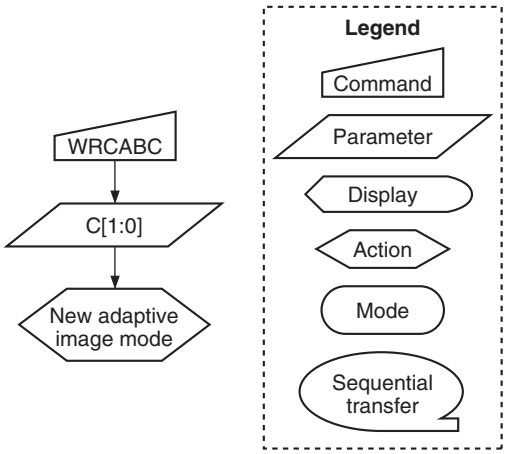
Status	Default value
Power on sequence	00h
SW reset	00h
HW reset	00h

Flow Chart



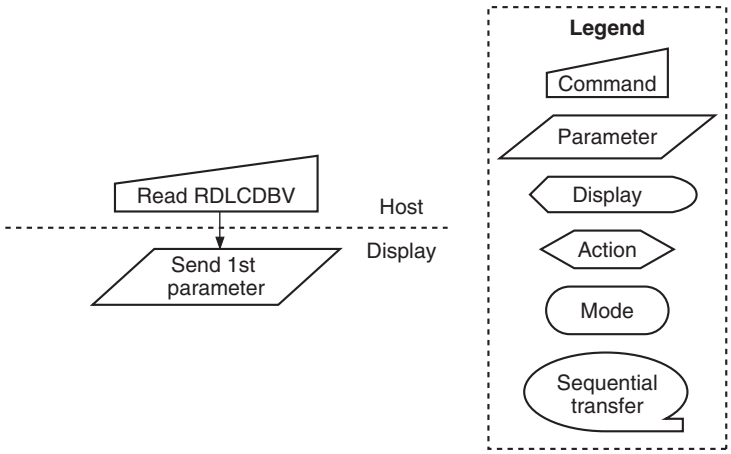
Write Content Auto Backlight Control (55h)

<table>
<tr><td>55H</td><td colspan="10">WRCABC (Write Content Auto Backlight Control)</td></tr>
<tr><td></td><td>D/CX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>55</td></tr>
<tr><td>Parameter</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>C1</td><td>C0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to adjust the mode of the image content based auto backlight control function.
It is possible to select 4 modes of content adaptive image functionality: -

<table><tr><td>C1</td><td>C0</td><td>Function</td></tr><tr><td>0</td><td>0</td><td>CABC Off</td></tr><tr><td>0</td><td>1</td><td>Desk Top Mode</td></tr><tr><td>1</td><td>0</td><td>Still Image Mode</td></tr><tr><td>1</td><td>1</td><td>Moving Image Mode</td></tr></table>
X = Don’t care</td></tr>
<tr><td>Restrictions</td><td colspan="10"></td></tr>
<tr><td>Register availability</td><td colspan="10"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><td>Status</td><td>Default value</td></tr><tr><td>Power on sequence</td><td>00h</td></tr><tr><td>SW reset</td><td>00h</td></tr><tr><td>HW reset</td><td>00h</td></tr></table></td></tr>
<tr><td>Flow chart</td><td colspan="10"> 
</td></tr>
</table>

Read Content Auto Backlight Control (56h)

<table>
<tr><td>56H</td><td colspan="10">RDCABC (Read Content Auto Backlight Control)</td></tr>
<tr><td></td><td>D/CX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>55</td></tr>
<tr><td>Parameter</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>C1</td><td>C0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="10">This command returns the setting for image content based auto backlight control function.
The setting can be one of 4 possible modes: -

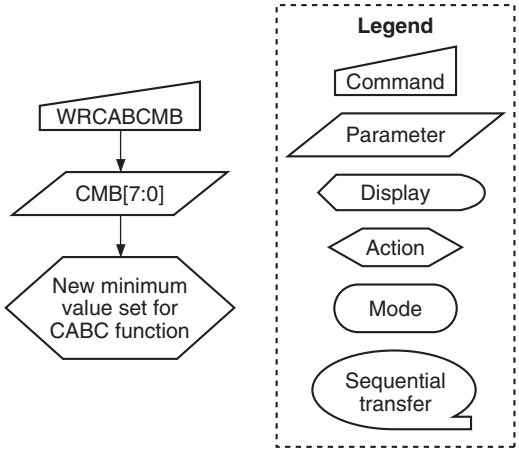
<table><tr><td>C1</td><td>C0</td><td>Function</td></tr><tr><td>0</td><td>0</td><td>CABC Off</td></tr><tr><td>0</td><td>1</td><td>Desk Top Mode</td></tr><tr><td>1</td><td>0</td><td>Still Image Mode</td></tr><tr><td>1</td><td>1</td><td>Moving Image Mode</td></tr></table>
X = Don’t care</td></tr>
<tr><td>Restrictions</td><td colspan="10"></td></tr>
<tr><td>Register availability</td><td colspan="10"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><td>Status</td><td>Default value</td></tr><tr><td>Power on sequence</td><td>00h</td></tr><tr><td>SW reset</td><td>00h</td></tr><tr><td>HW reset</td><td>00h</td></tr></table></td></tr>
<tr><td>Flow chart</td><td colspan="10"> 
</td></tr>
</table>

Write CABC Minimum Brightness (5Eh)

5EH	WRCABC (Write Content Auto Backlight Control)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	1	1	1	1	5F
Parameter	1	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	xx
Description	This command is used to set the minimum brightness value of the LCD for the CABC part of the ABC function. When CMB[7:0] = 00H this means the lowest brightness for CABC. When CMB[7:0] = FFH this means the Highest brightness for CABC. X = Don't care									
Restrictions										
Register availability										
Default										
Flow chart										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default value
Power on sequence	00h
SW reset	00h
HW reset	00h

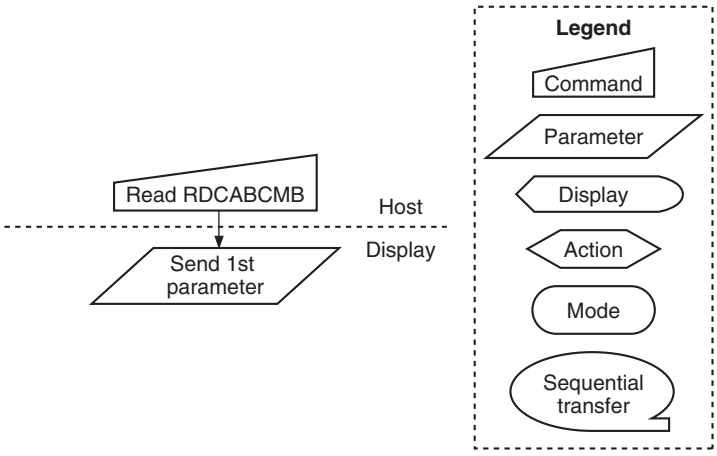


Read CABC Minimum Brightness (5Fh)

5FH	RDCABCMB (Read CABC minimum brightness)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	0	1	0	1	1	1	1	1	5F
Parameter	1	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	xx
Description	This command returns the minimum brightness value setting of CABC function. The represents the value written by WRCABCMB (5EH). X = Don't care									
Restrictions										
Register availability										
Default										
Flow chart										

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default value
Power on sequence	00h
SW reset	00h
HW reset	00h



Read ID1 (DAh)

DAH	RDID1 (Read ID1)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	1	0	1	0	DA
1st parameter	—	0	0	0	1	0	0	0	0	10
Description	This command returns the same information as “10h” of RDDIDIF command (04h).									
Restrictions										

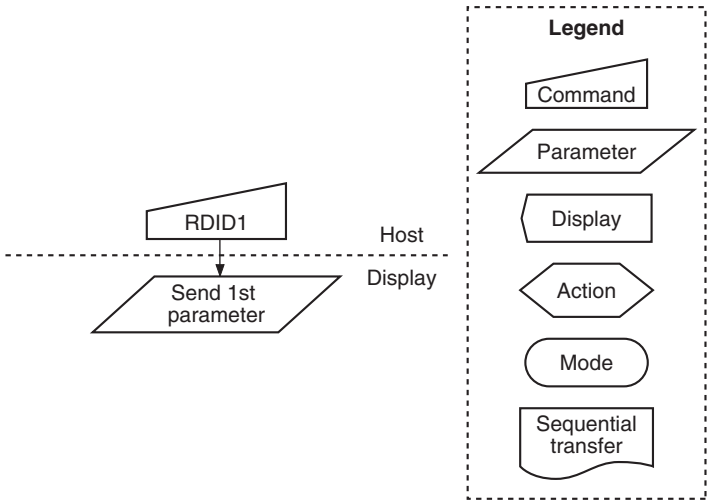
Register availability

Status	Availability
Normal mode, Sleep out	Yes
Partial mode, Sleep out	Yes
Sleep In	Yes

Default

Status	Default value
Power on sequence	10h
SW reset	10h
HW reset	10h

Flow chart



Read ID2 (DBh)

<table>
<tr><td>DBH</td><td colspan="10">RDID2 (Read ID2)</td></tr>
<tr><td></td><td>D/CX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DB</td></tr>
<tr><td>1st parameter</td><td>—</td><td>1</td><td>V6</td><td>V5</td><td>V4</td><td>V3</td><td>V2</td><td>V1</td><td>V0</td><td>80..FF</td></tr>
<tr><td>Description</td><td colspan="10">This read byte identifies version of LCD module. It is specified by Sony (with end customer agreement) and changes every time a revision is made to the LCD, material or construction. This command returns the same information as 2nd parameter of RDDIDIF command (04h). See table below:
<table><tr><th>ID byte value</th><th>Version</th><th>Changes</th></tr><tr><td>80h</td><td></td><td></td></tr><tr><td>81h</td><td></td><td></td></tr><tr><td>82h</td><td></td><td></td></tr><tr><td>83h</td><td></td><td></td></tr><tr><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td></tr></table></td></tr>
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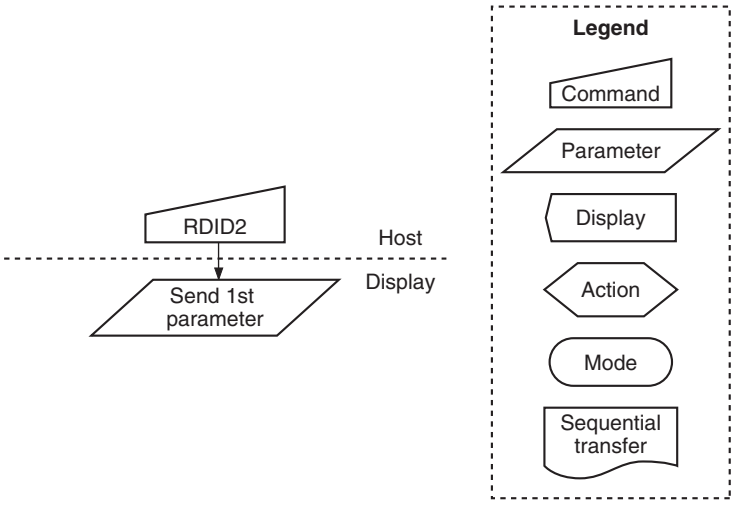
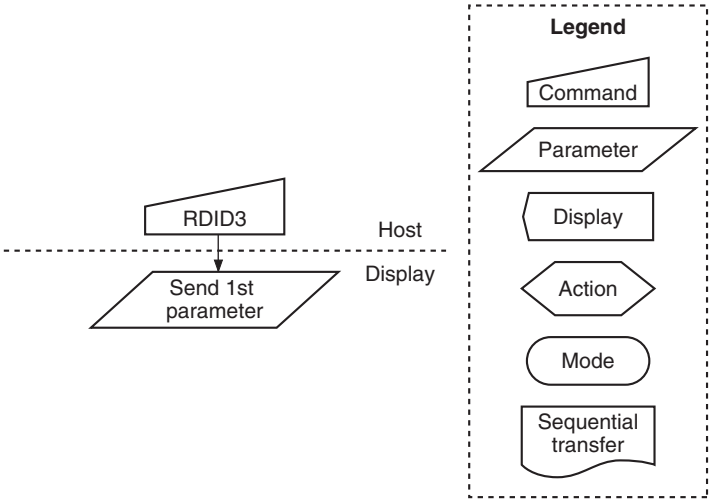
<tr><td>Register availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal mode, Sleep out</td><td>Yes</td></tr><tr><td>Partial mode, Sleep out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default value</th></tr><tr><td>Power on sequence</td><td>XXHEX</td></tr><tr><td>SW reset</td><td>XXHEX</td></tr><tr><td>HW reset</td><td>XXHEX</td></tr></table></td></tr>
<tr><td>Flow chart</td><td colspan="10"> 
</td></tr>
</table>

Read ID3 (DCh)

DCH	RDID3 (Read ID3)									
	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	1	1	0	0	Dc
1st parameter	—	I7	I6	I5	I4	I3	I2	I1	I0	I7
Description	This read byte identifies the LCD module. It is specified by end customer. This command returns the same information as 3rd parameter of RDDIDIF command (04h).									
Restrictions										
Register availability										
Default										
Flow chart										

Status	Availability
Normal mode, Sleep out	Yes
Partial mode, Sleep out	Yes
Sleep In	Yes

Status	Default value
Power on sequence	XXHEX
SW reset	XXHEX
HW reset	XXHEX



Electrooptical Characteristics Measurement

Electrooptical Characteristics (Reflective)

(Ta = 25℃, typ. condition)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle range	VAtb	CR ≥ 2	—	130	—	° (degree)
	VAlr		—	115	—	
Contrast ratio	CRbloff	Diffusion	8	17	—	
Refelectivity	Rdiff	Diffusion	1.1	1.7	—	%
White Chromaticity	Wxbloff	CIE 1931	0.300	0.340	0.380	CIE 1931
	Wybloff		0.325	0.365	0.405	

Note) Except where uniformity of brightness is affected by ground tab features on the backlight back metal frame.

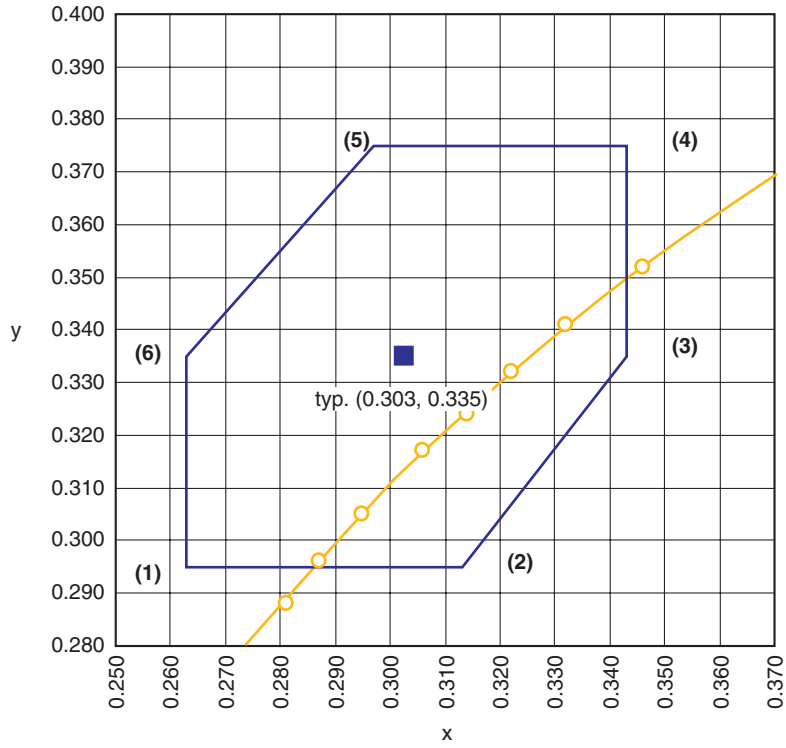
Electrooptical Characteristics (Transmissive mode)

(Ta = 25℃, typ. condition)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle range	VAtb	CR ≥ 10	—	T: 80 B: 80	—	° (degree)
	VAlr		—	L: 80 R: 80	—	
Contrast ratio	CRblon	Optimal	350	700	—	
Luminance	Lcenter	Iled = 16.5mA	280	400	—	cd/m^2
Luminance uniformity	Lunif		80	—	—	%
Color purity		Optimal	—	70	—	% (CIE area)
Response time	Ton + Toff	θ = 0° Ta = 25℃	—	35	50	ms
White chromaticity	Wxblon		0.263	0.303	0.343	CIE 1931
	Wyblon		0.295	0.335	0.375	
Red chromaticity	Rxblon		0.610	0.640	0.670	
	Ryblon		0.323	0.353	0.383	
Green chromaticity	Gxblon		0.263	0.298	0.333	
	Gyblon		0.593	0.628	0.663	
Blue chromaticity	Bxblon		0.112	0.142	0.172	
	Byblon		0.052	0.092	0.132	

Note) Except where uniformity of brightness is affected by ground tab features on the backlight back metal frame.

White Chromaticity Range



	x	y
(1)	0.263	0.295
(2)	0.313	0.295
(3)	0.343	0.335
(4)	0.343	0.375
(5)	0.297	0.375
(6)	0.263	0.335

typ.	0.303	0.335

Measurement Conditions

Basic measurement conditions

1. Driving voltage
   Typical conditions
2. Measurement temperature
   +25 ± 5℃ unless otherwise specified
3. Measurement humidity
   50 ± 10% unless otherwise specified
4. Measurement point
   One point on the center of panel unless otherwise specified
5. Light source
   D65 unless otherwise specified

Measurement setup, systems and equipment

“R1” for reflective mode

Test description : A (Fig. 1)
Test equipment : CM2002
Test illumination : Integration-sphere, specular excluded
Detector : $\theta 2 = 8^{\circ}$, $\phi = 270^{\circ}$
Temperature : Room temperature measurements
Test patterns : RGB, white, black

“R2” for reflective mode

Test description : B (Fig. 2)
Test equipment : LCD7200
Test illumination : Parallel illumination, $\theta 1 = 30^{\circ}$
Detector : Perpendicular
Temperature : All temperature measurements
Test patterns : White, black

“R3” for reflective mode

Test description : C (Fig. 3)
Test equipment : DMS703
Test illumination : Parallel illumination, perpendicular
Detector : $\theta 2 = 25\text{-}60^{\circ}$ (step 2°), $\phi = 270^{\circ}$ (step 90°)
Temperature : Room temperature measurements
Test patterns : White, black

“T1” for transmissive mode

Test description : D (Fig. 4)
Test equipment : MCPD7000
Test illumination : Display own lighting
Detector : Perpendicular ($\theta 2 = 0^{\circ}$)
Temperature : All temperature measurements
Test patterns : RGB, white, black

“T2” for transmissive mode

Test description : D (Fig. 4)
Test equipment : LCD7200
Test illumination : Parallel illumination (perpendicular) or display own lighting
Detector : Perpendicular
Temperature : All temperature measurements
Test patterns : RGB, white, black

“T3” for transmissive mode

Test description : D (Fig. 4)
Test equipment : DMS703
Test illumination : Display own lighting or external diffused backlight
Detector : $\theta 2 = 0\text{-}70^{\circ}$ (step 1°), $\phi = 270^{\circ}$ (step 90°)
Temperature : Room temperature measurements
Test patterns : White, black

Measurement equipment

1. MCPD7000
   Otsuka Electronics Co.,LTD.
   (http://www.photal.co.jp/english/product/mcpd7.html)

2. LCD7200
   Otsuka Electronics Co.,LTD.
   (http://www.photal.co.jp/english/product/lcd.html)

3. DMS703
   autronic MELCHERS Gmbh
   (http://www.autronic-melchers.com/products/measurement/dms/501.htm)

4. CM2002
   KONICA MINOLTA Holdings, INC.

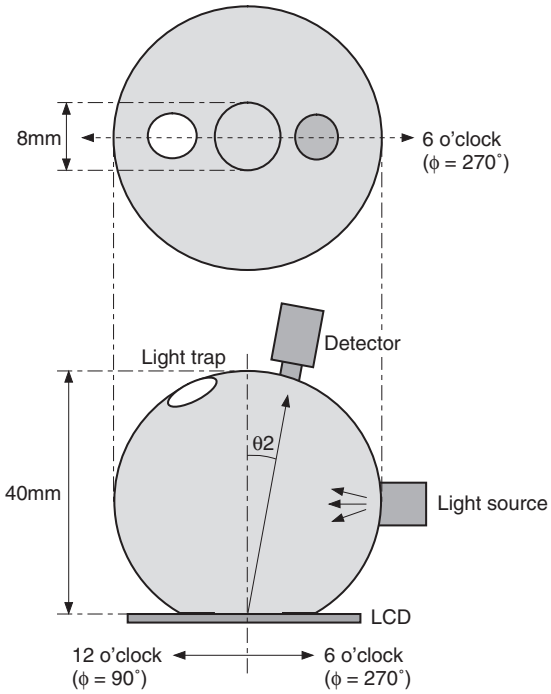


Fig. 1. Setup for Measurement A

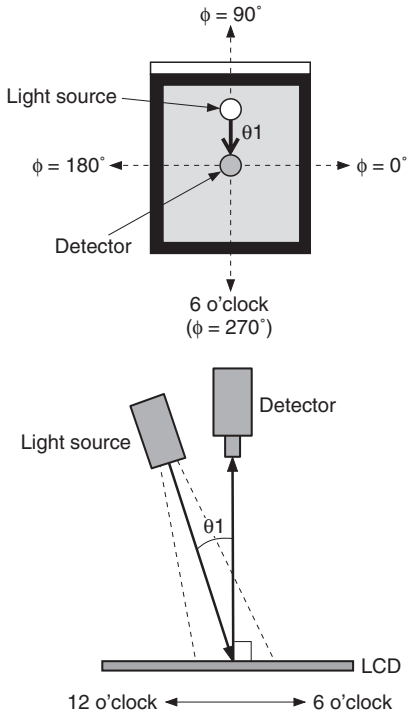


Fig. 2. Setup for Measurement B

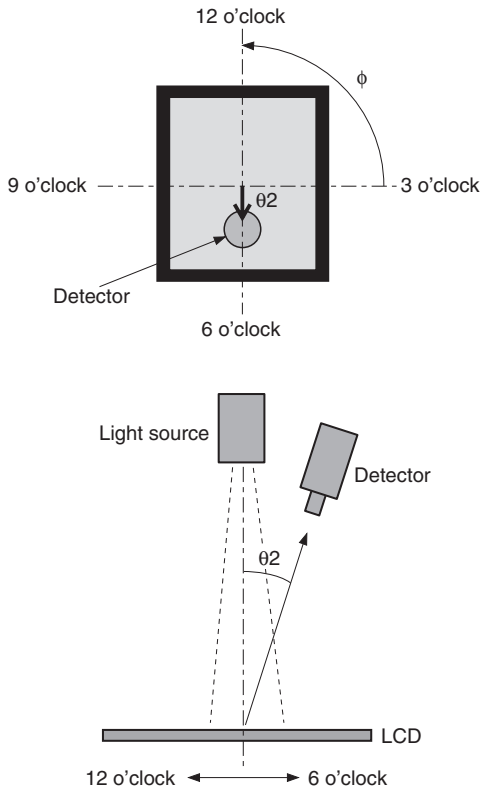


Fig. 3. Setup for Measurement C

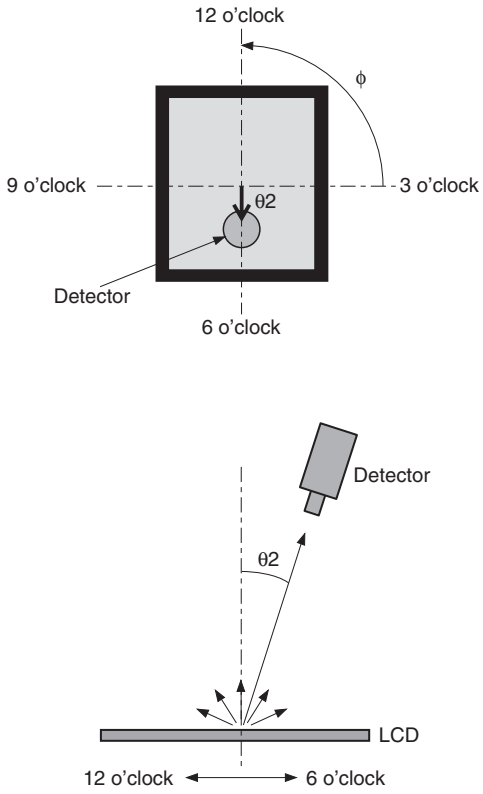


Fig. 4. Setup for Measurement D

Definition of optical characteristics

Reflectance [R] at backlight turning off [Measurement setup R2]

Reflectance of a white full screen and reflectance of a black full screen are defined below as:

$$R_w = \frac{L_{wbloff}}{L_{std}} \times \rho_{std}$$

$$R_b = \frac{L_{bbloff}}{L_{std}} \times \rho_{std}$$

Where:

R_w = Reflectance of a full white screen
R_b = Reflectance of a full black screen
ρ_{std} = Reflectance of a white diffuse reflectance standard (Labsphere SRS-99-020 or equivalent)
L_{wbloff} = Reflected luminance of full screen white state of powered on panel
L_{bbloff} = Reflected luminance of full screen black state of powered on panel
L_{std} = Reflected luminance of white diffuse reflectance standard (Labsphere SRS-99-020 or equivalent)

Contrast ratio [CRbloff] and [CRblon]

Contrast ratio for reflective mode is defined below as:

$$CRbloff = \frac{R_w}{R_b}$$ (Defined above) **[Measurement setup R2]**

Contrast ratio for transmissive mode is defined below as:

$$CRblon = \frac{L_{wblon}}{L_{bblon}}$$ **[Measurement setup T1]**

Where:

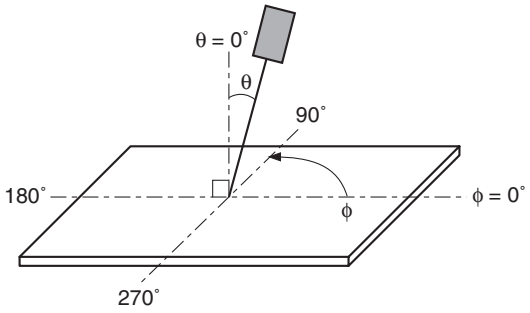
L_{wblon} = Luminance of full screen white with backlight turning on
L_{bblon} = Luminance of full screen black with backlight turning on

Definition of color chromaticity with backlight turning on
[Rxblon, Ryblon, Gxblon, Gyblon, Bxblon, Byblon, Wxblon, Wyblon] [Measurement setup T1]

The R, G, B, W are specified by x and y co-ordinate on the 1931 CIE chromaticity diagram.

Definition of viewing angle [Vatb, Valr] [Measurement setup R3], [Measurement setup T3]

For all optical characteristics theta and phi are defined as in the figure below.



Main viewing direction of 6 o'clock

Fig. 5. Definition of θ and ϕ

In the measurement system above (see Fig.5), viewing area is defined by the area which makes the CR ≥ 2 at Reflective mode, CR ≥ 10 at Transmissive mode.

[Vatb] = Total amount of viewing angle of the [Top direction] + [Bottom direction]
[Valr] = Total amount of viewing angle of the [Left direction] + [Right direction]

Note) "Bottom" is defined to the direction of the "Lower Edge" of product.

Definition of response time [Ton, Toff] **[Measurement setup T2]**

Ton is defined as the time from ON timing to 10% transmittance.
Toff is defined as the time from OFF timing to 90% transmittance.

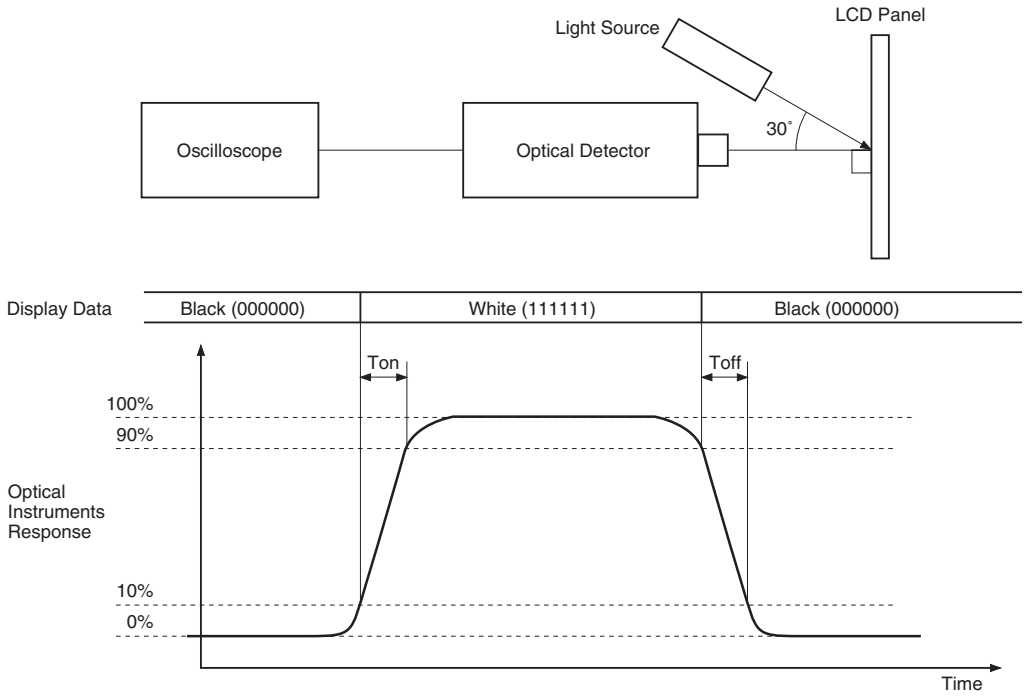


Fig. 6. Normally White Mode

Definition of luminance [Lcenter] and uniformity [Lunif] at backlight turning on

[Measurement setup T1]

Detector : Perpendicular ($\theta 2 = 0^{\circ}$)
Test patterns : White
Measurement point : Defined in the below figure

[Lcenter] = Luminance at the center point (#5).
Luminance uniformity ratio [Lunif] = (1 – |L (higher value) – L (lower value)| / L (higher value)) × 100 [%]

$$\% \text{ Uniformity} = \left(1 - \frac{|L_{max} - L_{min}|}{L_{max}}\right) \times 100 \ [\%]$$

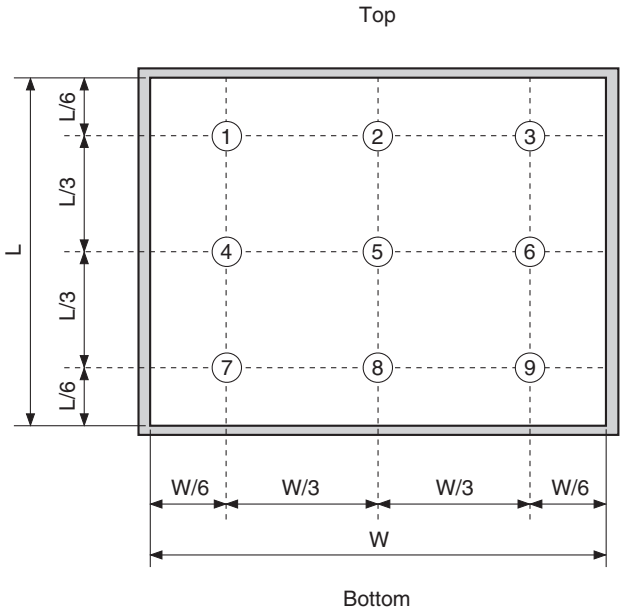
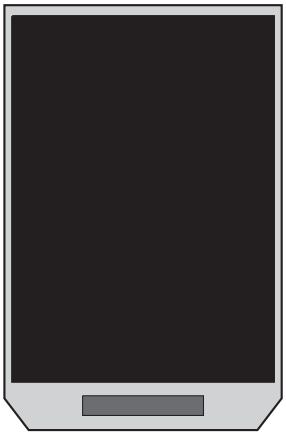


Fig. 7. The Spot Locations for Luminance Measurement

Note) FPC direction in the figure above is different in each product.

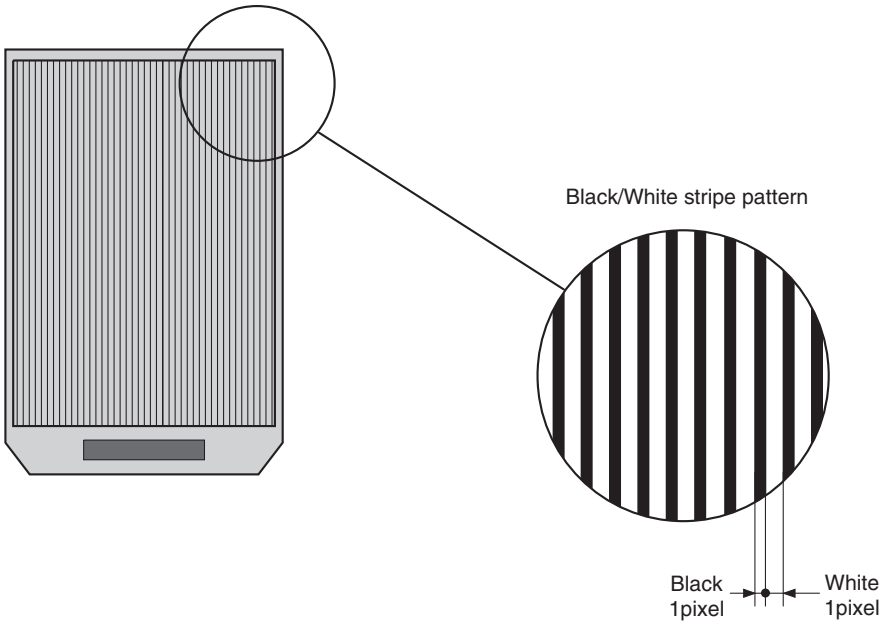
Picture Image for Measuring Power Consumption

Standby Mode



All black screen

Normal Mode



Note) Power consumption is measured under typical condition except V_{BATT} which is set at 3.7V.

Cosmetic Specification

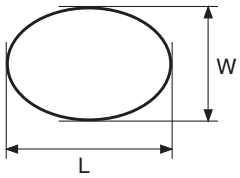
Polarizer Defect

Polarizer defect	Size [mm]	Acceptable quantity in active area	Check pattern
Bubble	0.1 < D ≤ 0.2	2	White (B/L off), (R)
	D > 0.2	0	
Scratch		W > 0.06 and L > 2.0	White (B/L off), (R)
Dent	D > 0.15	N > 5	White (B/L off), (R)

Black or White Lines

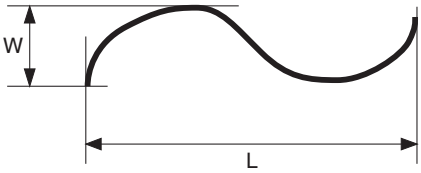
Defect	Size [mm]	Acceptable quantity in active area	
Spots	D ≤ 0.1	Disregard	
	0.1 ≤ D ≤ 0.25	N > 2	
	D > 0.25	0	
Black and White lines	W ≤ 0.03		Disregard
	0.03 < W ≤ 0.1	L ≤ 1.0	Disregard
		1.0 < L ≤ 5.0	2
		L > 5.0	0
	W > 0.1		See Spots Vriteria (#C01)

Cosmetic Criteria

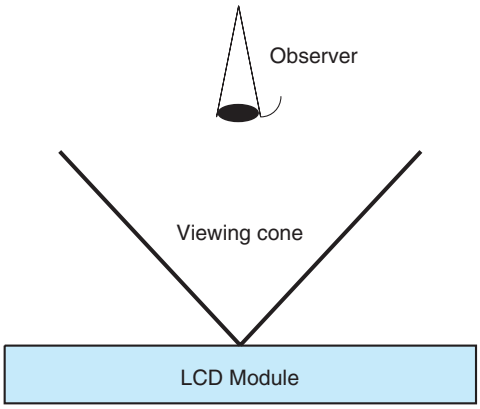


D = [Length (L) + Width (W)] / 2

Average Diameter of Spots and Bubbles



Length and Width of Lines and Scratches



Inspection conditions

Ambient light: 20W fluorescent lamp
Viewing distance: 30cm
Viewing angle: within viewing cone defined in the LCD specifications

Functional Failures

The table contains a list of known dot failures while the other table contains a list of known functional failures. The LCD modules are to be inspected by the manufacture before the module is shipped out of the factory. The codes in each tables are to used by the LCD vendors, the Contract Manufactures and Palm Quality to identify failures.

Visual defects		Acceptable quantity	Check patterns
Bright dot	Single	Total number ≤ 1	RGBW and Black raster (RT)
	2 adjacent	0	RGBW and Black raster (RT)
	3 adjacent	0	RGBW and Black raster (RT)
Dark dot	Single	Total number ≤ 3	RGBW and Black raster (RT)
	2 adjacent	Total number ≤ 1	RGBW and Black raster (RT)
Dark and bright lines		0	RGBW and Black raster (RT)
All dot defect		Total number ≤ 3	RGBW and Black raster (RT)

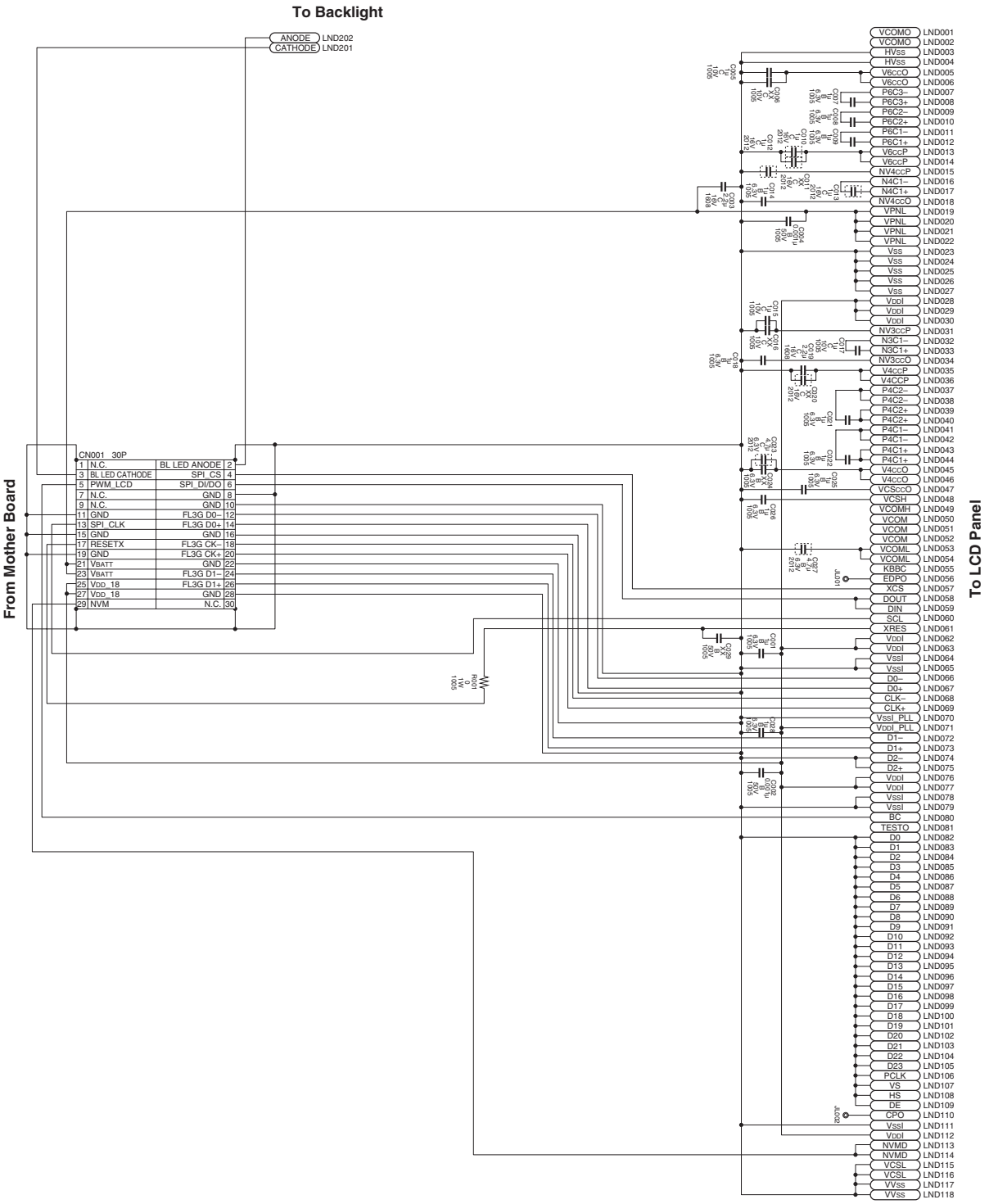
Electrical defects	Allowable [mm]
Bright dot	S ≥ 5
Dark dot	S ≥ 5
Any allowable defects	S ≥ 5

Definitions:
Pixel = 3 sub-pixels (R + G + B)
Dot = 1 sub-pixel (R or G or B)
Dark dot = 1 non-functioning sub-pixel (R or G or B)

Code	Failure	Description
F01	Missing lines	One or more permanent horizontal black on white screen, one or more permanent vertical black lines on a white screen, one or more horizontal white lines on a black screen, one or more vertical lines on a black screen.
F02	No display	No pixels are active when power and valid data are applied to the display.
F03	Bad display	All pixels are active when power and valid data are applied to the display.
F04	No backlight	No backlight is illuminated when the backlight is active.
F06	Low backlight	The backlight brightness is below the specified level.
F07	High or Low contrast	The contrast is either too light or too dark when set to a nominal position. The tolerance of this is defined in the LCD specifications. Vision tests should be calibrated to the LCD specification limits.
F08	Cracked or broken LCD	Visible crack on the LCD.
F09	Damaged components	One or more visibly damaged components on the LCD interface board that can cause the LCD to function incorrectly.
F10	Intermittent flicker	Flicker of the LCD during the display of information.

SONY does not guarantee or accept any failures caused which SONY considers related on GND-Tabs on back metal frame.

FPC Circuit


To Backlight
ANODE LND202
CATHODE LND201
From Mother Board
CN001 30P
1 N.C.
BL LED ANODE 2
3 BL LED CATHODE
SPI_CS 4
5 PWM_LCD
SPI_DI/DO 6
7 N.C.
GND 8
9 N.C.
GND 10
11 GND
FL3G D0– 12
13 SPI_CLK
FL3G D0+ 14
15 GND
GND 16
17 RESETX
FL3G CK– 18
19 GND
FL3G CK+ 20
21 VBATT
GND 22
23 VBATT
FL3G D1– 24
25 VDD_18
FL3G D1+ 26
27 VDD_18
GND 28
29 NVM
N.C. 30
To LCD Panel
VCOMO LND001
VCOMO LND002
HVss LND003
HVss LND004
V6ccO LND005
V6ccO LND006
P6C3– LND007
P6C3+ LND008
P6C2– LND009
P6C2+ LND010
P6C1– LND011
P6C1+ LND012
V6ccP LND013
V6ccP LND014
NV4ccP LND015
N4C1– LND016
N4C1+ LND017
NV4ccO LND018
VPNL LND019
VPNL LND020
VPNL LND021
VPNL LND022
Vss LND023
Vss LND024
Vss LND025
Vss LND026
Vss LND027
VDDI LND028
VDDI LND029
VDDI LND030
NV3ccP LND031
N3C1– LND032
N3C1+ LND033
NV3ccO LND034
V4ccP LND035
V4CCP LND036
P4C2– LND037
P4C2– LND038
P4C2+ LND039
P4C2+ LND040
P4C1– LND041
P4C1– LND042
P4C1+ LND043
P4C1+ LND044
V4ccO LND045
V4ccO LND046
VCSccO LND047
VCSH LND048
VCOMH LND049
VCOM LND050
VCOM LND051
VCOM LND052
VCOML LND053
VCOML LND054
KBBC LND055
EDPO LND056
XCS LND057
DOUT LND058
DIN LND059
SCL LND060
XRES LND061
VDDI LND062
VDDI LND063
VSSI LND064
VSSI LND065
D0– LND066
D0+ LND067
CLK– LND068
CLK+ LND069
VSSI_PLL LND070
VDDI_PLL LND071
D1– LND072
D1+ LND073
D2– LND074
D2+ LND075
VDDI LND076
VDDI LND077
VSSI LND078
VSSI LND079
BC LND080
TESTO LND081
D0 LND082
D1 LND083
D2 LND084
D3 LND085
D4 LND086
D5 LND087
D6 LND088
D7 LND089
D8 LND090
D9 LND091
D10 LND092
D11 LND093
D12 LND094
D13 LND095
D14 LND096
D15 LND097
D16 LND098
D17 LND099
D18 LND100
D19 LND101
D20 LND102
D21 LND103
D22 LND104
D23 LND105
PCLK LND106
VS LND107
HS LND108
DE LND109
CPO LND110
VSSI LND111
VDDI LND112
NVMD LND113
NVMD LND114
VCSL LND115
VCSL LND116
VVSS LND117
VVSS LND118
JM201
JM202

Reliability test items and conditions

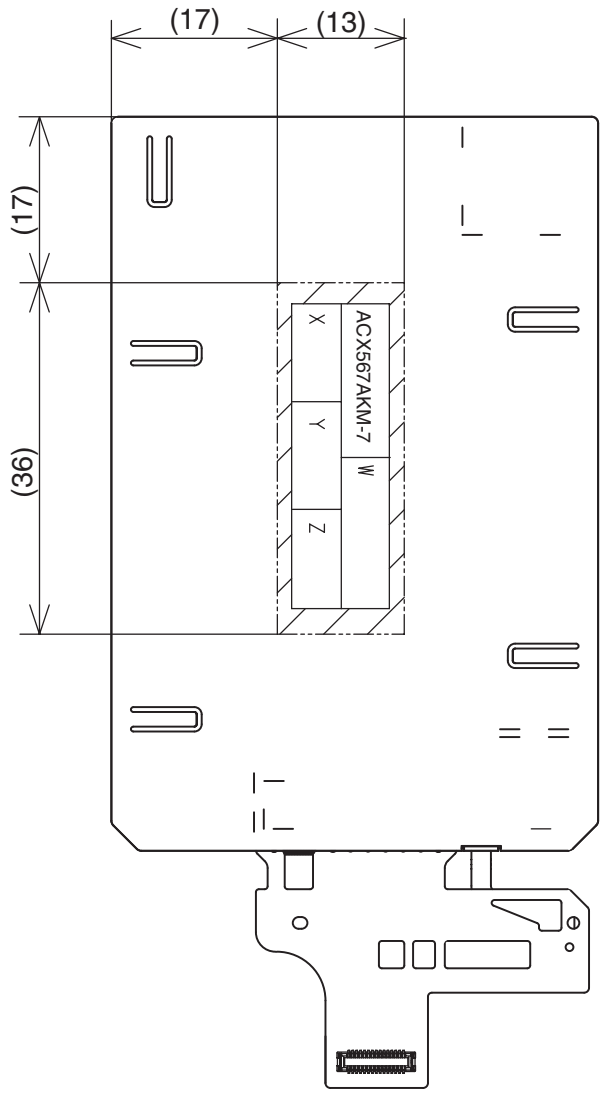
	Item	Conditions	Acceptance criteria
1	High temperature operating	+60℃, 240h	Normal performance after recovery time
2	High temperature storage	+70℃, 240h	Normal performance after recovery time
3	Low temperature operating	–10℃, 240h	Normal performance after recovery time
4	Low temperature storage	–30℃, 240h	Normal performance after recovery time
5	High temperature and humidity operating	+40℃, 95%RH, 240h	Normal performance after recovery time
6	High temperature and humidity storage	+60℃, 90%RH, 240h	Normal performance after recovery time
7	Thermal shock Non-operating	–30℃/+70℃, 05h, 100cycles	Normal performance after recovery time
8	Static electricity discharge	±200V, 200pF, 0Ω	FPC pin one time

Note) 1. Tested module shall be inspected after keeping under room temperature (15 to 35℃) and humidity (45 to 65%RH) for 2 hours.

2. In item 1, 2, 5 , 6 and 7, the degradation of polarizer are ignored.

3. There shall be no function defects in the high temperature operation, low temperature operation or high temperature and high humidity operation tests

Marking



Printing Contents

W: 160-10043-00
X: Rivision Code "EVT1" e.t.c.
Y: YYYY-MM-DD
Z: □ □ □ □ □ □ F

Control No.(Internal use)
Week manufactured
Year manufactured

Notes On Handling

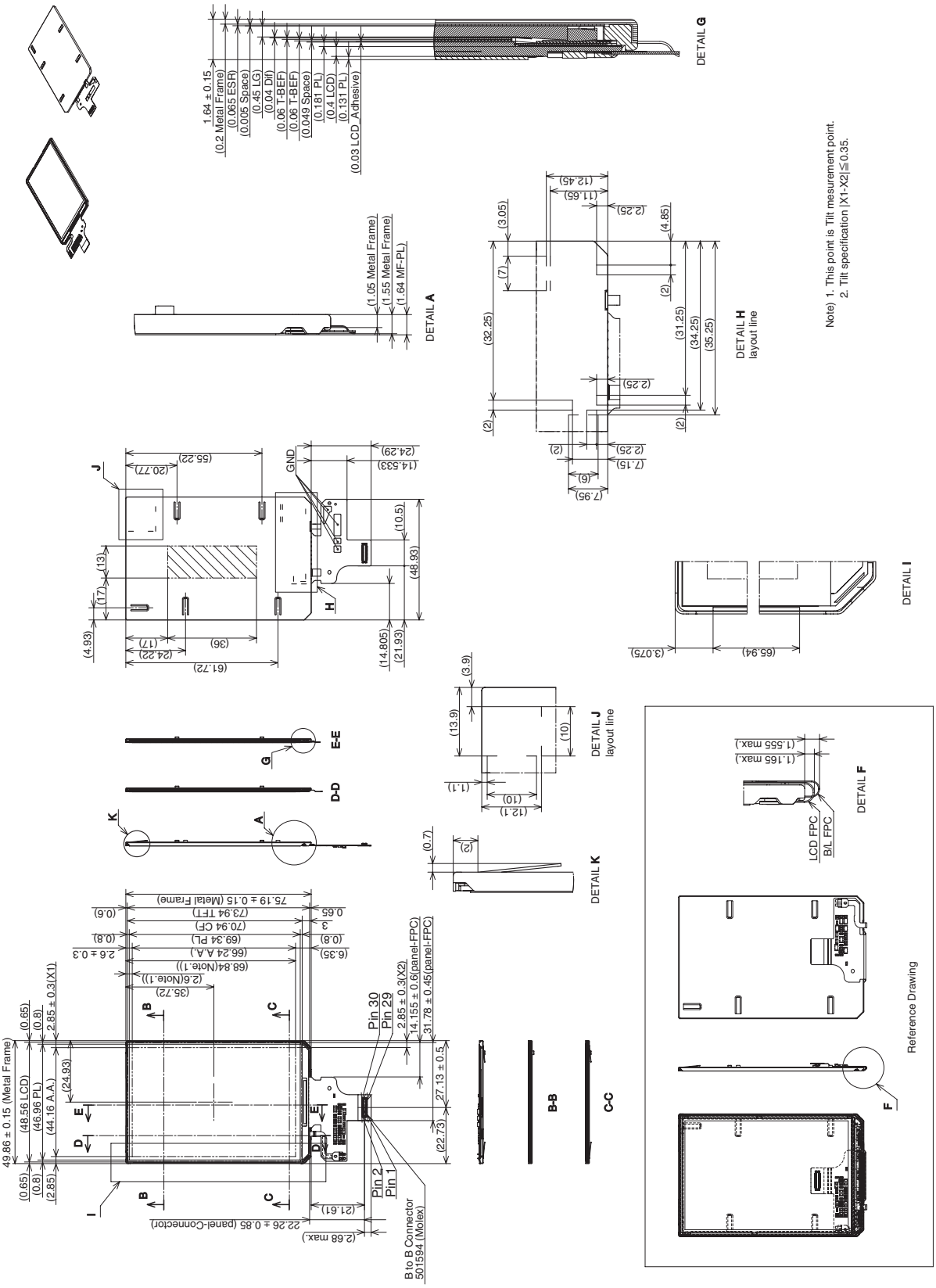
1. Static charge prevention
   Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.
   (1) Use non-chargeable gloves, or simply use bare hands.
   (2) Use an earth-band when handling.
   (3) Do not touch any electrodes of a panel.
   (4) Wear non-chargeable clothes and conductive shoes.
   (5) Install grounded conductive mats on the working floor and working table.
   (6) Keep panels away from any charged materials.
   (7) Use ionized air to discharge the panels.

2. Protection from dust and dirt
   (1) Operate in a clean environment.
   (2) Do not touch the polarizer surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
   (3) Use ionized air to blow dust off the panel.

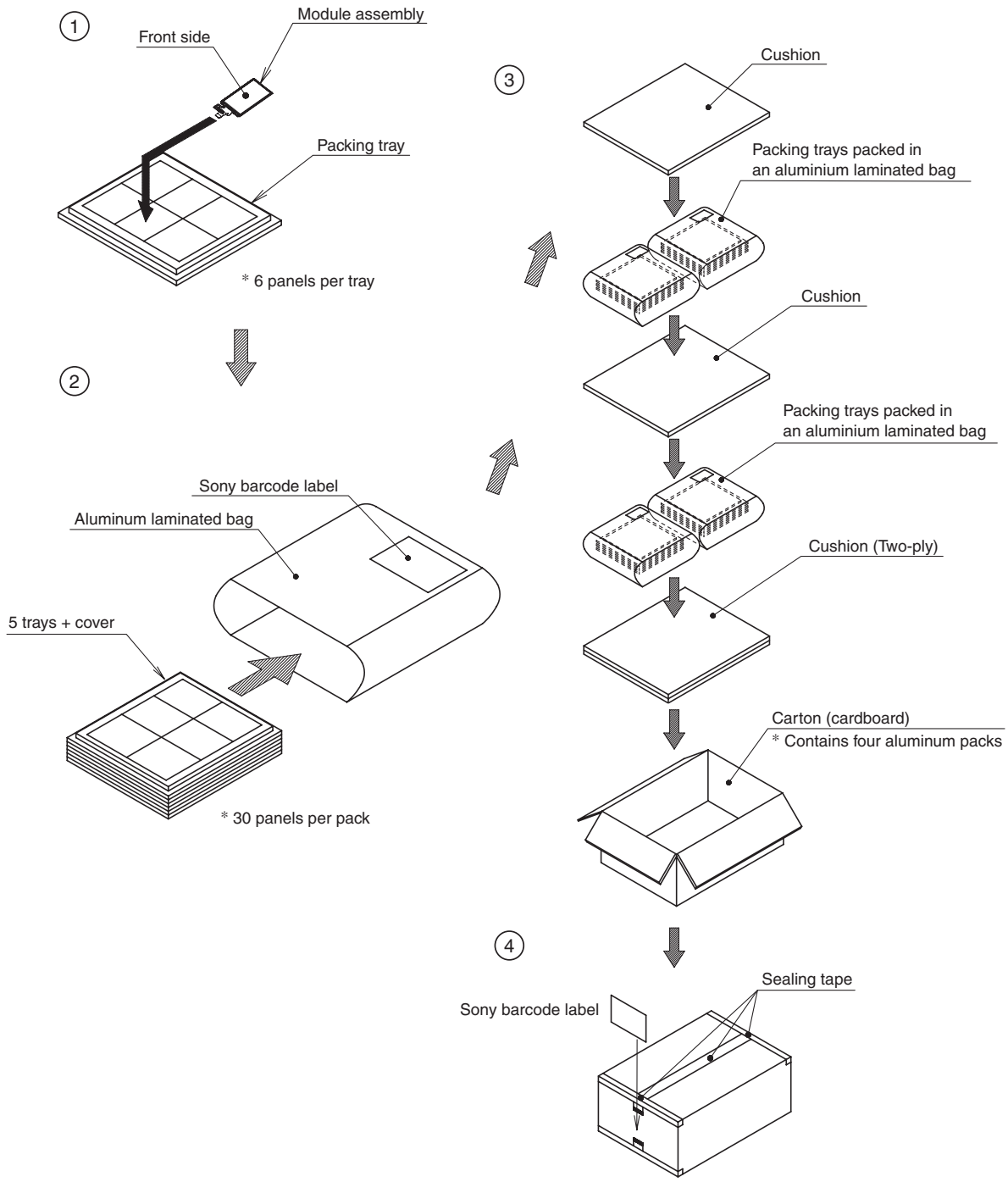
3. Other handling precautions
   (1) Do not drop the panel.
   (2) Do not twist or bend the panel.
   (3) Keep the panel away from heat sources.
   (4) Do not dampen the panel with water or other solvents.
   (5) Avoid storage or using the panel at High temperatures or High humidity, as this may result in panel damage.

Package Outline

(Unit: mm)



Packing Specification



Packing procedure.

1. Place the modules on a packing tray facing the direction shown in the figure.
2. Put the five packing trays and a cover (empty tray) in an aluminum laminated bag and seal the opening after degassing.
   Put the packing trays in the bag with the upper side of the modules facing the direction shown in the figure.
   Affix the label to the aluminum laminated bag.
3. Put the cardboard cushions and the aluminum packs in a carton as shown in the figure.
   Put the aluminum packs in the carton with the label facing the direction shown in the figure.
4. Seal the carton. (Affix sealing tape in an H-shape to the top and bottom of the outer carton.)
   Affix the specified label.