MODEL NO. : TM025CDH01

ISSUED DATE: 2010-11-25

VERSION : Ver 1.4

□Preliminary Specification
■Final Product Specification

Customer :_____

Approved by	Notes

SHANGHAI TIANMA Confirmed :

Prepared by	Checked by	Approved by
李成坚 2010.11.30 李秋琳 2010/11/30	张明明 2010.11.30 杨秋萍 2010.11.30	2010.11.30

This technical specification is subjected to change without notice

Table of Contents

Record of Revision

Rev	Issued Date	Description	Editor
1.0	2010-06-13	Preliminary Specification Release	Hui_wang
1.1	2010-07-22	Update the pin define at page5: Change 18 pin from VDD to GND Update the LCM Drawing at page 41 Add the package Drawing at page 42	Hui_wang
1.2	2010-08-13	Update the Each LED I_F =25mA at page 7, 36 Add Max Current 30mA in Page 6 As change I_F from 20mA to 25mA, so change Power consumption to 160mW at page 7	Hui_wang
1.3	2010-08-30	Update the V_F =6.4V at page 7, 36	Hui_wang
1.4	2010-11-25	Add Cell gap testing item at page 40	Shuangbing_li

1 General Specifications

Feature		Spec
Display Spec	Size	2.5 inch
	Resolution	320RGBx240
	Interface	8-bit RGB /8-bit Dummy RGB /CCIR656/601
	Color Depth	16.7M
	Technology Type	a-Si
	Pixel pitch (mm)	0.16875x0.16875
	Pixel Configuration	R.G.B. Delta
	Display Mode	TM With Normally White
	Surface Treatment(Up Polarizer)	HC
	Viewing Direction	12 o'clock
	Gray Scale Inversion Direction	6 o'clock
Mechanical Characteristics	LCM (W x H x D) (mm)	60.40x43.10x2.60
	Active Area(mm)	49.92x37.44
	With /Without TSP	Without TSP
	Weight (g)	TBD
	LED Numbers	2 LEDs
Electronic	Driver IC	ILI8961

Note 1: Viewing direction for best image quality is different from TFT definition, there is a 180 degree shift.

Note 2: Requirements on Environmental Protection: RoHS

Note 3 : LCM weight tolerance : +/- 5%

2 Input/Output Terminals

2.1 TFT LCD Panel

Matching Connector:

No	Symbol	I/O	Description	Remark
1	VCOM	I	Panel common voltage	
2	GRB	I	Global reset pin, it should be connected to VDDIO in normal operation.	
3	CS	I	Data input Enable.	
4	SDA	I	SPI data input	
5	SCL	I	SPI clock input	
6	HSYNC	I	Horizontal sync input	
7	VSYNC	I	Vertical sync input	
8	DCLK	I	Data clock input	
9	D7	I	Data input; MSB	
10	D6	I	Data input	
11	D5	I	Data input	
12	D4	I	Data input	
13	D3	I	Data input	
14	D2	I	Data input	
15	D1	I	Data input	
16	D0	I	Data input; LSB	
17	GND	P	Power ground	
18	GND	P	Power ground	
19	VDD	P	Power supply for charge pump circuit.	
20	VDDIO	P	Power supply for digital interface	
21	DVDD	C	Power setting capacitor connecting pin.	
22	V1	C	Power setting capacitor connecting pin.	
23	V2	C	Power setting capacitor connecting pin.	
24	V3	C	Power setting capacitor connecting pin.	
25	V4	C	Power setting capacitor connecting pin.	
26	VDD2	C	Power setting capacitor connecting pin.	

27	V5	C	Power setting capacitor connecting pin.	
28	V6	C	Power setting capacitor connecting pin.	
29	VDD3	C	Power setting capacitor connecting pin.	
30	VDD5	C	Power setting capacitor connect pin	
31	V7	C	Power setting capacitor connect pin	
32	V8	C	Power setting capacitor connect pin.	
33	VGH	O	Power setting capacitor connect pin.	
34	VGL	O	Power setting capacitor connect pin.	
35	AGND	C	Ground for analog circuits.	
36	FRP	O	Frame polarity output for panel VCOM.	
37	VCOMDC	O	VCOM DC output.	
38	VCAC	O	Power setting capacitor for VCOM AC.	
39	LED+	P	LED power anode	
40	LED-	P	LED power cathode	
41	VCOM	I	Panel common voltage	

Note2.1: I/O definition:

I--- Input; O---Output; P---Power/Ground; C---Capacitor; NC--- Not Connected

3 Absolute Maximum Ratings

3.1 Driving TFT LCD Panel

Ta = 25℃

Item	Symbol	Min	Max	Unit	Remark
Supply Voltage	VDD	-0.3	5.0	V	
Input Signal Voltage	D0~D7,VCOM,GRB,CS,SDA,SCL, HSYNC, VSYNC,DCLK,VCOM	-0.3	VDDIO +0.3	V	
Back Light Forward Current	I_{LED}	-	30	mA	2 LEDs in series
Operating Temperature	T_{OPR}	-20	70	℃	
Storage Temperature	T_{STG}	-30	80	℃	

4 Electrical Characteristics

4.1 Driving TFT LCD Panel

GND=0V, Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage		VDD	3.0	3.3	3.6	V	
Input Signal Voltage	High Level	VIH	0.7xVDDIO	-	VDDIO	V	VDDIO = 2.7V~3.6V
			0.8xVDDIO	-	VDDIO	V	VDDIO = 1.65V~2.7V
	Low Level	VIL	GND	-	0.3xVDDIO	V	VDDIO = 2.7V~3.6V
			GND	-	0.2xVDDIO	V	VDDIO = 1.65V~2.7V
Output Signal Voltage	High Level	VOH	VDDIO -0.4	-	VDDIO	V	VGH,VGL,FRP, VCOMDC, VCAC
	Low Level	VOL	GND	-	0.4	V	
(Panel+LSI) Power Consumption		Normal Mode	-	(16.0)	-	mA	CLK 27MHz
		-	-	-	-	-	
		Standby Mode	-	(120)	-	uA	

4.2 Driving Backlight

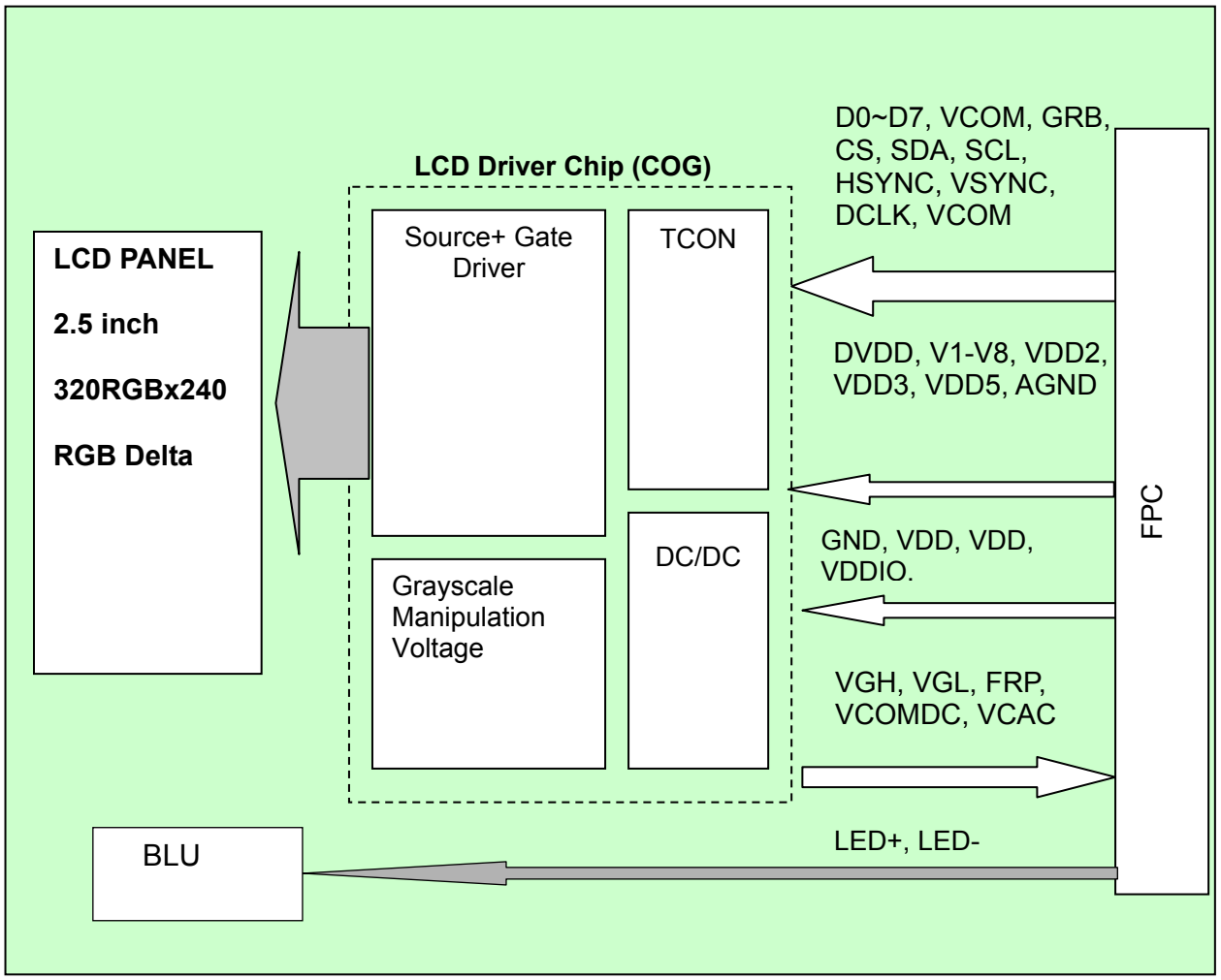
Ta=25℃

Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	I_F	--	25	--	mA	For one LED Note 1,2,3
Forward Voltage	V_F	--	6.4	--	V	
Power Consumption	W_{BL}	--	160	--	mW	

Note 1: The figure below shows the connection of backlight LED.

Note 2: One LED : I_F =25mA; Two LED:VF=6.4V
Note 3: The life of LED : 20,000 hours

4.3 Block Diagram



5 Timing Chart

5.1 3-WIRE SERIAL CONTROL INTERFACE

5.2 3-WIRE REGISTER TABLE

Register	Address								Parameter Data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R00h	0	1/0	0	0	0	0	0	0	Y_CbCr (0)	C601_EN (0)	x	x	VCAC (0110)			
R01h	0	1/0	0	0	0	0	0	1	VCDCEN (1)	x	VCDC (21h)					
R03h	0	1/0	0	0	0	0	1	1	Brightness (40h)							
R04h	0	1/0	0	0	0	1	0	0	Narrow (0)	C656_EN (0)	IF_SEL (00)		NP_SEL (10)		LDIR (1)	YDIR (1)
R05h	0	1/0	0	0	0	1	0	1	DRV_SET (0)	GRB (1)	PWM_SEL (011)			VGHL_EN (1)	PWM_EN (1)	x
R06h	0	1/0	0	0	0	1	1	0	HBLK_EN (0)	FB_SEL (00)		VBLK (15h)				
R07h	0	1/0	0	0	0	1	1	1	HBLK (46h)							
R08h	0	1/0	0	0	1	0	0	0	DRV_SEL (00)		x	x	x	x	x	x
R0Bh	0	1/0	0	0	1	0	1	1	REGSEL (0)	x	x	x	x	x	x	x
R0Ch	0	1/0	0	0	1	1	0	0	VST (00)		DE_EN (0)	CbCr (0)	DENP (0)	VSDP (1)	HSDP (1)	CLKINP (0)
R0Dh	0	1/0	0	0	1	1	0	1	CONTRAST (40h)							
R0Eh	0	1/0	0	0	1	1	1	0	x	R_CONT (40h)						
R0Fh	0	1/0	0	0	1	1	1	1	x	R_BRIGHT (40h)						
R10h	0	1/0	0	1	0	0	0	0	x	B_CONT (40h)						
R11h	0	1/0	0	1	0	0	0	1	x	B_BRIGHT (40h)						
R12h	0	1/0	0	1	0	0	1	0	TRMEN (00)							
R16h	0	1/0	0	1	0	1	1	0	x	x	x	x	x	GOP_EN (1)	x	x
R17h	0	1/0	0	1	0	1	1	1	x	L016P_SEL (101)			x	L008P_SEL (100)		
R18h	0	1/0	0	1	1	0	0	0	x	L050P_SEL (101)			x	L032P_SEL (100)		
R19h	0	1/0	0	1	1	0	0	1	x	L096P_SEL (100)			x	L072P_SEL (011)		
R1Ah	0	1/0	0	1	1	0	1	0	x	L120P_SEL (101)			x	L110P_SEL (100)		
R2Bh	0	1/0	1	0	1	0	1	1	x	x	x	x	x	x	X	STB (0)
R2Fh	0	1/0	1	0	1	1	1	1	x	VGH_SEL (11)		CF_SEL (0)	LC_SEL (00)		SOPC (01)	
R3Ch	0	1/0	1	1	1	1	0	0	GAMMA_EN (0)	L127P_SEL (011)			x	L000P_SEL (011)		
R3Dh	0	1/0	1	1	1	1	0	1	X	L127N_SEL (011)			X	L000N_SEL (111)		
R3Eh	0	1/0	1	1	1	1	1	0	X	L016N_SEL (101)			X	L008N_SEL (100)		
R3Fh	0	1/0	1	1	1	1	1	1	X	L050N_SEL (101)			X	L032N_SEL (100)		
R40h	1	1/0	0	0	0	0	0	0	X	L096N_SEL (100)			X	L072N_SEL (011)		
R41h	1	1/0	0	0	0	0	0	1	X	L120N_SEL (101)			X	L110N_SEL (100)		
R55h	1	1/0	0	1	0	1	0	1	x	INV_SEL (0)	DAT_INV (0)		x	x	x	X
R57h	1	1/0	0	1	0	1	1	1	VGHL_ENB (0)	x	x	x	x	x	X	X
R5Ah	1	1/0	0	1	1	0	1	0	x	x	x	x	x	x	VGL_SEL (10)	

Note:

1. When RSTB is low, all registers reset to default values.

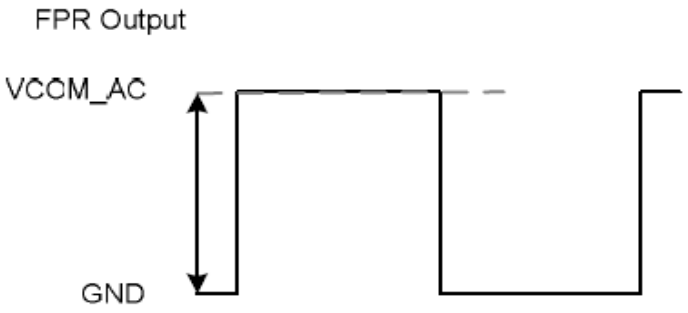
2. Serial commands are executed at next VSD signal.

5.3 3-WIRE REGISTER DESCRIPTION

VCAC (R00h[3:0]): VCOM voltage AC level seletion

D[3:0]				Low Voltage LC(V)	Normal Voltage LC1(V)	Normal Voltage LC 2(V)
0	0	0	0	3.6	4.0	5.0
0	0	0	1	3.7	4.1	5.1
0	0	1	0	3.8	4.2	5.2
0	0	1	1	3.9	4.3	5.3
0	1	0	0	4	4.4	5.4
0	1	0	1	4.1	4.5	5.5
0	1	1	0	**4.2 (default)**	**4.6 (default)**	**5.6 (default)**
0	1	1	1	4.3	4.7	5.7
1	0	0	0	4.4	4.8	5.8
1	0	0	1	4.5	4.9	5.9
1	0	1	0	4.6	5.0	6.0
1	0	1	1	4.7	5.1	6.1
1	1	x	x	4.8	5.2	6.2

*Note: Please reference LC type to R2Fh[3:2] LC_SEL



C601_EN (R00h[6]): CCIR601 interface control

D6	Function
0	Disable CCIR601. (**default**)
1	Enable CCIR601. (please refer to the table of R04H(IF_SEL) for detail descrption

Y_CbCr (R00h[7]): Y & CbCr exchange position (only valid for 8-bit input YUV640/YUV720)

	Under R0C[4] CbCr = '0'							
D7 = '0'	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3

Under R0C [4] CbCr = '1'							
Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3

(default)

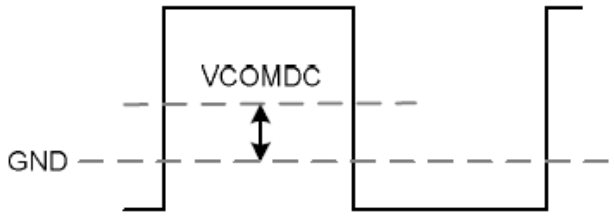
D7 = '1'	Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2
	Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R01h	VCDCEN (1)	x	VCDC (21h)					

VCDC (R01h[5:0]): VCOM voltage DC level selection (20mV/step)

D[5:0]	Low Voltage LC(V)	Normal Voltage LC 1 & 2(V)
00h	0.24	0.5
:	:	:
21h	**0.90 (default)**	**1.16 (default)**
:	:	:
3Fh	1.5	1.76

VCOMDC couple by FRP



VCDCEN (R01h[7]): VCOM DC enables control

D7	VCDCEN Fuction
0	VCOM DC function disabled. The VCOMDC pin is connected to GND.
1	VCOM DC function enabled. The VCOMDC voltage follows VCOM_DC setting. (**default**)

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R03h	Brightness (40h)							

Brightness (R03h[7:0]): RGB brightness level control

D[7:0]	Brightness Offset
00h	Dark. (-64)
40h	Center. (0). (**default**)
FFh	Bright. (+191)

Setting accuracy 1bit/step

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R04h	Narrow (0)	C656_EN (0)	IF_SEL (00)		NP_SEL (10)		LDIR (1)	YDIR (1)

YDIR(R04h[0]): Source driver output direction selection

D0	YDIR Function
0	Shift from right to left. Y1 ←Y2←...←Y959←Y960
1	Shift from left to right. Y1→Y2→...→Y959→Y960 (**default**)

LDIR(R04h[1]): Gate driver output direction selection

D1	LDIR Function
0	Shift from down to up. L1 ←L2←...←L239←L240
1	Shift from up to down. L1→L2→...→L239→L240 (**default**)

NP_SEL[1:0] (R04h[3:2]): NTSC/PAL input mode selection.

D[3:2]		NTSC/PAL Mode
0	0	PAL.
0	1	NTSC
1	X	Auto detection. (**default**)

IF_SEL[1:0] (R04h[5:4]): Input data format selection.

R00h[6]	D6	D[5:4]		Input Timing format
0	0	0	0	8-bit RGB. (**default**)
0	0	0	1	8-bit Dummy RGB 320 x 240
0	0	1	x	8-bit Dummy RGB 360 x 240
0	1	X	x	CCIR656
1	1	0	x	YUV640
1	1	1	0	YUV720

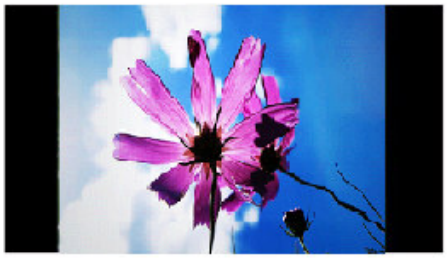
C656_EN(R04h[6]): CCIR656/CCIR601 or RGB/RGB-Dummy input interface selection.

D6	Data format
0	RGB input. (**default**)
1	CCIR656/YUV640/YUV720 input

Narrow(R04h[7]): Normal / Narrow display selection

D7	Function
0	Normal display. (**default**)
1	Narrow display.

Narrow = 0



Narrow = 1

*Not valid for parallel and serial 8-bit RGB interface.

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R05h	DRV_SET (0)	GRB (1)	PWM_SEL (011)			VGHL_EN (1)	PWM_EN (1)	x

PWM_EN(R05h[1]): Back light power converter control.

D1	PWM_EN Funciton
0	The back light power converter is off.
1	The back light power converter is controlled by STB's power on/off sequence. (**default**)

VGHL_EN(R05h[2]): VGH/VGL charge pump control

D2	VGHL_EN Funciton
0	VGH/VGL charge pump is always off.VGL will set to GND level.
1	VGH/VGL charge pump is controlled by STB's power on/off sequence. (**default**)

PWM_SEL(R05h[5:3]): PWM duty cycle selection for back light power convert

D[5:3]			PWM duty cycle
0	0	0	55%
0	0	1	60%
0	1	0	65%
0	1	1	70% (**default**)
1	0	0	75%
1	0	1	80%
1	1	0	85%
1	1	1	90%

GRB(R05h[6]): Global reset

D6	GRB Function
0	Reset all registers to default value.
1	Normal operation. (**default**)

DRV_SET(R05h[7]): DRV signal frequency selection

D7	DRV operation frequency
0	High Frequency. (**default**)
1	Low Frequency.

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R06h	HBLK_EN (0)	FB_SEL (00)		VBLK (15h)				

VBLK[4:0](R06h[4:0]): Vertical blanking setting for 8-bit RGB , 8-bit Dummy RGB & CCIR656

For 8-bit RGB, 8-bit Dummy RGB, YUV640, YUV720, CCIR656 NTSC mode, and Parallel RGB input mode.

D[4:0]	VBLK Function	Unit
00h~03h	3.	H
04h	4.	
15h	21. (**default**)	
1Fh	31.	

For 8-bit Dummy RGB, YUV640, YUV720, CCIR656 **PAL** mode (Vertical Blanking + 3)

D[4:0]	VBLK Function	Unit
00h	3.	H
04h	7.	
15h	24. (**default**)	
1Fh	34.	

FB_SEL[1:0] (R06h[6:5]): adjustable for DC-DC feedback threshold voltage

D[6:5]	Feedback Threshold Voltage
00	0.6 V. (**default**)
01	0.75V.
10	0.45V.
11	0.3V.

HBLK_EN (R06h[7]): Horizontal blanking function enable control

D[7]	HBLK EN Function
0	Disable(**default**)
1	Enable

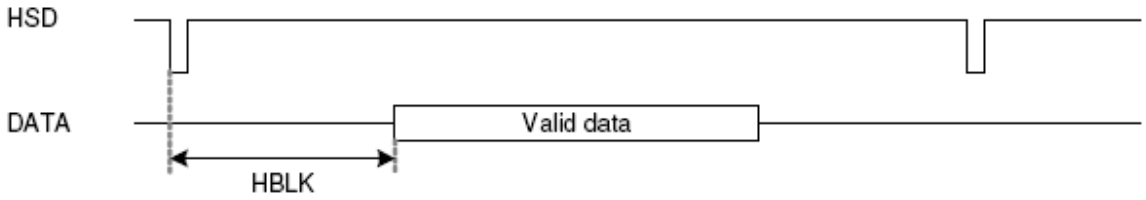
Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R07h	HBLK (46h)							

HBLK (R07h[7:0]): Horizontal blanking setting

HBLK_EN	D7~D0	HBLK	Unit	NTSC/PAL Mode
X	32h~45h	50~69	CLKIN(*)	8-bit RGB
X	46h	70		
X	47h~FFh	71~255		
X	X	241	CLKIN(*)	8-bit Dummy RGB
0	XXh	240	CLKIN(*)	YUV640, YUV720
1	00h~03h	3	CLKIN(*)	
	04h~FFh	4~255		
0	X	61	CLKIN(*)	Parallel RGB
1	00h~03h	3		
	04h~3Fh	4~63		

*The frequency of CLKIN is different under different input timing.

'X' : don't care



Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R08h	DRV_SEL (00)		x	x	x	x	x	x

DRV_SEL(R08h[7:6]) : Backlight driving capability setting

D7	D6	DRV_SEL capability
0	0	Normal capability. (**default**)
0	1	2 times the Normal capability.
1	0	3 times the Normal capability.
1	1	4times the Normal capability.

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R0Bh	REGSEL (0)	x	x	x	x	x	x	x

REGSEL (R0Bh[7]): MTP function control register

D7	REGSEL Function
0	VCOMDC Output Voltage is read from MTP memory. (**default**)
1	VCOMDC Output Voltage is controlled by the register R01h_VCDC[5:0].

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R0Ch	VST (00)		DE_EN (0)	CbCr (0)	DENP (0)	VSDP (1)	HSDP (1)	CLKINP (0)

CLKINP (R0Ch[0]): CLKIN polarity selection

D0	CLKINP Function
0	Latch data at CLKIN rising edge. (**default**)
1	Latch data at CLKIN falling edge

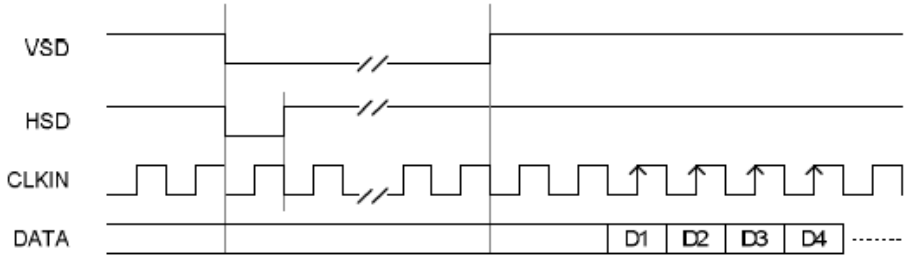
HSDP (R0Ch[1]): HSD polarity selection

D1	HSDP Function
0	Positive polarity.
1	Negative polarity. (**default**)

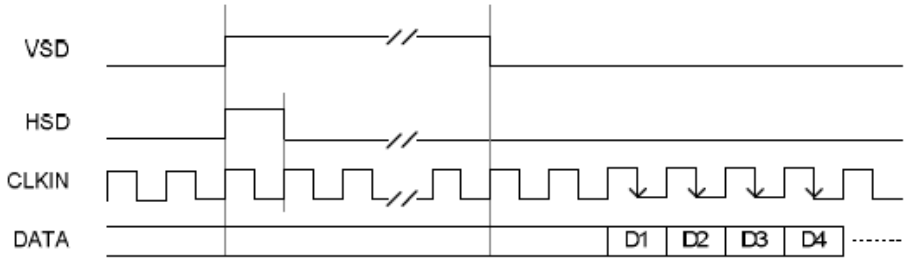
VSDP (R0Ch[2]): VSD polarity selection

D2	VSDP Function
0	Positive polarity.
1	Negative polarity. (**default**)

HSDP = 1, VSDP = 1, CLKINP = 0



HSDP = 0, VSDP = 0, CLKINP = 1



DENP (R0Ch[3]): DEN polarity selection

D3	DENP Function
0	Positive polarity (**default**)
1	Negative polarity

CbCr (R0Ch[4]): Cb & Cr exchange position (valid for CCIR656 and YUV640/YUV720)

D4	CbCr Function
0	Cb→Y→Cr. (**default**)
1	Cr→Y→Cb.

DE_EN(R0Ch[5]) : DE mode selection

D5	DE_EN Function
0	HV mode selected. (**default**)
1	DE mode selected.

* DE_EN only controls the HV and DE mode at 8-bit RGB, 8-bit Dummy RGB and Parallel Mode.

VST(R0Ch[7:6]): Vertical start time of odd/even frame

8-bit RGB / 8-bit Dummy RGB NTSC / 8-bit Dummy RGB PAL(*)

Parallel RGB input mode (PSEL= "Low")

VST		VBLK	Unit
D7	D6	ODD/EVEN	
X	0	21/21. (**default**)	H(Line)
X	1	21/20.	

CCIR656/YUV640/YUV720 NTSC/PAL(**)

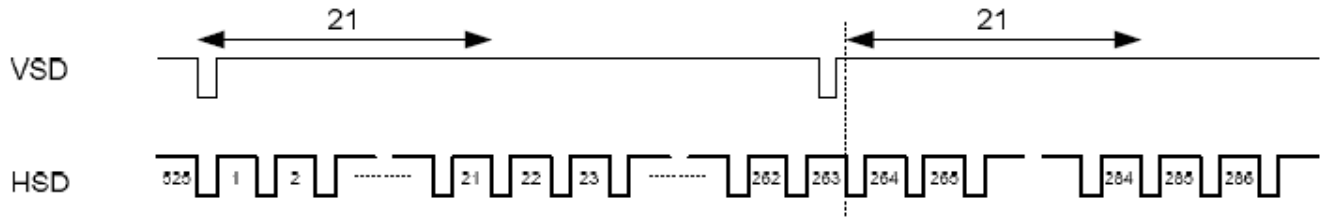
VST		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	21/21. (**default**)	H(Line)
0	1	21/22	
1	0	22/21	
1	1	22/22	

(*)The typical value of VBLK of 8-bit Dummy RGB PAL (24 H) is different from 8-bit RGB/8-bit Dummy RGB NTSC(21H).

(**) The typical value of VBLK of CCIR656 PAL (24 H) is different from CCIR656 NTSC (21H).

Note: V-Blanking must be adjusted base on the input data.

For example:



Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R0Dh	CONTRAST (40h)							

CONTRAST(R0Dh[7:0]) : RGB contrast level setting,the gain changes(1/64)/bit.

Gain formula=0.75+(R_CONT/256)

D[7:0]	Contrast Gain
00h	0
…	…
40h	1(**default**)
…	…
FFh	3.984

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R0Eh	x	R_CONT (40h)						

R-CONT(R0Eh[6:0]): Red sub-pixel contrast level setting,the gain changes (1/256)/bit.

Gain formula=0.75+(R_CONT/256)

D[6:0]	R Contrast Gain
00h	0.75
…	…
40h	1(**default**)
…	…
7Fh	1.246

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R0Fh	x	R_BRIGHT (40h)						

R-BRIGHT(R0Fh[6:0]): Red sub-pixel brightness level setting,setting accuracy: 1 step/bit.

D[6:0]	R Brightness Offset
00h	darker (-64)
…	…
40h	center (0) (**default**)
…	…
7Fh	brighter (+63)

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R12h	TRMEN (00)							

TRMEN (R12h): VCOM DC Trim Function Control Register

VCOMDC Trim function control register, Write the follow command sequentially to enable the VCOMDC trim function.

Adjust VCDC level:

Set TRMEN[7:0] = 00h and set REGSEL=1(R0Bh=80h)

Write proper VCDC[5:0] value using 3-wire command.

Programming the VCDC value into MTP memory:

Set VPP_MTP = 7.5V with external power supply for programming operation. (Requirement)

Set TRMEN[7:0] as following sequence : A0h → 5Fh → EEh →00h

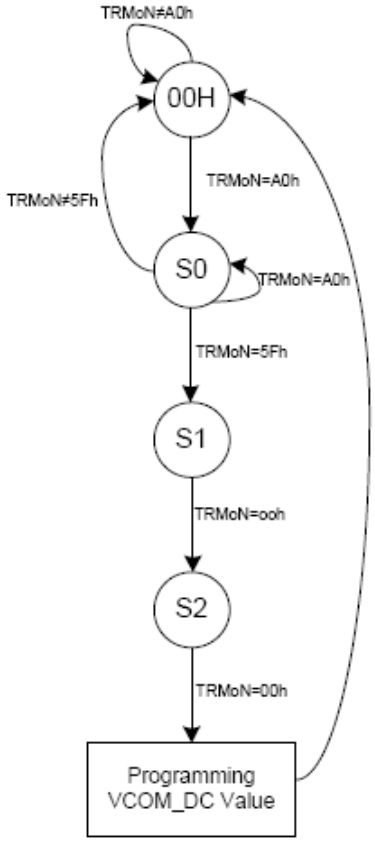
REGSEL will be clear to 0 after the programming procedure.

Procedure-1
Set RoGSoL = 1,
Please make sure VCDCoN=1

Procedure-2
Update VCDC vaule

Procedure-3
VCOMDC trim state please follow Note

Procedure-4
Handware clear RoGSoL=0, check RoGSoL =0 by 3-wire read check VCOMDC value



Note:

1. **The Trim Block can be writing for only "3" times**
2. **After finishing TRMEN command do not power off within 1 second.**
3. **Trim command exceed the limitation may cause the VCOMDC output unknown value.**
4. **The CLKIN input frequency should be 26MHz ~ 30MHz.**

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R16h	x	x	x	x	x	GOP_EN (1)	x	x

GON_EN (R16h): Select auto or manual gamma setting

D2	Gamma op enable Function
0	Manual set gamma by R17h~R1Ah.
1	Auto set to gamma2.2. (**default**)

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R17h	x	L016P_SEL (101)			x	L008P_SEL (100)		
R18h	x	L50P_SEL (101)			x	L032P_SEL (100)		
R19h	x	L096P_SEL (100)			x	L072P_SEL (011)		
R1Ah	x	L120P_SEL (101)			x	L110P_SEL (100)		

Registers : R17h ~R1Ah

L008P_SEL: Gamma op output selection to level VP8;

L016P_SEL: Gamma op output selection to level VP16;

L032P_SEL: Gamma op output selection to level VP32;

L050P_SEL: Gamma op output selection to level VP50;

L072P_SEL: Gamma op output selection to level VP72;

L096P_SEL: Gamma op output selection to level VP96;

L110P_SEL: Gamma op output selection to level VP110;

L120P_SEL: Gamma op output selection to level VP120;

Reference point	000	001	010	011	100	101	110	111
L008P(100)	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
L016P(101)	-5△V	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V
L032P(100)	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
L050P(101)	-5△V	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V
L072P(011)	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V	+4△V
L096P(100)	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
L110P(100)	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
L120P(101)	-5△V	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V

Note:(1) For Low Voltage LC application, △V= 25mV。

(2) For Normal Voltage LC application, △V= 40mV。

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R2Bh	x	x	x	x	x	x	x	STB (0)

STB(R2Bh[0]): Standby (Power saving) mode control

D0	STB Function
0	Standby Mode. (**default**)
1	Normal operation.

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R2Fh	x	VGH_SEL (11)		CF_SEL (0)	LC_SEL (00)		SPOC (01)	

SOPC (R2Fh[1:0]): Source output driving capability selection

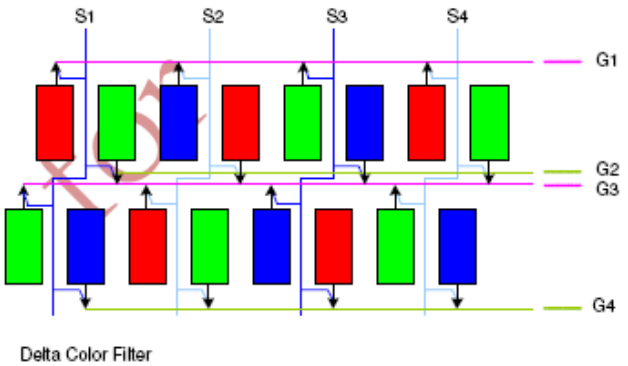
D1	D0	Source Driver Capability
0	0	-25%.
0	1	Normal. (**default**)
1	0	+25%
1	1	+50%

LC_SEL (R2Fh[3:2]): Source output driving capability selection

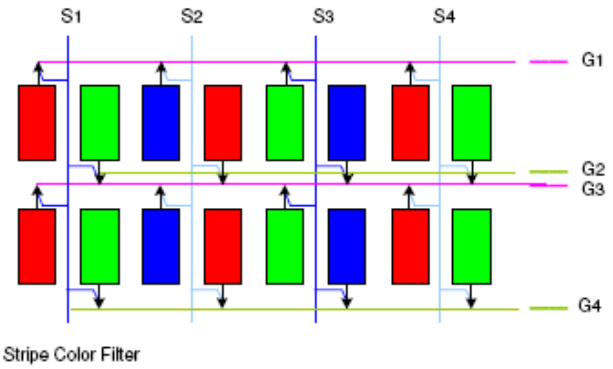
D3	D2	LC type selection
0	0	Low Voltage LC (**default**)
0	1	-
1	0	Normal Voltage LC 2
1	1	Normal Voltage LC 1

CF_SEL(R2Fh[4]): Color filter selection

D4	Function
0	Delta color filter. (**default**)
1	Stripe color filter.



Delta Color Filter



Stripe Color Filter

VGH_SEL(R2Fh[6:5]): VGH voltage level selection

D6	D5	VGH Voltage
0	0	|VGL| + 2V.
0	1	|VGL| + 3V.
1	0	|VGL| + 4V.
1	1	|VGL| + 5V. (**default**)

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R3Ch	GAMMA_EN (0)	L127P_SEL (011)			X	L000P_SEL (100)		

GAMMA_EN: Gamma Reference Point Control Enable

D7	GAMMA_EN Function
0	VN reference point control setting follow VP (**default**)
1	VP / VN Reference point control independently

L127P_SEL: Gamma op output selection to level VP127;

L000P_SEL: Gamma op output selection to level VP000;

Reference point	000	001	010	011	100	101	110	111
L000P(100)	-4△V	-3△V	-2△V	-1△V	Default	+1△V	+2△V	+3△V
L127P(011)	-3△V	-2△V	-1△V	Default	+1△V	+2△V	+3△V	+4△V

Note:(1) For Low Voltage LC application, △V= 25mV。

(2) For Normal Voltage LC application, △V= 40mV。

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R3Dh	X	L127N_SEL (011)			X	L000N_SEL (111)		
R3Eh	X	L016N_SEL (101)			X	L008N_SEL (100)		
R3Fh	X	L050N_SEL (101)			X	L032N_SEL (100)		
R40h	X	L096N_SEL (100)			X	L072N_SEL (011)		
R41h	X	L120N_SEL (101)			X	L110N_SEL (100)		

L127N_SEL: Gamma op output selection to level VN127;

L000N_SEL: Gamma op output selection to level VN000;

L016N_SEL: Gamma op output selection to level VN16;

L008N_SEL: Gamma op output selection to level VN8;

L050N_SEL: Gamma op output selection to level VN50;

L032N_SEL: Gamma op output selection to level VN32;

L096N_SEL: Gamma op output selection to level VN96;

L072N_SEL: Gamma op output selection to level VN72;

L120N_SEL: Gamma op output selection to level VN120;

L110N_SEL: Gamma op output selection to level VN110;

Reference point	000	001	010	011	100	101	110	111
L000N(000)	+7△V	+6△V	+5△V	+4△V	+3△V	+2△V	+1△V	Default
L008N(100)	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
L016N(101)	-5△V	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V
L032N(100)	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
L050N(101)	-5△V	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V
L072N(011)	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V	+4△V
L096N(100)	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
L110N(100)	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V	+3△V
L120N(101)	-5△V	-4△V	-3△V	-2△V	-△V	Default	+△V	+2△V

Note:(1) For Low Voltage LC application, △V= 25mV。

(2) For Normal Voltage LC application, △V= 40mV。

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R55h	x	INV_SEL (0)	DAT_INV (0)	x	x	x	x	x

DAT_INV (R55h[5]): Source output Inversion control

D5	DAT_INV Function
0	Data output normal. (**default**)
1	Data output inversion.

INV_SEL (R55h[6]): Inversion selection

D6	INV_SEL Function
0	One line inversion. (**default**)
1	Column inversion.

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R57h	VGHL_ENB (0)	x	x	x	x	x	x	x

VGHL_ENB (R57h[7]): VGH/VGL charge pump control

D7	VGHL_ENB Function
0	VGH/VGL charge pump enable. (**default**)
1	VGH/VGL charge pump enable,for external VGH/VGL application.

*Note: don't apply external power to VGH and VGL pad when VGHL_EN=0 and VGHL_ENB=0.

Register	Parameter Data							
	D7	D6	D5	D4	D3	D2	D1	D0
R5Ah	x	x	x	x	x	x	VGL_SEL (10)	

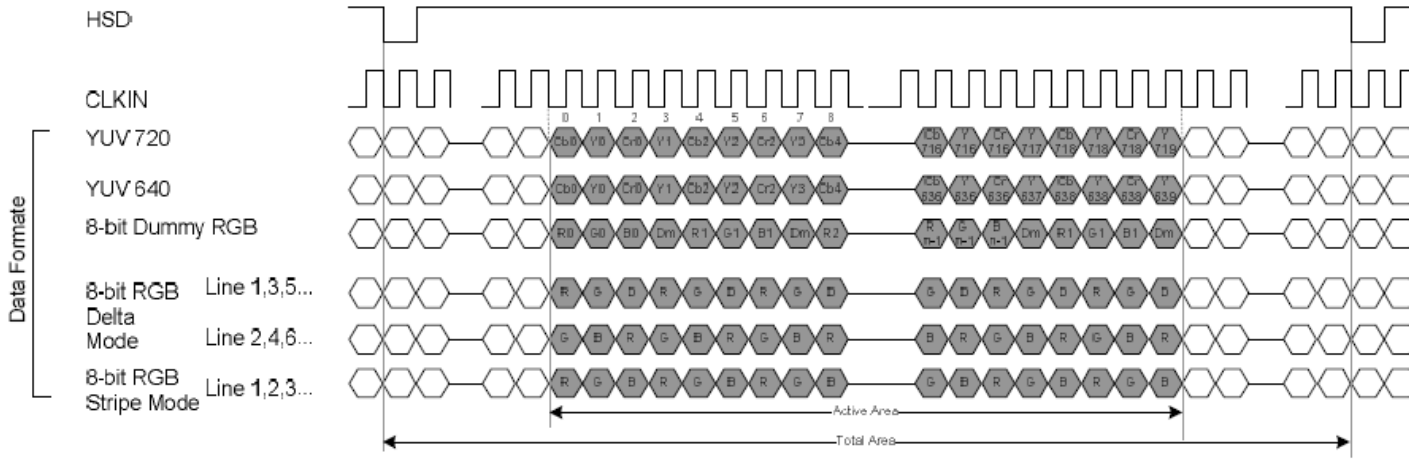
VGL_SEL (R5Ah[1:0]): VGL voltage level selection

D1	D0	VGL Voltage
0	0	-8V
0	1	-9V
1	0	-10V (**default**)
1	1	-11V

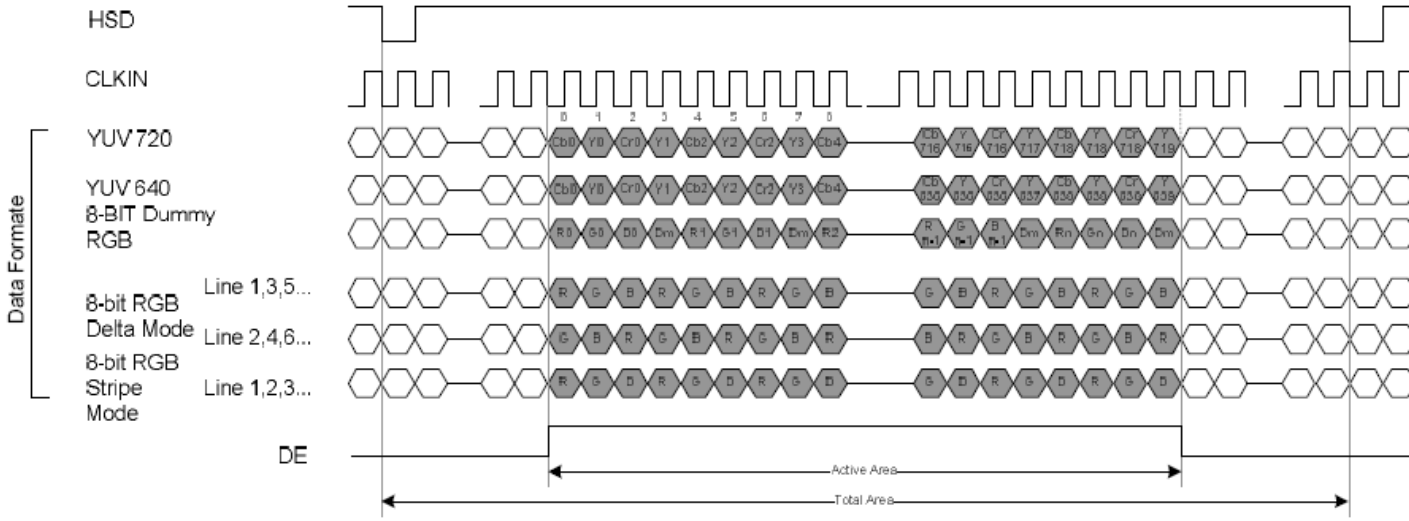
5.4 DATA INPUT FORMAT

Serial 8-bit RGB / 8-bit Dummy RGB / YUV Mode Data format

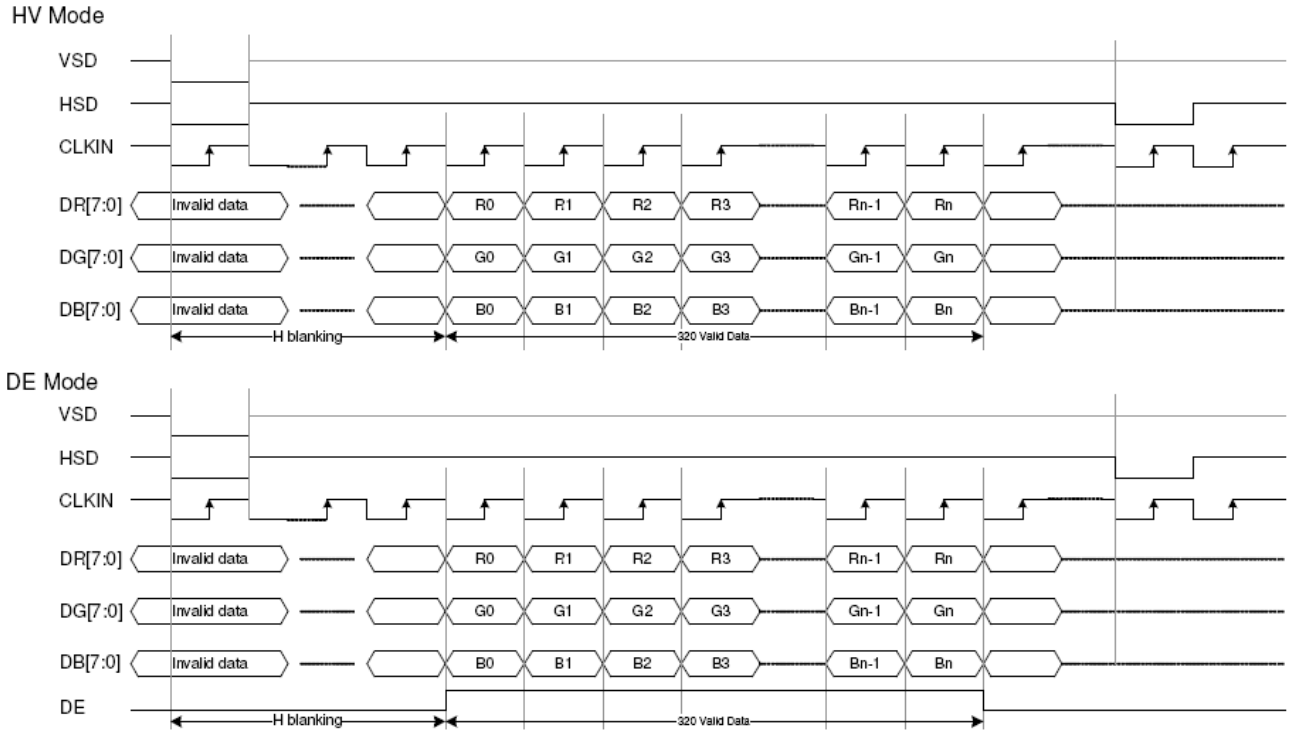
HV Mode



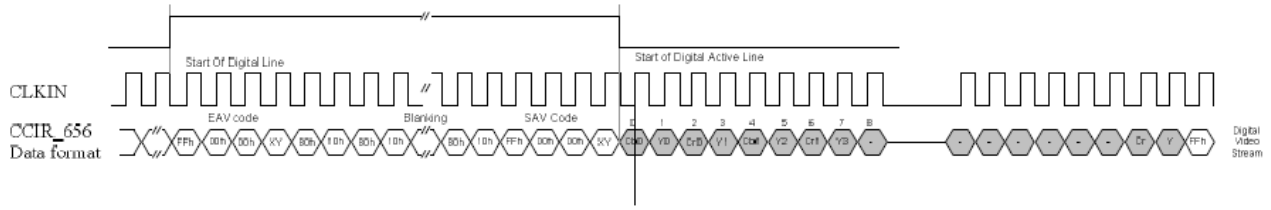
DE Mode



Parallel RGB Mode Data Format



CCIR_656 Mode Data format



- FF 00 00 XY signals are involoved with HSD, VSD and Field.
- XY encode following bits:

  F = field select

  V = indicate vertical blanking

  H = 1, if EAV else 0 for SAV

  P3-P0 = protection bits:

  P3 = V⊕H P2=F⊕H P1=F⊕V P0=F⊕V⊕H ⊕:Represents the exclusive-OR function.

XY							
D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	F	V	H	P3	P2	P1	P0

- Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.
- Horizontal blanking section cosists of repeating pattern 80 10 80 10

Data Active Area

Input Format	Format Standard	CLKIN(MHz)	H	Total AREA	Active AREA
YUV	CCIR_601	fCLKIN = 27	1	1716	1440
	CCIR_656			1728	
	CCIR_601	fCLKIN = 24.54	1	1560	1280
8-bit Dummy RGB	NTSC/PAL	fCLKIN = 27	1	1560	1440
		fCLKIN = 24.54		1560	1280
8-bit RGB	NTSC	fCLKIN = 27	1	1716	960
24bit RGB	320RGB x 240	fCLKIN =6.4	1	390	320 (RGB)

(Unit:CLKIN)

CCIR656/YUV640/YUV720 to RGB Conversion Formula

$R_n = 1.164*[(Y_{2n-1}+Y_{2n})/2-16] + 1.596*(Cr_n-128)$

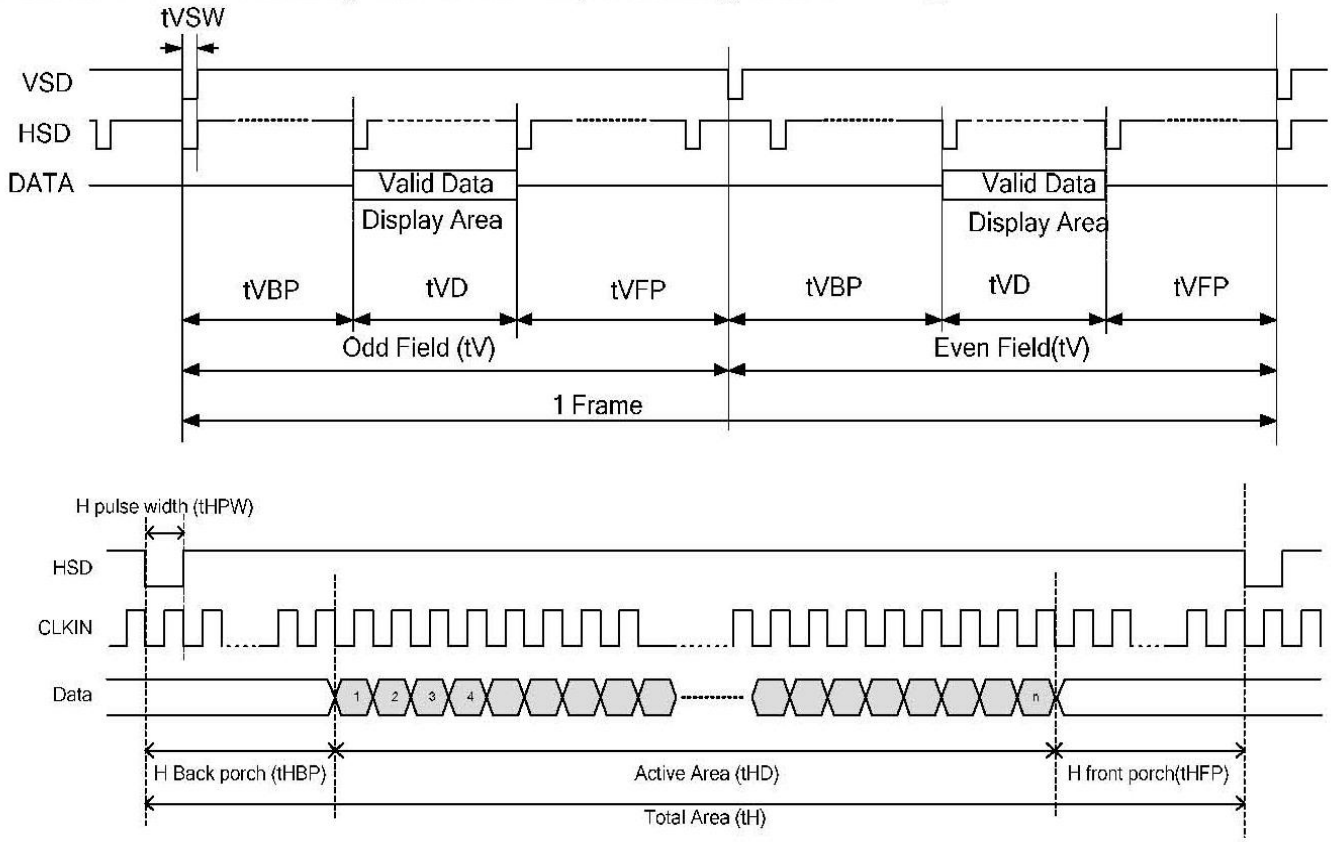
$G_n = 1.164*[(Y_{2n-1}-1+Y_{2n})/2-16] - 0.813*(Cr_n-128) – 0.392*(Cb_n-128)$

$B_n = 1.164*[(Y_{2n-1}+Y_{2n})/2-16] + 2.017*(Cb_n-128)$

Where Y: 16~235 Cr: 16~240 Cb: 16~240

5.5 INPUT TIMING FORMAT

8-bit RGB/8-bit Dummy RGB/YUV Input timing chart



8-bit RGB input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	13.5	27	27.19	MHz
HSD period		tH	1024	1716	1728	CLKIN
HSD display period		tHD		960		CLKIN
HSD back porch		tHBP	50	70	255	CLKIN
HSD front porch		tHFP	14	686	718	CLKIN
HSD pulse width		tHSW	1	1	tHBP-1	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1 CLKIN	1CLKIN	6H	
1 Frame			485	525	901	H

8-bit Dummy RGB input timing

8-bit Dummy RGB (320 mode/NTSC/24.535Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.535	30	MHz
HSD period		tH	1306	1560	1907	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	372	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

8-bit Dummy RGB (320 mode/PAL/24.375Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.375	30	MHz
HSD period		tH	1306	1560	1920	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	385	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

8-bit Dummy RGB (360 mode/NTSC/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1716	1907	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	35	212	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

8-bit Dummy RGB (360 mode/PAL/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1728	1920	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	47	225	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD Front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

YUV720 and YUV640 input timing

YUV 720 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1716	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	36	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	525	-	H

YUV 720 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1728	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	48	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	625	-	H

YUV 640 mode/NTSC input timing

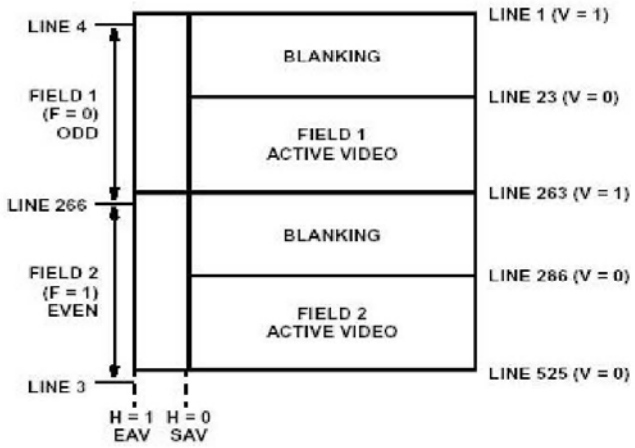
Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.535	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	525	-	H

YUV 640 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.375	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	625	-	H

CCIR656 input timing

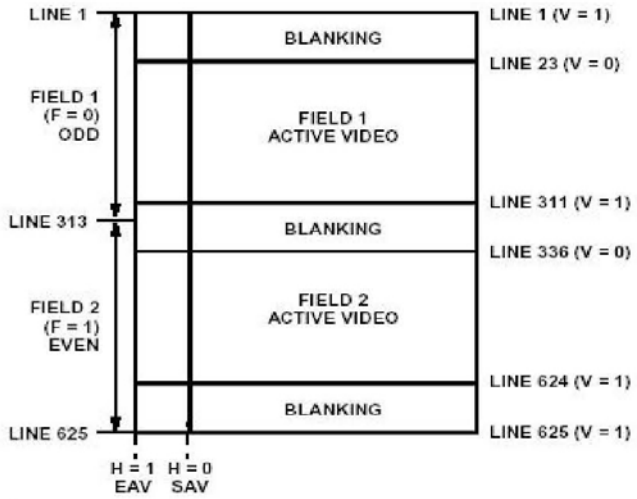
NTSC mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

PAL mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

5.6 AC ELECTRICAL CHARACTERISTICS

(VDD=3.0~3.6V, VDDIO=AVDD=VDD, AGND=GND=0V, TA=25°C)

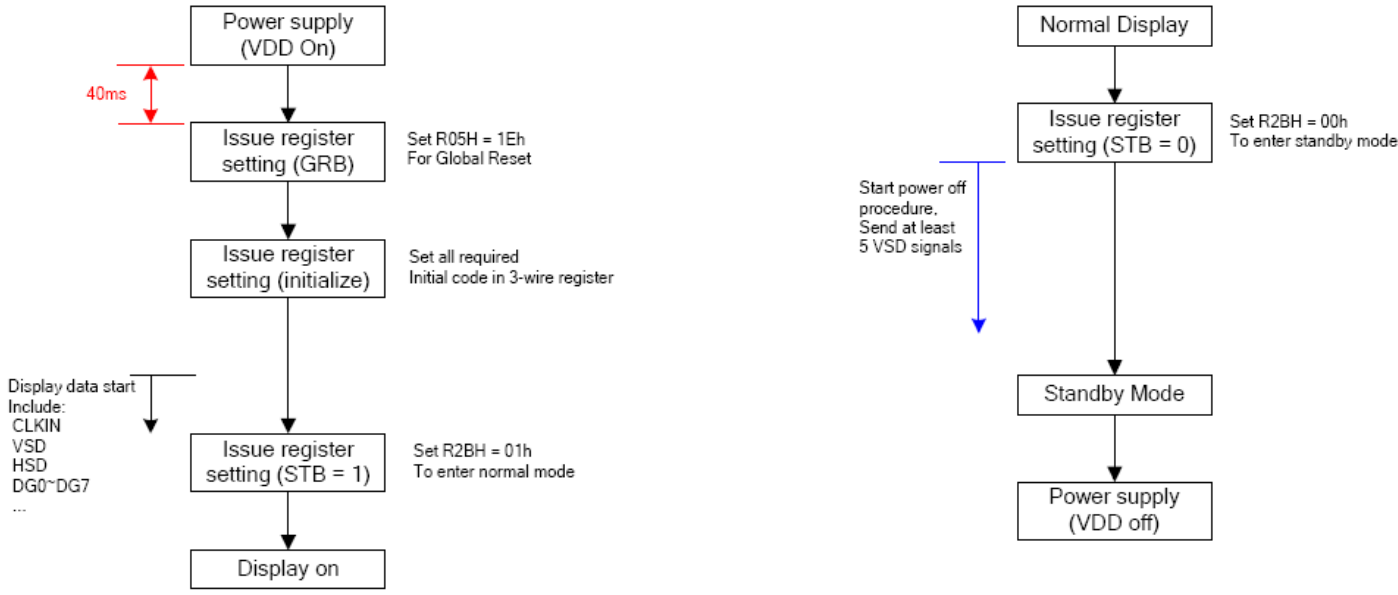
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
HSD period time	Th	60	63.56	67	us	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	DB0~DB7 to CLKIN
Data hold time	Tdhd	12	-	-	ns	DB0~DB7 to CLKIN
Time that VSD to 1st Gate output	Tstv	0	21	31	H	@ 8-bit RGB, 8-bit Dummy RGB NTSC, Delay by VBLK setting.
Time that CCIR_V to 1st Gate output	Tstv	0	22	31	H	@ CCIR656 NTSC, Delay by VBLK setting.
Time that CCIR_V to 1st Gate output	Tstv	3	24	34	H	@ 8-bit Dummy RGB & CCIR656 PAL, Delay by VBLK setting.
Source output setting time (*1)	Tst	-	-	8	us	R= 25K ohm , C= 30 pF 10% → 90% final.
Gate output setting time (*1)	Tstg	-	0.5	1	us	R= 3K ohm , C= 25 pF 10% → 90% final.
VCOM setting time (*1)	Tst,vcom	-	-	9	us	R= 200 ohm , C= 5 nF 10% → 90% final.
Time that HSD width	Twh	1	-	-	CLKIN	

Ps. (*1) Test Condition:

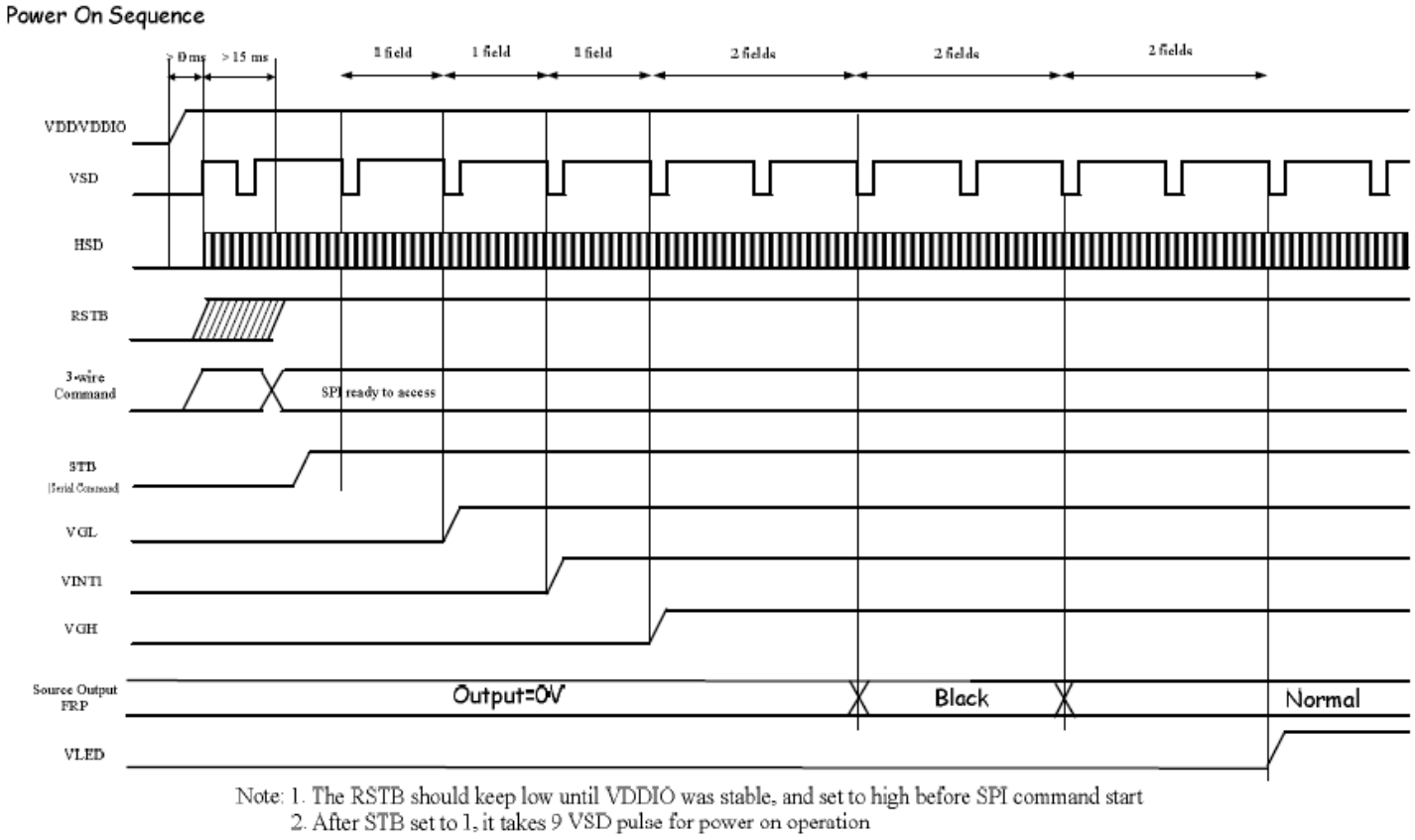
When the tested signal is changed from Vo, min to Vo,max, the time that is from the start of change to the time that the swing voltage at point B is less than +/- 20 mV is called the setting time of the tested signal.

6 Power On/Off Sequence

6.1 INITIALIZE FLOW CHART



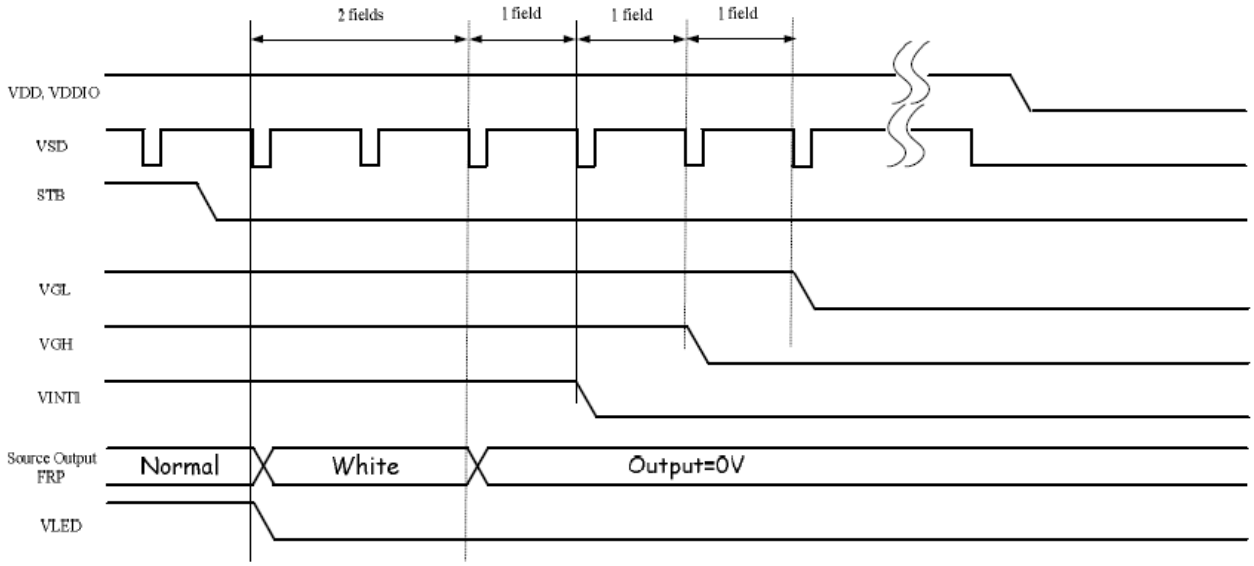
6.2 POWER ON SEQUENCE



Note: 1. The RSTB should keep low until VDDIO was stable, and set to high before SPI command start
2. After STB set to 1, it takes 9 VSD pulse for power on operation

6.3 POWER OFF SEQUENCE

Power Off Sequence



7 Optical Characteristics

7.1 Optical Specification

Ta=25℃

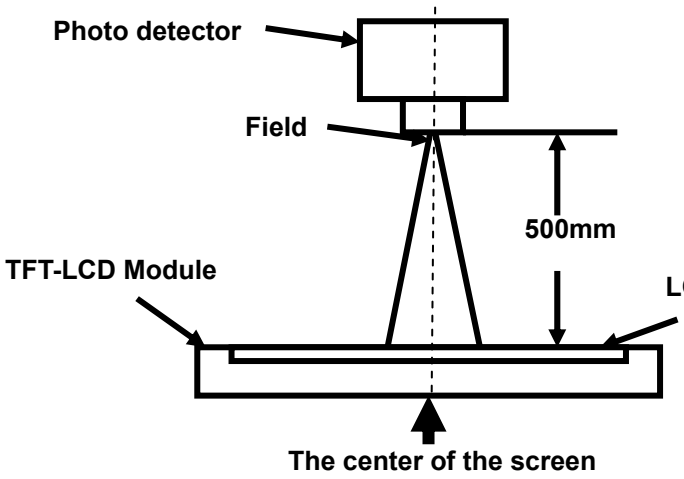
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	15	20	-	Degree	Note 2
		θB		45	50	-		
		θL		40	45	-		
		θR		40	45	-		
Contrast Ratio		CR	θ=0°	250	350	-		Note1 Note3
Response Time		Ton	25℃	-	25	45	ms	Note1 Note4
		Toff						
Chromaticity	White	x	Backlight is on	0.256	0.306	0.356		Note5, Note1
		y		0.276	0.326	0.376		
	Red	x		0.528	0.578	0.628		
		y		0.290	0.340	0.390		
	Green	x		0.297	0.347	0.397		
		y		0.289	0.539	0.589		
	Blue	x		0.101	0.151	0.201		
		y		0.057	0.107	0.157		
Uniformity		U	-	75	80	-	%	Note1 Note6
NTSC		-	-	-	40	-	%	Note 5
Luminance		L	-	200	250	-	cd/m^2	Note1 Note7

Test Conditions:

1. V_F=3.2V, I_F=25mA (Backlight Current), the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。

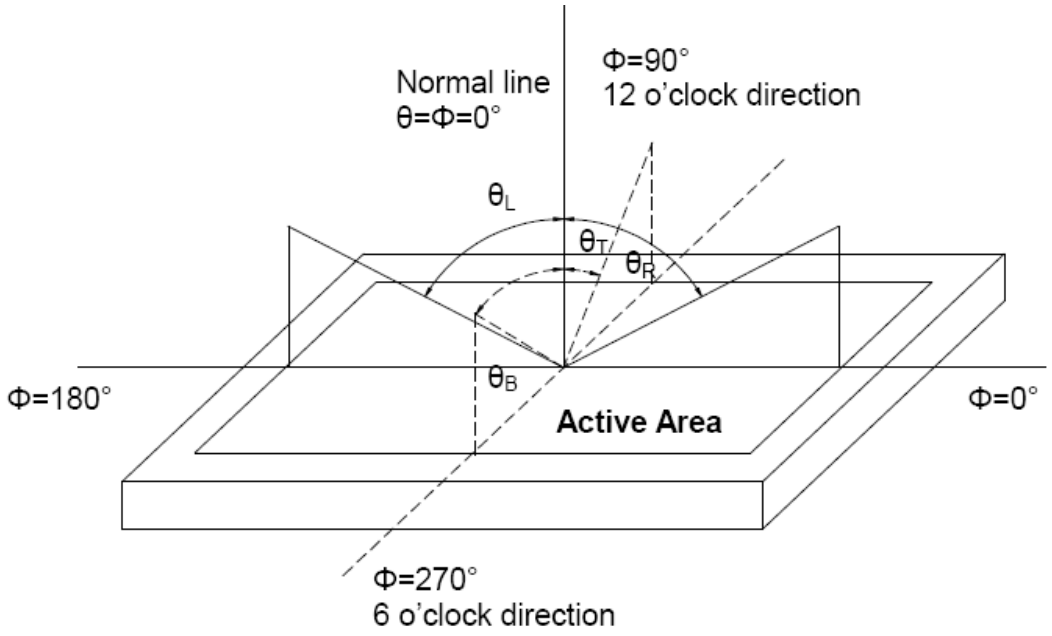


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

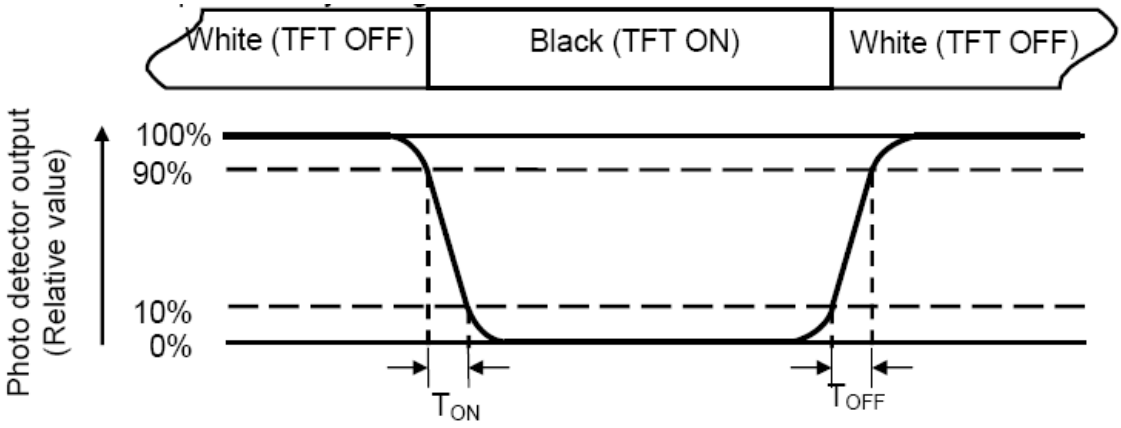
“White state “:The state is that the LCD should driven by Vwhite.

“Black state”: The state is that the LCD should driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin / Lmax

L-------Active area length W----- Active area width

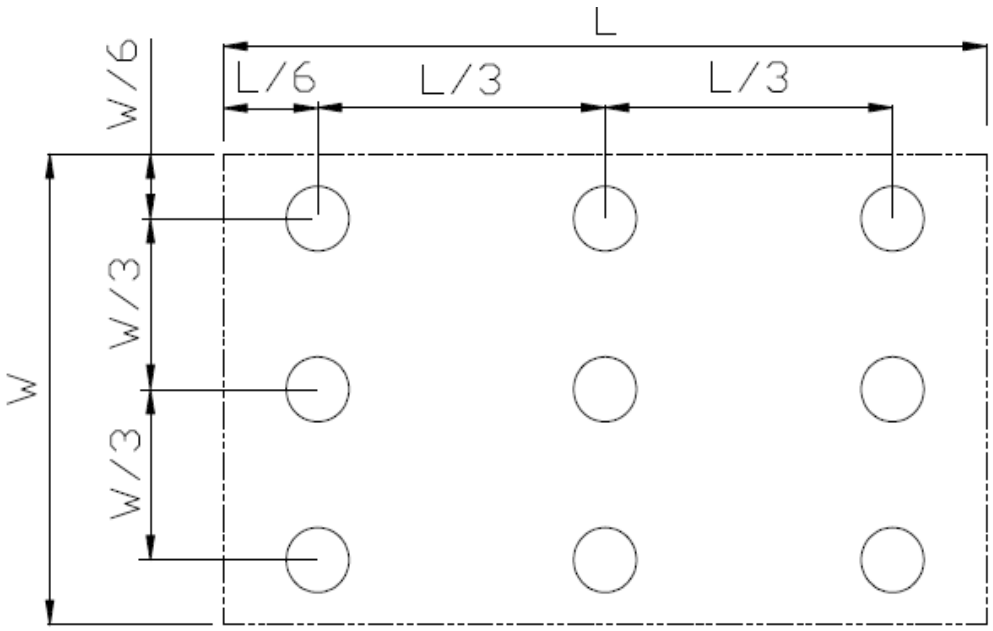


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

8 Environmental / Reliability Tests

No	Test Item	Condition	Remark
1	High Temperature Operation	Ts=+70℃, 240hrs	Note1 IEC60068-2-2,GB2423.2—89
2	Low Temperature Operation	Ta=-20℃, 240hrs	IEC60068-2-1 GB2423.1—89
3	High Temperature Storage	Ta=+80℃, 240hrs	IEC60068-2-2, GB2423.2—89
4	Low Temperature Storage	Ta=-30℃, 240hrs	IEC60068-2-1 GB2423.1—89
5	High Temperature & High Humidity Storage	Ta=+60℃, 90% RH 240 hours	Note2 IEC60068-2-3, GB/T2423.3—2006
6	Thermal Shock (Non-operation)	-30℃ 30 min~+70℃ 30 min, Change time:5min, 20 Cycles	Start with cold temperature, End with high temperature, IEC60068-2-14,GB2423.22—87
7	Electro Static Discharge (Operation)	C=150pF, R=330Ω,5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times; (Environment: 15℃～35℃, 30%～60%, 86Kpa～106Kpa)	IEC61000-4-2 GB/T17626.2—1998
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition)	IEC60068-2-6 GB/T2423.10—1995
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	IEC60068-2-27 GB/T2423.5—1995
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8—1995
11	Cell gap strength	30kgf 2 second add press【1point】 speed:1mm/min Check it after ten minutes	Note3

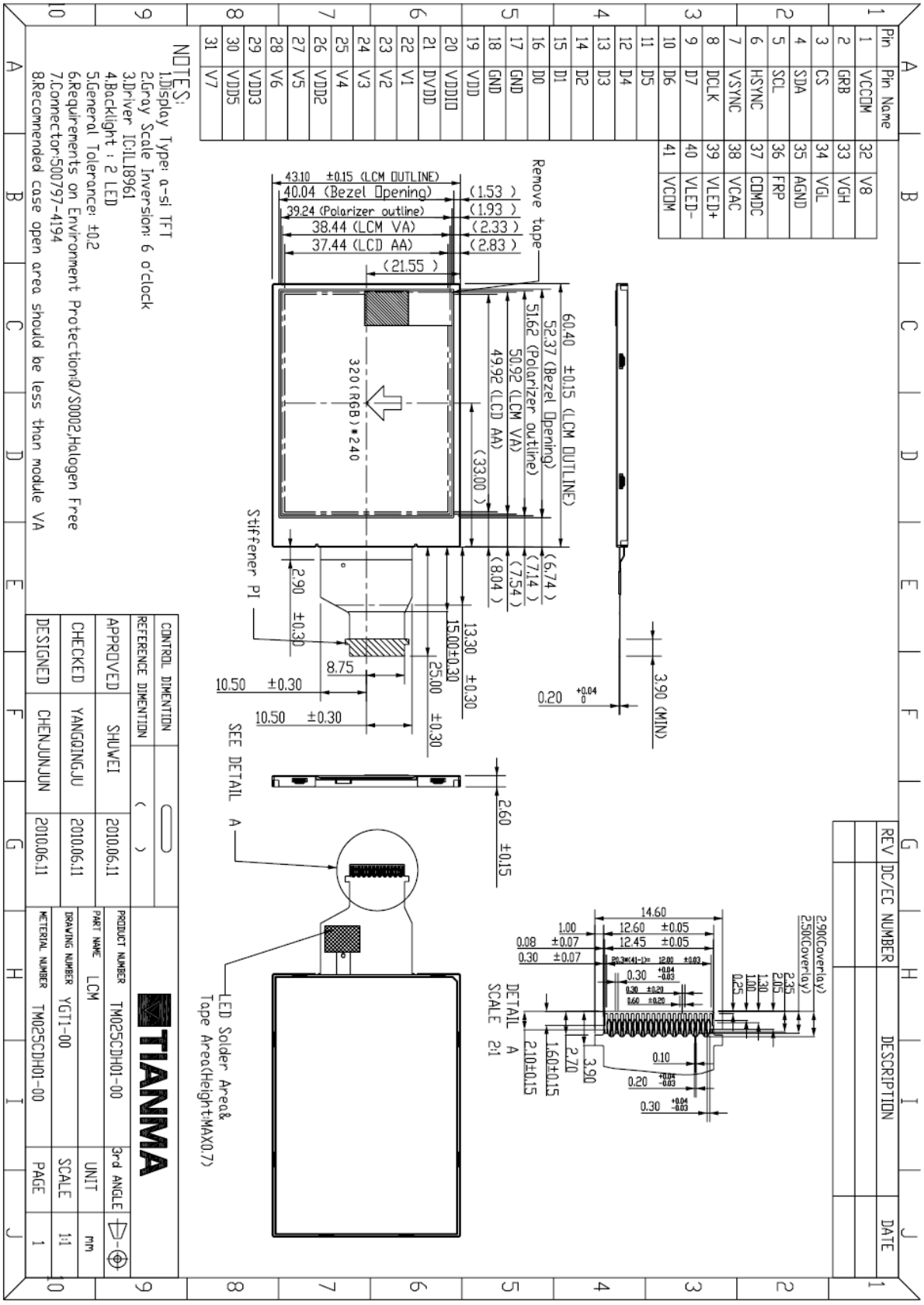
Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

Note3: ① limit sample which SDC provided to TM as baseline

② Customer Inspection pattern： dynamic pattern after powering on display without push Mura，it can pass

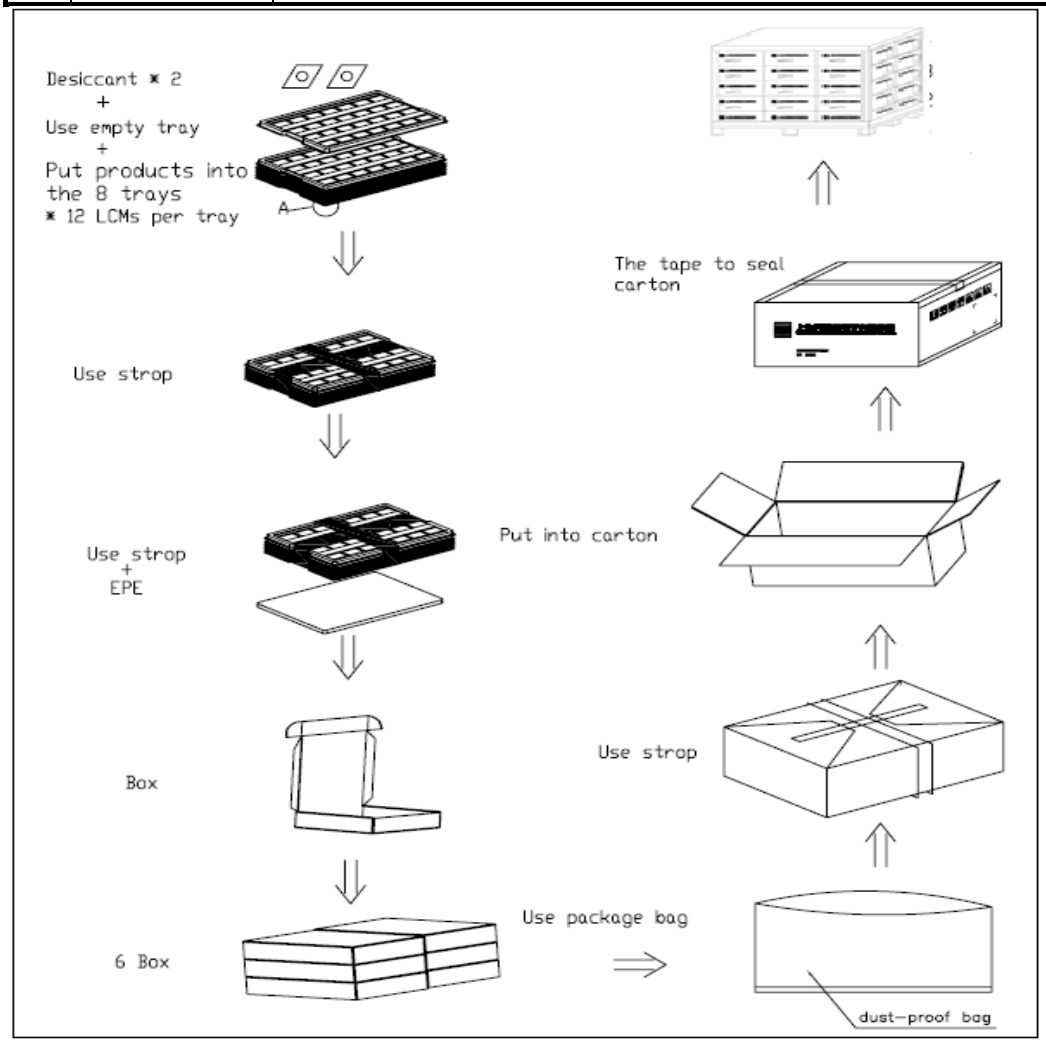
9 Mechanical Drawing



10 Packing Drawing

10.1 Packaging Material Table

No	Item	Model (Material)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	LCM module	TM025CDH01	60.40x43.10x2.60	TBD	576	
2	Tray	PET(Transmit)	315×247×11.3	TBD	54	Anti-static
3	EPE	EPE	315×247×5	0.009	6	
4	Desiccant	Desiccant	45x50	0.002	12	
5	Anti-static bag	PE	700x545	0.046	1	
6	Box	Corrugated Paper	345x260x70	0.227	6	
7	Carton	Corrugated Paper	544x365x250	1.01	1	
8	Total weight(Kg)	TBD				



11 Precautions For Use of LCD Modules

11.1 Handling Precautions

11.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

11.1.6 Do not attempt to disassemble the LCD Module.

11.1.7 If the logic circuit power is off, do not apply the input signals.

11.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1 Be sure to ground the body when handling the LCD Modules.

11.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage precautions

11.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature: 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions:

The LCD modules should be no falling and violent shocking during transportation, and also

should avoid excessive press, water, damp and sunshine.