TIANMA
Microelectronics Co.,LTD

SPECIFICATION FOR TFT LCD MODULE

MODEL NO:	TM028HDZ30
CUSTOMER:	TME
CUSTOMER P/N.	
VERSION	V1.0
CUSTOMER APPROVED	

□ Preliminary Specification

■ Final Specification

PREPARED	CHECKED	VERIFIED BY QA DEPT	VERIFIED BY R&D DEPT

TIANMA MICRO-ELECTRONICS CO., LTD
Address: 8F, 64th Building, Jinlong, Majialong Industrial Area, Nanshan District, Shenzhen, China Tel: +86-755-2609-4288 Fax: +86-755-8622-5774 +86-755-8622-5772
Web: www.tianma.cn www.tianma.com

REVISION RECORD

Date	Rev.No.	Page	Revision Items	Prepared
2011.4.1	**V1.0**		**The first release**	YL

CONTENTS

Page

1. General Specifications

TM028HDZ30 is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver IC, FPC and a back light unit. The 2.8″ display area contains 240 x 320 pixels and can display up to 262K colors. This product accords with RoHS environmental criterion.

Item	Contents	Unit	Note
LCD Type	a-si TFT	-	
Display Color	65K/262K		1
LCD Duty	1/320	-	
Viewing Direction	6:00	O'Clock	
Active Area(W×H)	43.20×57.60	mm	
Number of Dots	240(RGB)×320	mm	
Dot Pitch(W×H)	0.180X0.180	mm	
Controller	ILI9335B	-	
V_{cc}	2.8	V	
I_{OVCC}	1.8/2.8	V	
Outline Dimensions	Refer to outline drawing on next page		
Backlight	4-LEDs(white parallel)	-	
Weight	17.4	g	
Interface	CPU 8/16 bits	-	
Polarizer Mode	Transmissive/Positive	-	

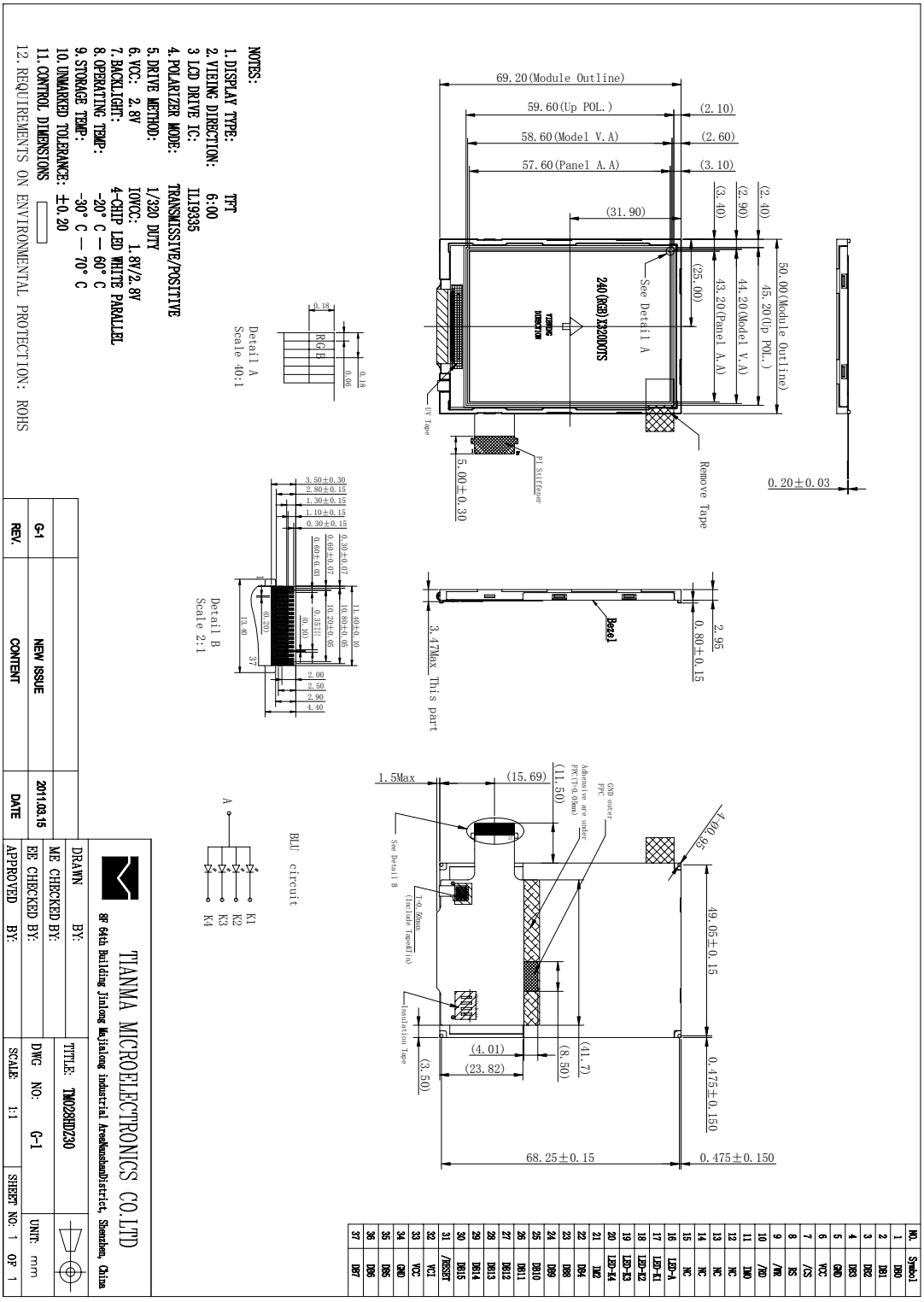
Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: Requirements on Environmental Protection:RoHS

Note 3: Customer should do assembly according to our FPC bending sketch in the outline drawing.

Note 4: Please approve our spec before placing mass production order. Otherwise we will regard customer has approved the spec when we receive the first 2Kpcs or above order from customer.

2. Outline Drawing

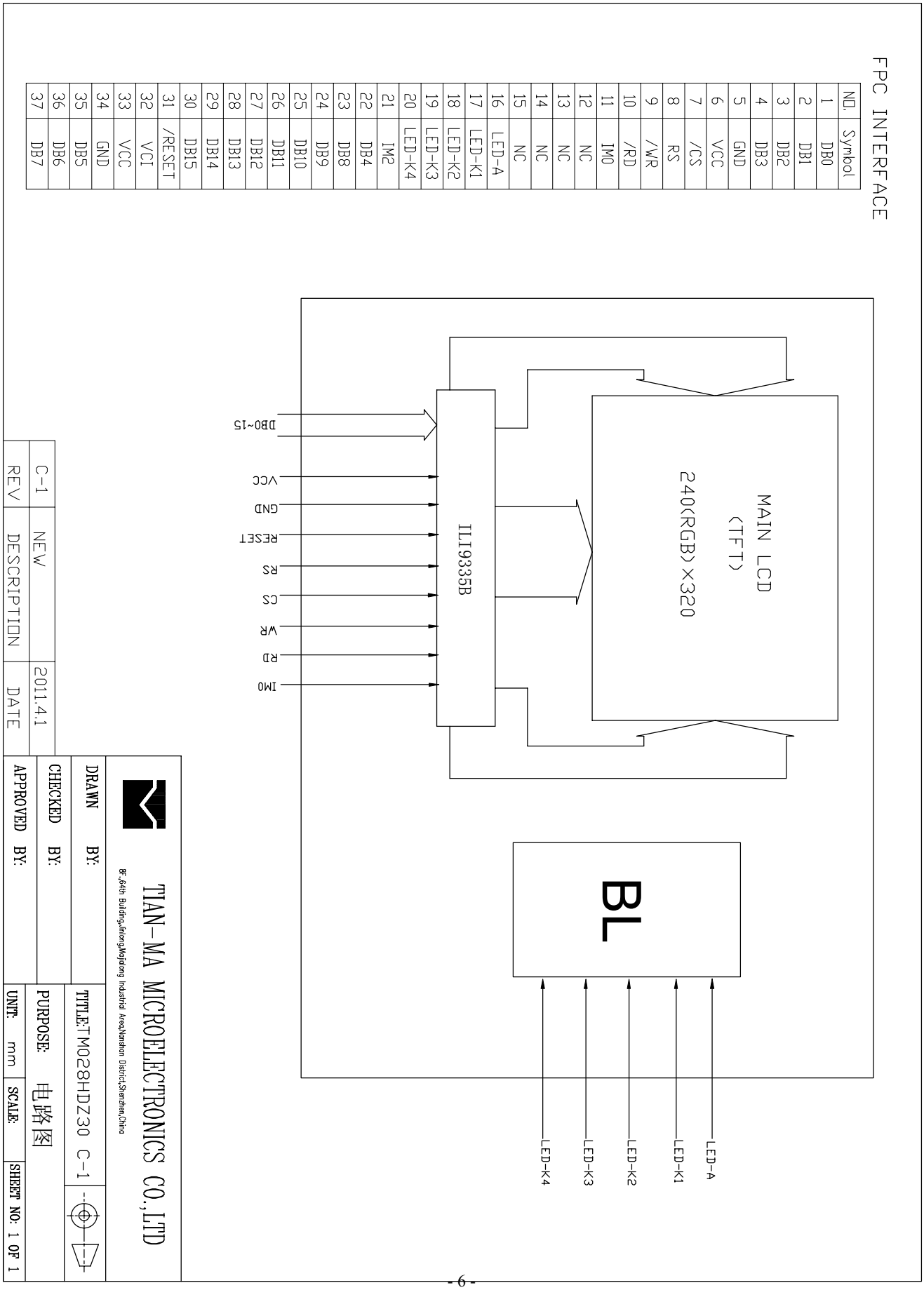


NO.	Symbol
1	DB0
2	DB1
3	DB2
4	DB3
5	GND
6	VCC
7	/CS
8	RS
9	/WR
10	/RD
11	IM0
12	NC
13	NC
14	NC
15	NC
16	LED-A
17	LED-K1
18	LED-K2
19	LED-K3
20	LED-K4
21	IM2
22	DB4
23	DB9
24	DB9
25	DB10
26	DB11
27	DB12
28	DB13
29	DB14
30	DB15
31	/RESET
32	VCI
33	VCC
34	GND
35	DB5
36	DB6
37	DB7

NOTE 1: FPC,BL,TP etc. may have not only one provider, appearance, silk-screen may exist difference.

NOTE 2: Customer's rind(handset rind etc.) and TIANMA's standard module may exist interference , Customer should advise on TIANM FAE or RD change rind.

3. Circuit Block Diagram



4. Absolute Maximum Ratings(Ta=25℃)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{CC}	-0.3	4.6	V	1，2
Logic Signal Input /Output Voltage	IOVCC	-0.3	4.6	V	
Operating Temperature	Top	-20	+60	℃	
Storage Temperature	Tst	-30	+70	℃	

Notes:

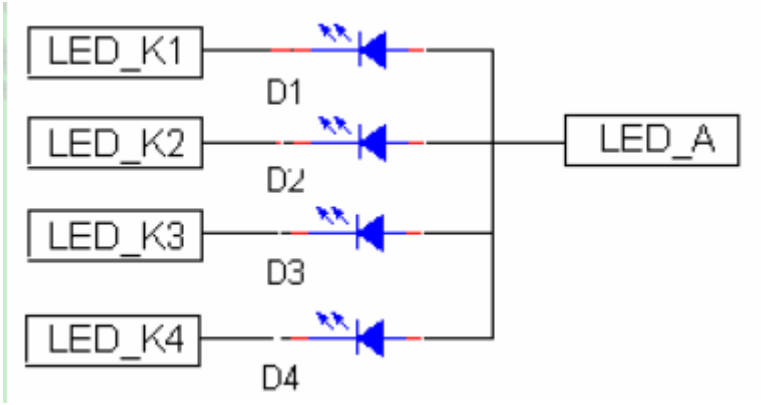
1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. V_{DD} >V_{SS} must be maintained.

5. Electrical Specifications and Instruction Code

5.1 Electrical characteristics(Vss=0V ,Ta=25℃)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Input voltage	'H'	V_{IH}	IOVCC =1.65~3.6V	0.8 IOVCC	-	IOVCC	V	
	'L'	V_{IL}	IOVCC =1.65~3.6V	-0.3	-	0.2 IOVCC	V	
Output Voltage	'H'	V_{OH}	I_{OH} = -0.1 mA	0.8 IOVCC	-	-	V	
	'L'	V_{OL}	IOVCC=1.65 ~3.6V	-	-	0.2 IOVCC	V	

5.2 LED backlight specification(Vss=0V ,Ta=25℃)



Item	Symbol	Min	Typ	Max	Unit	Condition	Note
Forward Voltage	V_F	2.9	3.2	3.5	V	If=80mA	
Luminance(9 point avg.)	L_a	3800	-	-	Cd/m^2	VR=5V	
Luminance Center	L_c	4200	4800	-	Cd/m^2	1. If=20mA/LED 2. Aper ture:9 point 3. instrument is :BM-7A 4. Uniformity=min/max*100%	
Uniformity		80	-	-	%		
Color Coordinate	X	0.25	0.28	0.31			
	Y	0.24	0.27	0.30			

5.3 Interface Signals

Pin No.	Symbol	I/O	Description	Comment
1	D0	I/O	Data input	
2	D1	I/O	Data input	
3	D2	I/O	Data input	
4	D3	I/O	Data input	
5	GND	P	Ground	
6	VCC	P	Power Supply	
7	CS	I	Chip select signal(active low)	
8	RS	I	Register select signal. Low: select an index or status register High: select a control register	
9	WR	I	Write execution control pin	
10	RD	I	Read execution control pin	
11	IM0	I	Mode selection	Note 1
12	NC	-		
13	NC	-		
14	NC	-		
15	NC	-		
16	LED-A	P	LED anode	
17	LED-K1	P	LED cathode	
18	LED-K2	P	LED cathode	
19	LED-K3	P	LED cathode	
20	LED-K4	P	LED cathode	
21	IM2	I	Mode Selection(connect to GND)	
22	D4	I/O	Data input	
23	D8	I/O	Data input	
24	D9	I/O	Data input	
25	D10	I/O	Data input	
26	D11	I/O	Data input	
27	D12	I/O	Data input	
28	D13	I/O	Data input	
29	D14	I/O	Data input	
30	D15	I/O	Data input	
31	RESET	I	Reset pin(active at low)	
32	VCI	P	Analog power supply	
33	VCC	P	Logic power supply	
34	GND	P	Ground	
35	D5	I/O	Data input	
36	D6	I/O	Data input	
37	D7	I/O	Data input	

Note 1:

IM0	MCU Interface Mode	Data bus
0	16 bit	DB[15:0]
1	8 bit	DB[15:8]

5.4 Interface Timing Chart

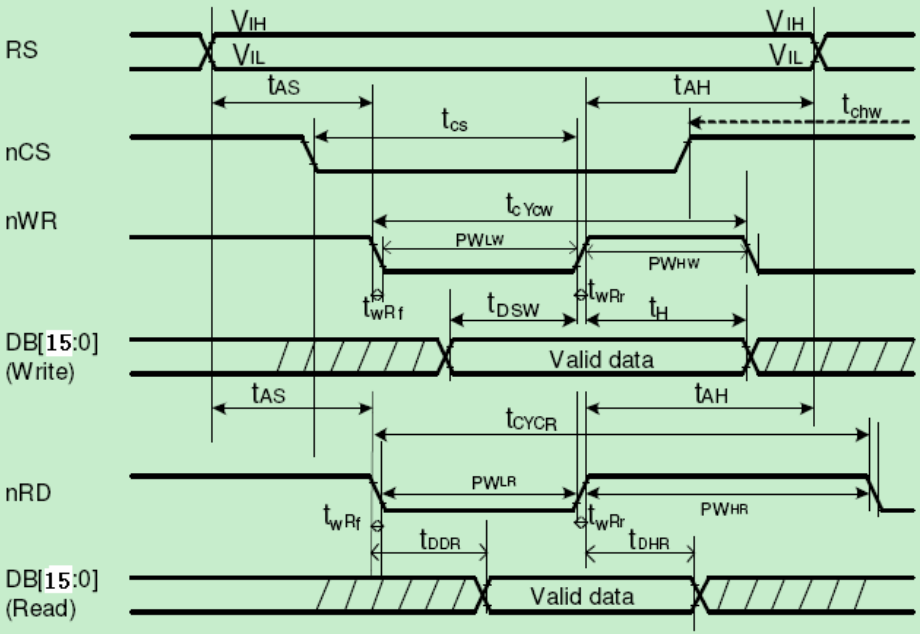
Note: Please refer to ILITEK's ILI9335B data sheet for more details.

ILITEK's ILI9335B interface protocol

5.4.1 Interface Timing Parameters && Interface Characteristics

Normal Write Mode (IOVCC = 1.65~3.6V)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	(75)	-		-
	Read	t_{CYCR}	ns	300	-	-	-
Write low-level pulse width		PW_{LW}	ns	(40)	-	500	-
Write high-level pulse width		PW_{HW}	ns	(30)	-	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	-	
nCS/ RS/ DB Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	-	25	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	-	
	Read (RS to nCS, RW/nRD)			5	-	-	
Address hold time		t_{AH}	ns	5	-	-	
Write data set up time		t_{DSW}	ns	10	-	-	
Write data hold time		t_H	ns	15	-	-	
Read data delay time		t_{DDR}	ns	-	-	100	
Read data hold time		t_{DHR}	ns	5	-	-	



5.4.2 Instruction Description (ILITEK's ILI9335B)

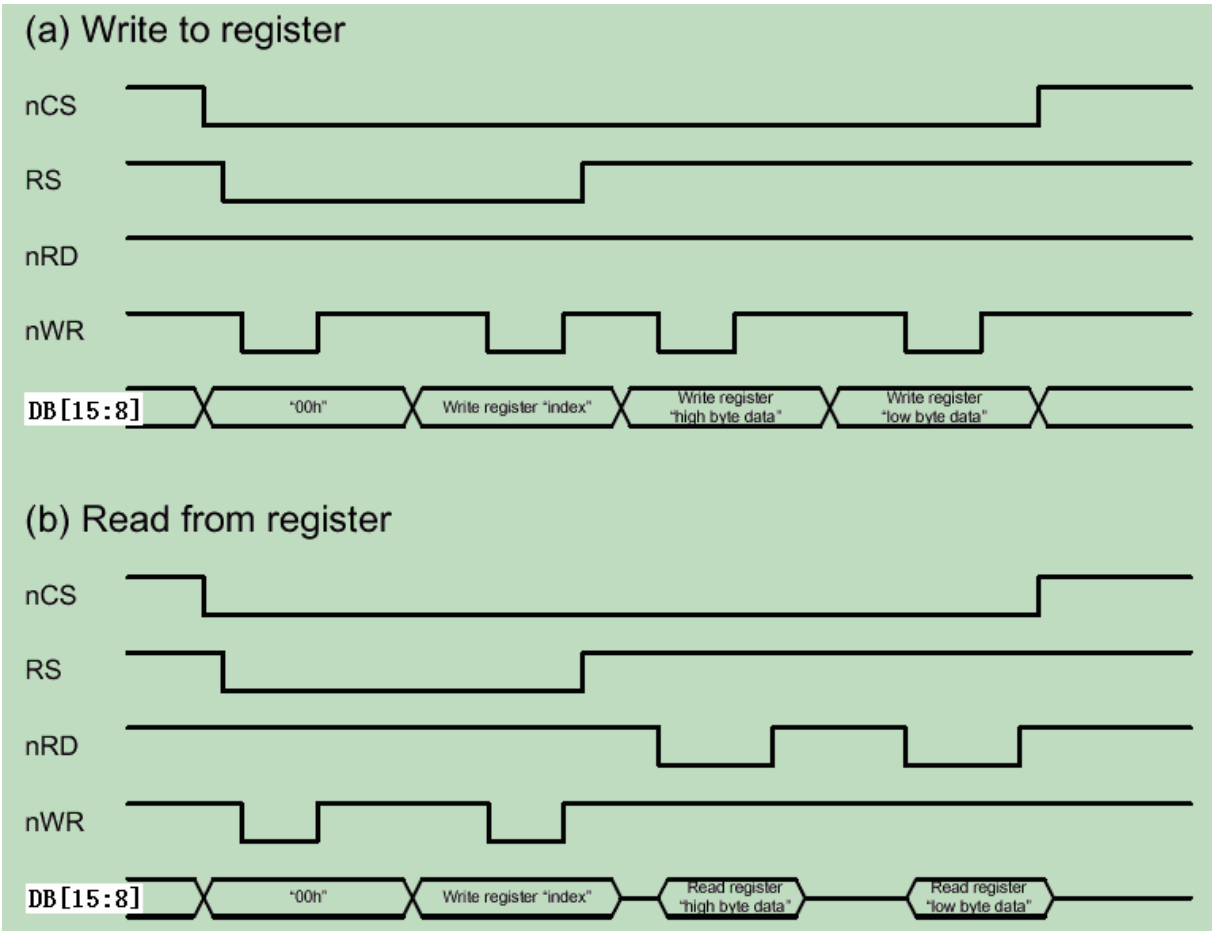
8.2. Instruction Descriptions

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	RO	1	1	0	0	1	0	0	1	1	0	0	1	1	0	1	0	1
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0
05h	16 bits data format control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EPF1	EPF0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0	BP7	BP6	BP5	BP4	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
10h	Power Control 1	W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	W	1	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interfaces.															
29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS[3]	FRS[2]	FRS[1]	FRS[0]
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]

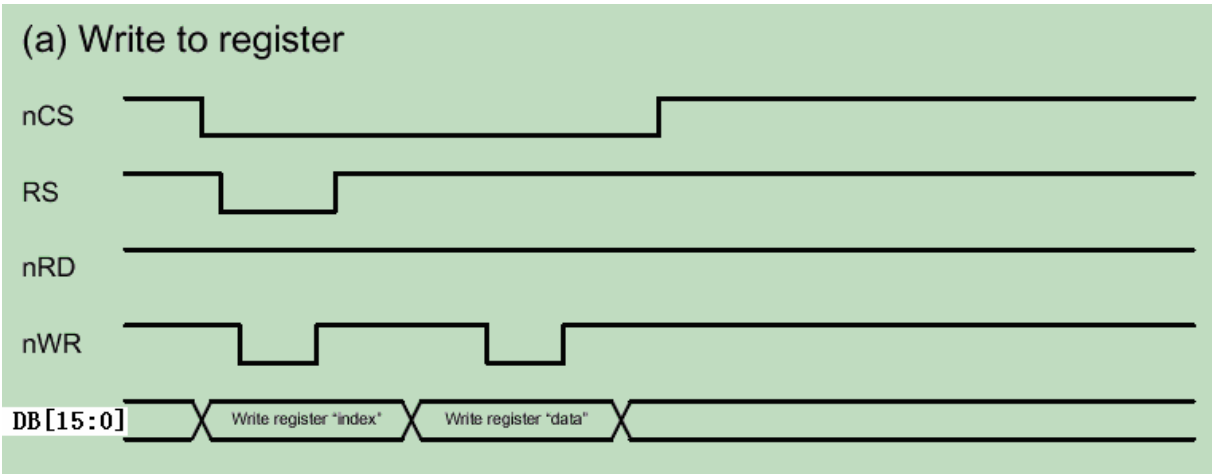
No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP08	PTDP07	PTDP06	PTDP05	PTDP04	PTDP03	PTDP02	PTDP01	PTDP00
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA08	PTSA07	PTSA06	PTSA05	PTSA04	PTSA03	PTSA02	PTSA01	PTSA00
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA08	PTEA07	PTEA06	PTEA05	PTEA04	PTEA03	PTEA02	PTEA01	PTEA00
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP18	PTDP17	PTDP16	PTDP15	PTDP14	PTDP13	PTDP12	PTDP11	PTDP10
84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA18	PTSA17	PTSA16	PTSA15	PTSA14	PTSA13	PTSA12	PTSA11	PTSA10
85h	Partial Image 2 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA18	PTEA17	PTEA16	PTEA15	PTEA14	PTEA13	PTEA12	PTEA11	PTEA10
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI00	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOWE3	NOWE2	NOWE1	NOWE0	0	0	0	0	0	0	0	0
A1h	OTP VCM Programming Control	W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_OTP5	VCM_OTP4	VCM_OTP3	VCM_OTP2	VCM_OTP1	VCM_OTP0
A2h	OTP VCM Status and Enable	W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
A4h	OTP for ID code writing	W	1	TEST_OTP_EN	0	OTP_SEL1	OTP_SEL2	0	1	0	0	0	0	0	0	0	0	0	0
A5h	OTP Programming ID Key	W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
E6h	Deep stand by mode control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB

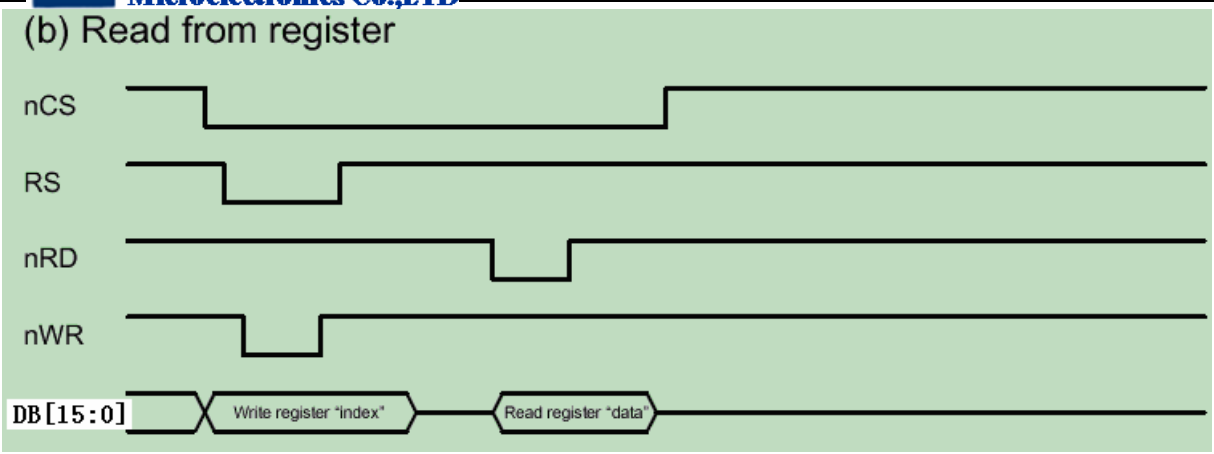
5.4.3 Interface Register write/read timing

I80 8-bit System Bus Interface Timing



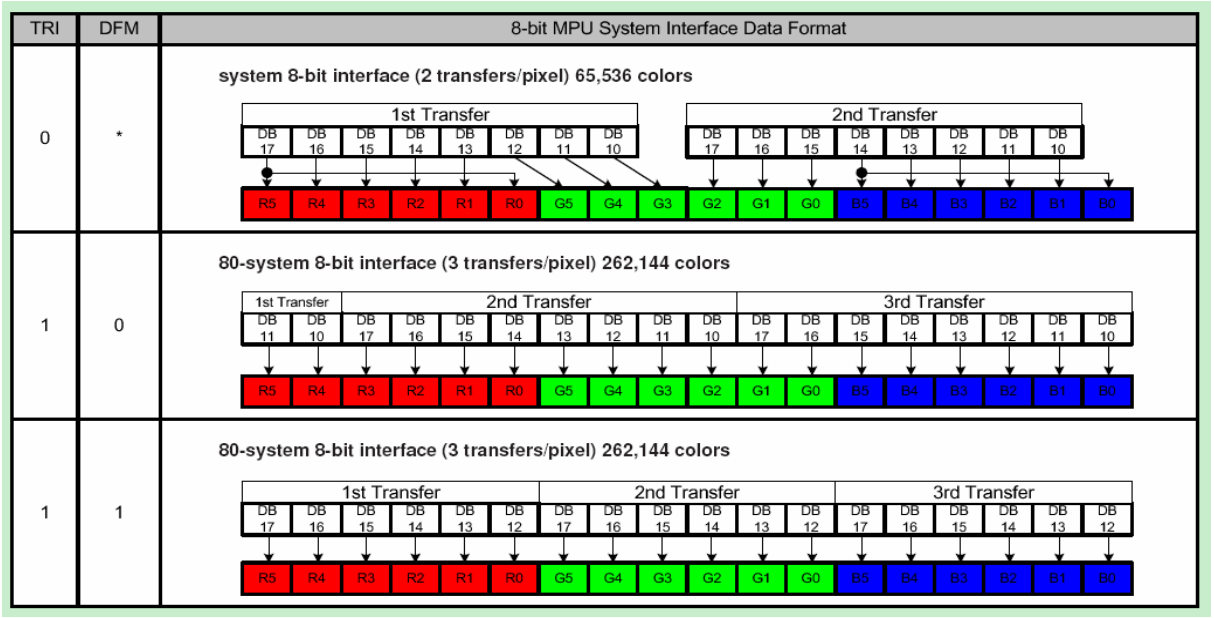
I80 16-bit System Bus Interface Timing



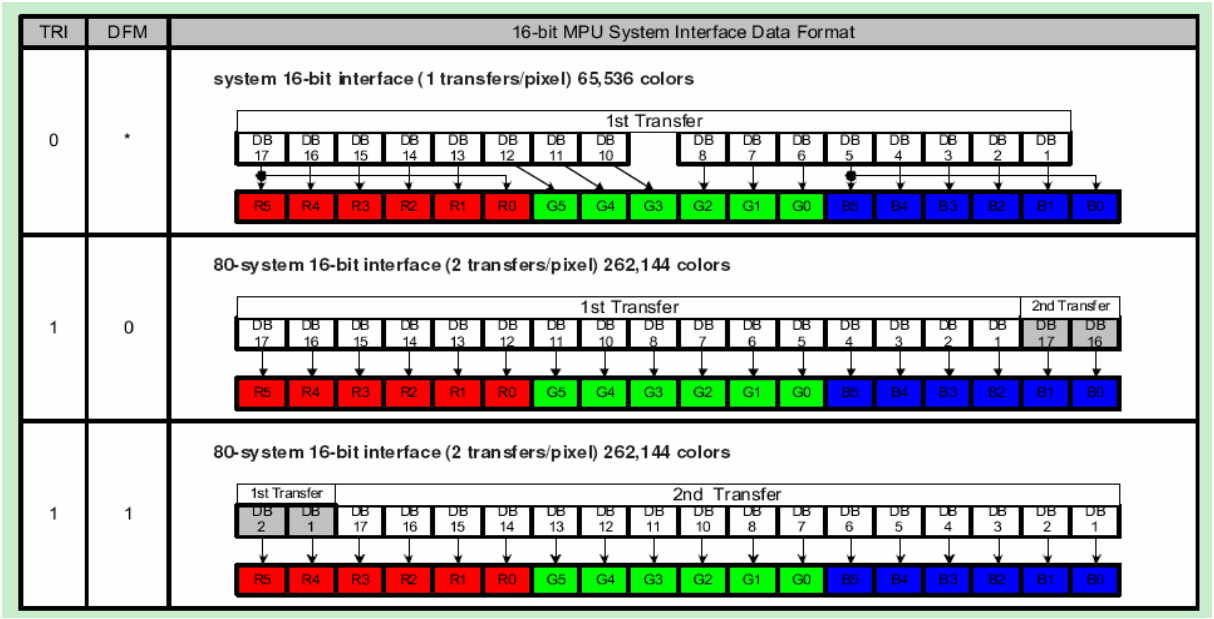


5.4.4 i80-System Interface Data Format

a) i80-System Interface with 8-bit Data Bus

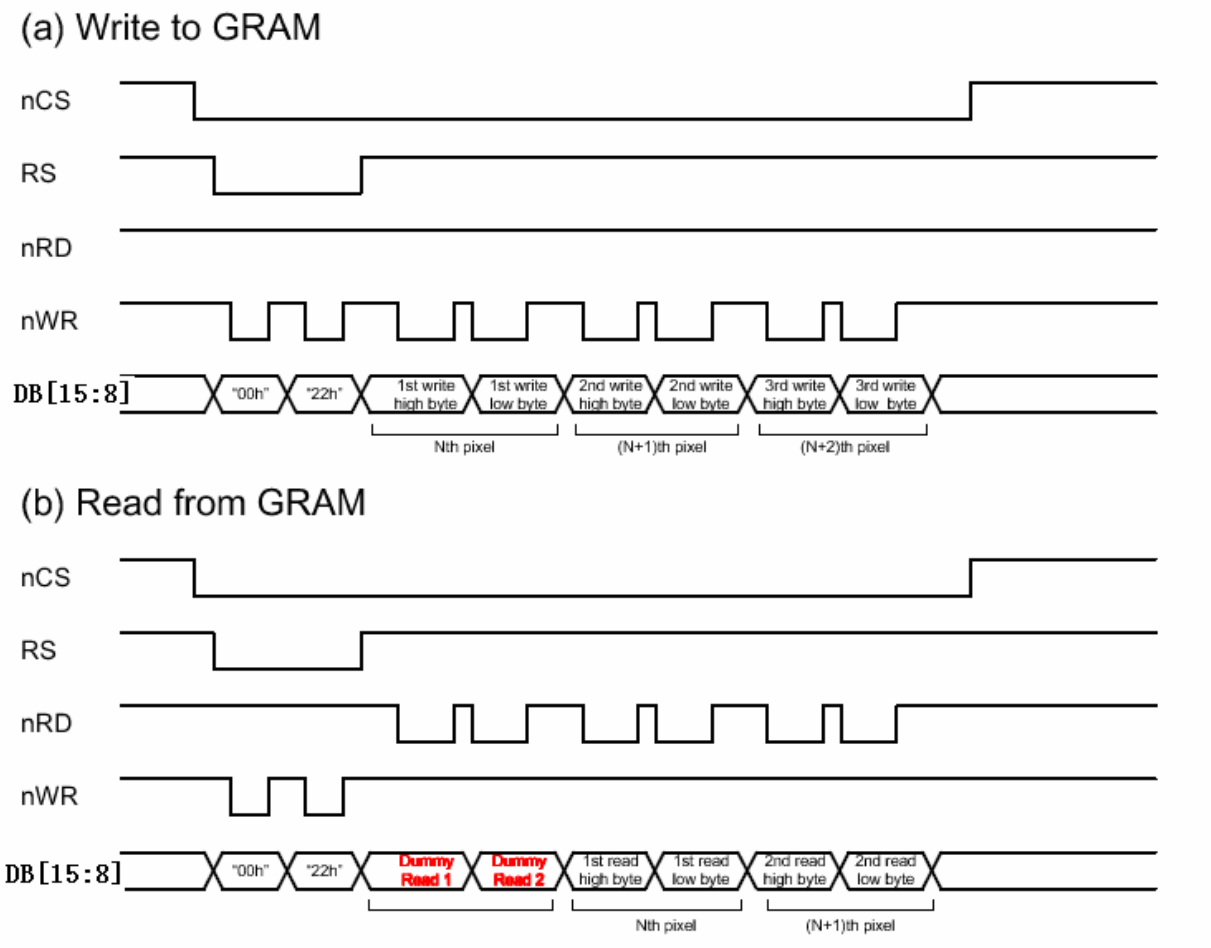


b)i80-System Interface with 16-bit Data Bus

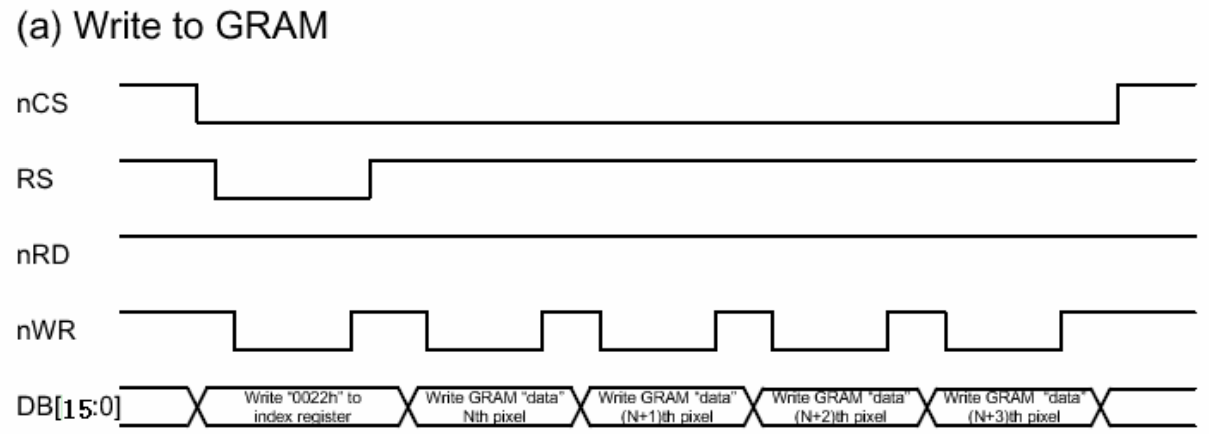


5.4.5 Data Bus GRAM Write/Read Timing

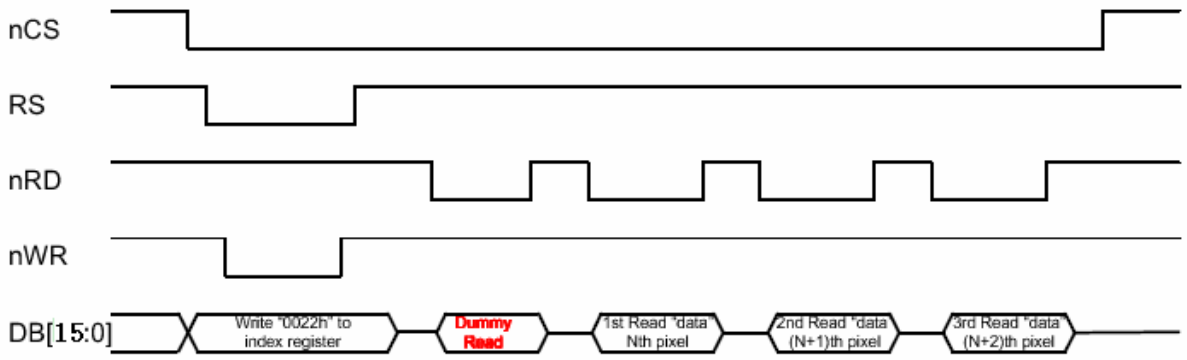
a)GRAM Timing of i80 8-bit System Interface



b)GRAM Timing of i80 16-bit System Interface



(b) Read from GRAM



5.4.6 Reset Timing Characteristics

Reset Timing Characteristics (IOVCC = 1.65 ~ 3.6 V)

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t_{RES_L}	ms	1	-	-
Reset rise time	t_{rRES}	µs	-	-	10
Reset high-level width	t_{RES_H}	ms	50	-	-

6. Optical Characteristics

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		θ=0° Φ=0°	190	210	-	Cd/m^2	1
Uniformity	△Bp			-	80%	-		1,2
Viewing Angle	θ1 (Φ=90°)		Cr≥10	60	70	-	Deg	3
	θ1 (Φ=270°)			50	60	-		
	θ2 (Φ=0°)			60	70	-		
	θ2 (Φ180°)			60	70	-		
Contrast Ratio	Cr		θ=0°	300	350	-	-	4
Response Time	T_r		25℃	-	20	30	ms	5
	T_f							
Color of CIE Coordinate	W	x	θ=0° Φ=0°	0.254	0.304	0.354	-	1,6
		y		0.313	0.363	0.413	-	
	R	x		0.560	0.610	0.660	-	
		y		0.284	0.334	0.384	-	
	G	x		0.246	0.296	0.346	-	
		y		0.508	0.558	0.608	-	
	B	x		0.080	0.130	0.180	-	
		y		0.114	0.164	0.214	-	
NTSC Ratio	S			-	50%			

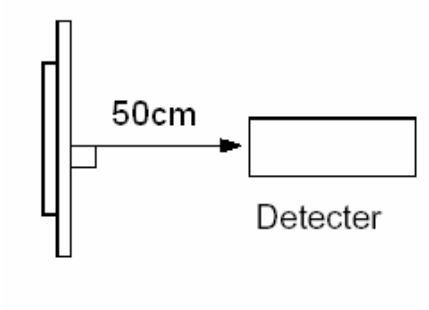
Note：The parameter is slightly changed by temperature, driving voltage and materiel.

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment PR-705 (Φ8mm)

Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

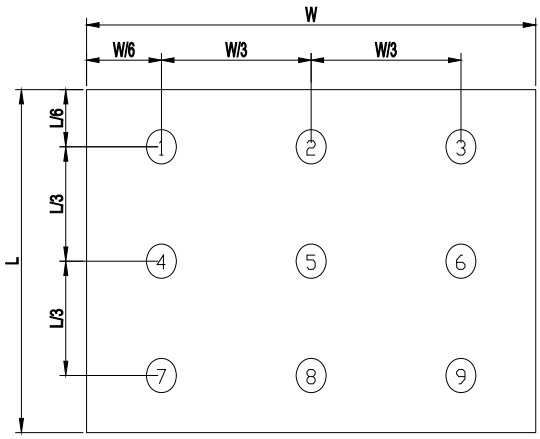


Note 2: The luminance uniformity is calculated by using following formula.

△Bp = Bp (Min.) / Bp (Max.)×100 (%)

Bp (Max.) = Maximum brightness in 9 measured spots

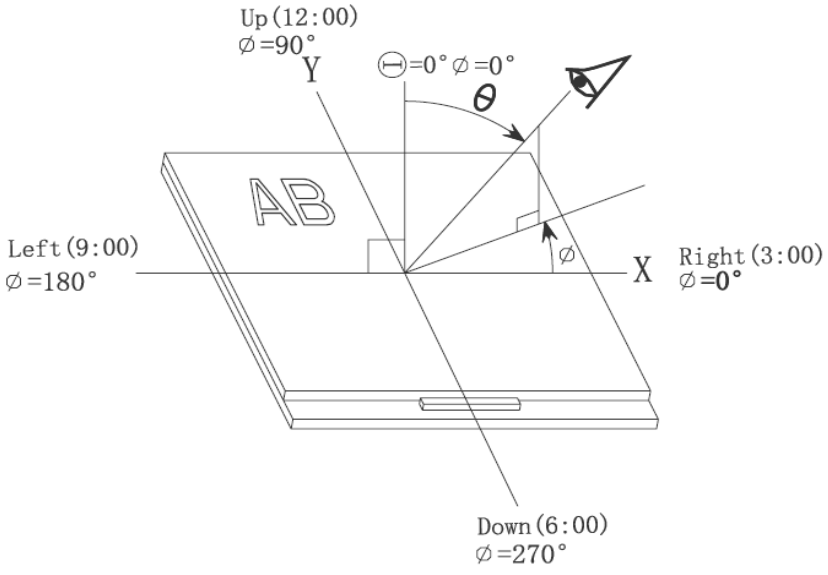
Bp (Min.) = Minimum brightness in 9 measured spots.



Measurement equipment PR-705 (Φ8mm)

Note 3: The definition of viewing angle:

Refer to the graph below marked by *θ* and *Φ*



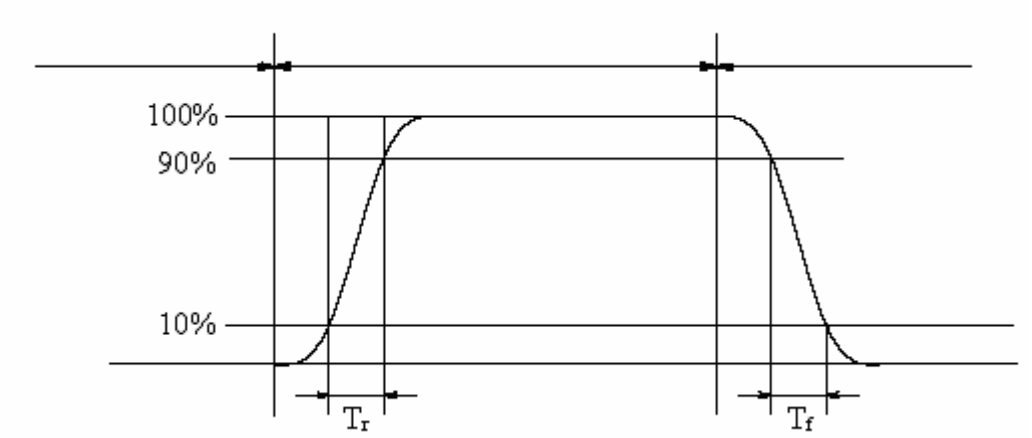
Note 4: The definition of contrast ratio (Test LCM using PR-705):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at “White” state}}{\text{Luminance When LCD is at “Black” state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

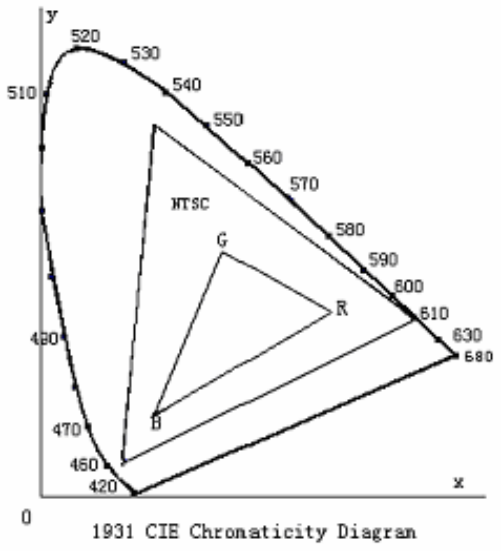
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.



Color gamut:

$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

7. Reliability Test Items and Criteria

No	Test Item	Test condition	Criterion
1	High Temperature Storage	Ta=+70℃,240hrs	After testing, cosmetic and electrical defects should not happen.
2	Low Temperature Storage	Ta=-30℃,240hrs	
3	High Temperature Operation	Ts=+60℃,240hrs	
4	Low Temperature Operation	Ta=-20℃,240hrs	
5	High Temperature & Humidity Operation	Ta=+60℃±2℃ 90%RH 240H Power on	
6	Thermal Shock(Non-operation)	-30℃ 30 min~+70℃ 30 min,Change time:5 min,20 Cycles	
7	Vibration Test(Non-operation)	Frequency range:10~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours For each direction of X,Y,Z. (6 hours for total)(Package condition)	
8	Shock Test(Non-operation)	60G 6ms,±X, ±Y, ±Z 3 times, for each direction	
9	Drop Test(package state)	Height:80 cm,1corner, 3edges, 6 sides each time	1.After testing, cosmetic and electrical defects should not happen. 2.the product should remain at initial place 3.Product uncovered or package broken is not permitted.

Note 1:Ts is the temperature of panel's surface.
Note 2:Ta is the ambient temperature of sample.
Note 3:Additional test Item proposed by customer shall be determined by mutual agreement between customer and Tianma

8 Quality level

8.1 Classification of defects

Major defects (MA): A major defect refers to a defect that may substantially degrade usability for product applications, including all functional defects(such as no display, abnormal display, open or missing segment, short circuit, missing component), outline dimension beyond the drawing, progressive defects and those affecting reliability.

Minor defects (MI): A minor defect refers to a defect which is not considered to be able to substantially degrade the product application or a defect that deviates from existing standards almost unrelated to the effective use of the product or its operation, such as black spot, white spot, bright spot, pinhole, black line, white line, contrast variation, glass defect, polarizer defect, etc.

8.2 Definition of inspection range

For dot defect of TFT LCD which is not smaller than 3 inches, dividing three areas to make a judgment (according to figure 1).

A area : center of viewing area

B area : periphery of viewing area

C area : Outside viewing area

For other defects, dividing two areas to make a judgment (according figure 2).

A zone : Inside Viewing area

B zone : Outside Viewing area

X1(A.A~V.A): -mm X2(A.A~V.A):-mm

Y1(A.A~V.A): -mm Y2(A.A~V.A): -mm

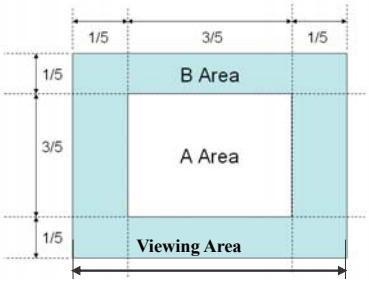


Figure 1

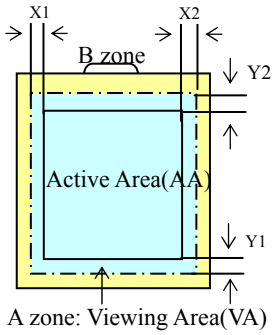


Figure 2

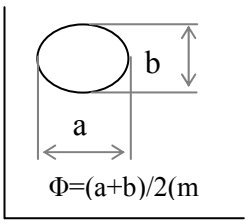
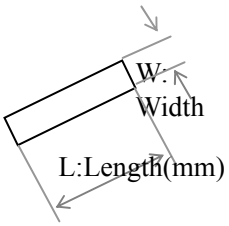
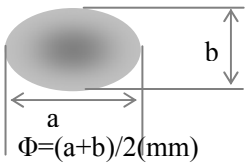
8.3 Inspection items and general notes

General notes	①Should any defects which are not specified in this standard happen, additional standard shall be determined by mutual agreement between customer and TIANMA. ②Viewing area should be the area which TIANMA guarantees. ③Limit sample should be prior to this Inspection standard. ④Viewing judgment should be under static pattern. ⑤Inspection conditions Inspection distance: 250 mm (from the sample) Temperature : 25±5 ºC Inspection angle : 45 degrees in 6 o′clock direction (all defects in viewing area should be inspected from this direction)	
Inspection items	Pinhole, Bright spot, Black spot, White spot, Black line, White Line, Foreign particle, Bubble	The color of a small area is different from the remainder. The phenomenon doesn't change with voltage
	Contrast variation	The color of a small area is different from the remainder. The phenomenon changes with voltage
	Polarizer defect	Scratch, Dirt, Particle, Bubble on polarizer or between polarizer and glass
	Dot defect (TFT LCD)	The pixel appears bright or dark abnormally when display
	Functional defect	No display, Abnormal display, Open or missing segment, Short circuit, False viewing direction
	Glass defect	Glass crack, Shaved corner of glass, Surplus glass
	PCB defect	Components assembly defect

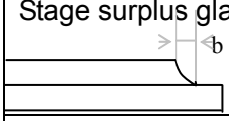
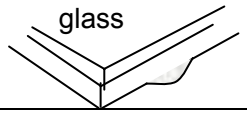
8.4 Outgoing Inspection level

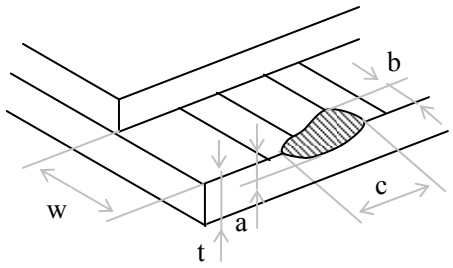
Outgoing Inspection standard	Inspection conditions	Inspection				
		Min.	Max.	Unit	IL	AQL
Major Defects	See 8.3 general notes	See 8.5			II	0.65
Minor Defects	See 8.3 general notes	See 8.5			II	1.5
Note：Sampling standard conforms to GB2828						

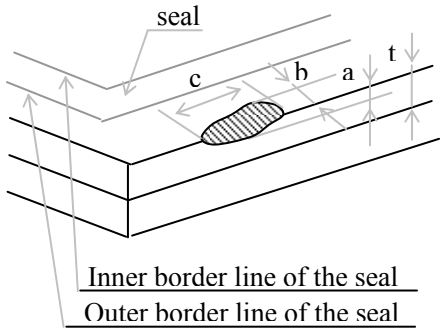
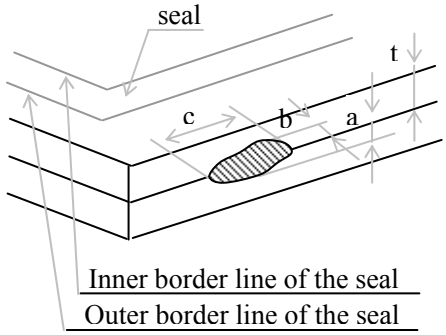
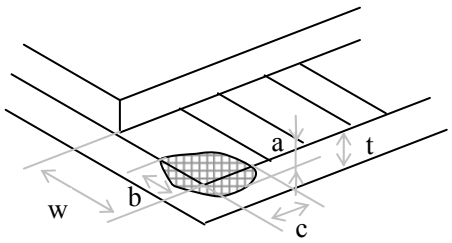
8.5 Inspection Items and Criteria

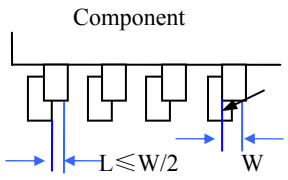
Inspection items			Judgment standard			
			Category		Acceptable number	
					A zone	B zone
1	Black spot, White spot, Bright Spot, Pinhole, Foreign Particle, Particle in or on glass, Scratch on glass		A	Φ≦0.10	Neglected	Neglected
			B	0.10<Φ≦0.15	2	
			C	0.15<Φ≦0.20	1	
			D	0.20<Φ	0	
			Total defective point(B,C)		3	
2	Black line, White line, and Particle Between Polarizer and glass, Scratch on glass		A	W≦0.01	Neglected	Neglected
			B	0.01<W≦0.03 L≦3.0	2	
			C	0.03<W≦0.05 L≦3.0	1	
			D	0.05<W	0	
			Total defective point(B,C)		3	
3	Contrast variation		A	Φ≦0.2	Neglected	Neglected
			B	0.2<Φ≦0.3	2	
			C	0.3<Φ≦0.4	1	
			D	0.4<Φ	0	
			Total defective point(B,C)		3	

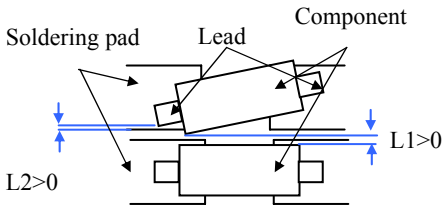
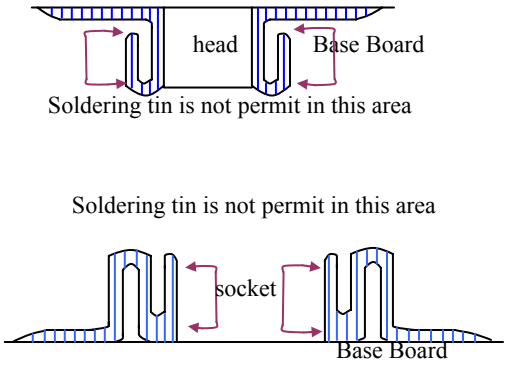
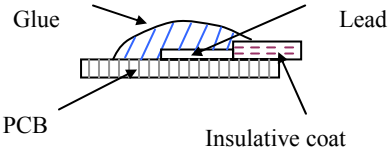
4	Dot defect (if TFT LCD is used)	TFT LCD is smaller than 3 inches	LCD Class	Defect	A area		B area
			A	Bright dot	1		Neglected
				Dark dot	1		
				Total	2		
		TFT LCD between 3~10.4 inches	LCD Class	Defect	A area	B area	C area
			B	Bright dot	2	2	Neglecte
				Dark dot	2	3	

				Total	6	d
		Notes: Bright dot: in R、G、B or dark display figure, the pixel appears bright. Dark dot: in R、G、B or white display figure, the pixel appears dark. Defect area must be less than an half size of the dot. The distance of two dot: L>5mm.				
5	Bubble inside cell		any size		none	none
6	Polarizer defect (if Polarizer is used)	Scratch ,damage on polarizer, Particle on polarizer or between polarizer and glass.	Refer to item 1 and item 2.			
		Bubble, dent and convex	A	Φ≦0.3	Neglected	Neglected
			B	0.3<Φ≦0.7	2	
			C	0.7<Φ	0	
7	Surplus glass	Stage surplus glass 	b≦0.3mm			
		Surrounding surplus glass 	Should not influence outline dimension and assembling.			
8	Open segment or open common		Not permitted			
9	Short circuit		Not permitted			
10	False viewing direction		Not permitted			
11	Contrast ratio uneven		According to the limit specimen			
12	Crosstalk		According to the limit specimen			
13	Black /White spot(display)		Refer to item 1			
14	Black /White line(display)		Refer to item 2			

Inspection items			Judgment standard		
			Category(application: B zone)		Acceptable number
15	Glass defect crack	①The front of lead terminals 	A	a≤ t, b≤1/5W, c≤3mm	Max.3 defects allowed
			B	Crack at two sides of lead terminals should not cover patterns and alignment mark	

		②Surrounding crack—non-contact side  	b < Inner borderline of the seal		
		③ Surrounding crack— contact side  	b < Outer borderline of the seal		
		④Corner  	A	a ≦ t, b ≦ 3.0, c ≦ 3.0	
			B	Glass crack should not cover patterns u and alignment mark and patterns.	

Inspection items			Judgment standard Category(application: B zone)
16	PCB defect	Component soldering: No cold soldering、short、open circuit、burr、tin ball The flat encapsulation component position deviation must be less than 1/3 width of the pin (Pic.1)； the sheet component deviation: Pin deviates from the pad and contact with the near components is not permitted（Pic.2）	

		lead defect: The lead lack must be less than 1/3 of its width; The lead burr must be less than 1/3 of the seam; Impurities connect with the near leads is not permitted	
		Connector soldering: Soldering tin is at contact position of the plug and socket is not permitted No foundation is scald Serious cave distortion on plug and socket contact pin is not permitted	
		Glue on root of the speaker receiver and motor lead: The insulative coat of the lead must join into the PCB; the protected glue must envelop to the insulative coat.	

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol

— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water

— Ketone

— Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct

assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

Relatively humidity: ≤80%

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

9.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.