MODEL NO. : TM104SCH01

ISSUED DATE: 2008-12-03

VERSION : Ver 2.2

□Preliminary Specification
■Final Product Specification

Customer :

Approved by	Notes

SHANGHAI TIANMA Confirmed :

Prepared by	Checked by	Approved by
2008-12-03		08'12/3

This technical specification is subjected to change without notice

Table of Contents

Record of Revision

Rev	Issued Date	Description	Editor
1.0	2008-05-07	Preliminary Release	Yebo Gu
1.1	2008-08-13	Add Gamma Voltage, Add Packing Drawing	Zhenying zhang
1.2	2008-08-27	Update Lamp Current	Zhenying zhang
2.0	2008-10-14	Final Product Specification Update Luminance Minimum Value to 185nits	Zhenying zhang
2.1	2008-11-18	Update Model Name from TS104SAATC01-00 to TM104SCH02	Zhenying zhang
2.2	2008-12-03	Revise Model Name from TM104SCH02 to TM104SCH01 Update Model Name in Mechanical Drawing Update Chromaticity Gx typical value from 0.333 to 0.300	Zhenying zhang

1 General Specifications

Feature		Spec
Display Spec.	Size	10.4 inch
	Resolution	800(RGB) x 600
	Interface	TTL
	Color Depth	262K
	Technology Type	a-Si
	Pixel Pitch (mm)	0.264x0.264
	Pixel Configuration	R.G.B. Vertical Stripe
	Display Mode	TM with Normally White
	Surface Treatment(Up Polarizer)	Anti-Glare(3H)
	Viewing Direction	12 o'clock
	Gray Scale Inversion Direction	6 o'clock
Mechanical Characteristics	LCM (W x H x D) (mm)	236.00x176.90x5.60
	Active Area(mm)	211.20x158.40
	With /Without TSP	Without TSP
	Weight (g)	283.0

Note 1: Viewing direction for best image quality is different from TFT definition, there is a 180 degree shift.

Note 2 : Requirements on Environmental Protection: RoHS

Note 3 : LCM weight tolerance : +/- 5%

2 Input/Output Terminals

2.1 TFT LCD Panel

Matching connector of Hirose FH12A-30S-0.5SH(55)

No	Symbol	I/O	Description	Comment
1	POL	I	Polarity selection	
2	STVD	I/O	Vertical start pulse input when U/D=H	Note1
3	OEV	I	Gate output enable	
4	CKV	I	Vertical clock	
5	STVU	I/O	Vertical start pulse input when U/D=L	Note1
6	GND	P	Power ground	
7	EDGSL	I	Clock edge selection	Note2
8	VCC	P	Power supply for digital circuit	
9	V9	I	Gamma voltage level 9	
10	VGL	P	Gate OFF voltage	
11	V2	I	Gamma voltage level 2	
12	VGH	P	Gate ON voltage	
13	V6	I	Gamma voltage level 6	
14	U/D	I	Up/down selection	Note1
15	VCOM	I	Common voltage	
16	GND	P	Power ground	
17	AVDD	P	Power supply for analog circuit	
18	V14	I	Gamma voltage level 14	
19	V11	I	Gamma voltage level 11	
20	V8	I	Gamma voltage level 8	
21	V5	I	Gamma voltage level 5	
22	V3	I	Gamma voltage level 3	
23	GND	P	Power ground	
24	R5	I	Red data(MSB)	
25	R4	I	Red data	
26	R3	I	Red data	
27	R2	I	Red data	
28	R1	I	Red data	
29	R0	I	Red data(LSB)	
30	GND	P	Power ground	
31	GND	P	Power ground	
32	G5	I	Green data(MSB)	
33	G4	I	Green data	

34	G3	I	Green data	
35	G2	I	Green data	
36	G1	I	Green data	
37	G0	I	Green data(LSB)	
38	STHL	I/O	Horizontal start pulse input when R/L =H	Note1
39	REV	I	Control display data are inverted or not. When “REV”=H, data will be inverted.	
40	GND	P	Power ground	
41	DCLK	I	Dot clock input. Latching source data onto the line latches at the rising or falling edge by EDGSL signal selected.	
42	VCC	P	Power supply for digital circuit	
43	STHR	I/O	Horizontal start pulse input when R/L =L	Note1
44	LD	I	Latches the polarity of outputs and switches the new data to outputs.	
45	B5	I	Blue data (MSB)	
46	B4	I	Blue data	
47	B3	I	Blue data	
48	B2	I	Blue data	
49	B1	I	Blue data	
50	B0	I	Blue data (LSB)	
51	R/L	I	Right/ left selection	Note1
52	V1	I	Gamma voltage level 1	
53	V4	I	Gamma voltage level 4	
54	V7	I	Gamma voltage level 7	
55	V10	I	Gamma voltage level 10	
56	V12	I	Gamma voltage level 12	
57	V13	I	Gamma voltage level 13	
58	AVDD	P	Power supply for analog circuit	
59	GND	P	Power ground	
60	VCOM	I	Common voltage	

I/O definition:

I-----Input O---Output P----Power/Ground

Note1: The following SPEC is for PCB1.

Scan control input		In/Out state for start pulse				Scanning direction
U/D	R/L	STVD	STVU	STHR	STHL	
GND	VCC	O	I	O	I	Up to down, left to right
VCC	GND	I	O	I	O	Down to up, right to left
GND	GND	O	I	I	O	Up to down, right to left
VCC	VCC	I	O	O	I	Down to up, left to right

Note2:

When EDGSL=L	Latching source data onto the line latches at the rising edge.
When EDGSL=H	Latching source data onto the line latches at the rising edge and falling edge.

2.2 CN2 (CCFL connector)

No	Symbol	I/O	Description	Wire Color
1	VL1	P	CCFL power supply(high voltage)	Pink
2	VL2	P	CCFL power supply(GND)	White

3 Absolute Maximum Ratings

3.1 Driving TFT LCD Panel

GND=0V,Ta = 25℃

Item	Symbol	Min	Max	Unit	Remark
Power Voltage	VDD	-0.3	5.0	V	
	AVDD	-0.5	15.0	V	
	VGH	-0.3	42.0	V	
	VGL	-20.0	0.3	V	
	VGH-VGL	-0.3	40.0	V	
Input voltage	V_{IN}	-0.3	5.0	V	Note1
Operating Temperature	T_{OPR}	-20	70	℃	
Storage Temperature	T_{STG}	-30	80	℃	

Note1: V_{IN} represent POL,STVD,OEV,CKV,STVU,STHL,REV,STHR,DCLK,LD,EDGSL,U/D,R/L, R0~R5,G0~G5,B0~B5

4 Electrical Characteristics

4.1 Driving TFT LCD Panel

GND=0V, Ta=25℃

Item		Symbol	Min	Typ	Max	Unit	Remark
Digital supply Voltage		VCC	3.0	3.3	3.6	V	
Analog supply Voltage		AVDD	9.4	9.8	10.2	V	
Gate on voltage		VGH	19.8	22.0	24.2	V	
Gate off voltage		VGL	-7.7	-7.0	-6.3	V	
Common Electrode Driving Signal		VCOM	-	4.36	-	V	Note3
Input level of Gamma voltage		V1~V7	0.4xAVDD	-	AVDD-0.1	V	
		V8~V14	0.1	-	0.6xAVDD	V	
Input Signal Voltage	Low Level	V_{IL}	0	-	0.2xVCC	V	Note1
	High Level	V_{IH}	0.8xVCC	-	VCC	V	
Output Signal Voltage	Low Level	V_{OL}	0	-	0.2xVCC	V	Note2
	High Level	V_{OH}	0.8xVCC	-	VCC	V	
Current of digital supply voltage		I_{CC}	-	11.00	16.00	mA	VCC=3.3V Note2
Current of analog supply voltage		I_{AVDD}	-	50.00	75.00	mA	AVDD=9.8V Note2
Current of Gate on voltage		I_{GH}	-	0.30	0.45	mA	VGH=22.0V Note2
Current of Gate off voltage		I_{GL}	-	0.51	0.75	mA	VGL=-7.0V Note2

Note1:Input Signal:POL,STVD,OEV,CKV,STVU,STHL,REV,STHR,DCLK,LD,EDGSL,U/D,R/L, R0~R5,G0~G5,B0~B5
Note2:Output Signal: STVD, STVU, STHL, STHR
Note3:The value may be different for different LCM.
Note4:To test the current dissipation, using the “color bar” testing pattern shown as below:

1. White
2. Yellow
3. Cyan
4. Green
5. Magenta
6. Red
7. Blue
8. Black

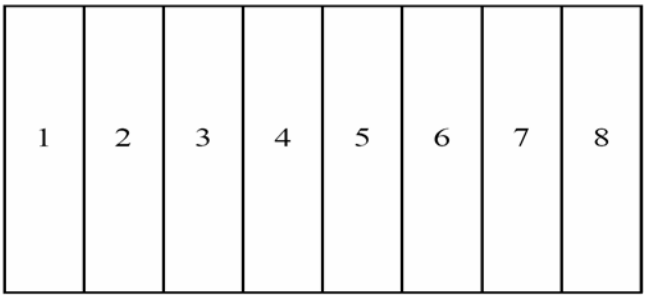


Figure 4.1 Current dissipation testing pattern

4.2 Driving Backlight

Ta=25℃

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Lamp voltage	V_L	468	520	572	Vrms	
Lamp current	I_L	3.0	5.5	7.0	mArms	
Lamp start voltage	V_{LS}	-	-	890	Vrms	
Lamp frequency	F_L	40	60	80	KHz	

Note 1: The Minimum Life of CCFL : 20,000 hours

4.3 Gamma Correction Voltage

Gamma correction reference voltage setting

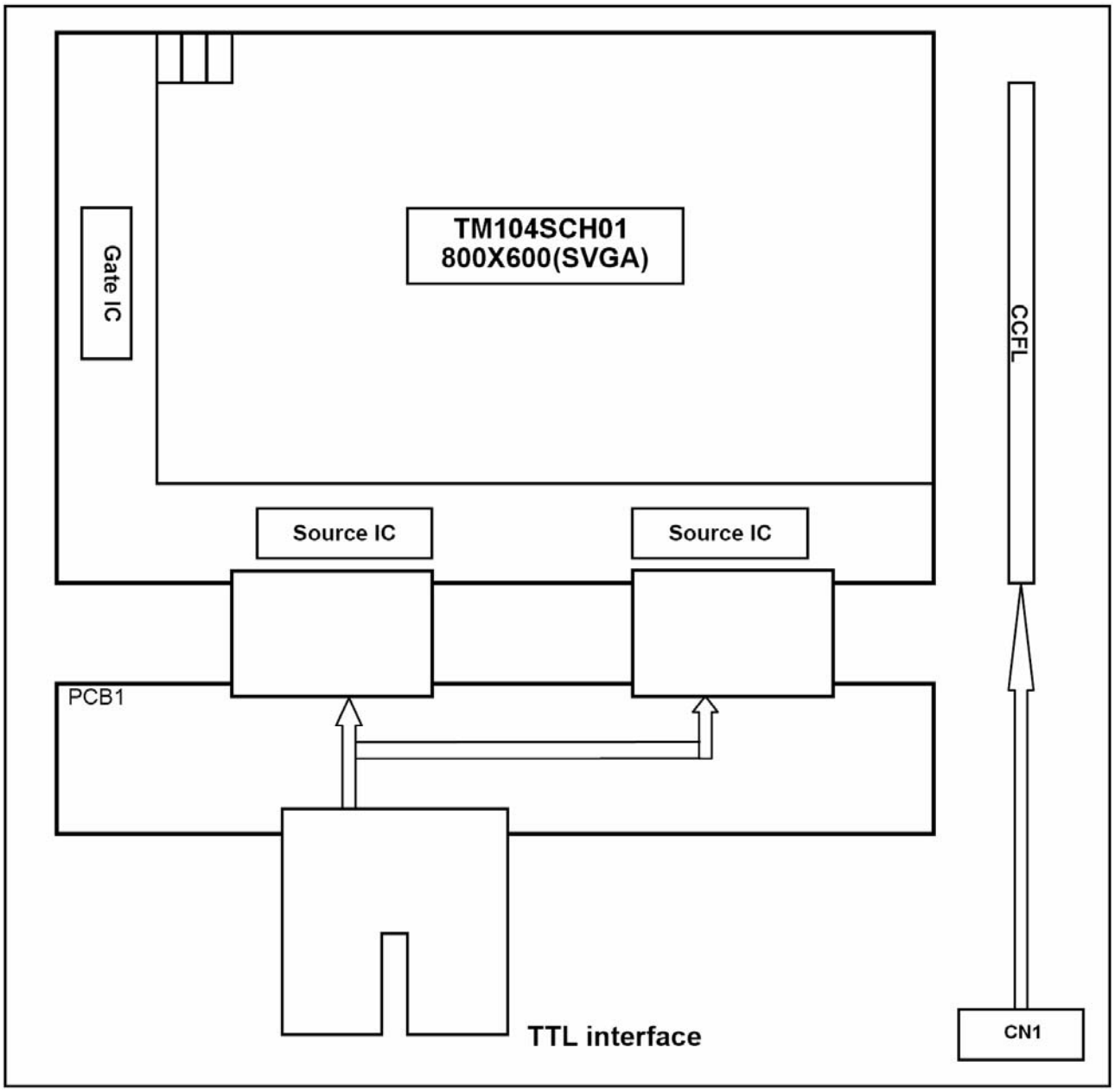
Parameter	Symbol	Min	Typ	Max	Unit	Remark
Gamma correction reference voltage V1~V14	V1	-	9.600	AVDD-0.1	V	
	V2	-	9.362	-	V	
	V3	-	7.798	-	V	
	V4	-	7.195	-	V	
	V5	-	6.803	-	V	
	V6	-	6.159	-	V	
	V7	-	5.000	-	V	
	V8	-	4.800	-	V	
	V9	-	3.641	-	V	
	V10	-	2.997	-	V	
	V11	-	2.605	-	V	
	V12	-	2.002	-	V	
	V13	-	0.438	-	V	
	V14	AVSS+0.1	0.200	-	V	

Note1: AVDD-0.1> V1 > V2> V3 > V4 > V5 > V6 > V7; V8 > V9 > V10 > V11 > V12 > V13 > V14 >AVSS+0.1V

Note2: This table is for Gamma 2.2

Table 4.3 Gamma correction reference voltage

4.4 Block Diagram



5 Timing Chart

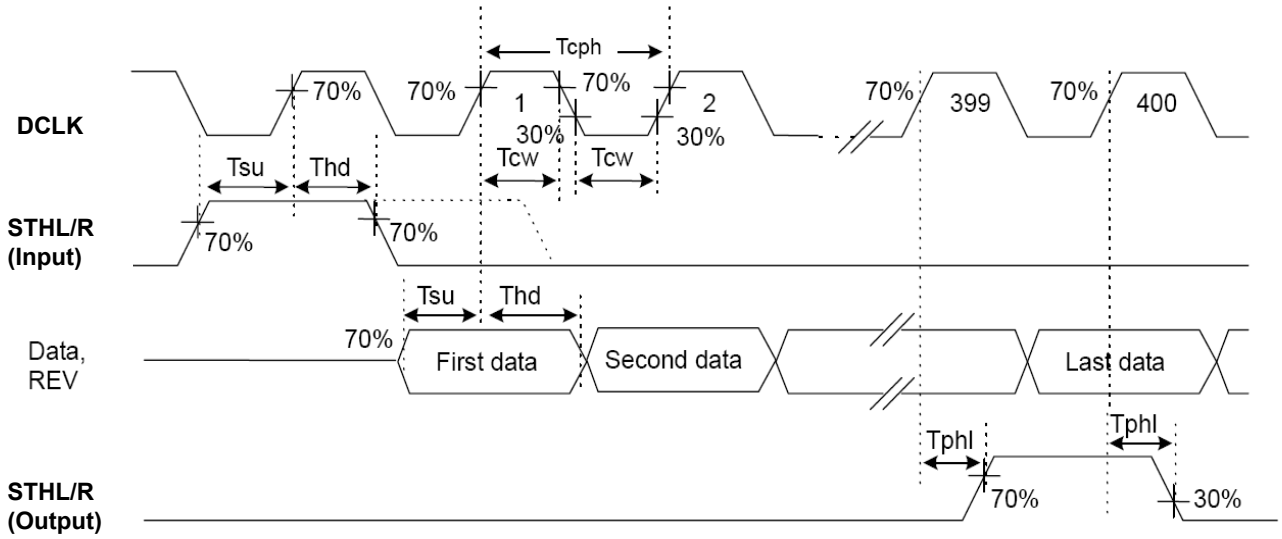
5.1 Source Driver Input Timing

(VCC=3.3V, AVDD=10V, AVSS=GND=0V, Ta=25℃)

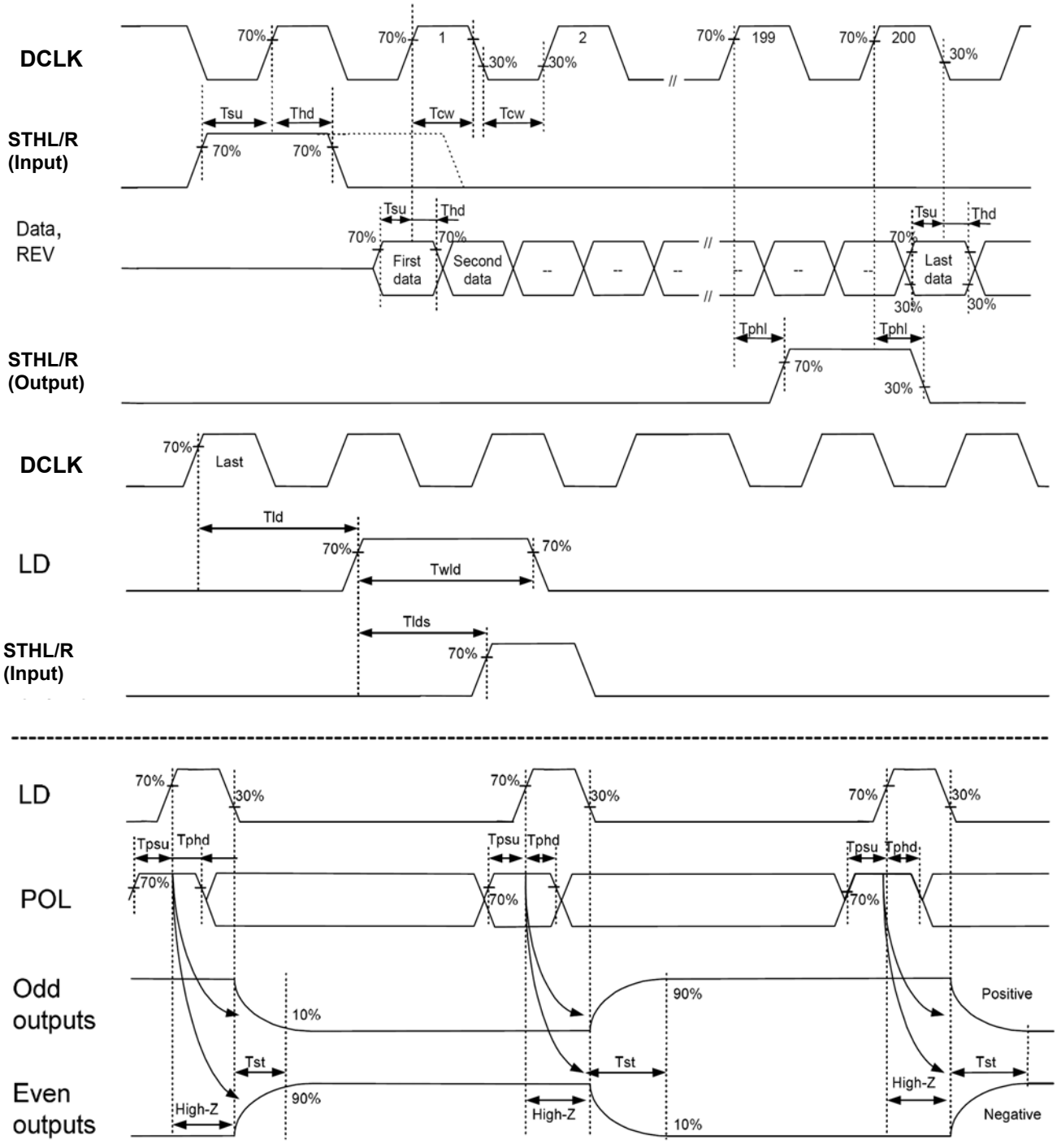
Parameter	Symbol	Min	Typ	Max	Unit	Condition
DCLK frequency	F_{CLK}	-	40	45	MHz	EDGSL="0"
	F_{CLK}	-	20	22.5	MHz	EDGSL="1"
DCLK pulse width	Tcw	40%	-	60%	Tcph	Tcph is DCLK cycle
Data set-up time	Tsu	4	-	-	ns	
Data hold time	Thd	2	-	-	ns	
Propagation delay of STHR/L	Tphl	6	10	15	ns	CL=25pF (Output)
Time that the last data to LD	Tld	1	-	-	Tcph	
Pulse width of LD	Twld	2	-	-	Tcph	
Time that LD to STHL/R	Tlds	5	-	-	Tcph	
POL set-up time	Tpsu	6	-	-	ns	POL to LD
POL hold time	Tphd	6	-	-	ns	POL to LD
Output stable time	Tst	-	-	9	us	10% or 90% target voltage. CL=60pF, R=2Kohm
Repair output delay stable time	Tst1	-	-	20	us	CL=190pF, R=5.5Kohm

Table 5.1 timing parameter

<< EDGSL= "0", Default >>



<< EDGSL= "1">>

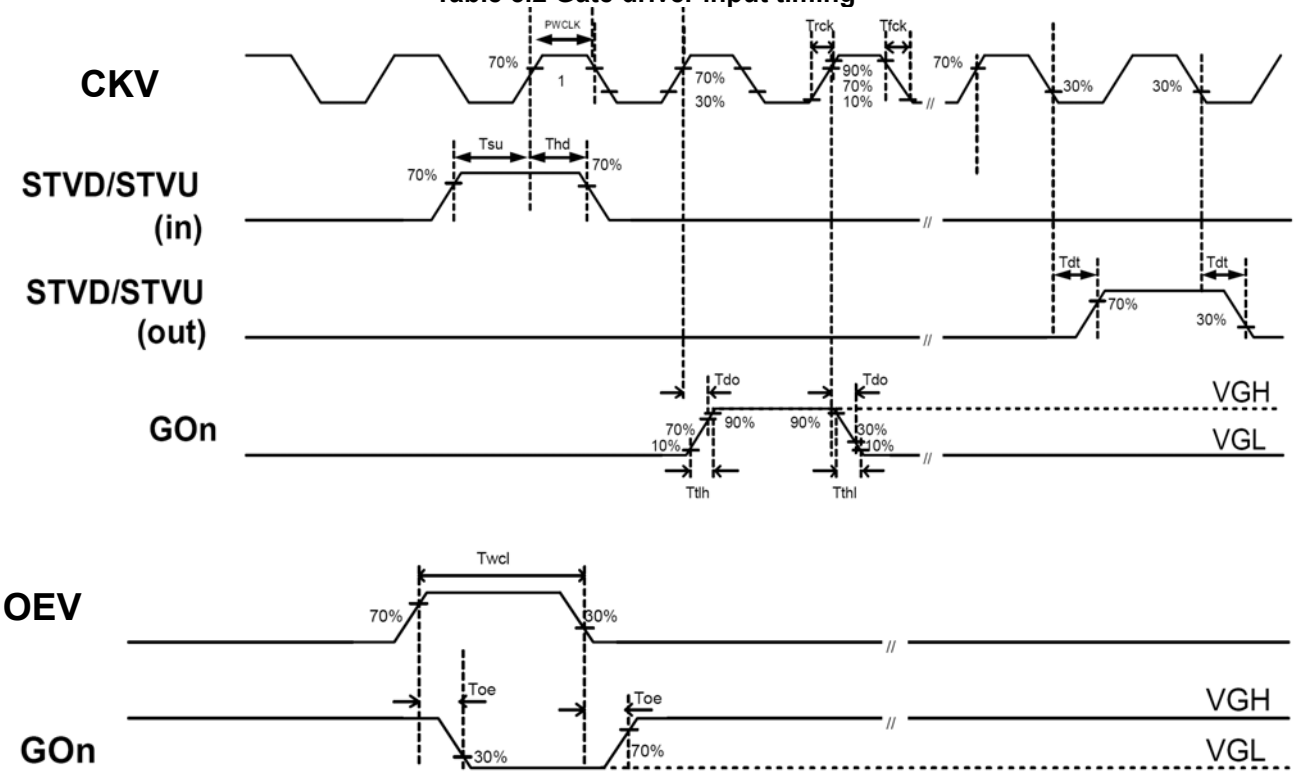


5.2 Gate Driver Input Timing

(VGH=25V, VGL=-15V, VCC=3.3V, GND=0V, Ta=25℃)

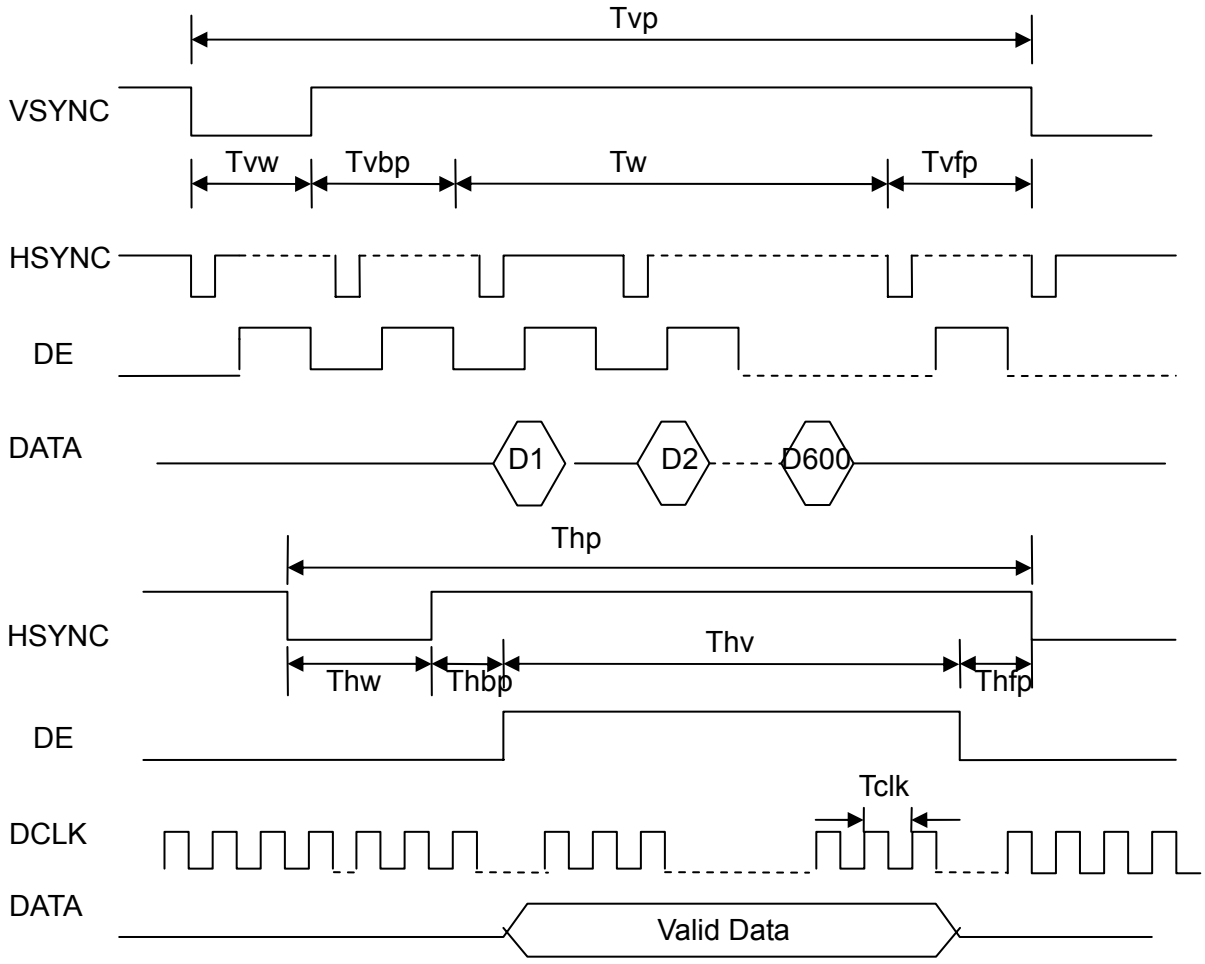
Symbol	Parameters	Min	Typ	Max	Unit	Condition
Tdt	STVD/STVU delay time	-	-	500	ns	CL=20pF
Tdo	Driver output delay time	-	-	900	ns	CL=200pF When Twcl=1us
Tthl	Output falling time	-	400	800	ns	CL=200pF 90% to 10%
Ttlh	Output rising time	-	500	1000	ns	CL=200pF 10% to 90%
Toe	OEx to driver output delay time	-	-	900	ns	CL=200pF
Fclk	Clock(CKV) frequency	-	-	200	KHz	In cascade connection
Trck	Clock rising time	-	-	100	ns	CL=20pF
Tfck	Clock falling time	-	-	100	ns	CL=20pF
PWCLK	Clock pulse width (High&Low)	500	-	-	ns	
Tsu	STVD/STVU set-up time	200	-	-	ns	
Thd	STVD/STVU hold time	300	-	-	ns	
Twcl	Output enabled pulse width	1	-	-	us	

Table 5.2 Gate driver input timing



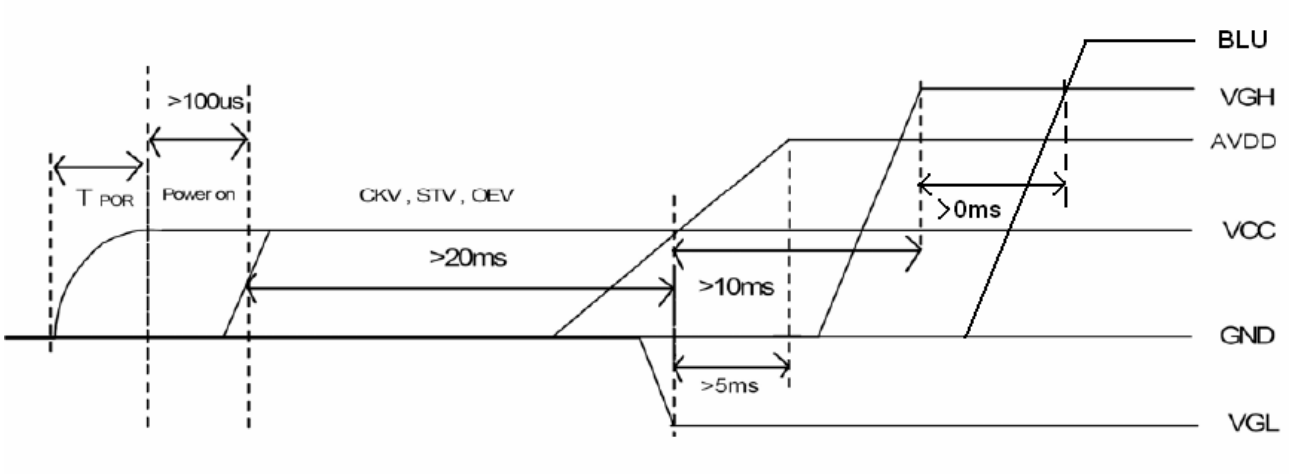
5.3 DCLK, Hsync, Vsync timing (Recommended setting)

Parameter		Symbol	Min	Typ	Max	Unit	Remark
Dot clock frequency		Tclk	-	40	45	MHz	
Hsync	Period	Thp	866	1056	1064	Tclk	
	Horizontal total blank	Thw+Thbp+Thfp	66	256	264	Tclk	
	Valid Data Width	Thv	-	800	-	Tclk	
Vsync	Period (Frame rate)	Tvp	628	635	650	Thp	
	Vertical total blank	Tvw+Tvbp+Tvfp	28	35	50	Thp	
	Valid Data Width	Tw	-	600	-	Thp	



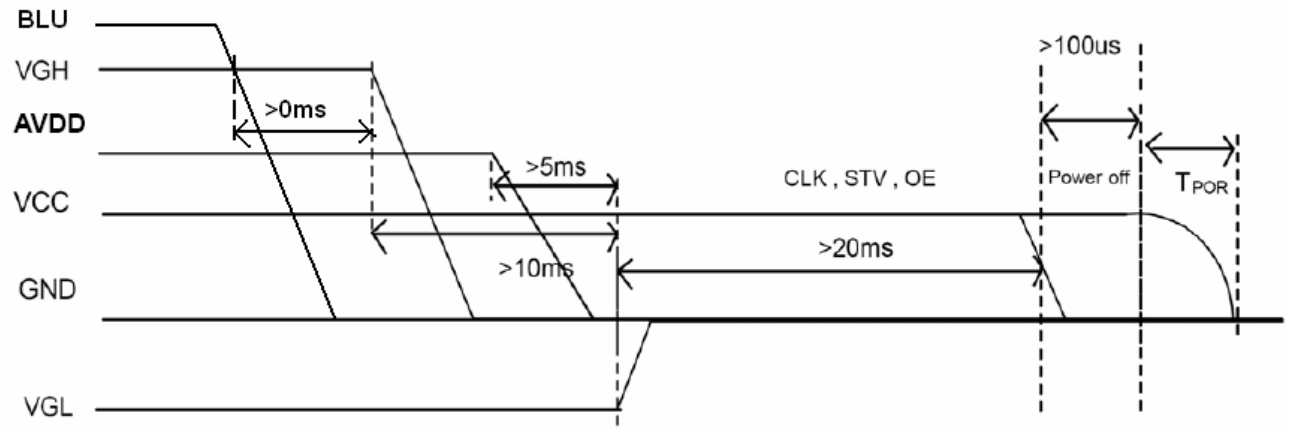
5.4 Power On/Off Sequence

5.4.1 Power on Sequence



VCC→AVDD→VGL→VGH→Data→B/L
Figure 5.4.1 power on sequence

5.4.2 Power off Sequence



B/L→Data→VGH→AVDD→VGL→VCC
Figure 5.4.2 power off sequence

6 Optical Characteristics

6.1 Optical Specification

Ta=25℃

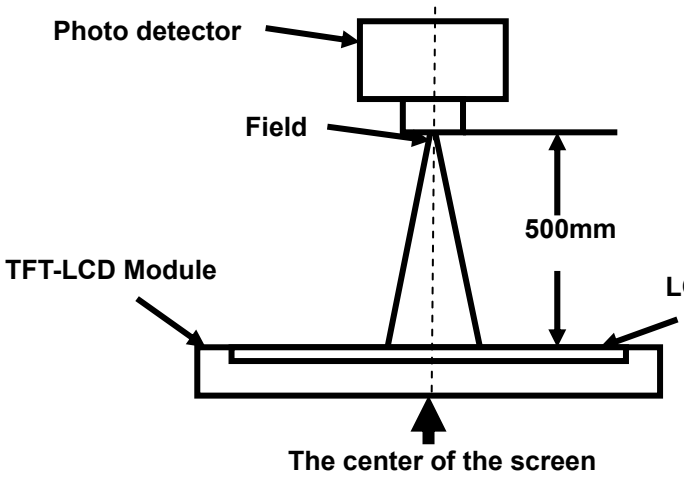
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	35	45	-	Degree	Note 2
		θB		55	65	-		
		θL		55	65	-		
		θR		55	65	-		
Contrast Ratio		CR	θ=0°	300	400	-	-	Note1 Note3
Response Time		T_{ON}	25℃	-	10	15	ms	Note1 Note4
		T_{OFF}		-	15	25		
Chromaticity	White	x	Backlight is on	0.261	0.311	0.361	-	Note5 Note1
		y		0.280	0.330	0.380		
	Red	x		0.550	0.600	0.650		
		y		0.297	0.347	0.397		
	Green	x		0.250	0.300	0.350		
		y		0.517	0.567	0.617		
	Blue	x		0.097	0.147	0.197		
		y		0.065	0.115	0.165		
Uniformity		U	-	70	80	-	%	Note1 Note6
NTSC		-	-	-	50	-	%	Note 5
Luminance		L		185	230	-	cd/m^2	Note1 Note7

Test Conditions:

1. The ambient temperature is 25±2℃.humidity is 65±7%
2. The test systems refer to Note 1 and Note 2.
3. Testing invertor: TDK/TAD347SR-4

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。

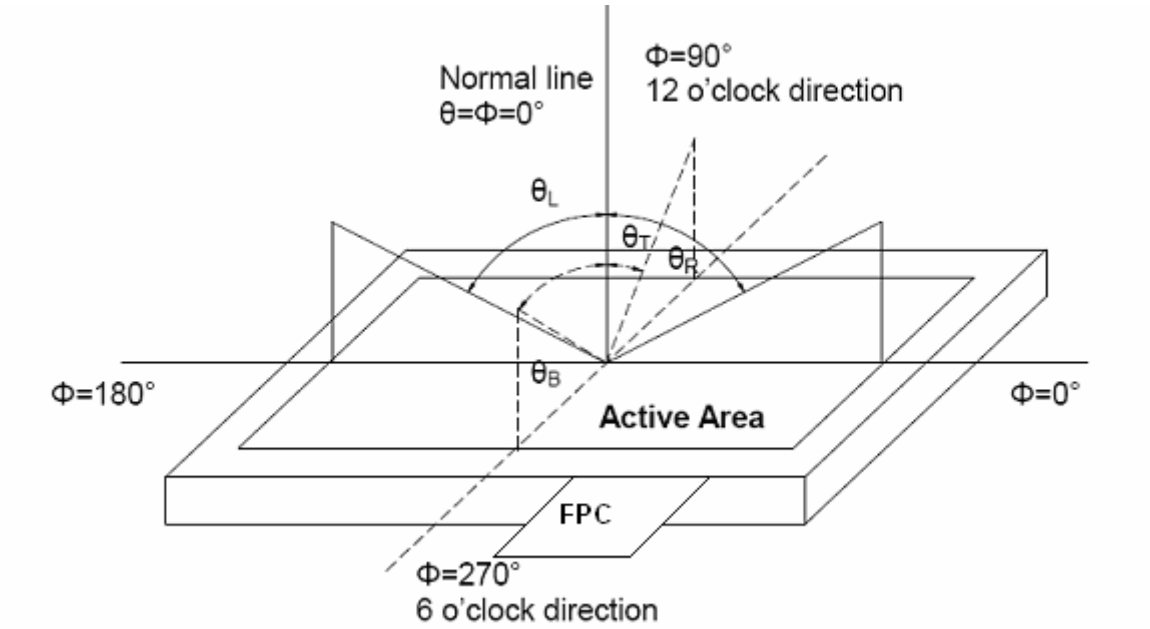


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

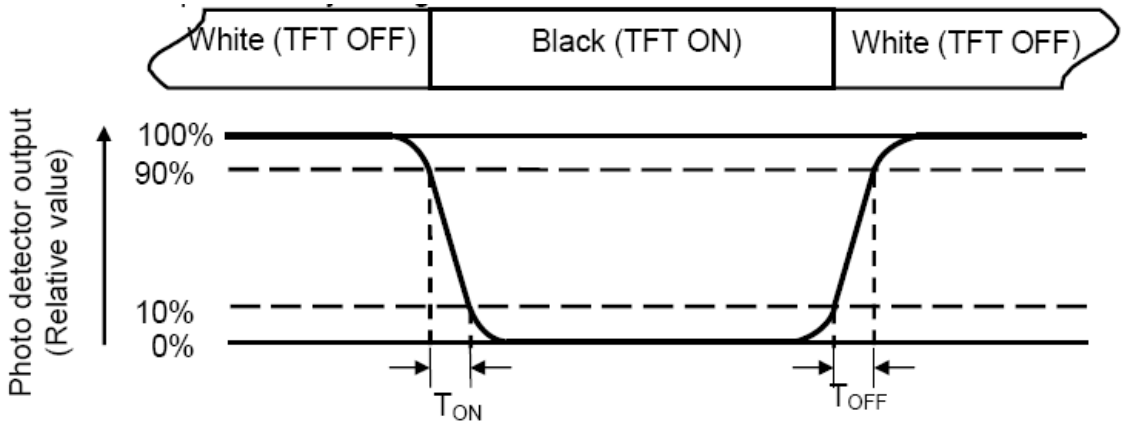
“White state “:The state is that the LCD should driven by Vwhite.

“Black state”: The state is that the LCD should driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

L-------Active area length W----- Active area width

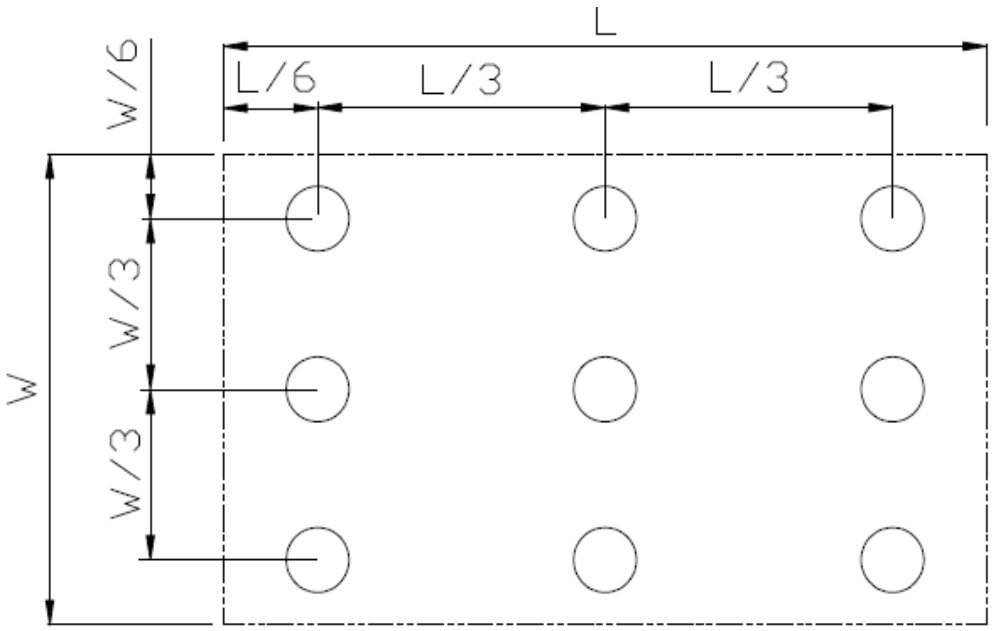


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance :

Measure the luminance of white state at center point.

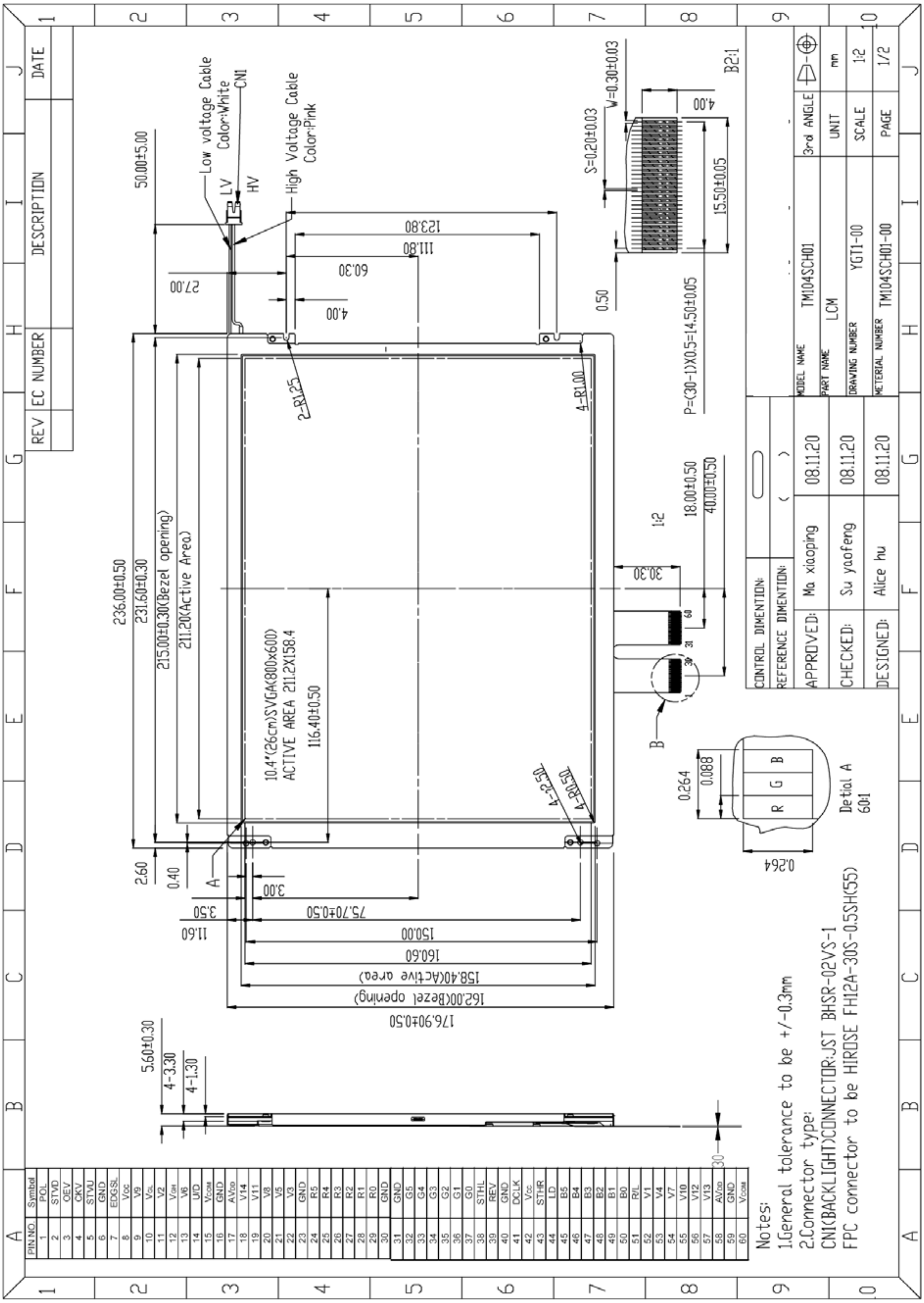
7 Environmental / Reliability Test

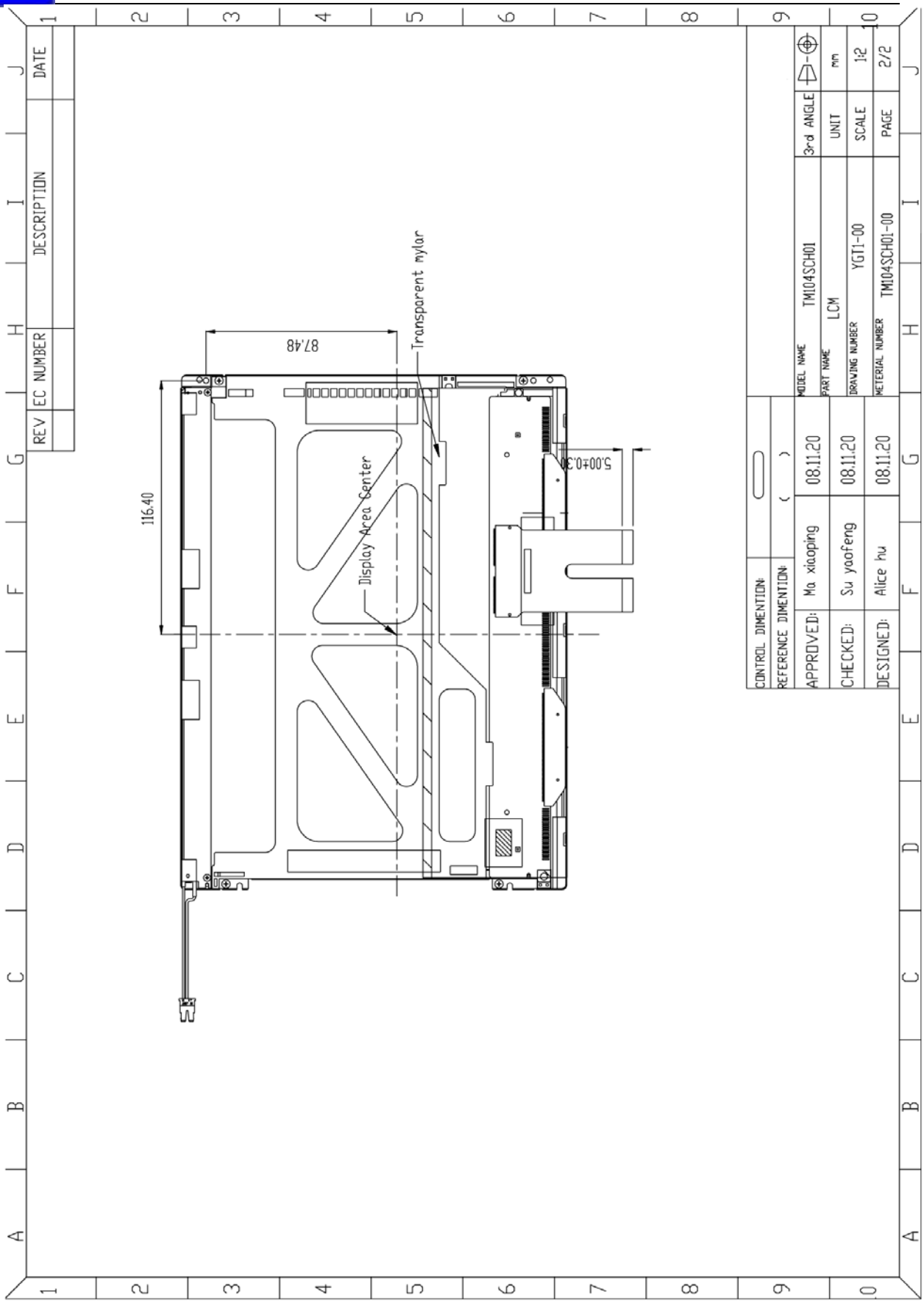
No	Test Item	Condition	Remark
1	High Temperature Operation	Ts=+70℃, 240hrs	Note1 IEC60068-2-2,GB2423.2—89
2	Low Temperature Operation	Ta=-20℃, 240hrs	IEC60068-2-1 GB2423.1—89
3	High Temperature Storage (non-operation)	Ta=+80℃, 240hrs	IEC60068-2-2, GB2423.2—89
4	Low Temperature Storage (non-operation)	Ta=-30℃, 240hrs	IEC60068-2-1 GB2423.1—89
5	High Temperature & High Humidity Operation	Ta = +60℃, 90% RH max,240 hours	Note2 IEC60068-2-3, GB/T2423.3—2006
6	Thermal Shock (non-operation)	-20℃ 30 min~+70℃ 30 min, Change time:5min, 100 Cycles	Start with cold temperature, end with high temperature IEC60068-2-14,GB2423.22—87
7	Electro Static Discharge (operation)	C=150pF,R=330Ω, Air:±15Kv, Contact:±8Kv, 10times/terminal	IEC61000-4-2 GB/T17626.2—1998
8	Vibration (non-operation)	Frequency range:10～55Hz, Stroke:1.5mm Sweep:10Hz～55Hz～10Hz 2hours for each direction of X.y.z (6 hours for total)	IEC60068-2-6 GB/T2423.10—1995
9	Shock (non-operation)	80G 6ms, ±X,±Y,±Z 3 times for each direction	IEC60068-2-27 GB/T2423.5—1995
10	Package Drop Test	Height:80 cm,1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/2423.8—1995
11	Package Vibration Test	Random Vibration: 0.015GxG/Hz for 5-200Hz, -6dB/Octave from 200-500Hz 2 hours for each direction of X,Y,Z (6 hours for total)	IEC60068-2-34

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

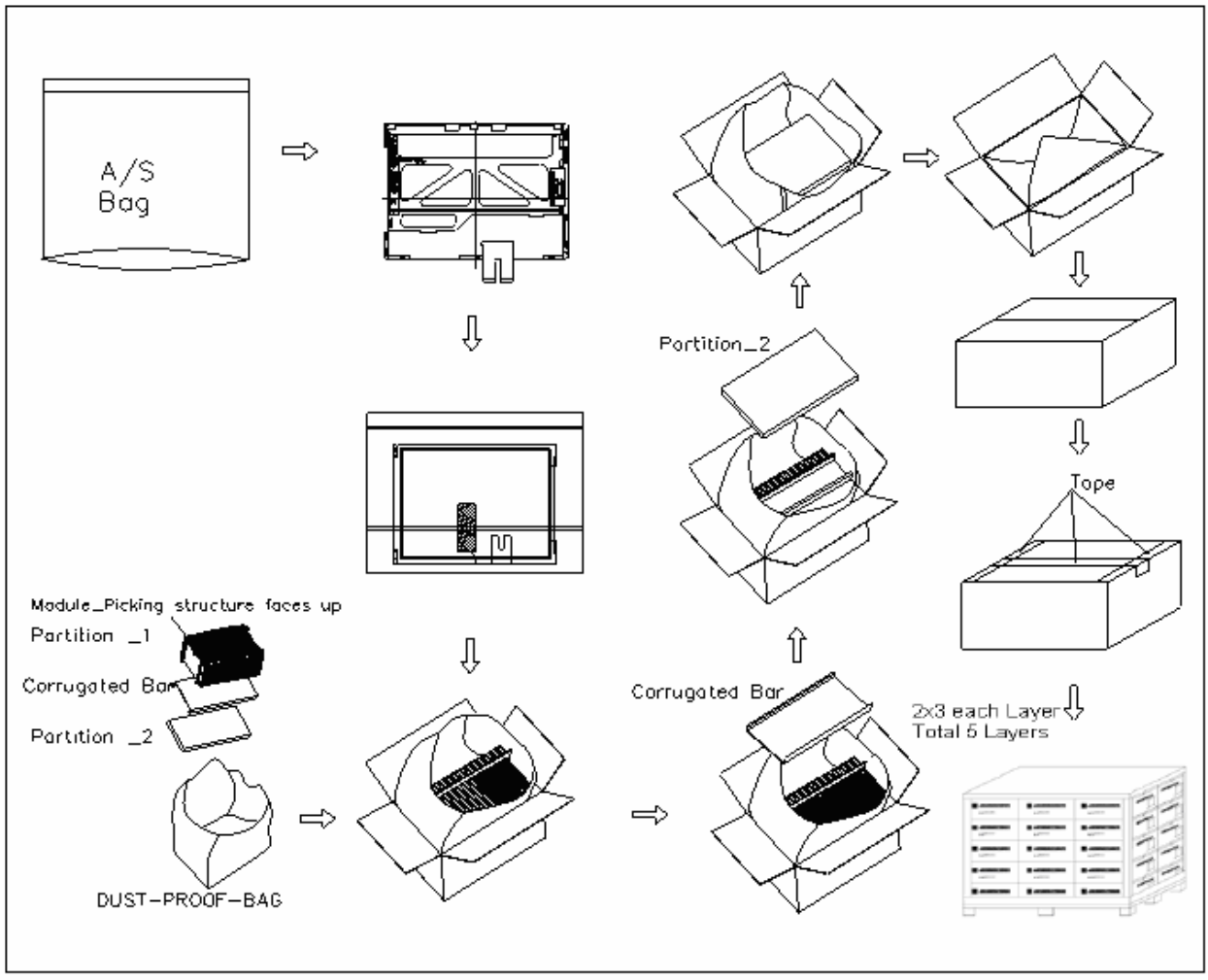
8 Mechanical Drawing


Low voltage Cable Color:White
CN1
High Voltage Cable Color:Pink
LV
HV
50.00±5.00
123.80
111.80
60.30
27.00
4.00
236.00±0.50
231.60±0.30
215.00±0.30(Bezel opening)
211.20(Active Area)
10.4"(26cm)SVGA(800x600)
ACTIVE AREA 211.2X158.4
116.40±0.50
2-R1.25
4-R1.00
4-R2.50
4-R0.50
3.00
3.50
11.60
75.70±0.50
150.00
160.60
158.40(Active area)
162.00(Bezel opening)
176.90±0.50
5.60±0.30
4-3.30
4-1.30
S=0.20±0.03
W=0.30±0.03
4.00
15.50±0.05
0.50
P=(30-1)X0.5=14.50±0.05
18.00±0.50
40.00±0.50
30.30
B2:1
1:2
Detial A 60:1
0.264
0.088
R G B
Notes:
1.General tolerance to be +/-0.3mm
2.Connector type:
CN1(BACKLIGHT)CONNECTOR:JST BHSR-02VS-1
FPC connector to be HIROSE FH12A-30S-0.5SH(55)
CONTROL DIMENTION:
REFERENCE DIMENTION:
APPROVED: Ma xiaoping 08.11.20
CHECKED: Su yaofeng 08.11.20
DESIGNED: Alice hu 08.11.20
MODEL NAME TM104SCH01
PART NAME LCM
DRAWING NUMBER YGT1-00
METERIAL NUMBER TM104SCH01-00
3rd ANGLE
UNIT mm
SCALE 1:2
PAGE 1/2
REV EC NUMBER DESCRIPTION DATE



9 Packing Drawing

No	Item	Model (Material)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	LCM module	TM104SCH01	236.00x176.90x5.60	0.28	25	
2	Partition_1	CORRUGATED PAPER	513x333x217	1.96	1	
3	Anti-static Bag	PE	247x256x0.05	0.04	25	
4	DUST-PROOF BAG	PE	700×530	0.06	1	
5	Partition_1	CORRUGATED PAPER	505x332x4.0	0.1	2	
6	CORRUGATED	CORRUGATED PAPER	513x248	0.09	2	
7	Carton	CORRUGATED PAPER	530x350x250	1.12	1	
8	Total weight(Kg)	11.5				



10 Precautions For Use of LCD Modules

10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.