

## Target

Ver 0.00

# **TFT LCD Specification**

# Model NO.: TD035SHEC1



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## Record of Reversion

Rev	Issued Date	Description
0.00	Apr, 08,2005	New

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### 1. FEATURES

The 3.5" LCD module is the Transflective active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and it's COG design. The LCD module includes touch panel, backlight and TFT LCD panel with minimal external circuits and components required.

### 2. GENERAL SPECIFICATION

lte	em	Description	Unit
Display Size (Diagon	al)	3.5 inch (8.9cm)	-
Display Type		Transflective	-
Active Area (HxV)		53.28 X 71.04	mm
Number of Dots (HxV	)	240 x RGB x 320	dot
Dot Pitch (HxV)		0.074 X 0.222	mm
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (6 bits)	-
Outline Dimension (H	xVxT)	64.3 X 87.1X2.95(Max 3.15)*	mm
Weight		TBD	g
	LCD Panel +	25 (Тур)	
Power consumption	T-CON + L/S		mW
	Backlight	288 (Typ, I <sub>F</sub> = 20mA)	

\* Exclude FPC and protrusions.

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## 3. INPUT/OUTPUT TERMINALS

## 3.1 TFT LCD module

Pin	Symbol	I/O	Description	Remark
1	DE	I	Data Enable Signal	
2	MCLK	I	LCM Pixel Clock	
3	RESET	I	Reset Signal	
4	YU	-	N/C	
5	DVSS	I	Digital Ground	
6	VCOM_I	I	VCOM Signal Input for LCD Panel	
7	VCOM_I	I	VCOM Signal Input for LCD Panel	
8	AVSS	I	Analog Ground	
9	VVEE	I	Input Voltage for gate off	
10	VVEE	I	Input Voltage for gate off	
11	VGH	I	Input Voltage for Level Shifter I/O	
12	VGH	I	Input Voltage for Level Shifter I/O	
13	DVSS	I	Digital Ground	
14	XL	-	N/C	
15	VCOM_H	0	Positive Power Output for VCOM	Connect big capacitor (10uF)
16	VCOM_O	0	VCOM Signal of IC Output	
17	VCOM_O	0	VCOM Signal of IC Output	
18	VCOM_L	0	Negative Power Output for VCOM	Connect big capacitor (10uF)
19	AVSS	I	Analog Ground	
20	DVDD	I	Digital Supply Power	
21	DVDD	I	Digital Supply Power	
22	AVDD	I	Analog Supply Power	
23	AVDD	I	Analog Supply Power	
24	YL	-	N/C	
25	DVSS	I	Digital Ground	
26	IV6P	0	for image sticking circuit	Negative voltage output for panel
27	XR	-	N/C	
28	TB_RL	I	Shift direction (Right/Left) H: D1→D240 L: D240→D1 Shift direction (Top/Bottom) H: Top→Bottom L: Bottom→Top	
29	R5	I	Data Bit Input (Red MSB)	
30	R4	1	Data Bit Input	
			'	

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31	R3	I	Data Bit Input	
32	R2	I	Data Bit Input	
33	R1	I	Data Bit Input	
34	R0	I	Data Bit Input (Red LSB)	
35	G5	I	Data Bit Input (Green MSB)	
36	G4	I	Data Bit Input	
37	G3	I	Data Bit Input	
38	G2	I	Data Bit Input	
39	G1	I	Data Bit Input	
40	G0	I	Data Bit Input (Green LSB)	
41	В5	I	Data Bit Input (Blue MSB)	
42	B4	I	Data Bit Input	
43	В3	I	Data Bit Input	
44	B2	I	Data Bit Input	
45	B1	I	Data Bit Input	
46	В0	I	Data Bit Input (Blue LSB)	
47		_	<b>6</b>	Connect big capacitor
47	47 150 0		for image sticking circuit	(4.7uF or more)
40	501		Digital Ground	
40	SCL	I	(Serial interface clock input)	
10	SDA		Digital Ground	
49	50A		(Serial interface data input/output)	
50	CS .		Digital Ground	
50			(Serial interface chip select input)	
51	DVSS	I	Digital Ground	
52	HSYNC	I	Horizontal SYNC Input	
53	DVSS	I	Digital Ground	
				CM=L:
54	CM		Display mode select	Full display mode (65k/262k color)
04				CM=H:
				Partial display mode (8 color)
55	vs		Positive Power Output for Source	
	-	0	Driver	
56	VSYNC	I	Vertical SYNC Input	
57	LED+	I	LED Power (Anode)	
58	LED+	I I	LED Power (Anode)	

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59	LED-	0	LED Power (Cathode)	
60	LED-	0	LED Power (Cathode)	
61	DVSS	I	Digital Ground	

## 3.2 Back light pin assignment



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#### 4. ABSOLUTE MAXIMUM RATINGS

					GND=0V
Item	Symbol	MIN	MAX	Unit	Remark
Logio Supply Voltago	DVDD	-0.3	+3.6	V	
Logic Supply Vollage	AVDD	-0.3	6	V	
Dower Supply for HA/ Driver	VGH	-0.3	+19	V	
Power Supply for m/v Driver	VVEE	-5.8	-5.2	V	Note 1
Backlight LED forward Voltage	V <sub>F</sub>	-	4	V	
Backlight LED reverse Voltage	V <sub>R</sub>	-	5	V	
Backlight LED forward current (Ta=25°C)	l <sub>F</sub>	-	30	mA	Note2
Operating Temperature	Topr	-10	+60	°C	
Storage Temperature	Tstg	-20	+70	٦	

Note1. The operating voltage is between +0.5V and -5.0V at the moment when the power is turned on

Note 2. Relation between maximum LED forward current and ambient temperature is showed as bellow.

Ambient Temperature vs.
 Allowable Forward Current



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### 5. ELECTRICAL CHARACTERISTICS

#### 5.1 Driving TET I CD Panel

5.1 Driving TFT LCD PanelT a=2							
Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logio Supply Voltag		DVDD	2.4	2.8	3.3	V	
Logic Supply Vollage	3	AVDD	4.8	5	5.6	V	
Dowor Supply for H/		VGH	9.5	10	10.5	V	
	v Driver	VVEE	-5.8	-5.5	-5.2	V	
Logic Ipput Voltage	High	VIH	0.8DVDD	-	DVDD+0.3	V	R[5:0], G[5:0],
Logic input voltage	Low	VIL	DVSS	_	0.2DVDD	V	B[5:0], CLK DE
Leakage current		L	-1	Ι	1	uA	
DVDD Supply Current		<b>I</b> dvdd	-	0.74	1.9	mA	Note 1,2
AVDD Supply Current		I <sub>AVDD</sub>	-	1.65	4.0	mA	Note 3
VGH Supply Current	t	I <sub>VGH</sub>	-	0.07	0.2	mA	
VVEE Supply Curre	nt	I <sub>VVEE</sub>	-	0.05	0.5	mA	

Note 1: The typical supply current specification is measured at the line inversion test pattern (black and white interlacing horizontal lines as the diagram shown below)



Note 2: DVDD rush currents accept 120mA, 500u sec during system booting.

Note 3: Gamma correction voltage is set to achieve the optimum at AVDD=5.0V. Use the voltage at level as close to 5.0V as possible.

#### 5.2 DC/DC Spec

ltem	Input voltage			Input Current	Input ripple(Max)	
	MIN	TYP	MAX			
DVDD	2.4V	2.8V	3.3V	0.74		
AVDD	4.8V	5V	5.6V	1.65	50 mV	Note 1
VGH	9.5V	10V	10.5V	0.07	150mV	
VVEE	-5.8 V	-5.5 V	-5.2 V	0.05		

Note 1: AVDD is analog voltage supply therefore use as less ripple as possible.

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Ta=25°C

#### 5.3 Driving backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I <sub>F</sub>	-	20	30	mA	LED/Part
LED Life Time	-	-	10,000	-	Hr	l <sub>F</sub> : 15mA
Forward Current Voltage	V <sub>F</sub>	-	3.6	4.0	V	l <sub>⊧</sub> : 20mA ,LED/Part

Note: Backlight driving circuit is recommend as the fix current circuit.

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#### 6. BLOCK DIAGRAM





## 7. TIMING CHART

## 7.1 Display timing

Display	Parameter	Symbol	Conditions	F	Llnit		
Display ModeParameterModeVertical cycleVertical data startVertical front porchVertical front porchVertical blanking periodVertical active areaHorizontal cycleHorizontal front porchHorizontal Sync Pulse widthHorizontal Data startHorizontal active areaClack frequency	Symbol	Conditions	MIN	TYP	MAX	Unit	
	Vertical cycle	VP		323	326	340	Line
	Vertical data start	VDS	VS+VBP	2	4	_	Line
	Vertical front porch	VFP		1	2	-	Line
	Vertical blanking period	VBL	VS+VBP+VFP	3	6	-	Line
	Vertical active area	VDISP		1	320	_	Line
NI I	Horizontal cycle	HP		260	280	300	dot
Normal	Horizontal front porch	HFP		4	10	—	dot
	Horizontal Sync Pulse width	HS		8	10	_	dot
	Horizontal Back porch	HBP		18	20	_	dot
	Horizontal Data start	HDS	HS+HBP	26	30	—	dot
	Horizontal active area	HDISP		240	240	240	dot
	Clock frequency	tclk		4.5	5.44	7.0	MHz
	Clock liequency	fclk			184		nS

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## Input timing chart

< Vertical Timing chart >



#### <Horizontal Timing chart>



\*1. The frequency of CLK should be continued whether in display or blank region to ensure IC operating normally.

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## Setup/ Hold Timing chart





## AC Characteristics:

Parameter	Symbol	Conditions		Unit		
T drameter	Cymbol	Conditions	MIN	TYP	MAX	Onic
Vertical Sync. Setup time	tvsys		20		_	ns
Vertical Sync. Hold time	tvsyh		20	Ι		ns
Horizontal Sync. Setup time	thsys		20	Ι		ns
Horizontal Sync. Hold time	thsyh		20	Ι		ns
Phase difference of Sync. Signal Falling edge	thv		-(HS-1)	_	1HP-1	clk
Clock "L" Period	tckl		30	50	70	%
Clock "H" Period	tckh		30	50	70	%
Data setup time	tds		20			ns
Data Hold time	tdh		20	_	_	ns
Digital logic input	Trise/Tfall				15	ns

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### 8. Power On/Off Sequence



Power on sequence:

VDD1/2 & AVDD & Input signal → RESET → VVEE → VGH

Power off sequence:

VGH → VVEE → VDD1/2 & AVDD & Input signal → RESET



Ta=25°C

## 9. Optical Characteristics

9.1 Optical Specification

(1) Back light Off

Item	Symbol		Symbol		Symbol		Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
	Θ 11+	Ə 12	CP = 2	70	85	-	Dograa	Note 9-1						
viewing Angles	Θ21+	Θ 22	UK - 2	75	95	-	Degree							
Chromaticity	\//bita	х	0 -0°	0.26	0.31	0.36	-	Note 9-3						
	vvnite	У	0-0	0.29	0.34	0.39	-							
Contrast Ratio	CR	2	Θ =0°	10:1	15:1	-	-	Note 9-2						
Reflectivity	R		Θ =0°	TBD	20	-	%	Note 9-4						

## (2) Back Light On

								Ta=25°C	
Item	Symbo	bl	Condition	MIN	TYP	MAX	Unit	Remarks	
	Θ 11+ Θ	12	CD = 2	100	120	-	Degree	Note 0 1	
viewing Angles	Θ 21+ Θ	22	UR = 2	90	110	-	Degree	Note 9-1	
Response Time	Tr+Tf		Θ =0°	-	35	45	ms	Note 9-5	
Contrast Ratio	CR		Θ =0°	80:1	100:1	-	-	Note 9-6	
Luminance	L		Θ =0° I <sub>F</sub> =20mA	TBD	130	-	cd/m <sup>2</sup>	Note 9-7	
NTSC	-		-	32	36	-	%	Note 9-7	
Uniformity	-		-	70	80	-	%	Note 9-8	
Chromaticity	\A/bita	х	0 -0°	0.26	0.31	0.36		Note 0.2	
	vville	у	0-0	0.28	0.33	0.38	-	Note 9-3	

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### 9.2 Basic measure condition

- (1) Driving voltage
  - VDD= 12.0V, VEE=-6.5V
- (2) Ambient temperature: Ta=25°C
- (3) Testing point: measure in the display center point and the test angle  $\Theta = 0^{\circ}$
- (4) Testing Facility

Environmental illumination: = 1 Lux

a. System A



b. System B









Note 9-2: Contrast ratio in back light off (Measure System A)

Contrast Ration is measured in optimum common electrode voltage.

 $CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$ 

Note 9-3: White chromaticity as back light off: (Measure System A)

Note 9-4: Reflectivity (R) (Measure System A)

In the measuring system A,. calculate the reflectance by the following formula.

 $Reflectivity(R) = \frac{Output from the white display panel}{Output from the reflectance standard} X Reflectance factor of reflectance standard$ 

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Contrast Ration is measured in optimum common electrode voltage.

- CR = Luminance with white image Luminance with black image
- Note 9-7: Luminance: (Measure System B) Test Point: Display Center
- Note 9-8: Uniformity (Measure System B)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:





#### 10. Reliability

No	Test Item	Condition
1	High Temperature Operation	Ta=+60°C, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40°C, 95% RH, 240hrs
3	Low Temperature Operation	Ta= -10°C, 240hrs
4	High Temperature Storage (non-operation)	Ta=+70°C, 240hrs
5	Low Temperature Storage (non-operation)	Ta= -20°C, 240hrs
<u> </u>	Thermal Charle (non-energian)	-20°C $\leftarrow \rightarrow$ 70°C,30 cycles
ю	Thermal Shock (non-operation)	30 min 30 min
	Surface Discharge (nen exerction) (LCD	C=150pF, R=330 Ω;
7		Discharge: Air: ±15kV; Contact: ±8kV
	sunace)	5 times / Point; 5 Points / Panel
		Frequency: 10~55Hz; Amplitude: 1.5mm
8	Vibration (non-operation)	Sweep Time: 11min
		Test Time: 2 hrs for each direction of X, Y, Z
0	Shock (non-onoration)	Acceleration: 100G; Period: 6ms
Э		Directions: ±X, ±Y, ±Z; Cycles: Three times

## **11. Handling Cautions**

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#### 11.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

- (1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is.
- (2) The machine and working table for the panel should have ESD protection strategy.
- (3) In handling the panel, ionized airflow decreases the charge in the environment is necessary.
- (4) In the process of assemble the module, shield case should connect to the ground.

#### **11.2 Environment**

Working environment of the panel should be in the clean room.

#### 11.3 Others

- (1) Turn off the power supply before connecting and disconnecting signal input cable.
- (2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.
- (3) Water drop on the surface or condensation as panel power on will corrode panel electrode.
- (4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.
- (5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible

#### 12. Application Note

#### 12.1 Note for image discharge circuit

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- (1) The image will remain on display when the power is suddenly cut off in abnormal condition, ie, unit dropped and battery fell out. The phenomenon is because the electrical charge well be held in pixel, if there is no extra input signal to release it, the residual image occurs.
- (2) The imaging discharge circuit is used for clearing the image residual on display. The circuit is designed on panel IC and customer can input signal to driver the function especially in the case that the battery or power supplier unit are removable.



(3) The circuit below is designed on panel IC to avoid image sticking.

#### 12.2 Note for V-com circuit

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The circuit is designed for V-com fine-tune, please refer the circuit below to design application circuit.



#### 12.3 Note for SPI command

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The LCM support the 3-pin serial interface to set internal register. Read/Write bit RW, Serial address A6 to A0 and serial data D7 to D0 are read at the rising edge of the serial clock, via the serial input pin. This data is synchronized on the rising edge of eighth serial clock and is then converted to parallel data. The serial interface signal timing chart is shown below.

#### Serial Interface Signal Timing Chart

Write Mode (RW=L)



The shift register and counter are reset to their initial values when the chip select signal is inactive. Do not set the chip select signal to inactive between transmission of an 8-bit address and 8-bit data set for the command.

When using SCL wiring, the module has to be designed carefully to avoid any noise coming from reflection or from external sources. We recommand checking operation with the actual module.

If there is a break in data transmission by RESETB or CS pulse, while transferring a Command or Parameter, before Bit D0 of the byte has been completed, then LCM will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CS) is activated after RESETB have been High state.



#### Read Mode (RW=H)



The read mode of the interface means that the micro controller reads data from the LCM. To do so the micro controller first has to send a command: the read status command. Then the following byte is transmitted in the opposite direction. After that CS is required to go high.

The LCM samples the SDA data input at rising SCL edges, but shifts SDA data output at falling SCL edges. Thus the micro controller is supposed to read SDA data at rising SCL edges.

After the read status command has been sent, the SDA line must be set to tristate not later then at the rising SCL edge of the last bit.

The LCM can read data of the Register0 to Register63



#### Serial interface and Reset waveform (VIH=0.8VDD1, VIL=0.2VDD1)



Serial interface and Reset														
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit								
Clock cycle	tCYS	-	150	-	-	ns								
Clock High Period	tPWH	-	60	-	-	ns								
Clock Low Period	tPWL	-	60	-	-	ns								
Data Set-up Time	tDSS	-	60	-	-	ns								
Data Hold Time	tDHS	-	60	-	-	ns								
CS High width	tCSW	-	1	-	-	us								
CS Set-up Time	tCSS	-	60	-	-	ns								
CS Hold Time	tCHS	-	70	-	-	ns								
SCL to CS	tSCC		40	-	-	ns								
Output Access Time	tACC		10	-	50	ns								
Output Disable Time	tODE		25	-	80	ns								
RSTB low width	tRSTBW	-	1000	-	-	ns								
RESET complete time	tRESC	-	-	-	1000	ns								

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#### Command descriptions :

#### Reset the internal register by setting low level the RESETB pin or software reset command.

Register	Default	Bit name			Se	etting	g val	ue			Description	Remark
[Dec]	[Hex]		D7	D6	D5	D4	D3	D2	D1	D0		
R0	00h	CHIPID[2:0]									Chip ID (Read only)	The Chip ID can be changed by
					0	0	0				ID 0(LDS312A)	MASK Option.
					0	0	1				ID 1(LDS312B)	
					-	-	-				-	
					1	1	0				ID 6	
					1	1	1				ID 7	
		REVID[2:0]									Revision ID (Read only)	The Revision ID can be changed
								0	0	0	REV 0	by MASK Option.
								0	0	1	REV 1	
								-	-	-	- PEV 5(E)	
								1	1	0	REV 6	
								1	1	1	BEV 7	
R1	68h	VCM8[7:5]						-	-	-	VCOM amplitude adjustment by VCOMH voltage change	VCOMH voltage change
	0011	10110[1:0]	0	0	0							veelin volage olarige
			0	0	1					-	-0.2V	
			0	1	0						-0.2V	
			0	1	1						0.0V	
			1	0	0						0.1V	
			1	0	1						0.2V	
			1	1	0						0.3V	
			1	1	1						0.4V	
		VCM8[3:0]			-				-	-		VCOM DC value setting
		V OIVIO[0.0]					0	0	0	0	VCOMH=3 90V · VCOML=0 20V	Voolin_Do valde setting
							0	0	0	1	VCOMH=3 92V : VCOMI =0.22V	
							0	0	1	0	VCOMH=3.94V : VCOMI =0.24V	
							0	0	1	1	VCOMH=3.96V VCOML=0.26V	
							0	1	0	0	VCOMH=3 98V · VCOMI =0 28V	
							0	1	0	1	VCOMH=4.00V : VCOML=0.30V	
							0	1	1	0	VCOMH=4.02V ; VCOML=0.32V	
							0	1	1	1	VCOMH=4.04V ; VCOML=0.34V	
							1	0	0	0	VCOMH=4.06V ; VCOML=0.36V	
							1	0	0	1	VCOMH=4.08V ; VCOML=0.38V	
							1	0	1	0	VCOMH=4.10V ; VCOML=0.40V	
							1	0	1	1	VCOMH=4.12V ; VCOML=0.42V	
							1	1	0	0	VCOMH=4.14V ; VCOML=0.44V	
							1	1	0	1	VCOMH=4.16V ; VCOML=0.46V	
							1	1	1	0	VCOMH=4.18V ; VCOML=0.48V	
							1	1	1	1	VCOMH=4.20V ; VCOML=0.50V	
R2	00h	MSEL									Interface mode select	Mode slection
			0								VSYNC + HSYNC + DE mode	
			1								VSYNC + HSYNC mode	
		SYNCP	L	<u> </u>							SYNC polarity select	
			<u> </u>	┣	0	—	—	—	—	—	Negative	
					1	L	L				Positive	
		DINT	L	L			<u> </u>	-	-		Input data mapping select	
			L	L		0	L				18 bit interface (262k color)	
			L	L		1	<u> </u>				16 bit interface (65k color, R:G:B=5:6:5)	
		DCKP	<u> </u>	┣		—		—	—	—	Input clock polarity change	
			⊢	<u> </u>		<u> </u>	0	<u> </u>	<u> </u>	—	INO CHANGE	
	<u>.</u>	VOTO: -		<u> </u>	<u> </u>	-	1	_	_			
R3	04h	VS1S[3:0]	⊢	1			-	-	-	-	Vertical valid data start time select (VBP)	
			⊢	1		<u> </u>	0	0	0	0		
			⊢	$\vdash$		-	0	0	0	1		$128 \times 160 = 13 \text{ HSYNC}$
			⊢	+		-	0	0	1	0		240x240 = 4 HSYNC
			┣—	1		—	0	0		1		
			⊢	+		-	0	1	0	1	5 HSVNC	
			⊢	+		-	-	-	-	-	-	
			⊢	+		-	1	1	1	1	15 HSYNC	
-												

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Register	Default	Bit name Setting value									Description	Bemark
[Dec]	[Hex]		D7	D6	D5	D4	D3	D2	D1	D0		
 P4	1Dh			<u> </u>				_			Horizontal valid data start time select (HRP)	Default
114	1DII	11313[3.0]		-	0	0	0	0	0	0	10 DCK	OVGA = 30 DCK
				-	0	0	0	0	0	1	10 DCK	QCIF+ = 44 DCK
					0	0	0	0	1	0	10 DCK	128x160 = 36 DCK
					0	0	0	0	1	1	10 DCK	240x240 = 30 DCK
					0	0	0	1	0	0	10 DCK	
					0	0	0	1	0	1	10 DCK	
					0	0	0	1	1	0	10 DCK	
					0	0	0	1	1	1	10 DCK	
					0	0	1	0	0	0	10 DCK	
					0	0	1	0	0	1	10 DCK	
					0	0	1	0	1	0	10 DCK	
					0	0	1	0	1	1	11 DCK	
					0	0	1	1	0	0	12 DCK	
					-	-	-	-	-	-	-	
					0	1	1	1	1	0	30 DCK	
					-	-	-	-	-	-		
Dr	04h	DA DOIT-01			1	1	1	1	1	1	b3 DCK	
К5	vin	PARS[7:0]	L_	_			_	_	_	_		mode
			0	0	0	0	0	0	0	0	Do not setting when PARS[8]=0, Gate256 is selected when PARS[8]=1	DF=H: Normal display line
			0	0	0	0	0	0	1	0	Gate2 is selected when PARS(8)=0, Gate257 is selected when PARS(8)=1	DE=L: Non-display line (White)
			0	0	0	0	0	0	1	0	Gate2 is selected when PARS[6]=0, Gate256 is selected when PARS[6]=1	
			0	0	0	0	0	0	-		Gales is selected when PARO[0]=0, Gale209 is selected when PARO[0]=1	When VSYNC+HSYNC mode,
			0	-	- 1	- 1	1	1	1	1	- Gate63 is selected when PARSI81=0. Gate319 is selected when PARSI81=1	Normal display line can be
			0	1	0	0	0	0	0	0	Gate64 is selected when PARS[8]=0. Gate320 is selected when PARS[8]=1	selected by R5,6,7 and 8.
			0	1	0	0	0	0	0	1	Gate65 is selected when PARS[8]=0. Do not setting when PARS[8]=1	
			0	1	0	0	0	0	1	0	Gate66 is selected when PARS[8]=0. Do not setting when PARS[8]=1	
			- 1	-	- 1	-	1	1	1	-	- Cate127 is selected when BADS[8]=0. Do not setting when BADS[8]=1	
			4	0	0	0	0	0	0	0	Cate 127 is selected when PARS[0]=0, Do not setting when PARS[0]=1	
				0	0	0	0	0	0	0	Gate 126 is selected when PARS[6]=0, Do hot setting when PARS[6]=1	
				0	0	0	0	0	0	1	Gate 129 is selected when PARS(6)=0, Do not setting when PARS(6)=1	
			1	0	0	0	0	0	1	0	Gate130 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	1	1	1	1	1	0	0	Gate252 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	0	1	Gate253 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	1	0	Gate254 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
DA	00h	DADOM	1	1	1	1	1	1	1	1	Gate255 is selected when PAR5[8]=0, Do not setting when PAR5[8]=1	
RO	oon	PARSIO								•		
										0	Gate1 – Gate255 IS selected	
	20h									-	Galezoo - Galezou Is selected	
π/	2011	FARE[1.0]		<u> </u>		_	<u> </u>	_	<u> </u>	<u> </u>		
			0	0	U	U	0	0	0	0	Do not setting when PARE[8]=0, Gate256 is selected when PARE[8]=1	DF=H: Normal display line
			0	0	0	0	0	0	1	0	Gate 1 is scienced when PARE[8]=0, Gate257 is selected when PARE[8]=1	DE=L: Non-display line (White)
			0	0	0	0	0	0	1	1	Gate3 is selected when PARE[8]=0. Gate250 is selected when PARE[9]=1	
			-	-	-	-	-	-	-	-	כמוכט ום סטונטונע אוונדרד הוגבנטידט, סמוכנטס ום סכוכטוכע אווכדר הוגבנסיד ו	When VSYNC+HSYNC mode,
			0	0	0	1	1	1	1	1	Gate31 is selected when PARE[8]=0, Gate286 is selected when PARE[8]=1	Normal display line can be
			0	0	1	0	0	0	0	0	Gate32 is selected when PARE[8]=0. Gate287 is selected when PARE[8]=1	selected by R5,6,7 and 8.
			0	0	1	0	0	0	0	1	Gate33 is selected when PARE[8]=0, Gate288 is selected when PARE[8]=1	
			0	0	1	0	0	0	1	0	Gate34 is selected when PARE[8]=0, Gate289 is selected when PARE[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	0	1	1	1	1	1	0	Gate63 is selected when PARE[8]=0. Do not setting when PARE[8]=1	
			1	0	1	1	1	1	1	1	Gate64 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	0	0	0	0	0	0	Gate65 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	0	0	0	0	0	1	Gate66 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	1	1	1	1	1	0	0	Gate252 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	0	1	Gate253 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	1	0	Gate254 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	1	1	Gate255 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
R8	00h	PARE[8]									Partial end line select	
										0	Gate1 – Gate255 is selected	
			1	1	1					1	Gate256 – Gate320 is selected	



Register	Default	Bit name	Setting value					Setting value Description				ue			Description	Remark
[Dec]	[Hex]		D7	D6	D5	D4	D3	D2	D1	D0						
R10	00h	CMDR									Software reset					
										0	Normal					
										1	Software reset					
R11	67h	VCM8[7:5]									VCOM amplitude adjustment by VCOMH voltage change	VCOMH voltage change				
			0	0	0						-0.3V	(8 color partial mode)				
			0	0	1						-0.2V					
			0	1	0						-0.1V					
			0	1	1						0.0V					
			1	0	0						0.1V					
			1	0	1						0.2V					
			1	1	0						0.3V					
			1	1	1						0.4V					

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## 12.4 Notes for FPC circuit layout



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## 13. Mechanical Drawing





## 14. Packing Drawing



- (2). Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.2 pcs desiccant put above the empty tray.
- (3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.
- (4) Put 1pc cardboard inside the carton bottom, then pack the finished package into the carton.
- (5). Carton sealing with adhesive tape.

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