Ver 0.1

TFT LCD Specification

Model NO.: TD035SHEC2

Customer Signature
Date

Table of Contents

Record of Reversion

Rev	Issued Date	Description
0.1	Mar, 7, 2005	New Create

1. FEATURES

The 3.5” LCD module is the Transflective active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and it’s COG design. The LCD module includes backlight and TFT LCD panel with minimal external circuits and components required.

2. GENERAL SPECIFICATION

Item		Description	Unit
Display Size (Diagonal)		3.5 inch (8.9cm)	-
Display Type		Transflective	-
Active Area (HxV)		53.28 X 71.04	mm
Number of Dots (HxV)		240 x RGB x 320	dot
Dot Pitch (HxV)		0.074 X 0.222	mm
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (18 bits)	-
Outline Dimension (HxVxT)		64.3 X 87.1X2.95(Max 3.15)*	mm
Weight		35	g
Power consumption	LCD Panel + T-CON + L/S	TBD (Typ)	mW
	Backlight	288 (Typ, I_F= 20mA)	

* Exclude FPC and protrusions.

3. INPUT/OUTPUT TERMINALS

3.1 TFT LCD module

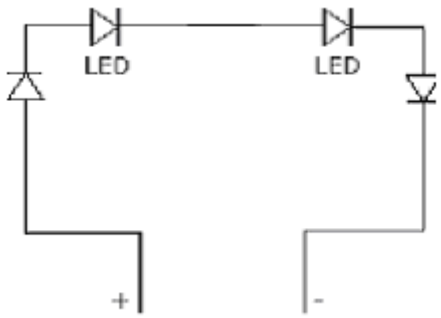
Recommend connector: FH23-61S-0.3SHW(05)/HIROSE

Pin	Symbol	I/O	Description	Remark
1	NC	--	NC pin	
2	MCLK	I	LCM Pixel Clock	
3	RESET	I	Reset Signal	Low active
4	YU	--	N/C	
5	DVSS	I	Digital Ground	
6	VCOM_I	I	VCOM Signal Input for LCD Panel	
7	VCOM_I	I	VCOM Signal Input for LCD Panel	
8	AVSS	I	Analog Ground	
9	VVEE	I	Input Voltage for gate off	
10	VVEE	I	Input Voltage for gate off	
11	VGH	I	Input Voltage for Level Shifter I/O	
12	VGH	I	Input Voltage for Level Shifter I/O	
13	DVSS	I	Digital Ground	
14	XL	-	N/C	
15	VCOM_H	O	Positive Power Output for VCOM	Connect capacitor (4.7~10uF/6V or more)
16	VCOM_O	O	VCOM Signal of IC Output	
17	VCOM_O	O	VCOM Signal of IC Output	
18	VCOM_L	O	Negative Power Output for VCOM	Connect capacitor (4.7~10uF/6V or more)
19	AVSS	I	Analog Ground	
20	DVDD	I	Digital Supply Power	
21	DVDD	I	Digital Supply Power	
22	AVDD	I	Analog Supply Power	
23	AVDD	I	Analog Supply Power	
24	YL	-	N/C	
25	DVSS	I	Digital Ground	
26	IV6P	O	N/C	
27	XR	-	N/C	

28	TB_RL	I	Shift direction (Right/Left) H: D1→D240 L: D240→D1 Shift direction (Top/Bottom) H: Top→Bottom L: Bottom→Top	
29	R5	I	Data Bit Input (Red MSB)	
30	R4	I	Data Bit Input	
31	R3	I	Data Bit Input	
32	R2	I	Data Bit Input	
33	R1	I	Data Bit Input	
34	R0	I	Data Bit Input (Red LSB)	
35	G5	I	Data Bit Input (Green MSB)	
36	G4	I	Data Bit Input	
37	G3	I	Data Bit Input	
38	G2	I	Data Bit Input	
39	G1	I	Data Bit Input	
40	G0	I	Data Bit Input (Green LSB)	
41	B5	I	Data Bit Input (Blue MSB)	
42	B4	I	Data Bit Input	
43	B3	I	Data Bit Input	
44	B2	I	Data Bit Input	
45	B1	I	Data Bit Input	
46	B0	I	Data Bit Input (Blue LSB)	
47	ISC	O	N/C	
48	SCL	I	Digital Ground (When not used) (Serial interface clock input)	
49	SDA	I	Digital Ground (When not used) (Serial interface data input/output)	
50	CS	I	Digital Ground (When not used) (Serial interface chip select input)	
51	DVSS	I	Digital Ground	
52	HSYNC	I	Horizontal SYNC Input	
53	DVSS	I	Digital Ground	
54	CM	I	Display mode select	CM=L: Full display mode (65k/262k color) CM=H: Partial display mode (8 color)

55	VS	O	Positive Power Output for Source Driver	Connect capacitor (4.7~10uF/6V or more)
56	VSYNC	I	Vertical SYNC Input	
57	LED+	I	LED Power (Anode)	
58	LED+	I	LED Power (Anode)	
59	LED-	O	LED Power (Cathode)	
60	LED-	O	LED Power (Cathode)	
61	DVSS	I	Digital Ground	

3.2 Back light pin assignment



(57,58) (59,60)

4. ABSOLUTE MAXIMUM RATINGS

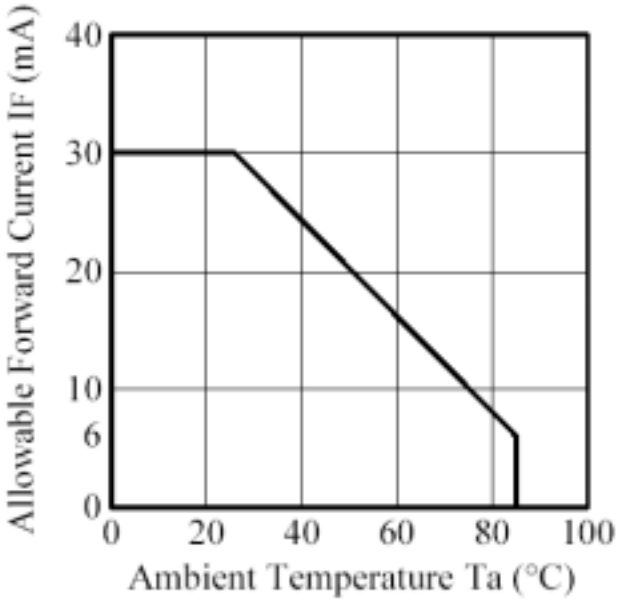
GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	DVDD	-0.3	+3.6	V	
	AVDD	-0.3	6	V	
Power Supply for H/V Driver	VGH	-0.3	+19	V	
	VVEE	-5.8	0	V	Note 1
Backlight LED forward Voltage	V_F	-	4	V	
Backlight LED reverse Voltage	V_R	-	5	V	
Backlight LED forward current (Ta=25℃)	I_F	-	30	mA	Note2
Operating Temperature	Topr	-10	+60	℃	
Storage Temperature	Tstg	-20	+70	℃	

Note1. The operating voltage is between +0.5V and –5.0V at the moment when the power is turned on

Note 2. Relation between maximum LED forward current and ambient temperature is showed as bellow.

■ Ambient Temperature vs. Allowable Forward Current



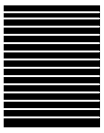
5. ELECTRICAL CHARACTERISTICS

5.1 Driving TFT LCD Panel

T a=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage		DVDD	2.5	2.8	3.6	V	
		AVDD	4.8	5.0	5.6	V	
Power Supply for H/V Driver		VGH	9.5	10	10.5	V	
		VVEE	-5.8	-5.5	-5.2	V	
Logic Input Voltage	High	VIH	0.8DVDD	–	DVDD	V	R[5:0], G[5:0], B[5:0], CLK DE,RESET, CM
	Low	VIL	DVSS	–	0.2DVDD		
Leakage current		IL	-1	–	1	uA	
DVDD Supply Current		I_{DVDD}	-	TBD	TBD	mA	Note 1,2
AVDD Supply Current		I_{AVDD}	-	TBD	TBD	mA	Note 3
VGH Supply Current		I_{VGH}	-	TBD	TBD	mA	
VVEE Supply Current		I_{VVEE}	-	TBD	TBD	mA	

Note 1: The typical supply current specification is measured at the line inversion test pattern (black and white interlacing horizontal lines as the diagram shown below)



Note 2: Gamma correction voltage is set to achieve the optimum at AVDD=5.0V. Use the voltage at level as close to 5.0V as possible.

5.2 DC/DC Spec

Item	Input voltage			Input Current	Input ripple(Max)	
	MIN	TYP	MAX			
DVDD	2.5V	2.8V	3.6V	TBD	TBD	
AVDD	4.8V	5.0V	5.6V	TBD	TBD	Note 1
VGH	9.5V	10V	10.5V	TBD	TBD	
VVEE	-5.8 V	-5.5 V	-5.2 V	TBD	TBD	

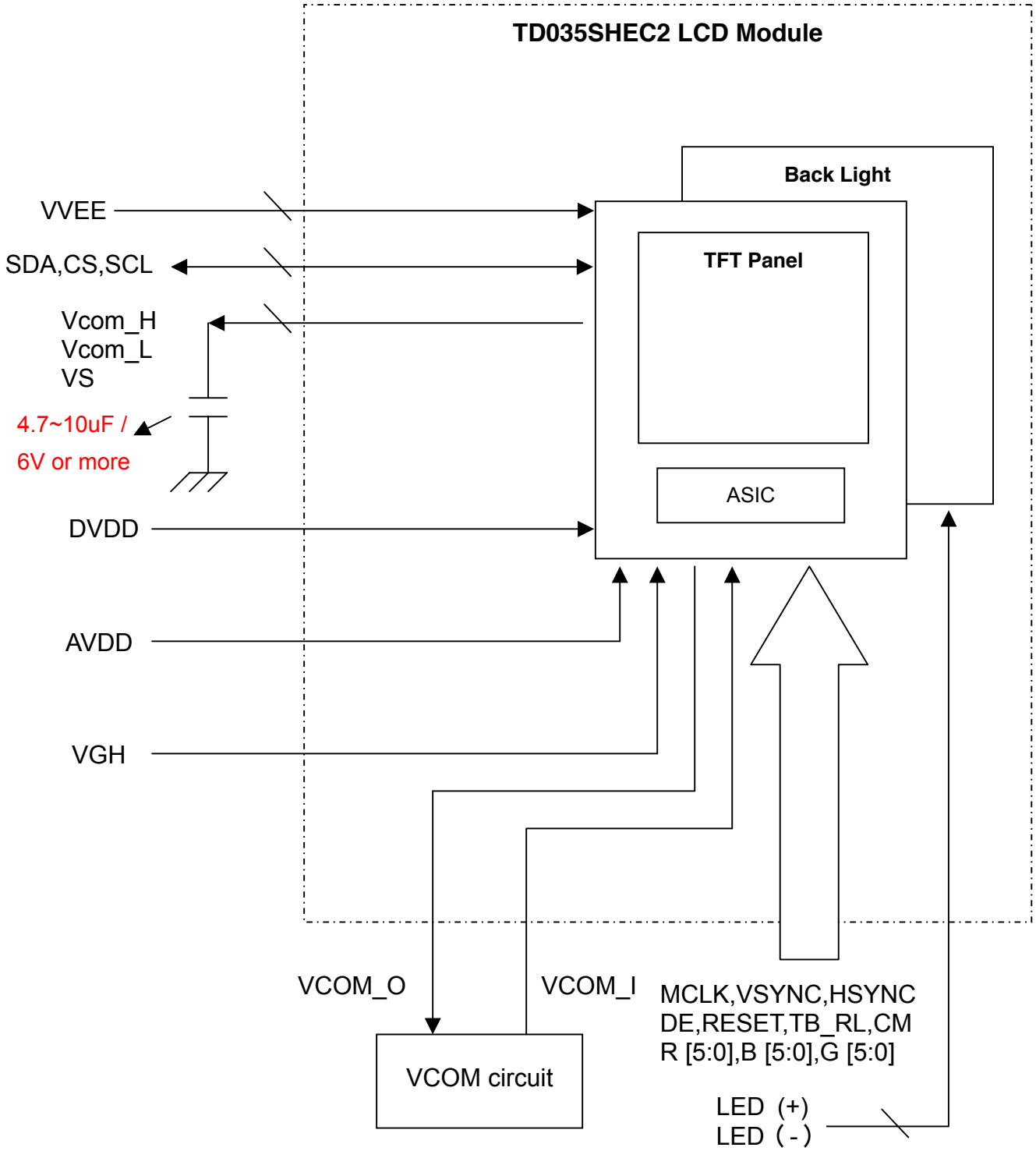
Note 1: AVDD is analog voltage supply therefore use as less ripple as possible.

5.3 Driving backlight Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	30	mA	LED/Part
LED Life Time	-	-	10,000	-	Hr	I_F: 15mA
Forward Current Voltage	V_F	-	3.6	4.0	V	I_F: 20mA ,LED/Part

Note: Backlight driving circuit is recommend as the fix current circuit.

6. BLOCK DIAGRAM



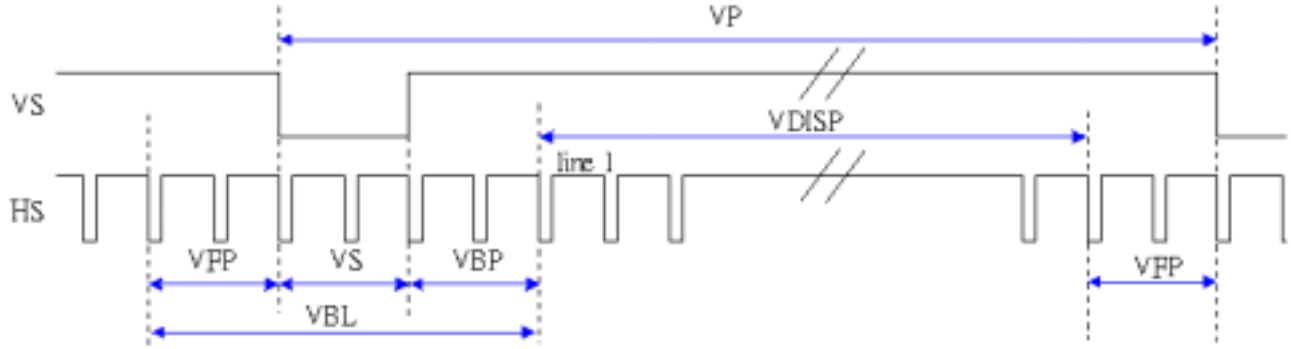
7. TIMING CHART

7.1 Display timing

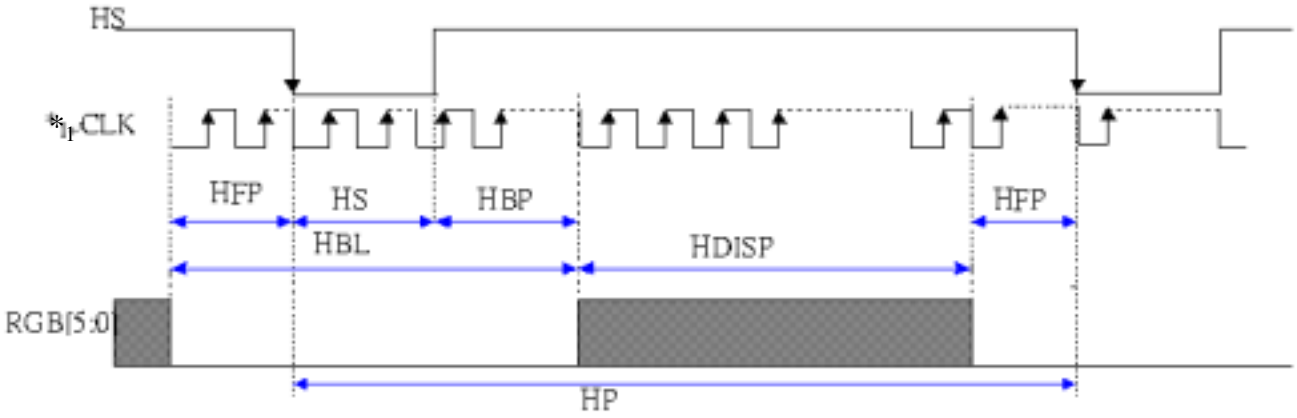
Display Mode	Parameter	Symbol	Conditions	Ratings			Unit
				MIN	TYP	MAX	
Normal	Vertical cycle	VP		323	326	340	Line
	Vertical data start	VDS	VS+VBP	2	4	–	Line
	Vertical front porch	VFP		1	2	–	Line
	Vertical blanking period	VBL	VS+VBP+VFP	3	6	–	Line
	Vertical active area	VDISP		–	320	–	Line
	Horizontal cycle	HP		260	280	300	dot
	Horizontal front porch	HFP		4	10	–	dot
	Horizontal Sync Pulse width	HS		8	10	–	dot
	Horizontal Back porch	HBP		18	20	–	dot
	Horizontal Data start	HDS	HS+HBP	26	30	–	dot
	Horizontal active area	HDISP		240	240	240	dot
	Clock frequency	fclk		5.02	6.39	6.85	MHz
		tclk		199	156	146	nS

Input timing chart

＜Vertical Timing chart＞

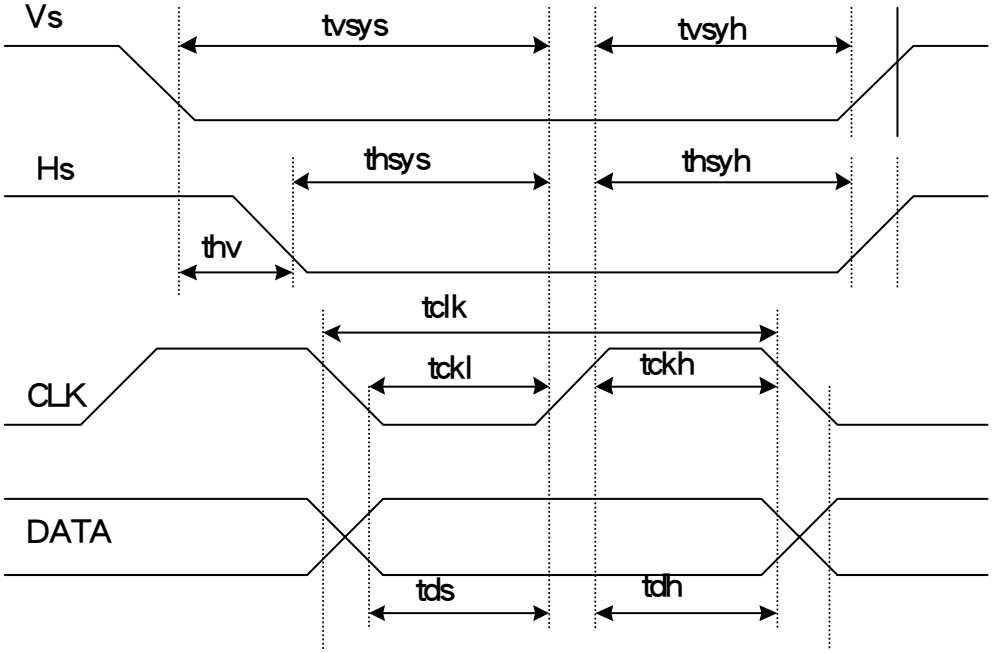


＜Horizontal Timing chart＞



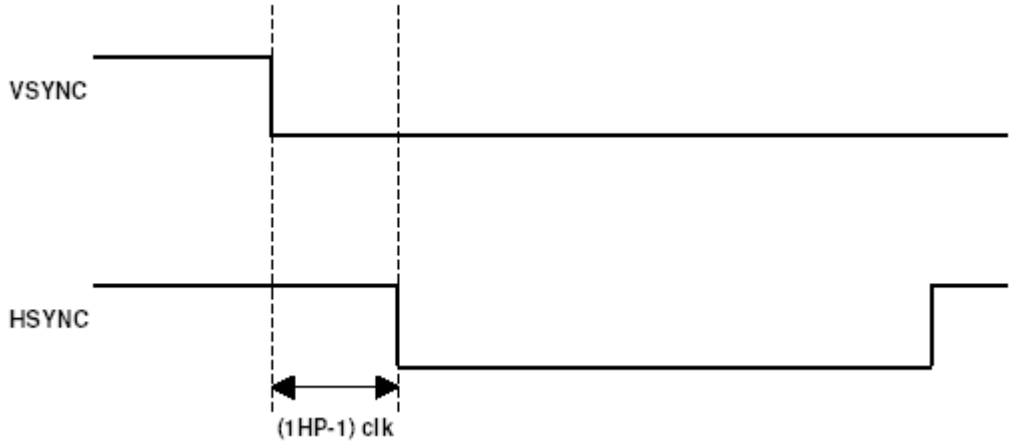
*1. The frequency of CLK should be continued whether in display or blank region to ensure IC operating normally.

Setup/ Hold Timing chart

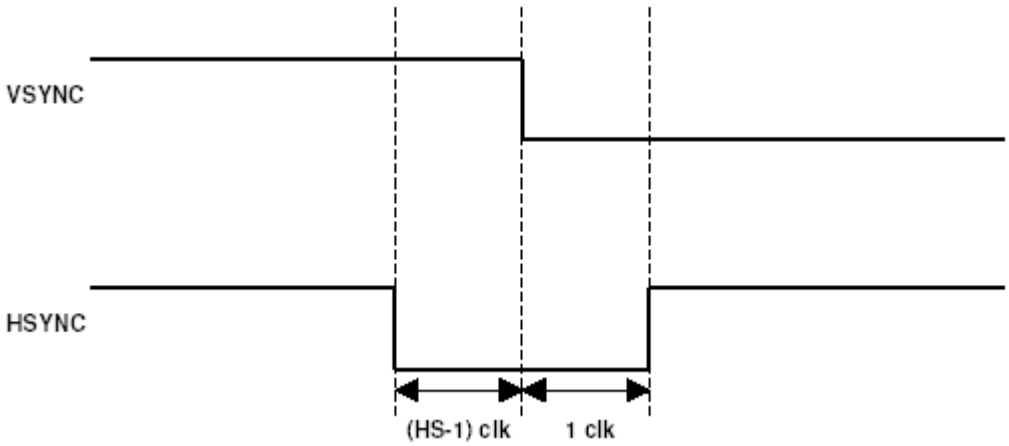


Phase difference of Sync.

Maximum Timing chart：



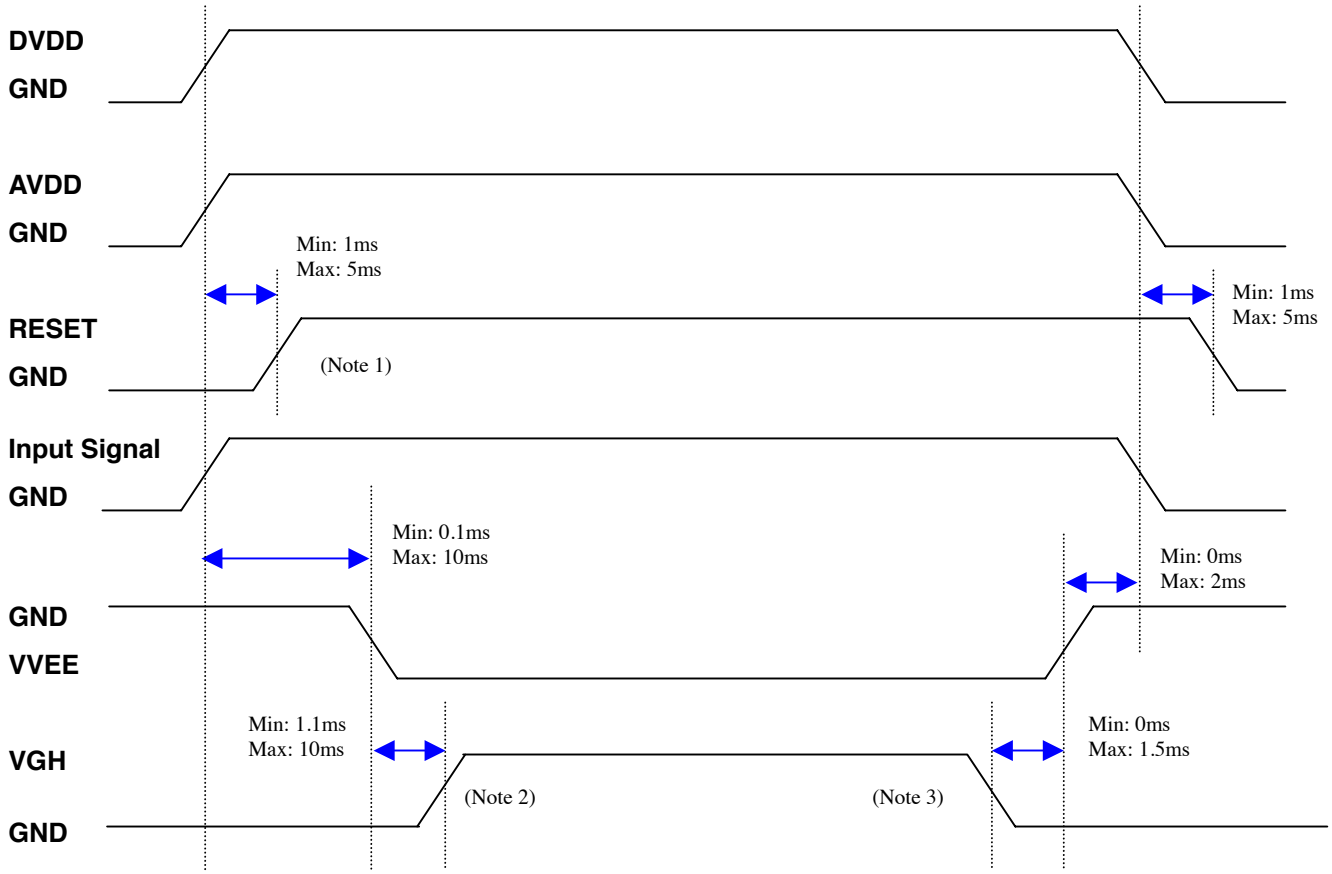
Minimum Timing chart:



7.2 AC Characteristics:

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Vertical Sync. Setup time	tvsys		20	–	–	ns
Vertical Sync. Hold time	tvsyh		20	–	–	ns
Horizontal Sync. Setup time	thsys		20	–	–	ns
Horizontal Sync. Hold time	thsyh		20	–	–	ns
Phase difference of Sync. Signal Falling edge	thv		-(HS-1)	–	1HP-1	clk
Clock “L” Period	tckl		30	50	70	%
Clock “H” Period	tckh		30	50	70	%
Data setup time	tds		20	–	–	ns
Data Hold time	tdh		20	–	–	ns
Digital logic input	Trise/Tfall				15	ns

8. Power On/Off Sequence



Power on sequence:

DVDD & AVDD & Input signal → RESET → VVEE → VGH

Power off sequence:

VGH → VVEE → DVDD & AVDD & Input signal → RESET

(Note 1) Display start at the 10th falling edge of VSYNC after RESET rising (first 1 frame=white)

(Note 2) To avoid image retention，please input white image for two frame before power off.

9. Optical Characteristics

9.1 Optical Specification

9.1.1 Back light Off

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11+Θ12		CR ≥ 2	70	85	-	Degree	Note 9-1
	Θ21+Θ22			75	95	-		
Chromaticity	White	x	Θ=0°	0.26	0.31	0.36	-	Note 9-3
		y		0.29	0.34	0.39	-	
Contrast Ratio	CR		Θ=0°	10:1	15:1	-	-	Note 9-2
Reflectivity	R		Θ=0°	TBD	20	-	%	Note 9-4

9.1.2 Back Light On

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	Θ11+Θ12		CR ≥ 2	100	120	-	Degree	Note 9-1
	Θ21+Θ22			90	110	-		
Response Time	Tr+Tf		Θ=0°	-	35	45	ms	Note 9-5
Contrast Ratio	CR		Θ=0°	80:1	100:1	-	-	Note 9-6
Luminance	L		Θ=0° I_F=20mA	TBD	130	-	cd/m^2	Note 9-7
NTSC	-		-	32	36	-	%	Note 9-7
Uniformity	-		-	70	80	-	%	Note 9-8
Chromaticity	White	x	Θ=0°	0.26	0.31	0.36	-	Note 9-3
		y		0.28	0.33	0.38		

9.2 Basic measure condition

9.2.1 Driving voltage:

VGH= 10.0V, VVEE= -5.5V

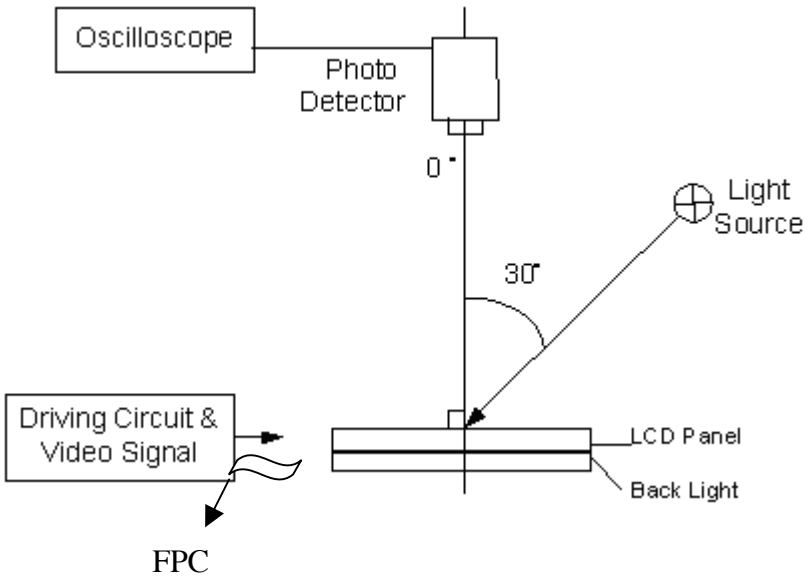
9.2.2 Ambient temperature: Ta=25℃

9.2.3 Testing point: measure in the display center point and the test angle Θ=0°

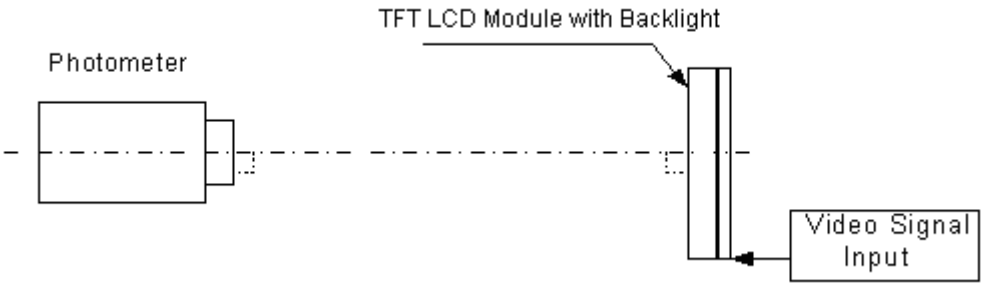
9.2.4 Testing Facility

Environmental illumination: ≤ 1 Lux

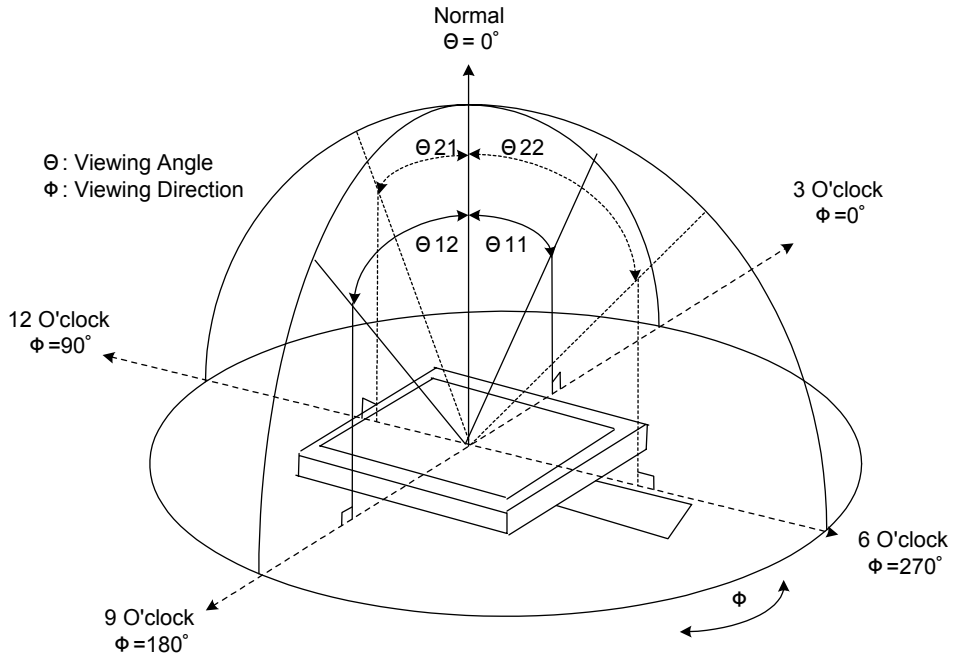
A. System A



B. System B



Note 9-1: Viewing angle diagrams (Measure System A)



Note 9-2: Contrast ratio in back light off (Measure System A)

Contrast Ratio is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

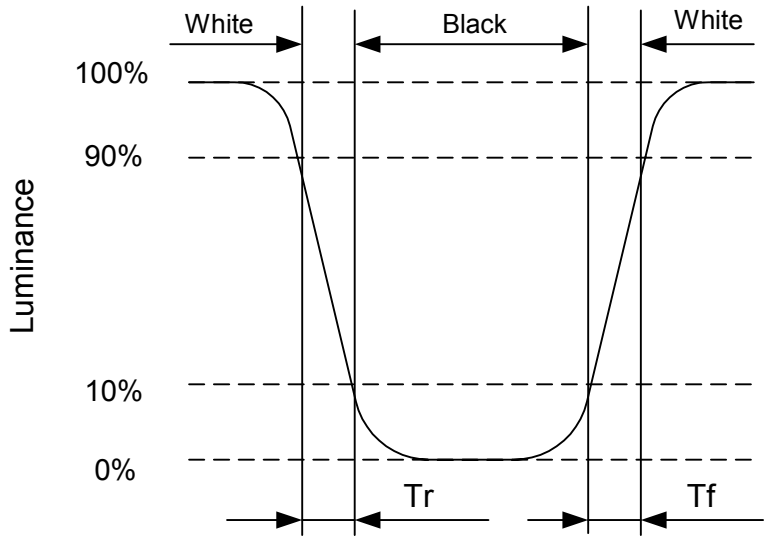
Note 9-3: White chromaticity as back light off: (Measure System A)

Note 9-4: Reflectivity (R) (Measure System A)

In the measuring system A,. Calculate the reflectance by the following formula.

$$\text{Reflectivity(R)} = \frac{\text{Output from the white display panel}}{\text{Output from the reflectance standard}} \text{ X } \text{Reflectance factor of reflectance standard}$$

Note 9-5: Definition of response time: (Measure System B)



Note 9-6: Contrast Ratio in back light On (Measure System B)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

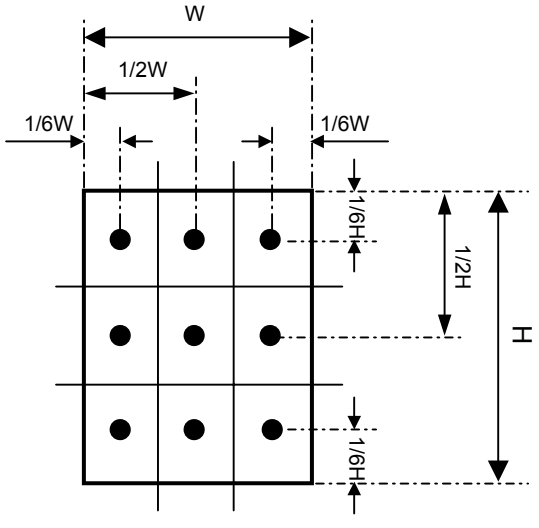
Note 9-7: Luminance: (Measure System B)

Test Point: Display Center

Note 9-8: Uniformity (Measure System B)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$



Active Area (W x H)

10. Reliability

No	Test Item	Condition
1	High Temperature Operation	Ta=+60℃, 240hrs
2	High Temperature & High Humidity Operation	Ta=+40℃, 95% RH, 240hrs
3	Low Temperature Operation	Ta= -10℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+70℃, 240hrs
5	Low Temperature Storage (non-operation)	Ta= -20℃, 240hrs
6	Thermal Shock (non-operation)	-20℃ ← → 70℃,30 cycles 30 min 30 min
7	Surface Discharge (non-operation) (LCD surface)	C=150pF, R=330 Ω; Discharge: Air: ±15kV; Contact: ±8kV 5 times / Point; 5 Points / Panel
8	Vibration (non-operation)	Frequency: 10~55Hz; Amplitude: 1.5mm Sweep Time: 11min Test Time: 2 hrs for each direction of X, Y, Z
9	Shock (non-operation)	Acceleration: 100G; Period: 6ms Directions: ±X, ±Y, ±Z; Cycles: Three times

11. Handling Cautions

11.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

11.1.1 In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is.

11.1.2 The machine and working table for the panel should have ESD protection strategy.

11.1.3 In handling the panel, ionized airflow decreases the charge in the environment is necessary.

11.1.4 In the process of assemble the module, shield case should connect to the ground.

11.2 Environment

Working environment of the panel should be in the clean room.

11.3 Others

11.3.1 Turn off the power supply before connecting and disconnecting signal input cable.

11.3.2 Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

11.3.3 Water drop on the surface or condensation as panel power on will corrode panel electrode.

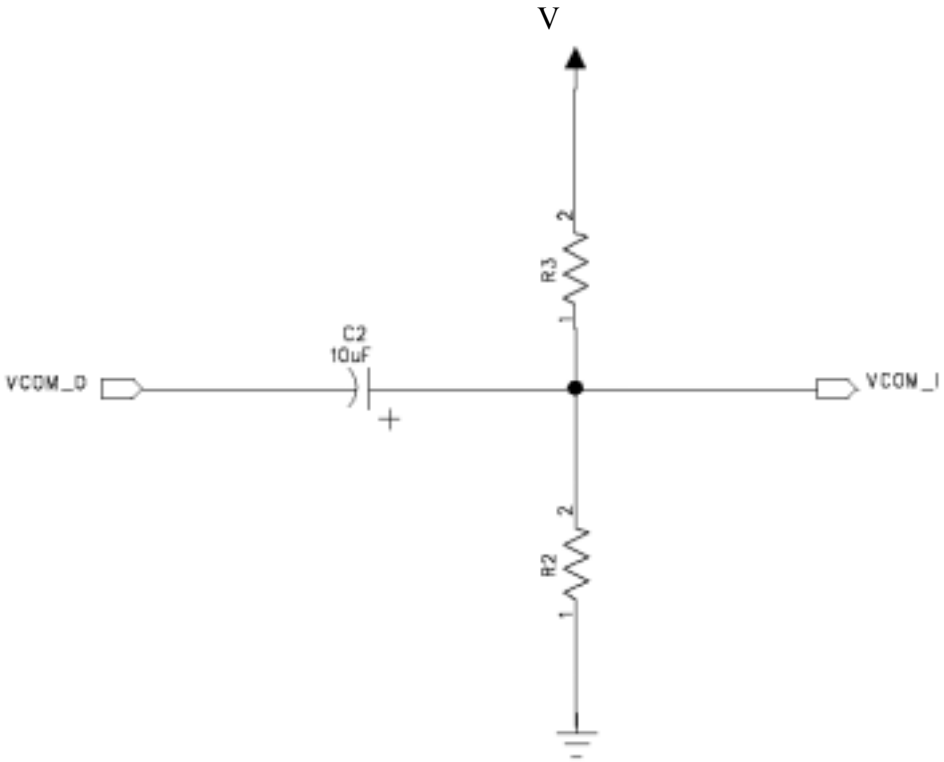
11.3.4 As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

11.3.5 In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible

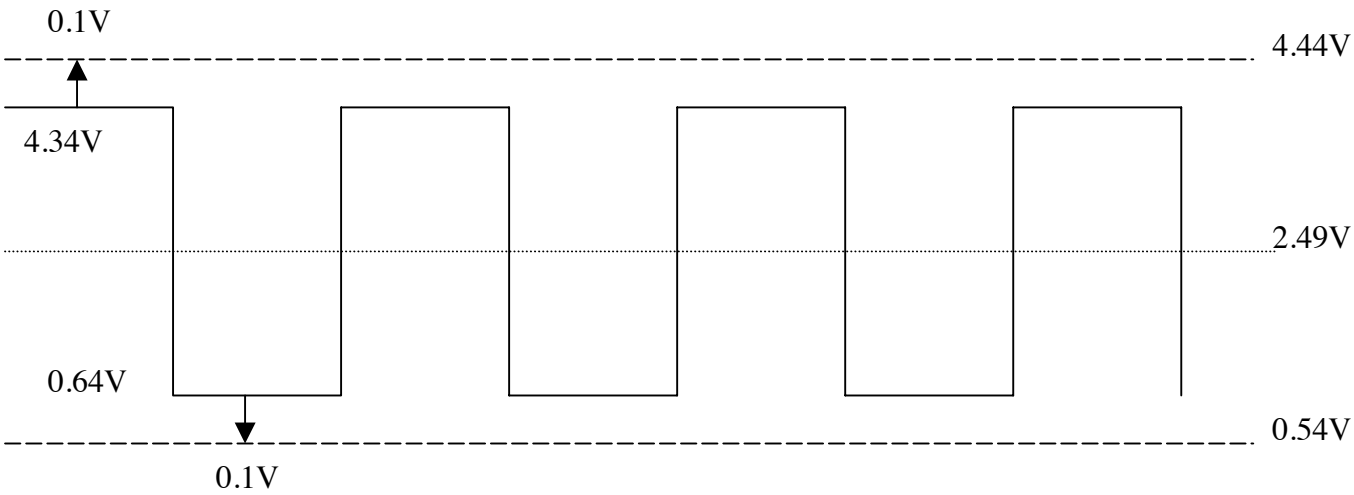
12. Application Note

12.1 Note for V-com circuit

The circuit is designed for V-com fine-tune, please refer the circuit below to design application circuit.



Vcom waveform



Note:

V：5 V

R2：10~30 K Ohm

R3：10~30 K Ohm

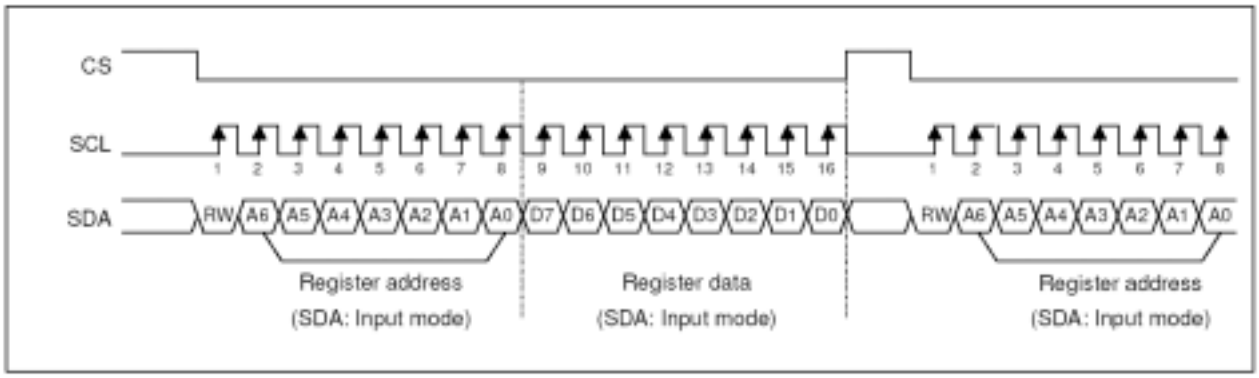
Resistors tolerance：0.5~1 %

12.2 Note for SPI command

The LCM support the 3-pin serial interface to set internal register. Read/Write bit RW, Serial address A6 to A0 and serial data D7 to D0 are read at the rising edge of the serial clock, via the serial input pin. This data is synchronized on the rising edge of eighth serial clock and is then converted to parallel data. The serial interface signal timing chart is shown below.

Serial Interface Signal Timing Chart

Write Mode (RW=L)

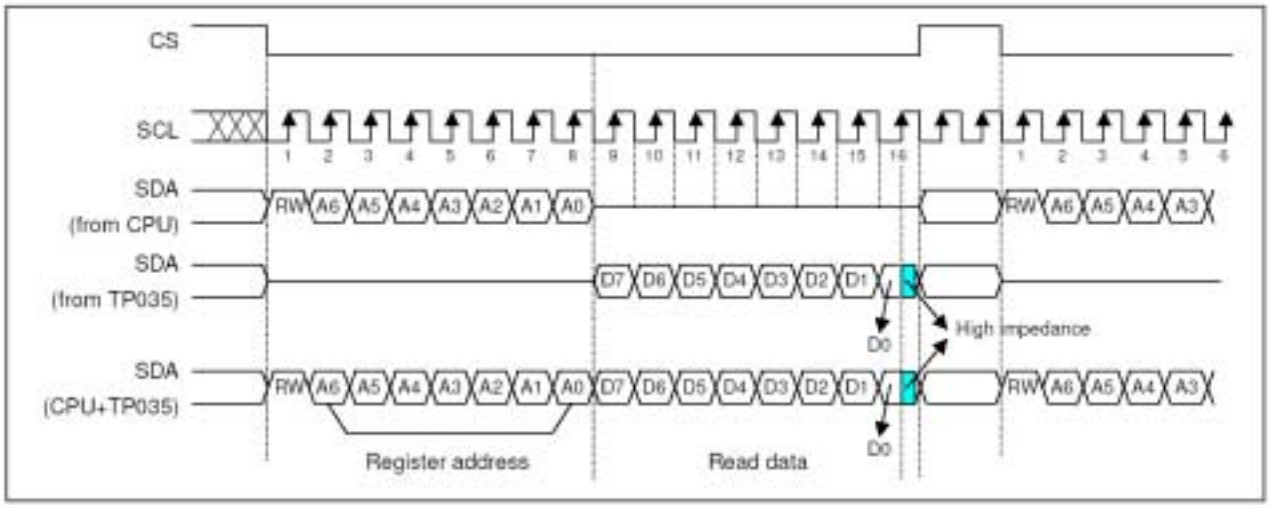


The shift register and counter are reset to their initial values when the chip select signal is inactive. Do not set the chip select signal to inactive between transmission of an 8-bit address and 8-bit data set for the command.

When using SCL wiring, the module has to be designed carefully to avoid any noise coming from reflection or from external sources. We recommand checking operation with the actual module.

If there is a break in data transmission by RESETB or CS pulse, while transferring a Command or Parameter, before Bit D0 of the byte has been completed, then LCM will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CS) is activated after RESETB have been High state.

Read Mode (RW=H)



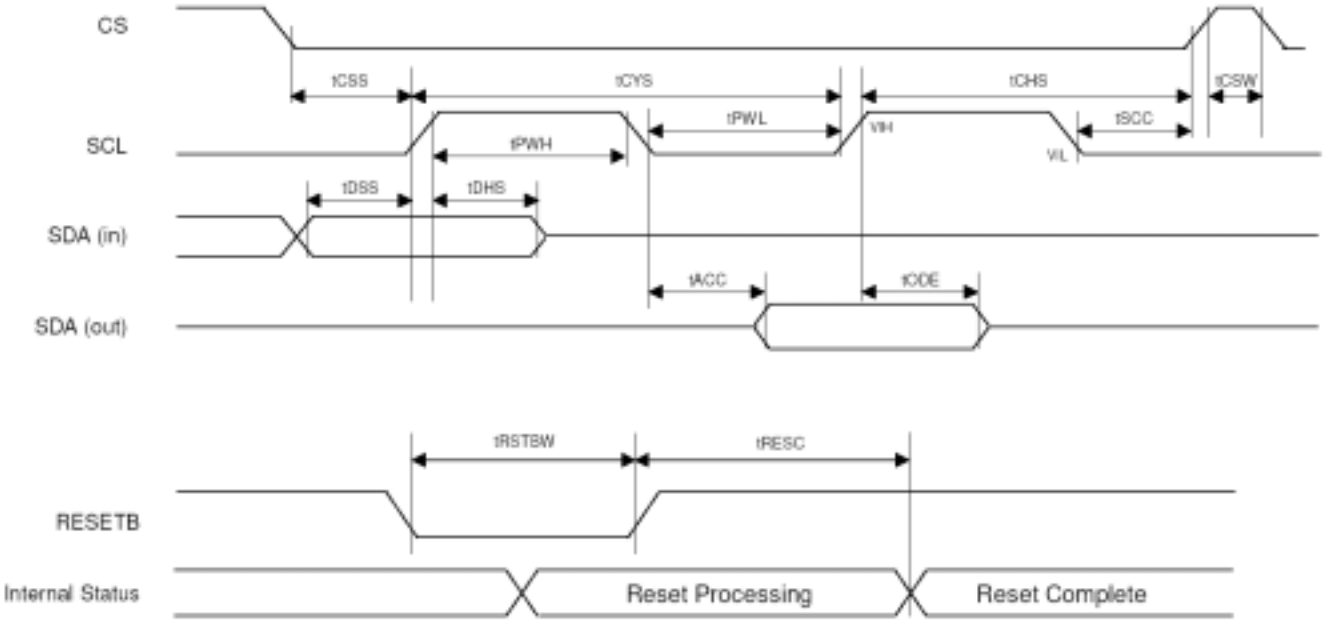
The read mode of the interface means that the micro controller reads data from the LCM.
To do so the micro controller first has to send a command: the read status command.
Then the following byte is transmitted in the opposite direction. After that CS is required to go high.

The LCM samples the SDA data input at rising SCL edges, but shifts SDA data output at falling SCL edges.
Thus the micro controller is supposed to read SDA data at rising SCL edges.

After the read status command has been sent, the SDA line must be set to tristate not later then at the rising SCL edge of the last bit.

The LCM can read data of the Register0 to Register63

Serial interface and Reset waveform (VIH=0.8VDD1, VIL=0.2VDD1)



Serial interface and Reset						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Clock cycle	tCYS	-	150	-	-	ns
Clock High Period	tPWH	-	60	-	-	ns
Clock Low Period	tPWL	-	60	-	-	ns
Data Set-up Time	tDSS	-	60	-	-	ns
Data Hold Time	tDHS	-	60	-	-	ns
CS High width	tCSW	-	1	-	-	us
CS Set-up Time	tCSS	-	60	-	-	ns
CS Hold Time	tCHS	-	70	-	-	ns
SCL to CS	tSCC		40	-	-	ns
Output Access Time	tACC		10	-	50	ns
Output Disable Time	tODE		25	-	80	ns
RSTB low width	tRSTBW	-	1000	-	-	ns
RESET complete time	tRESC	-	-	-	1000	ns

Command descriptions：

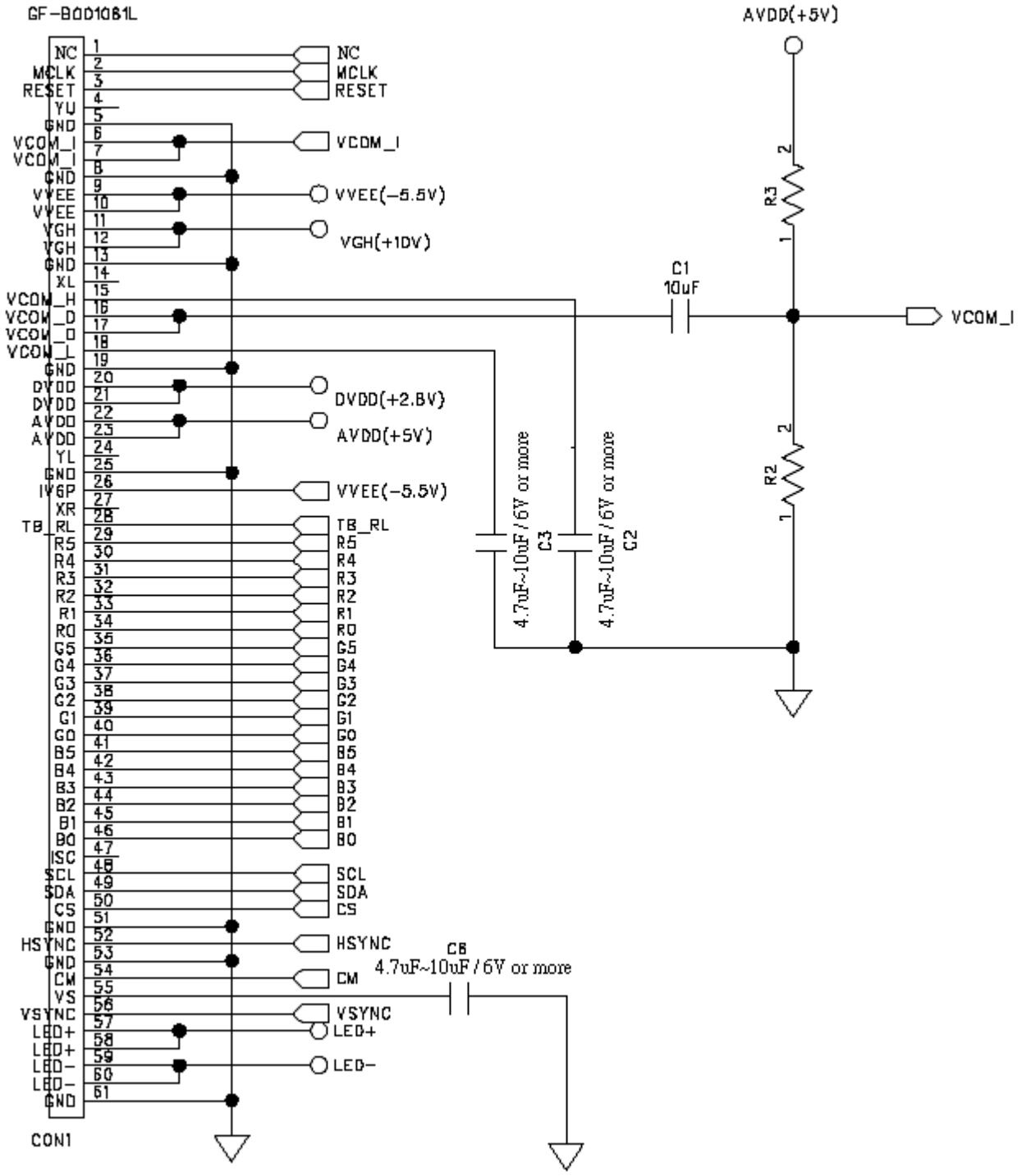
Reset the internal register by setting low level the RESETB pin or software reset command.

Register [Dec]	Default [Hex]	Bit name	Setting value								Description	Remark
			D7	D6	D	D4	D3	D2	D1	D0		
R0	00h	CHIPID[2:0]									Chip ID (Read only)	The Chip ID can be changed by MASK Option.
			1								D7=1 for SPFD5413	
					0	0	0				ID0	
					0	0	1				ID1	
					0	1	1				ID2	
					-	-	-					
					1	1	1				ID7	
		REVID[2:0]									Revision ID (Read only)	The Revision ID can be changed by MASK Option.
								0	0	0	REV 0	
								0	0	1	REV 1	
								0	1	0	REV2	
								0	1	1	REV3	
								-	-	-		
								1	1	1	REV 7	
R1	68h	VCM[7:5]									VCOM amplitude adjustment by VCOMH voltage change	VCOMH voltage change
			0	0	0						-0.3V	
			0	0	1						-0.2V	
			0	1	0						-0.1V	
			0	1	1						0.0V	
			1	0	0						0.1V	
			1	0	1						0.2V	
			1	1	0						0.3V	
			1	1	1						0.4V	
		VCM[3:0]									VCOM voltage select	VCOM_DC value setting
							0	0	0	0	VCOMH=3.90V ; VCOML=0.20V	
							0	0	0	1	VCOMH=3.92V ; VCOML=0.22V	
							0	0	1	0	VCOMH=3.94V ; VCOML=0.24V	
							0	0	1	1	VCOMH=3.96V ; VCOML=0.26V	
							0	1	0	0	VCOMH=3.98V ; VCOML=0.28V	
							0	1	0	1	VCOMH=4.00V ; VCOML=0.30V	
							0	1	1	0	VCOMH=4.02V ; VCOML=0.32V	
							0	1	1	1	VCOMH=4.04V ; VCOML=0.34V	
							1	0	0	0	VCOMH=4.06V ; VCOML=0.36V	
							1	0	0	1	VCOMH=4.08V ; VCOML=0.38V	
							1	0	1	0	VCOMH=4.10V ; VCOML=0.40V	
							1	0	1	1	VCOMH=4.12V ; VCOML=0.42V	
							1	1	0	0	VCOMH=4.14V ; VCOML=0.44V	
							1	1	0	1	VCOMH=4.16V ; VCOML=0.46V	
							1	1	1	0	VCOMH=4.18V ; VCOML=0.48V	
							1	1	1	1	VCOMH=4.20V ; VCOML=0.50V	
R2	00h											Mode slection
		SYNCP									SYNC polarity select	
				0							Negative	
				1							Positive	
		DINT			0						Input data mapping select	
					1						18 bit interface (262k color)	
											16 bit interface (65k color, R:G:B=5:6:5)	
		DCKP									Input clock polarity change	
						0					No change	
						1					Change	
R3	04h	VSTS[3:0]									Vertical valid data start time select (VBP)	Default: QVGA = 4 HSYNC QCIF+ = 7 HSYNC 128x160 = 13 HSYNC 240x240 = 4 HSYNC
							0	0	0	0	2 HSYNC	
							0	0	0	1	2 HSYNC	
							0	0	1	0	2 HSYNC	
							0	0	1	1	3 HSYNC	
							0	1	0	0	4 HSYNC	
							0	1	0	1	5 HSYNC	
							-	-	-	-	-	
							1	1	1	1	15 HSYNC	

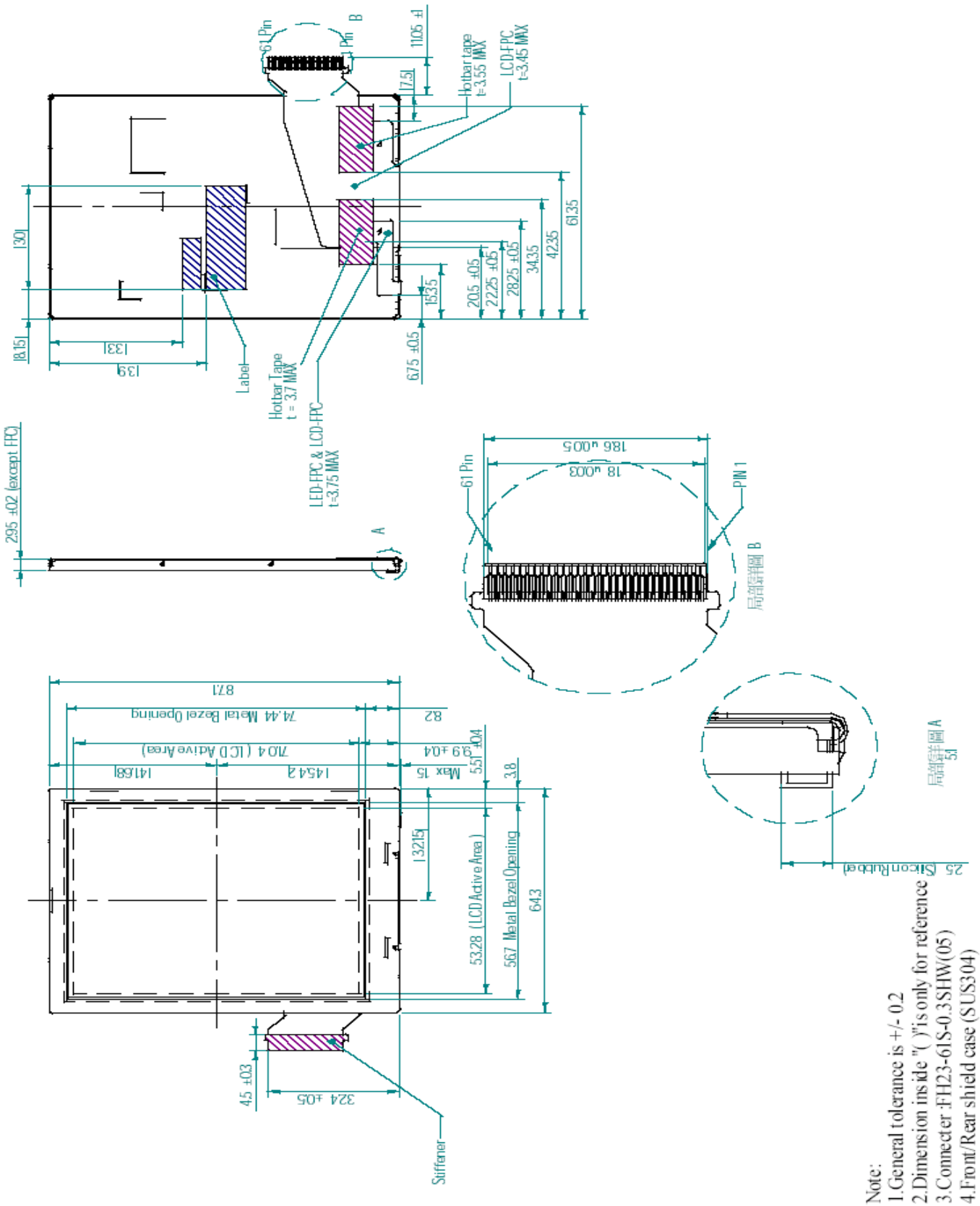
Register [Dec]	Default [Hex]	Bit name	Setting value								Description	Remark
			D7	D6	D5	D4	D3	D2	D1	D0		
R4	1Dh	HSTS[5:0]									Horizontal valid data start time select (HBP)	Default: QVGA = 30 DCK QCIF+ = 44 DCK 128x160 = 36 DCK 240x240 = 30 DCK
				0	0	0	0	0	0	0	10 DCK	
				0	0	0	0	0	1	0	10 DCK	
				0	0	0	0	1	0	0	10 DCK	
				0	0	0	0	1	1	0	10 DCK	
				0	0	0	1	0	0	0	10 DCK	
				0	0	0	1	0	1	0	10 DCK	
				0	0	0	1	1	0	0	10 DCK	
				0	0	0	1	1	1	0	10 DCK	
				0	0	1	0	0	0	0	10 DCK	
				0	0	1	0	0	1	0	10 DCK	
				0	0	1	0	1	0	0	10 DCK	
				0	0	1	0	1	1	0	11 DCK	
				0	0	1	1	0	0	0	12 DCK	
					-	-	-	-	-	-	-	
				0	1	1	1	1	0	0	30 DCK	
					-	-	-	-	-	-	-	
				1	1	1	1	1	1	1	63 DCK	
R5	01h	PARS[7:0]									Partial start line select	When VSYNC+HSYNC mode, Normal display line can be selected by R5,6,7 and 8.
			0	0	0	0	0	0	0	0	Do not setting when PARS[8]=0, Gate256 is selected when PARS[8]=1	
			0	0	0	0	0	0	0	1	Gate1 is selected when PARS[8]=0, Gate257 is selected when PARS[8]=1	
			0	0	0	0	0	0	1	0	Gate2 is selected when PARS[8]=0, Gate258 is selected when PARS[8]=1	
			0	0	0	0	0	0	1	1	Gate3 is selected when PARS[8]=0, Gate259 is selected when PARS[8]=1	
			-	-	-	-	-	-	-	-	-	
			0	0	1	1	1	1	1	1	Gate63 is selected when PARS[8]=0, Gate319 is selected when PARS[8]=1	
			0	1	0	0	0	0	0	0	Gate64 is selected when PARS[8]=0, Gate320 is selected when PARS[8]=1	
			0	1	0	0	0	0	0	1	Gate65 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			0	1	0	0	0	0	1	0	Gate66 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	1	1	1	1	1	1	1	Gate127 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	0	0	0	0	0	0	0	Gate128 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	0	0	0	0	0	0	1	Gate129 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	0	0	0	0	0	1	0	Gate130 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	1	1	1	1	1	0	0	Gate252 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	0	1	Gate253 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	1	0	Gate254 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
			1	1	1	1	1	1	1	1	Gate255 is selected when PARS[8]=0, Do not setting when PARS[8]=1	
R6	00h	PARS[8]									Partial start line select	
										0	Gate1 – Gate255 is selected	
										1	Gate256 – Gate320 is selected	
R7	20h	PARE[7:0]									Partial end line select	When VSYNC+HSYNC+DE mode, DE=H: Normal display line DE=L: Non-display line (White) When VSYNC+HSYNC mode, Normal display line can be selected by R5,6,7 and 8.
			0	0	0	0	0	0	0	0	Do not setting when PARE[8]=0, Gate256 is selected when PARE[8]=1	
			0	0	0	0	0	0	0	1	Gate1 is selected when PARE[8]=0, Gate257 is selected when PARE[8]=1	
			0	0	0	0	0	0	1	0	Gate2 is selected when PARE[8]=0, Gate258 is selected when PARE[8]=1	
			0	0	0	0	0	0	1	1	Gate3 is selected when PARE[8]=0, Gate259 is selected when PARE[8]=1	
			-	-	-	-	-	-	-	-	-	
			0	0	0	1	1	1	1	1	Gate31 is selected when PARE[8]=0, Gate286 is selected when PARE[8]=1	
			0	0	1	0	0	0	0	0	Gate32 is selected when PARE[8]=0, Gate287 is selected when PARE[8]=1	
			0	0	1	0	0	0	0	1	Gate33 is selected when PARE[8]=0, Gate288 is selected when PARE[8]=1	
			0	0	1	0	0	0	1	0	Gate34 is selected when PARE[8]=0, Gate289 is selected when PARE[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	0	1	1	1	1	1	0	Gate63 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	0	1	1	1	1	1	1	Gate64 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	0	0	0	0	0	0	Gate65 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	0	0	0	0	0	1	Gate66 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			-	-	-	-	-	-	-	-	-	
			1	1	1	1	1	1	0	0	Gate252 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	0	1	Gate253 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	1	0	Gate254 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
			1	1	1	1	1	1	1	1	Gate255 is selected when PARE[8]=0, Do not setting when PARE[8]=1	
R8	00h	PARE[8]									Partial end line select	
										0	Gate1 – Gate255 is selected	
										1	Gate256 – Gate320 is selected	

Register [Dec]	Default [Hex]	Bit name	Setting value								Description	Remark
			D7	D6	D5	D4	D3	D2	D1	D0		
R10	00h	CMDR									Software reset	
										0	Normal	
										1	Software reset	
R11	68h	VCM8[7:5]									VCOM amplitude adjustment by VCOMH voltage change	VCOMH voltage change (8 color partial mode)
			0	0	0						-0.3V	
			0	0	1						-0.2V	
			0	1	0						-0.1V	
			0	1	1						0.0V	
			1	0	0						0.1V	
			1	0	1						0.2V	
			1	1	0						0.3V	
			1	1	1						0.4V	

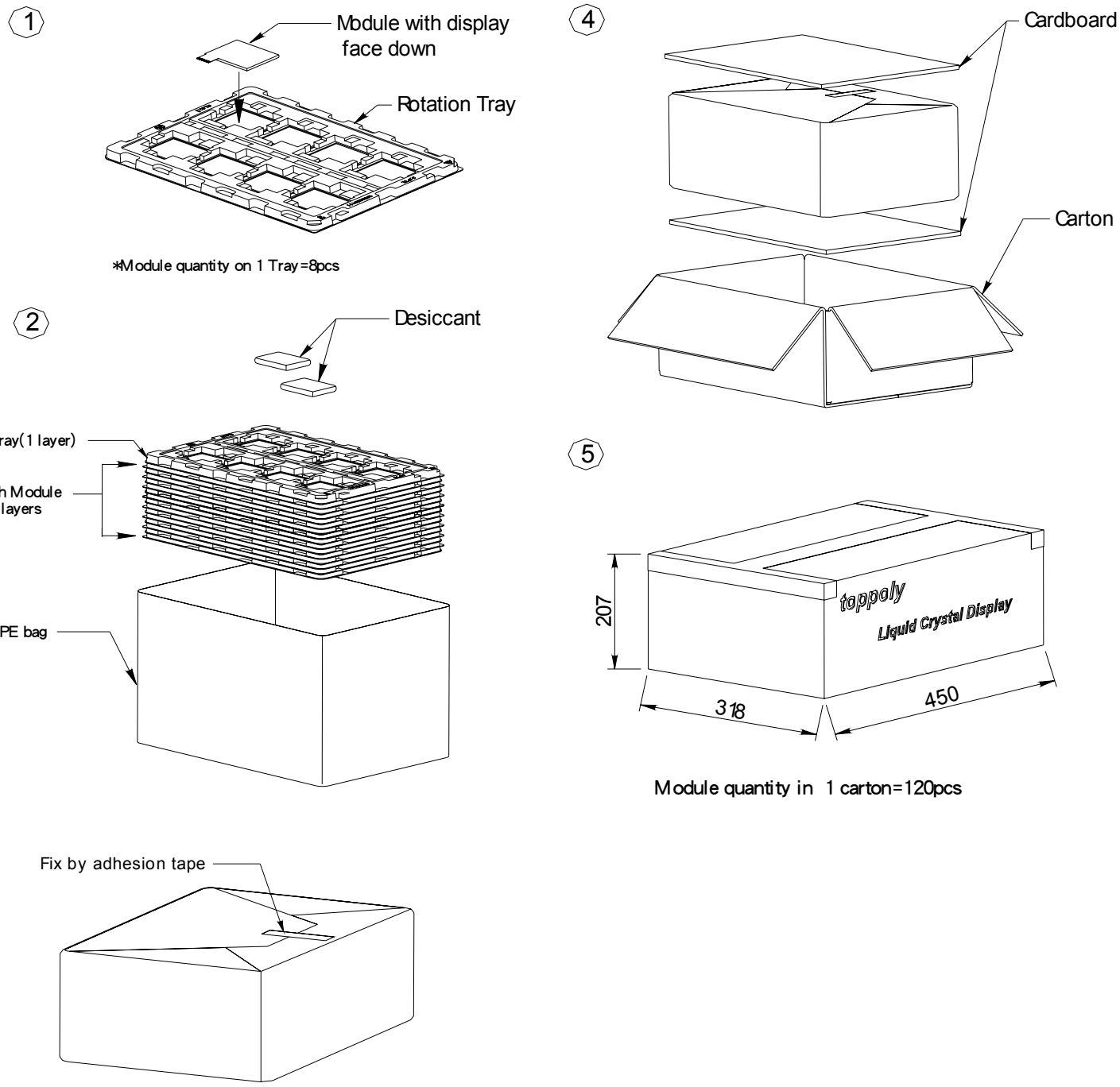
12.3 Note for FPC circuit layout



13. Mechanical Drawing



14. Packing Drawing



TD035SHEC1 module delivery packing method

14.1 Module packed into tray cavity with display face down.

14.2 Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.
2 pcs desiccant put above the empty tray.

14.3 Stacking tray unit put into the LDPE bag and fix by adhesive tape.

14.4 Put 1pc cardboard inside the carton bottom, then pack the finished package into the carton.

14.5 Carton sealing with adhesive tape.