TORISAN

ENGINEERING SPECIFICATIONS

TFT COLOR LCD MODULE

TM058WA-22L04

- 15cm (5.8 inch Wide) diagonal
- Resolution (400xR•G•Bx234 dots)
- With CFL backlight unit
- Nonglare surface type

(PRELIMINARY)

Ver. 2 Sep.10.2002

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■ *REVISION HISTORY*

DATE	REVISION NO.	PAGE	DESCRIPTIONS
Apl.10.2002	Ver.1	-	Initial release
Sep.10.2002	Ver.2	3	OPTICAL CHARACTERISTICS (1) Viewing angle range MIN Value→MAX Value
Sep.10.2002	Ver.2	9	Addition of DISPLAY AREA
Sep.10.2002	Ver.2	10	ELECTRICAL CHARACTERISTICS Power supply voltage for gatedriverVGL; (MIN) -16.5→-16.0V,(TYP) -17.0→-15.0V,(MAX) -17.5→-14.0V

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4.Please use this product correctly according to operating conditions and precautions for use stated in this document.
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7.Separate inspection standard spec is applied for cosmetic criteria.

8.If you should have questions on this product, please kindly contact our sales section.

■ *MECHANICAL CHARACTERISTICS*

ITEM	SPECIFICATION	UNIT
Module size	145.0(W)×89.0(H)×11.5typ(t)	mm
Resolution	400×R•G•B(W)×234(H)	pixel
Dot pitch	0.106(W)×0.307(H)	mm
Pixel pitch	0.318(W)×0.307(H)	mm
Active viewing area	127.2(W)×71.8(H)	mm
Bezel opening area	131.6(W)×75.9(H)	mm
Weight	165 TYP.	g

■ *ABSOLUTE MAXIMUM RATINGS*

ITEM		SYMBOL		CONDITIONS	MIN	MAX	UNIT	NOTE
Logic/Source power supply voltage		VSH		-	-0.3	6.0	V	
Power supply voltage for gate driver	H	VGH		-	-0.3	25	V	
	H-L	VGH-VGL		-	0	34.5	V	
	L	VGL		-	VGH-34.5	-0.3	V	
Common electrode driving signal		VCOM	DC	-	0	3.5	V	
			P-P	-	-	7.0	V	
TFT exclusive RGB		VR,VB,VG		-	-0.3	VSH	V	
Input signals		V_I		-	-0.3	VSH	V	
Output signals		V_O		-	-0.3	VSH	V	
Lamp current		L_I		-	3.0	5.0	mA	
Ambient temperature		T_{ST}		Storage	-30	85	deg.	Note 1),2)
		T_{OP}		Operation	-30	85		
Humidity		-		TaC=<60deg.		90	%RH	not beyond 240H Note 3)

Note 1) Care should be taken so that the LCD module may not be subjected to the temperature beyond this specification.

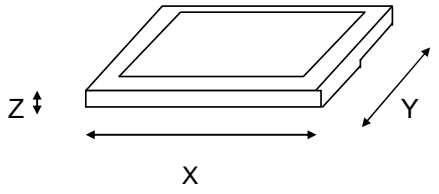
Note 2) Ambient temperature shows temperature on LCD surface. Module temperature is apt to increace while it's driving due to CFL heat etc. Please design carefully not to exceed +85 degree C on every surface of LCD that shoud come to contact with any other equipment. Temperature for operation is one which only assures LCD operation. Contrast, response time,or other LCD quality is regulated under condition of Ta=+25 degree C.

Note 3) Please be advised that dew condensation level should be less than maximum wet bulb temperature 58 degree C. Dew condensation may induce leak current, and also influence LCD performance.

■ *MECHANICAL ENVIRONMENT*

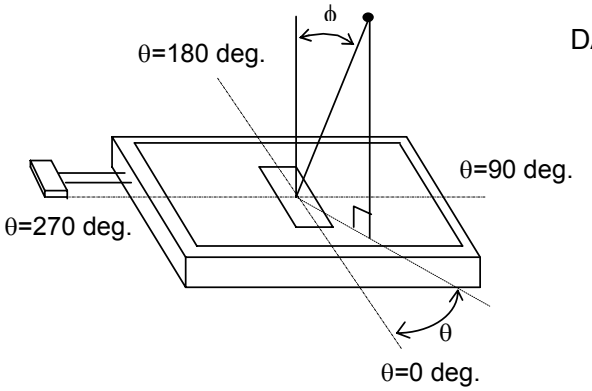
Vibration	-	Storage	-	2.9	G	Note 1)
Shock	-	Storage	-	100	G	XYZ 6ms/direction

Note 1) Vibration frequency : 8 - 33.3 Hz displacement : 1.3mm
Vibration frequency : 33.3 - 400Hz acceleration : 28.4m/S^2
Sweep time : 15 min./1 sweep
total test time : X,Y-2Hr Z-4Hr

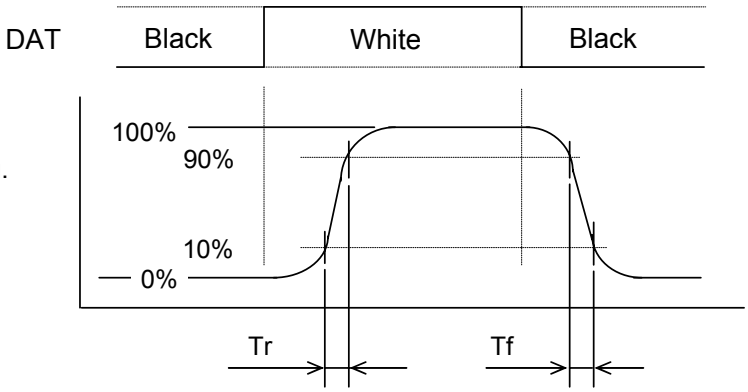


■ *OPTICAL CHARACTERISTICS (1)*

ITEM		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Viewing angle range		ϕ	K=>5	θ = 0 deg.	-	-	40	deg.	Note 1),4)
				θ = 90 deg.	-	-	60		
				θ =180 deg.	-	-	30		
				θ =270 deg.	-	-	60		
Contrast ratio		K	θ =0 deg.,ϕ =0		60	-	-	-	Note 2),4)
Response time	Rise	tr	θ =0 deg.,ϕ =0		-	30	-	ms.	Note 3),4)
	Fall	tf			-	20	-		
Color of CIE Coordinate	White	x	θ =0 deg.,ϕ =0		-	0.297	-		Note 4)
		y			-	0.301	-		



Note 1) θandϕ are defined as above figure.



Note 3) Response time

Note 2) Contrast ratio "K" is defined below formula.

$$K = \frac{\text{Brightness at ON (White)}}{\text{Brightness at OFF (Black)}}$$

Note 4) Measurement codition

1.VSH=5.3V,VGH=15.5V,VGL=-15.0V,VCOM DC=1.7V,VCOM P-P=6.0V
2.VR/VG/VB DC=VSH/2, VR/VG/VB Vp-p=4.0V
3.Fullmode
4.Follow brightness measurement condition in next item.

■ *OPTICAL CHARACTERISTICS (2)*

ITEM	SYM.	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Brightness	B		-	360	-	cd/m^2	

Note) The brightness shall be the following point.

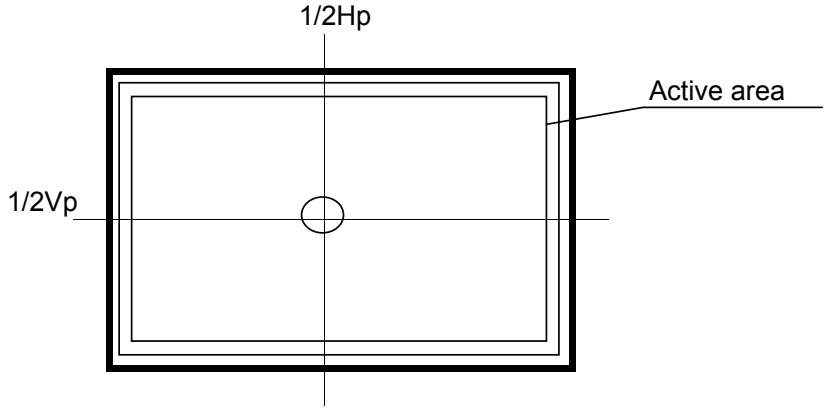


Fig.1 Measurement point

Vp :Total Number of Vertical pixel
Hp :Total Number of horizontal pixel

Measurement equipment : BM-7(TOPCON Corp.)
Measurement condition

1.Ambient temperature : 25 ±2 deg.
2.LCD : All pixels are WHITE
3.Measure after 30 minutes of CFL warm up.
4 IL=4.5mArms, CFL inverter:
Operating TDK CXA-L0612A-VJL or equivalent inverter with capability of frequency 50kHz, Lamp current max.4.5mA

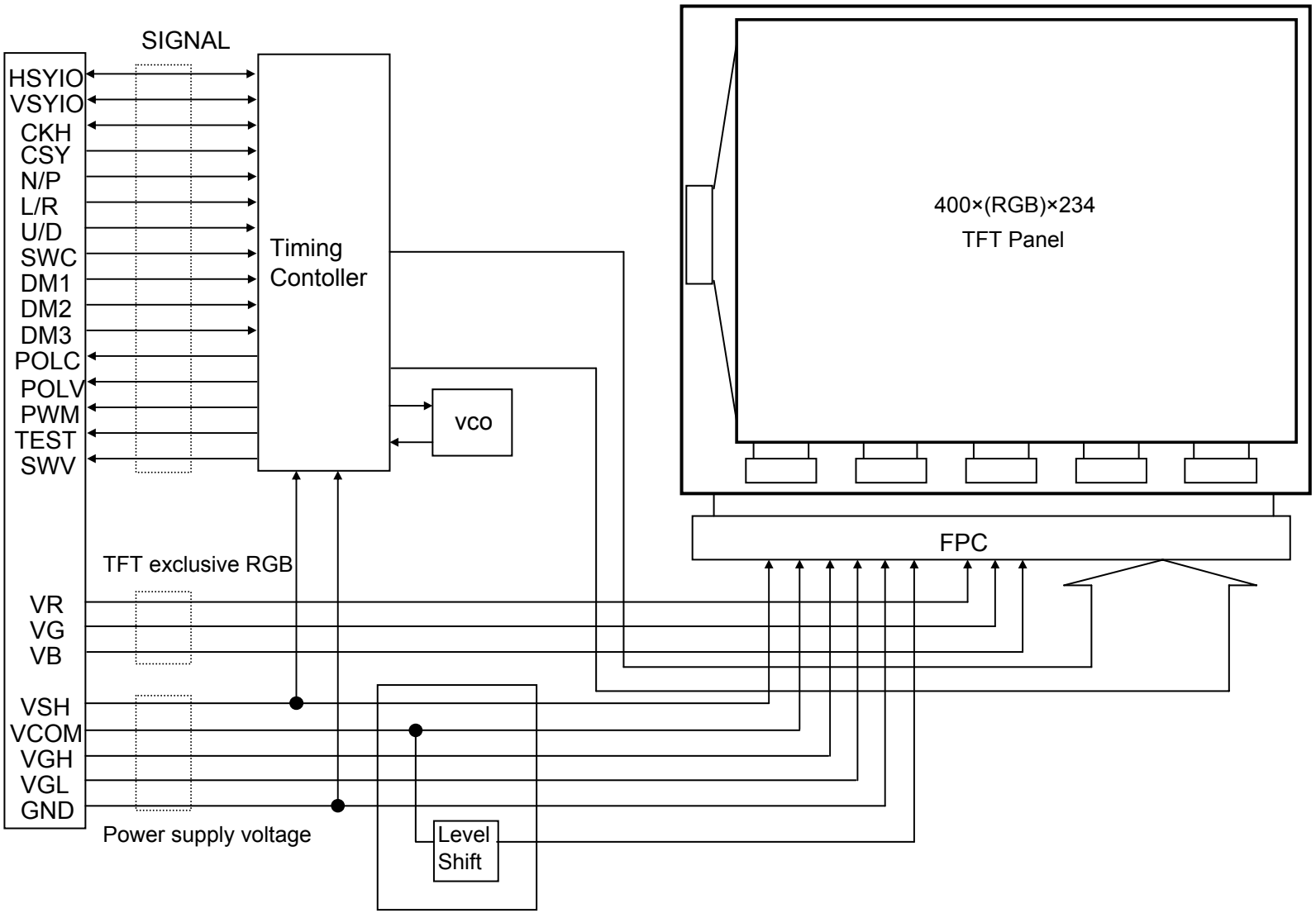
■ *BACKLIGHT CHARACTERISTICS*

ITEM	SYM.	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Lamp voltage	V_L		-	700	-	Vrms	at IL=4.5mArms
Lamp current	I_L		3.0	-	4.5	mArms	(Recommended value)
Operating frequency	f_L		40	50	60	KHz	(Recommended value)
Start up voltage	V_S1		-	-	1550	Vrms	at Ta= 25 deg.
Start up voltage	V_S2		-	-	1600	Vrms	at Ta=-30 deg.
Lamp life	t_{OL}		10000	-	-	Hours	at IL=4.5mArms, Note 1)
Backlight power supply	WL		-	2.8	-	W	at IL=4.5mArms

Note 1) CFL Lamp life indicates time from initial Lamp brightness to half of original brightness.
Note 2) Inverter GND shall be connected to LCD frame.(Please refer to outer dimension drawing) LCD frame is connected to internal circuitry GND.

■ ***BLOCK DIAGRAM***

IF BLOCK 24PIN



■ *INTERFACE PIN CONNECTIONS*

LCM : CN

PIN NO.	SYMBOL	I/O	FUNCTION
1	HSYIO	I/O	Input/Output horizontal sync.signal(low active)
2	POLC	O	Polarity alternating signal for common signal
3	CSY	I	Composite sync.signal(high active)
4	VGH	I	Power supply for gate driver(high level)
5	POLV	O	Polarity alternating signal for video signal)
6	VB	I	Color video signal(Blue)
7	VR	I	Color video signal(Red)
8	VG	I	Color video signal(Green)
9	GND	I	GND
10	VSH	I	Positive power supply voltage
11	VGL	I	Power supply for gate driver(low level)
12	VCOM	I	Common electrode driving signal
13	N/P	I	Selection for NTSC or PAL(NTSC=VSH,PAL=GND)
14	VSYIO	I/O	Input/Output vertical sync.signal(low active)
15	L/R	I	Selection for horizontal scanning direction
16	U/D	I	Selection for vertical scanning direction
17	SWC	I	Selection for input/output direction of CKH,HSYNC,VSYNC
18	PWM	O	Timinng signal for PWM dimming of backlight
19	TEST	O	Open use only
20	CKH	I/O	Input/output clock signal
21	DM1	I	Selection for display mode
22	DM2	I	Selection for display mode
23	DM3	I	Selection for display mode
24	SWV	O	Video selection timming signal

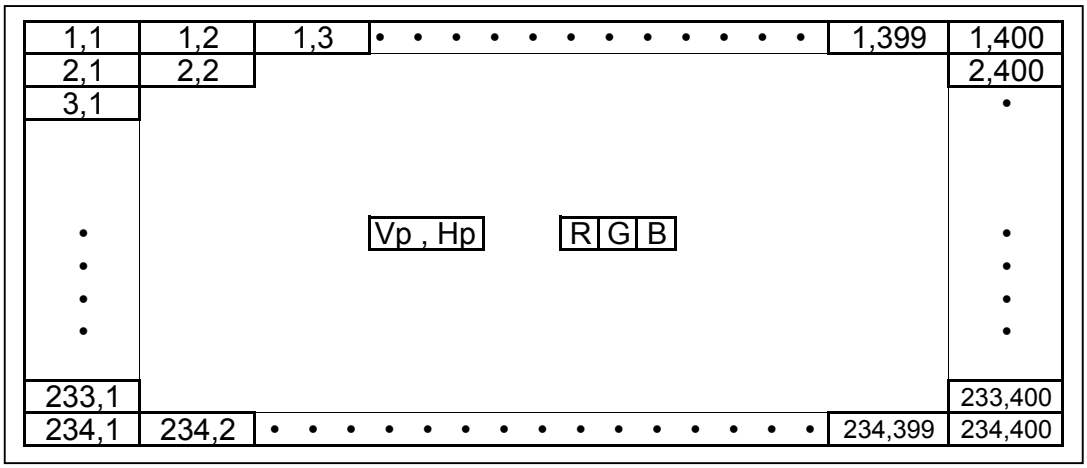
I/F CN : SFR24R-1ST(FCI)
Suitable FPC : Pitch 0.8mm,Width 20mm

Back Light : FLCN

PIN NO.	SYMBOL	FUNCTION
1	H.V	High voltage for CFL
2	N.C	No Connection
3	LGND	Low voltage for CFL

FLCN : BHR-03VS-1(JST)
Suitable mating connector : SM02(8.0)B-BHS-1(JST)

■ *RELATIONSHIP BETWEEN INPUT DATA AND DISPLAY POSITION*



■ *FUNCTION,MODE AND TERMINALS*

Mode terminals					Sync. signal I/O terminals					
SWC	N/P	DM1	DM2	DM3	HSYIO	VSYIO	CKH	SWV	CSY	CONDITIONS
H	H or L	L L L	H L L	L H L	Hsync output	Vsync output	Lo output	Test signal output	Conposite sync input	Test mode
H	H	H	L	H	Hsync output	Vsync output	Lo output	masking signal output	Conposite sync input	NTSC or PAL mode (Normal mode)
H	H or L	other settings H or L			Hsync output	Vsync output	Lo output	Lo output	Conposite sync input	NTSC or PAL mode (Full,Wide,Cinema)
L	H	H	H	H	Hsync input	Vsync input	Pixel clock input	Lo output	Input Hi or Lo fixed value	External clock synchronous mode

Note 1) We recommend external clock synchronize method except for TV display usage.

Note 2) Please invert polarity of video signal VR,VG and VB in sync with invert timing of POLV signal.(Please refer Figure A.)

Note 3) Please invert polarity of VCOM in sync with invert timing of POLC signal. (Please refer Figure B.)

Note 4) Horizontal synchronized signal is output in sync with CSY signal when SWC is Hi. When SWC is Low, LCD module is operated in sync with Horizontal synchronized signal for HSYIO terminal.(Please refer Figure C,D,G and F.)

Note 5) In normal mode, non-display area at both edge of display can be better screened by masking video signal following SWV output signal. (Please refer timing chart E.)

Note 6) PWM signal for CFL brigtness control is output form PWM terminal. (Please refer Figure H.) But please use it when normal NTSC or PAL signals are inputted.

■ *DISPLAY METHOD AND CHARACTERISTICS*

H=VSH L=GND

DM1	DM2	DM3	Display Mode	Display method, Feature	SOURCE	Horizontal: Disply area	Horizontal: Sampling	Vertical: Disply area NTSC	Vertical: Disply area PAL	EXAMPLE
H	H	H	Full mode	Display 4:3 image long sideways.	4:3 signal Navigation Signal	Signal area	Senter Both side Same	S=1/1	S=6/7 Compress	Fig.2-1
H	H	L	Wide1 mode	Display perfect circle around center better than Full screen mode.	4:3 signal	Signal area	Senter :Slow Botn side:Fast	S=1/1	S=6/7 Compress	Fig.2-2
H	L	H	Normal mode	Display perfect circle all around the screen. Both edge screen can be masked with SWV.	4:3 signal	Signal area & Blank	Senter :Slow Botn side:Fast Modulation wide1,2<Nomal	S=1/1	S=6/7 Compress	Fig.2-3
H	L	L	Cinema mode	Display 16:9 image.	Wide signal(16:9)	Signal area	Senter Both side Same	S=4/3 Extend	S=1/1	Fig.2-4
L	H	H	Wide 2 mode	Display perfect circle around center better than Wide 1 mode. Top and bottom images are eliminated.	4:3 signal	Signal area	Senter :Slow Botn side:Fast	S=5/4 Extend	S=10/11 Compress	Fig.2-5
L	H	L	Test mode	This mode is unusable due to test mode.	-	-	-	-	-	-
L	L	H	Test mode	This mode is unusable due to test mode.	-	-	-	-	-	-
L	L	L	Test mode	This mode is unusable due to test mode.	-	-	-	-	-	-

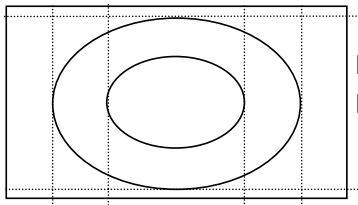


Fig2-1
Full mode

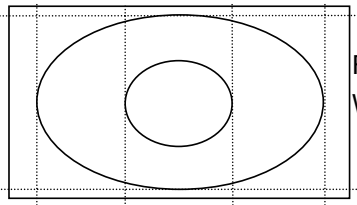


Fig2-2
Wide1 mode

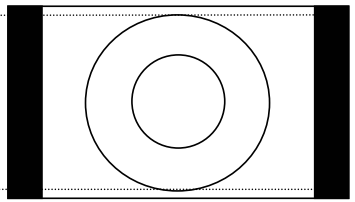


Fig2-3
Normal mode

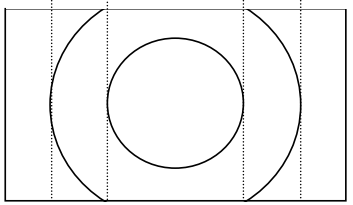


Fig2-4
Chinema mode

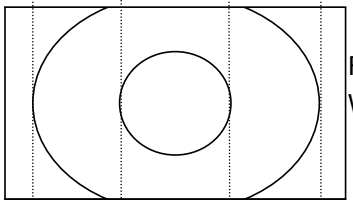


Fig2-5
Wide 2 mode

<DISPLAY AREA>

1.NTSC MODE(N/P=H, SWC=H)

(a1)Horizontal…Full mode, Wide1 mode, Wide2 mode, Cinema mode

From falling edge of HSYIO output to 13.1-63.2μS.

(a2)Horizontal…Normal mode

From falling edge of HSYIO output to 7.9-68.4μS.

(b1)Vertical…Full mode, Wide2 mode, Normal mode

From falling edge of VSYIO output to 20H-253H.

(b2)Vertical…Cinema mode

From falling edge of VSYIO output to 49H-224H.

(b3)Vertical…Wide2 mode

From falling edge of VSYIO output to 42H-228H.

2.PAL MODE(N/P=L, SWC=H)

(a1)Horizontal…Full mode, Wide1 mode, Wide2 mode, Cinema mode

From falling edge of HSYIO output to 13.1-63.2μS.

(a2)Horizontal…Normal mode

From falling edge of HSYIO output to 7.9-68.4μS.

(b1)Vertical…Full mode, Wide2 mode, Normal mode

From falling edge of VSYIO output to 26H-298H.

Except for Even Nunber Field (14n+12) and (14n+20),

Odd Number Field (14n+17) and (14n+23).

n=(1,2,3,…,20)

(b2)Vertical…Cinema mode

From falling edge of VSYIO output to 49H-282H.

(b3)Vertical…Wide2 mode

From falling edge of VSYIO output to 35H-289H.

Except for Even Nunber Field (22n+14) and (22n+21),

Odd Number Field (22n+25) and (22n+32).

n=(1,2,3,…,12)

3.EXTERNAL CLOCK MODE(N/P=H, SWC=L, DM1,2,3=H)

(a1)Horizontal

From falling edge of HSYIO output to 86-485CLK.

CLK is indicated as external CLK number.

(b3)Vertical

From falling edge of VSYIO output to 20H-253H.

■ *ELECTRICAL CHARACTERISTICS*

ITEM		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Logic/Source power supply voltage		VSH		5.0	5.3	5.5	V	Note 3)
Power supply voltage for gate driver	H	VGH		15.0	15.5	16.0	V	
	L	VGL		-16.0	-15.0	-14.0	V	
Common electrode driving signal		VCOM	DC center	1.0	1.7	3.0	V	Note 1)
			P-P	4.0	5.0	6.0	V	Note 2),4)
TFT exclusive RGB		VR,VG,VB	DC center	TYP-0.1	VSH/2	TYP+0.1	V	Note 3)
			AC White pattern	+1.5	2.0	VSH/2	V	POLV=H Note4),5)
			AC Black pattern	-1.5	-2.0	-VSH/2	V	POLV=H Note4),5)
			AC White pattern	-1.5	-2.0	-VSH/2	V	POLV=L Note4),5)
			AC Black pattern	+1.5	2.0	VSH/2	V	POLV=L Note4),5)
Input signals		V_{IH}	High level	0.7VSH	-	VSH	V	Note 6)
		V_{IL}	Low level	0	-	0.3VSH	V	
Input signals		V_{IH}	High level	0.8VSH	-	VSH	V	Note 7)
		V_{IL}	Low level	0	-	0.2VSH	V	
Output signals		V_{OH}	High level	VSH-2.1	-	-	V	Note 8)
		V_{OL}	Low level	-	-	0.4	V	
Power Supply current		I_{VSH}	VSH=5.3V	-	45	70	mA	Note 9,10)
		I_{VGH}	VGH=15.5V	-	1	1.3	mA	
		I_{VGL}	VGL=-15.0V	-	5.7	6.0	mA	
Power Supply		WS		-	330	460	mW	

Note 1) Please adjust DC voltage on opposite electrode (VCOM) to optimum BIAS voltage in order to minimize flicker.

Note 2) Please optimize voltage of each module to achieve optimum contrast.

Note 3) Please control voltage fluctuation less than 0.1V after VCOM is adjusted.

Note 4) =+/- amplitude shall be symmetry.

Note 5) In case of POLV=Low, the signal polarity inverts working with polarity of VCOM.

Note 6) Symmetric terminal name: HSYIO,VSYIO(CMOS INPUT)

Note 7) Symmetric terminal name: CSY,DM1,DM2,DM3,L/R,N/P,SWC,U/D,HSYIO,VSYIO(CMOS Schmitt INPUT)

Note 8) Symmetric terminal name: POLC,POLV,PWM,SWV,HSYIO,VSYIO,CKH(CMOS OUTPUT)
(COMS output level)

Note 9) Under the following conditions:

Display pattern: ALL BLACK FULL MOD fv:60Hz

VCOM DC=1.7V,VCOM P-P=5.0V
VR/VG/VB DC=VSH/2 VR/VG/VB Vp-p=4.0V

Note10) Value for module circuitry portion (except for backlight)

■ *ELECTRICAL CHARACTERISTICS AC TIMING*

NTSC :fH=15.73kHz,fV=60Hz,t HI=4.7μs
PAL :fH=15.63kHz,fV=50Hz,t HI=4.7μs

<COMMON: EXTERNAL CLK MODE/BUILT-IN CLK MODE>(SWC=Hi or Low)

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Input voltage		VID	0	-	VSH	V	
Input composite sync	rising time	t rVI	-	-	0.2	μs	
[CSY]Vertical location	falling time	t fVI	-	-	0.2	μs	
Polarity alternating delay time [POLV-VRGB]		tDV	-	-	4	μs	
Polarity alternating delay time[POLC-VCOM]		tDC	-	-	4	μs	
Output polarty signal	rising time	t rPL	-	-	0.5	μs	
[POLC,POLV]	falling time	t fPL	-	-	0.5	μs	

<BUILT-IN CLK MODE>(SWC=Hi)

ITEM			SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Input composite sync horizntal location	frequency	NTSC	fH(N)	15.13	15.73	16.33	kHz	Note 1
		PAL	fH(P)	15.03	15.63	16.23	kHz	
	pulse wide	NTSC	tHI(N)	4.2	4.7	5.2	μs	
		PAL	tHI(P)	4.2	4.7	5.2	μs	
	rising time		trHI1	-	-	0.2	μs	
[CSY]	falling time		tfHI1	-	-	0.2	μs	
Input composite sync Vertical location	frequency	NTSC	fV(N)	fH/284	fH/262.5	fH/258	Hz	Note 1
		PAL	fV(P)	fH/344	fH/312.5	fH/304	Hz	
	pulse wide	NTSC	tVI(N)	-	3	-	H	
[CSY]		PAL	tVI(P)	-	2.5	-	H	
Output horizontal sync signal	frequency		fH0	-	fH	-	kHz	Note 2
	pulse wide		tH0	-	4.7	-	μs	
	rising time		trH0	-	-	0.5	μs	
[HSYIO]	falling time		tfH0	-	-	0.5	μs	
horizontal sync phase	rising HSY		tpd1	-	2.1	-	Hz	
[HSYIO-CSY]	falling HSY		tpd2	-	2.1	-	Hz	
Output vertical sync signal	frequency		fV0	-	fV	-	Hz	
	pulse wide		tV0	-	4	-	H	1H=1/fH
	Output phase		tVH0	-	11	-	μs	Sync HSYIO
[VSYIO]	rising time		trV0	-	-	0.5	μs	
	falling time		t fV0	-	-	0.5	μs	
Vertical sync phase	ODD FIELD		t DV1	-	1	-	H	
[CSY-VSYIO]	EVEN FIELD		t DV2	-	0.5	-	H	

Note 1) Standard complex synchronized signal [CSY] type of NTSC/PAL signal shall be inputted. It would be a factor of display quality degradation if nonstandard synchronized signal were inputted.
Note 2) Varied by tpd1 value.

<EXTERNAL CLK MODE>(SWC=Low)

ITEM		SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Input CLK sync signal [CKH]	frequency	fCL1	7.2	8.0	8.8	MHz	
	H pulse wide	tWH	20.0	-	-	ns	
	L pulse wide	tWL	20.0	-	-	ns	
	rising time	trCL1	-	-	10.0	ns	
	falling time	tfCL1	-	-	10.0	ns	
Input horizontal sync signal [HSYIO]	frequency	fHI	fCLI/550	fCLI/508	fCLI/490	kHz	
	pulse wide	tHI	1.0	5.0	9.0	μs	
	rising time	trHI2	-	-	0.05	μs	
	falling time	tfHI2	-	-	0.05	μs	
Input Vertical sync signal [VSYIO]	frequency	fVI	50	fHI/262	fHI/258	Hz	
	pulse wide	tVI	1	3	5	H	
HSYIO-CKHIO	Data setup time	t SU1	25	-	-	ns	Note 3)
	Data hold time	t HO1	25	-	-	ns	
VSYIO-HSYIO	Data setup time	t SU2	1.0	-	-	μs	Note 4)
	Data hold time	t HO2	1.0	-	-	μs	

Note 3) In external clock input mode, they show input phase contrast of CKH and HSYIO signal.
Data is loaded latching with CKH rising signal.

Note 4) In external clock input mode, they show input phase contrast of HSYIO andVSYIO signal.
Data is loaded latching with HSYIO falling signal.

■ *ELECTRICAL CHARACTERISTICS AC TIMING*

<COMMON: EXTERNAL CLK MODE/BUILT-IN CLK MODE>(SWC=Hi or Low)

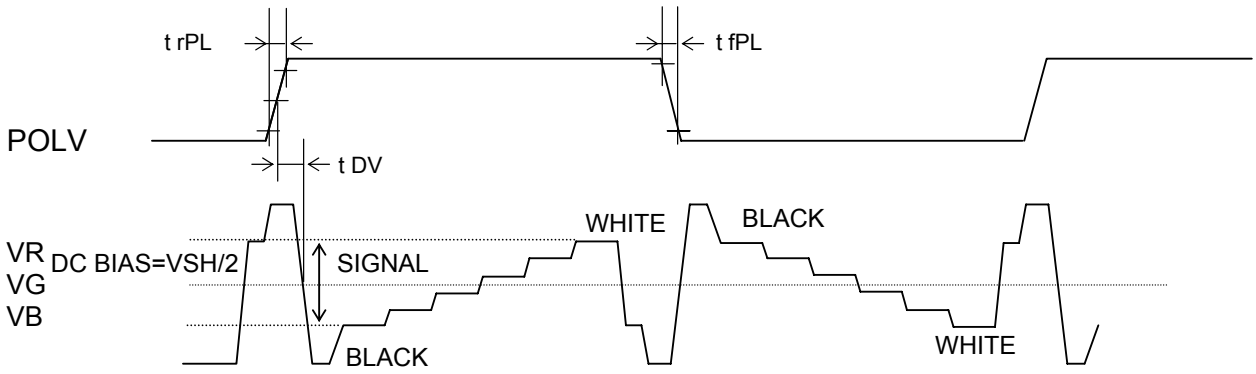


Fig-A

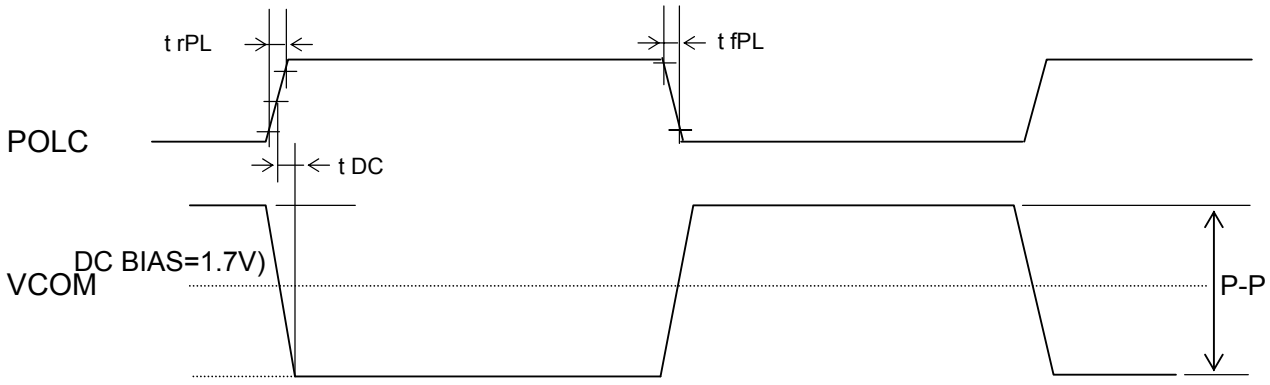


Fig-B

<BUILT-IN CLK MODE>(SWC=Hi NTSC/PAL)

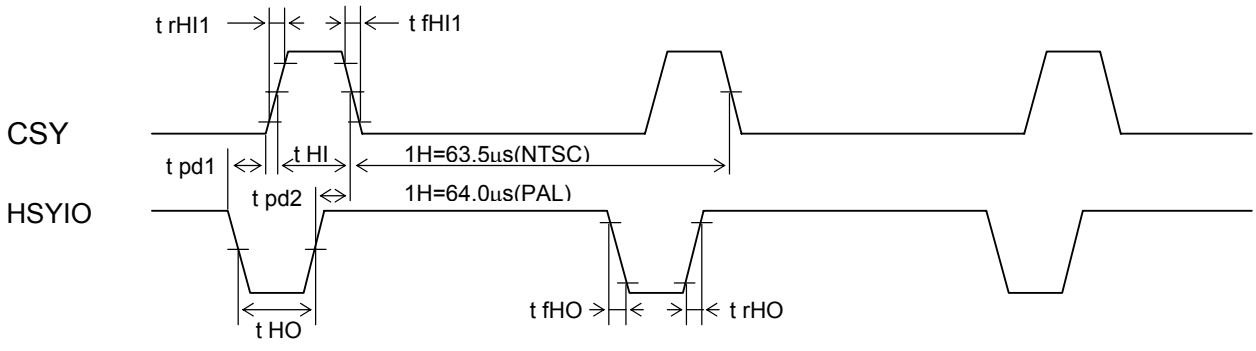


Fig-C

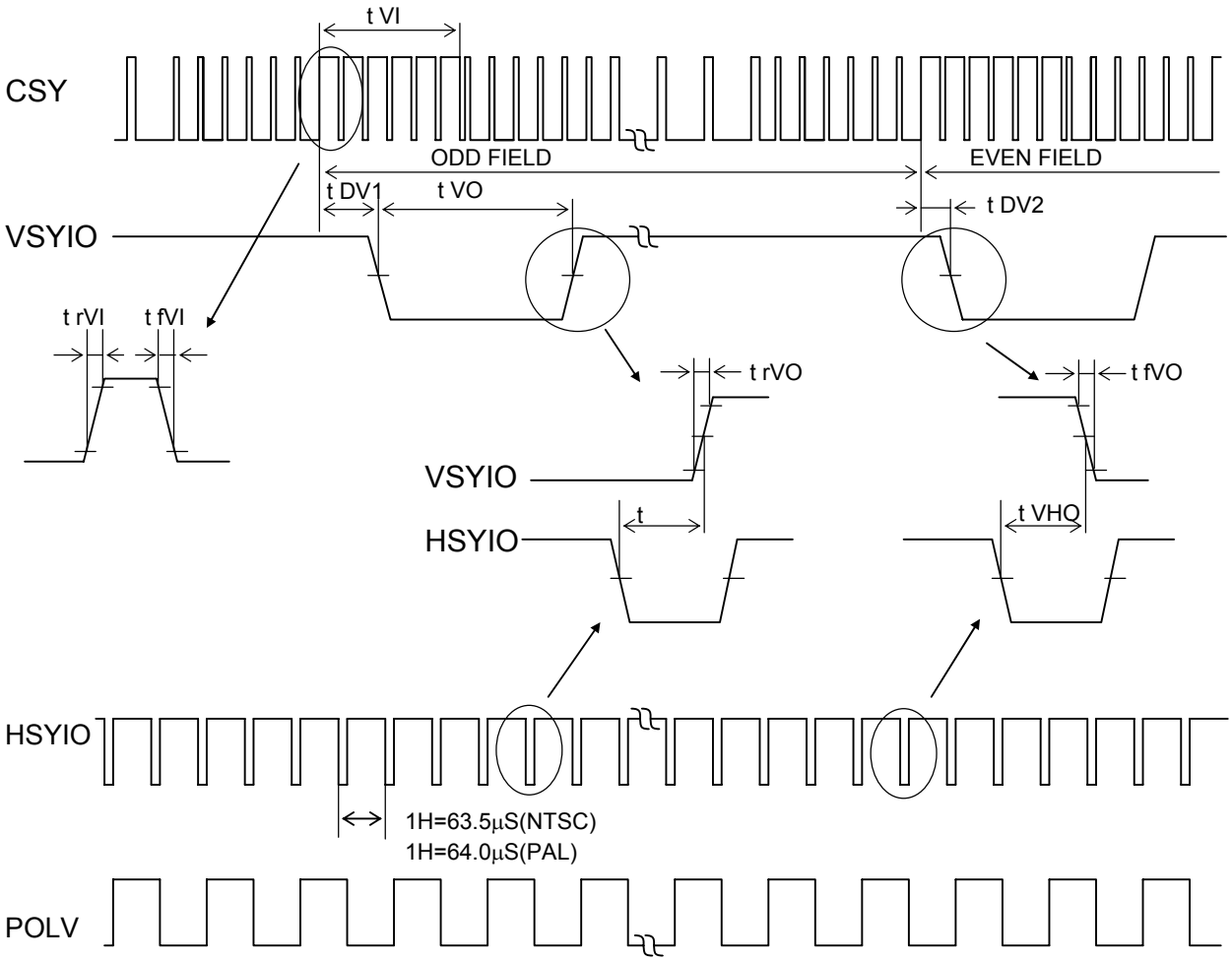


Fig-D

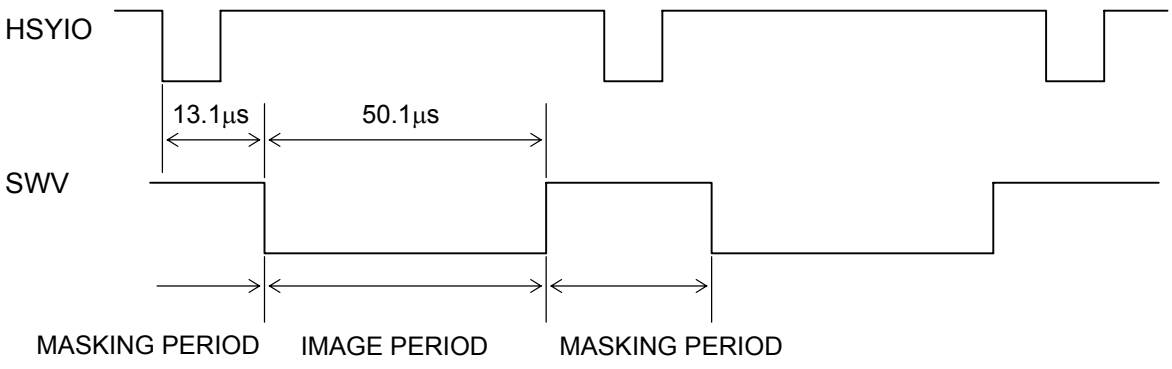


Fig-E (NORMAL MODE DM1=Hi, DM2=Low, DM3=Hi)

<EXTERNAL CLK MODE>(SWC=Low)

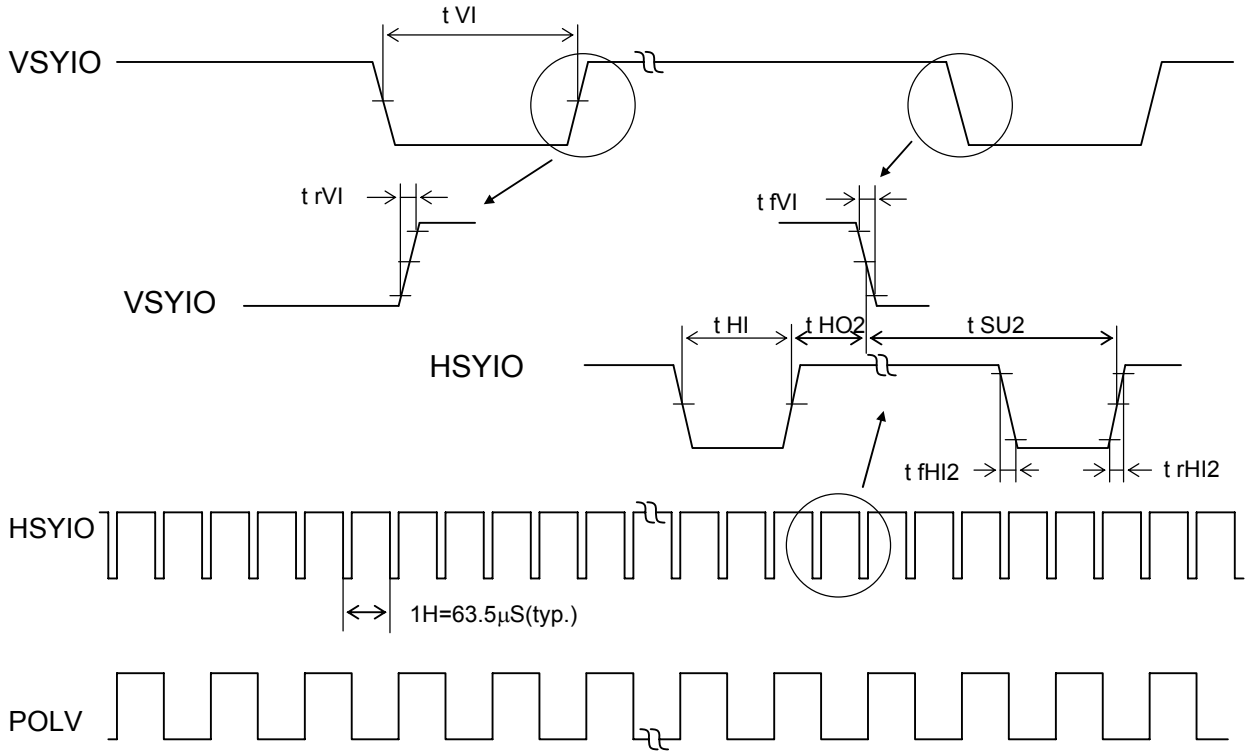


Fig-F (N/P=Hi)

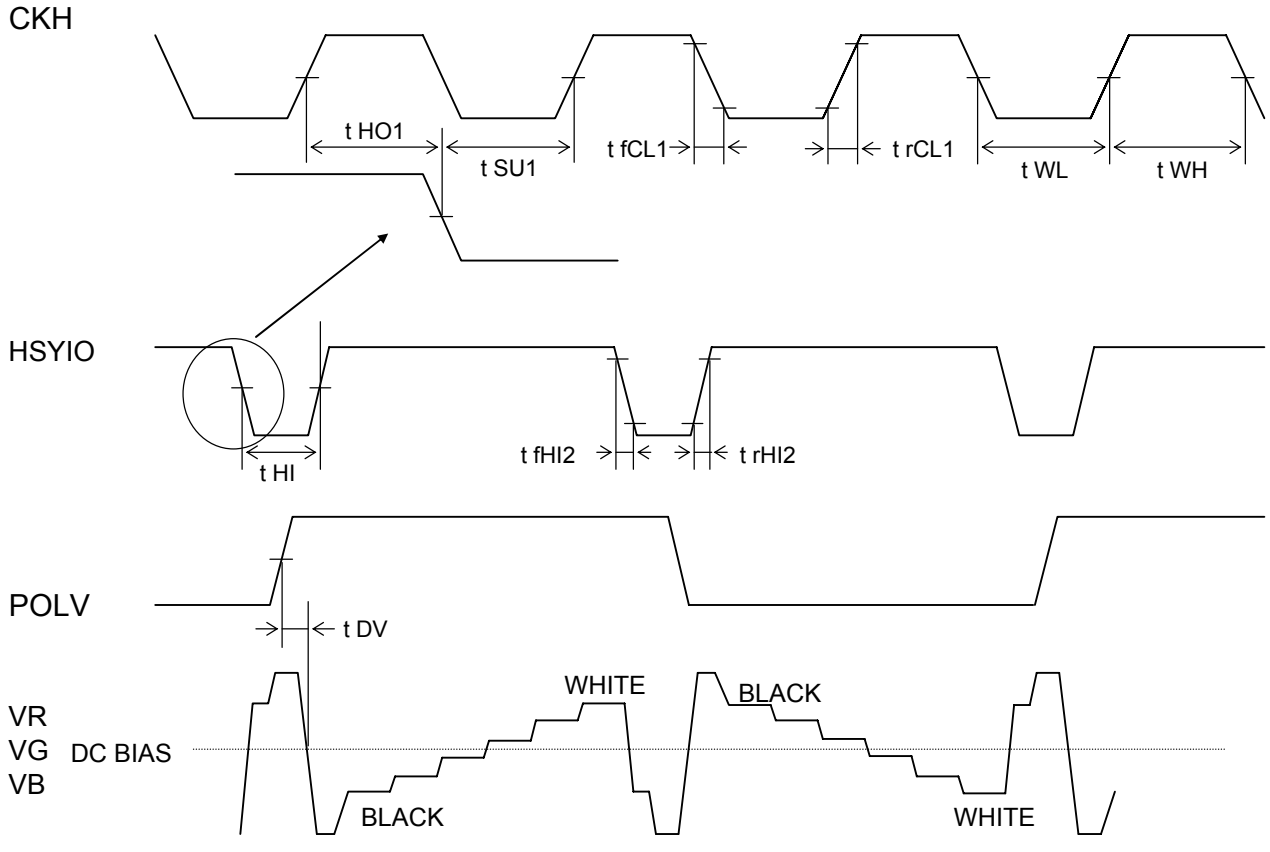


Fig-G(N/P=Hi, DM1=DM2=DM3=Hi)

■ *PWM DIMMING TIMING*

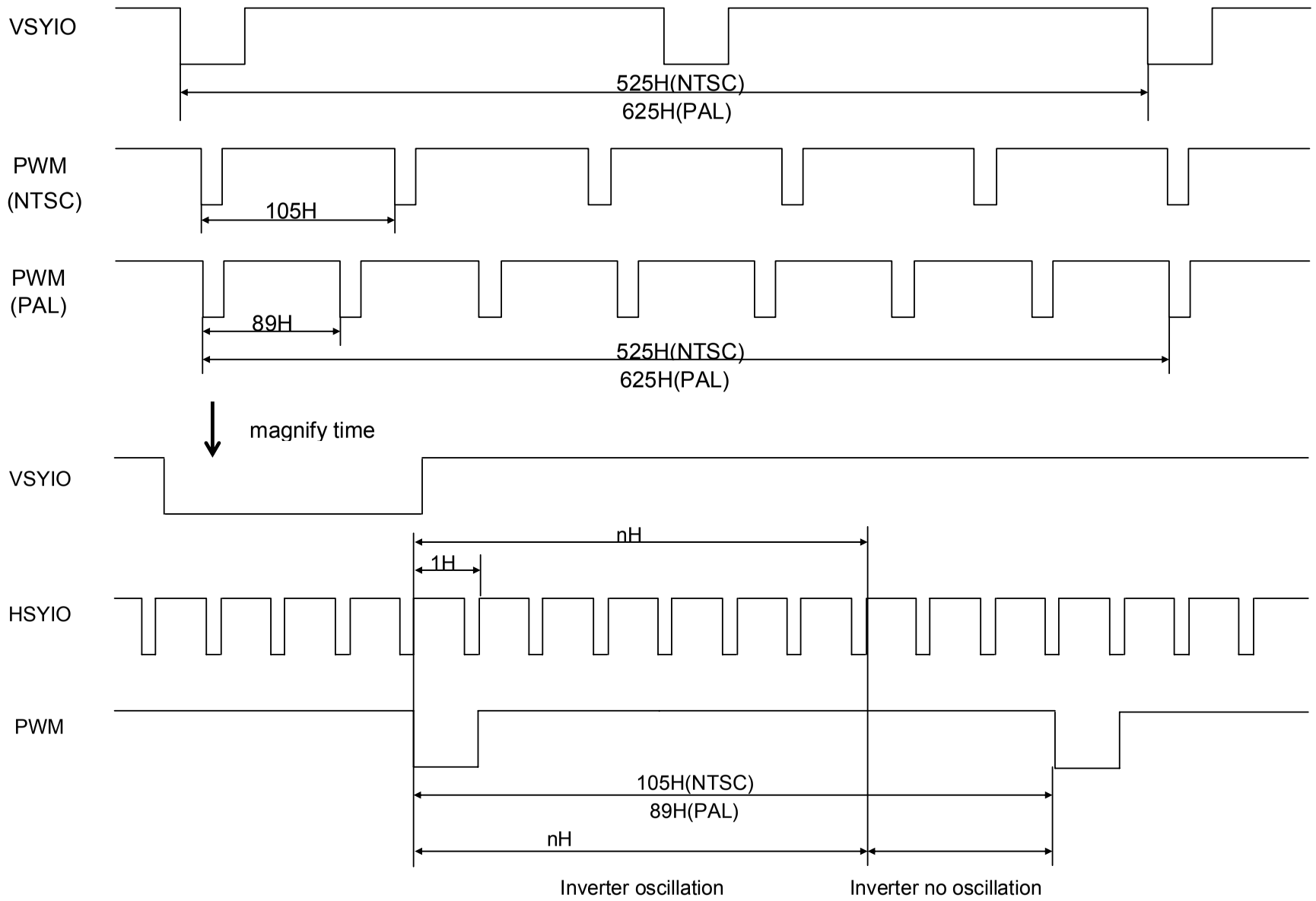
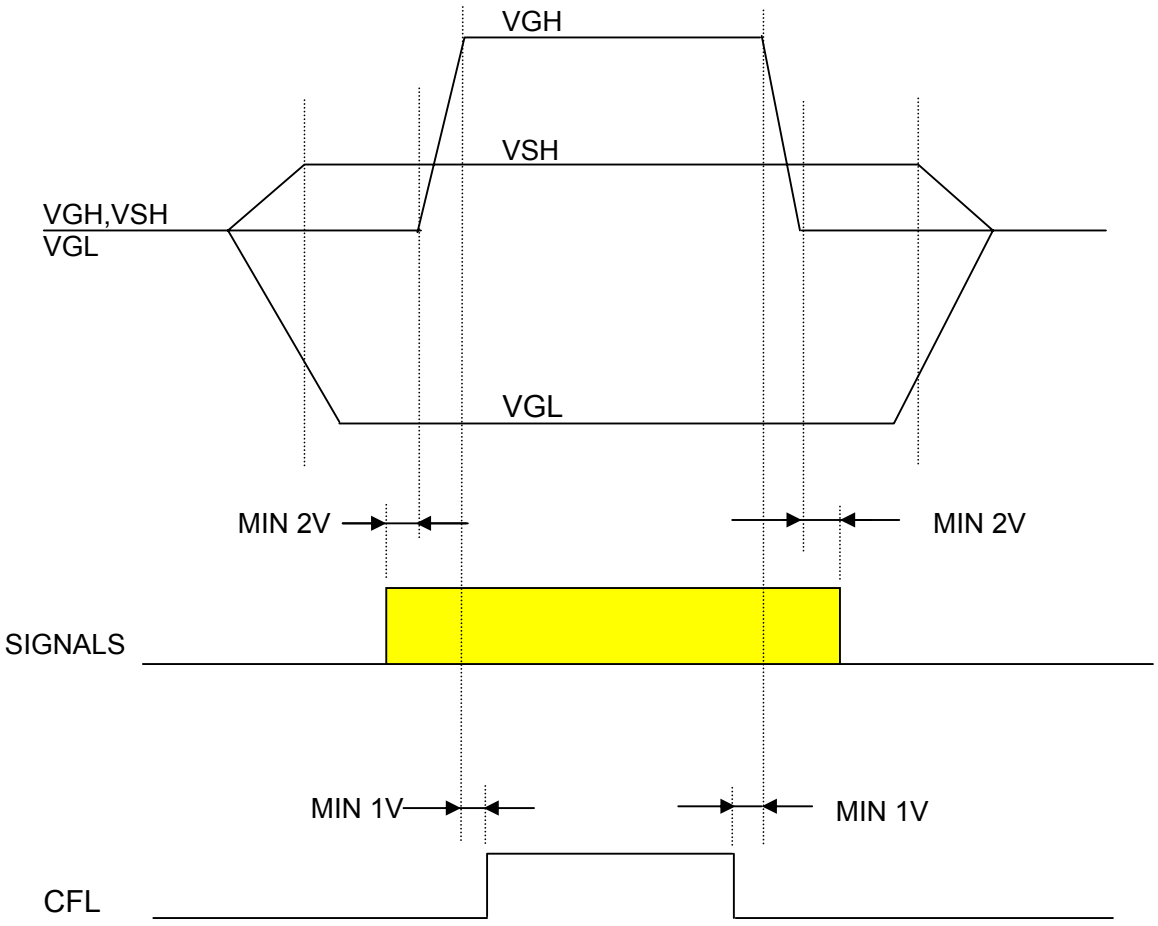


Fig-H

■ *POWER ON/OFF SEQUENCE REQUIREMENT*



* (V=1 FIELD time)

■ *PRECAUTIONS (INSTRUCTIONS FOR SAFE AND PROPER USE)*

1.Instructions for safety

1. Please do not disassemble or modify LCD module to avoid the possibility of electric shock, damage of electronic components, scratch at display surface and invasion of foreign particles. In addition, such activity may result in fire accident due to burning of electronic component.LCD module disassembled or modified by customer is out of warranty.

2. Please be careful in handling of LCD module with broken glass.
   When the display glass breaks, please pay attention not to injure your fingers. The display surface has the plastic film attached, which prevents dispersion of glass pieces, however touching broken edge will injure your fingers. Also CFL (Cold Cathode Fluorescent Lamp) is made of glass, therefore please pay attention in the same way.

3. Please do not touch the fluid flown out of broken display glass.
   If the fluid should stick to hand or clothes, wipe off with soap or alcohol immediately and then wash it with water. If the fluid should get in eyes, wash eyes immediately with pure water for more than 15 minutes and then consult the doctor.

4. Please make secure connection of CFL connector.
   Please make sure that CFL connector from LCD module is connected with output connector on inverter circuit securely. Poor connection may cause smoke or fire accident due to high voltage in circuit. If connection may not be secure, please switch off the power supply for LCD module and CFL and then make secure connection.
   Please do not make connection with another connector than recommended mating connector.

5. CFL contains mercury inside. Please follow regulations or rules established by local autonomy at its disposal.

6. Please be careful to electric shock.
   Before handling LCD module, please switch off the power supply.
   Since high voltage is applied to CFL terminal, cable, connector and inverter circuit in operation mode, touching them will cause electric shock.

2.Instructions for designing

1. Mounting of LCD
   Please fix LCD module at all mounting flanges shown in this specification for installation onto system. The used screws should have proper dimensions.
   Furthermore, designing of mounting parts should be adequate so that LCD module is not warped or twisted, to achieve good display quality.

2. Polarity of power supply for CFL
   Please give careful consideration in designing so that each polar of cable should be connected correctly at assembling (i.e. high voltage side is connected to high voltage side and low voltage side is connected to low voltage side). Since longer CFL cable may cause insatiable start-up of CFL and reduction of brightness, please make cable short as much as possible.

3. Designing of power supply circuit for CFL
   Please design the circuit so that high voltage output can be kept for more than 1 second. The shorter time may not start up CFL. The driving inverter circuit is recommended to be the type which CFL current can be controlled.
   The type which voltage is controlled is not recommended, because it may cause big current under high temperature and insatiable start-up of CFL under low temperature.

4. Heat radiation
CFL generates heat at lighting and causes temperature rise inside system. Therefore, designing to radiate heat like radiation slits at cabinet is recommended to meet the specified operating temperature range for LCD module.

5. Noise on power line
Spike noise contained in power line causes abnormal operation of driving circuit and abnormal display. To avoid it, spike noise should be suppressed below VDD +/- 200mVp-p. (In any case, absolute maximum rating should be kept.)

6. Power sequence
Before LCD module is switched on, please make sure that power supply and input signals of system, testing equipment, etc. meet the recommended power sequence.

7. Absolute maximum rating
Absolute maximum rating specified in this specification has to be kept in any case. It shows the maximum that cannot be exceeded.
Exceeding it may cause burning or non-recoverable break of electronic components in circuit. Please make system design so that absolute maximum rating is not exceeded even if ambient temperature, input signal and components are varied.

8. Protection for power supply
Please study to adapt protection for power supply against trouble of LCD module, depending on usage condition of system. Fuse installed on LCD module should be never modified. Any modification to make the function of fuse ineffective may cause burning or break of printed wiring board or other components at circuit trouble.

9. Protection against electric shock
High voltage is applied to CFL connector, inverter circuit and CFL at lighting. Please make design not to expose or be accessible to such high voltage parts to avoid electric shock.

10. Protection cover and cut-off filter for ultraviolet rays
When LCD module is used under severe condition like outdoor, it is recommended to use transparent protection cover over display surface to avoid scratches and invasion of dust and water. In addition, when recommended. Please be careful not to get condensation.

3.Instructions for use and handling

1. Protection against Static electricity
C-MOS LSI and semiconductors are easily damaged by static discharge. LCD module should be handled on conductive mat by person grounded with wrist strap etc. to avoid getting static electricity. Please be careful not to generate static electricity during operation.

2. Protection against dust and stain
LCD module should be handled in circumstance as clean as possible.
It is recommended to wear fingerstalls or ductless and soft gloves before handling to avoid getting dust or stain on display surface.

3. Protection film for display surface
It is recommended to remove protection film at nearly final process of assembling to avoid getting scratch or dust. To remove film, please pick up its edge with dull-head tweezers or cellophane tape at first and then remove film gradually taking more than 3 seconds. If film is removed quickly, static electricity may be generated and may damage semiconductors or electronic components.

4. Contamination of display surface
When display surface of LCD module is contaminated, please wipe the surface softly with cotton swab or clean cloth. If it is not enough, please take it away with cellophane tape or wipe the surface with cotton swab or clean cloth containing benzine. In this case, please be careful so that benzine does not get in inside of LCD module, because it may be damaged.

5. Water drop on LCD surface
Please do not leave LCD module with water drop. When the display surface gets water drop, please wipe it off with cotton swab or soft cloth immediately, otherwise display surface will be deteriorated.
If water gets in inside of LCD module, circuit may be damaged.

6. Please make sure that LCD module is not warped or twisted at installation into system. Even temporary warp or twist may be the cause for failure.

7. Mechanical stress
Please be careful not to apply strong mechanical stress like drop or shock to LCD module. Such stress may cause break of display glass and CFL or may be the cause for failure.

8. Pressure to display surface
Please be careful not to apply strong pressure to display surface. Such pressure may cause scratches at surface or may be the cause of failure.

9. Protection against scratch
Please be careful not to hit, press or rub the display surface with hard material like tools. In addition, please do not put heavy or hard material on display surface, and do not stack LCD modules. Polarizer at front surface can be easily scratched.

10. Plugging in of connector
Please be careful not to apply strong stress to connector part of LCD module at plugging in or out, because strong stress may damage the inside connection. At plugging in connector, place LCD module on the flat surface and hold the backside of connector on LCD module. Please make sure that connector is plugged in correctly. Insecure connection may be the cause for failure during operation.In addition, please be careful not to put the connecting cable between cabinet of system and LCD module at installing LCD module into system.

11. Handling of CFL cable and FPC (Flexible Printed Circuit)
Please be careful not to pull or scratch CFL cable, because CFL or soldered part of cable may be damaged consequently.
Also FPC should not be pulled or scratched.

12. Switching off before plugging in connector
Please make sure that power is switched off before plugging in connector.
If power is on at plugging in or out, circuit of LCD module may be damaged.
When LCD is switched on for test or inspection, please make sure that power supply and input signals of driving system meet the specified power sequence.

13.Temperature dependence of LCD display

Response speed (optical response) of LCD display is dependent on temperature. Under low temperature, response speed is slower.

Also brightness and chromaticity change slightly depending on temperature.

14.Slow light-up of CFL under low temperature

Under low temperature, start-up of CFL gets difficult. (The time from switch-on to stable lighting becomes longer.)

As characteristic of CFL, operation under low temperature makes the life time shorter. To avoid this, it is recommended to operate under normal temperature.

15.Condensation

LCD module may get condensation on its display surface and inside in the circumstance where temperature changes much in short time.

Condensation can cause deterioration or failure. Therefore, please be careful not to get condensation.

16.Remaining of image

Displaying the same pattern for long time may cause remaining of image even after changing the pattern. This is not failure but will disappear with time.

4.Instructions for storage and transportation

1. Storage

Please store LCD module in the dark place of room temperature and low humidity in original packing condition, to avoid condensation that may cause failure.

Since sudden temperature change may cause condensation, please store in circumstance of stable temperature.

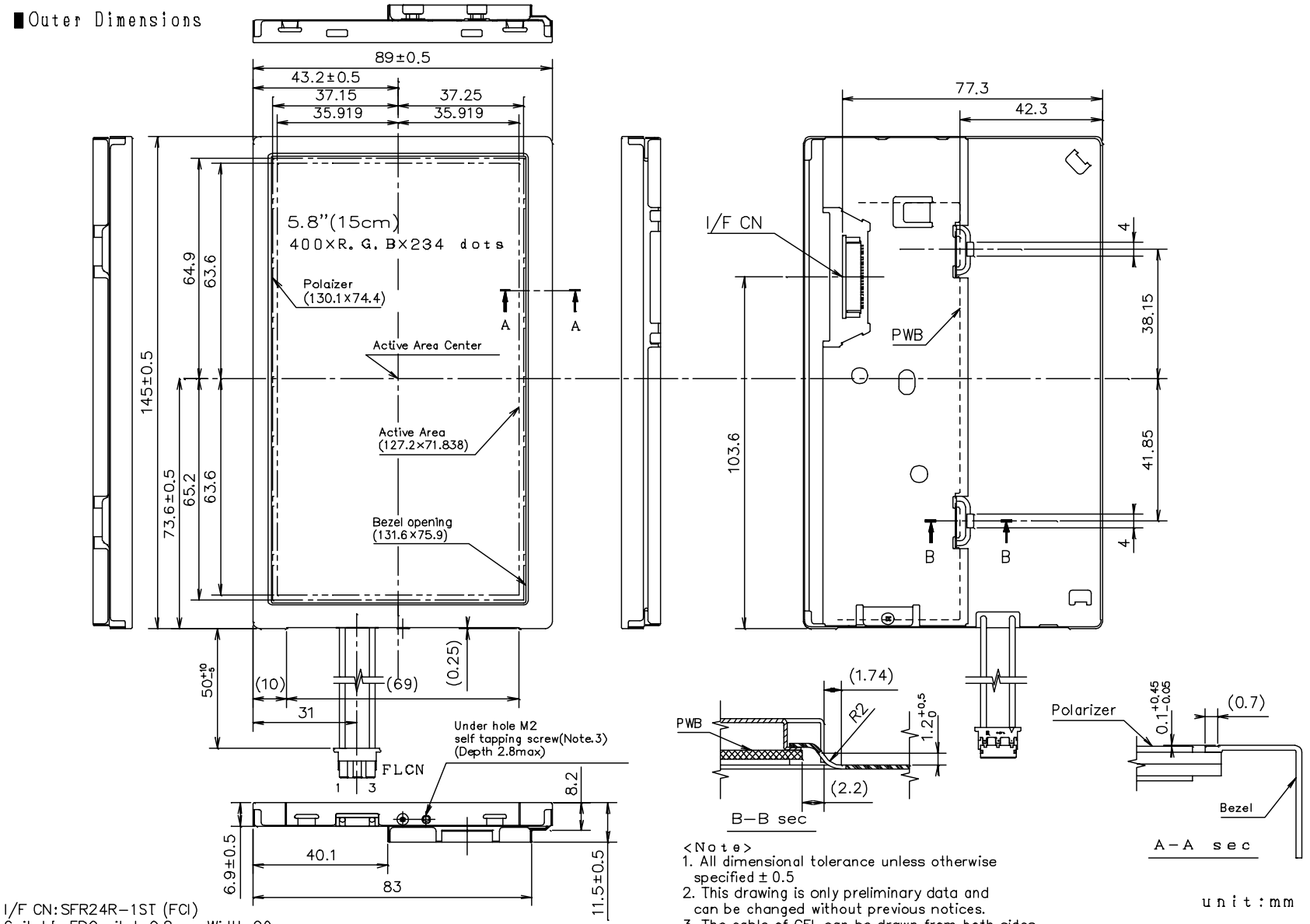
2. Stacking number

Since excessive weight causes deformation and damage of carton box, please stack only up to the number stated on carton box for storage and transportation.

3. Handling

Since LCD module consists of glass and precise electronic components, it will be damaged by excessive shock and drop. Therefore, please handle the carton box carefully to minimize shock at loading, reloading and transportation.

■Outer Dimensions



I/F CN: SFR24R-1ST (FCI)
Suitable FPC: pitch 0.8mm, Width 20mm
FLCN: BHR-03VS-1 (JST)

<Note>
1. All dimensional tolerance unless otherwise specified ± 0.5
2. This drawing is only preliminary data and can be changed without previous notices.
3. The cable of CFL can be drawn from both sides.

unit: mm