# LTPS LCD Specification

## Model Name: 990000024

| Customer Signature |
| --- |
| |
| **Date** |
| |

This technical specification is subjected to change without notice

## Table of Contents

## Record of Revision

| Rev | Issued Date | Description |
|---|---|---|
| 0.00 | May. 20, 2007 | New create. |
| 0.1 | Aug, 1, 2007 | Update 3 Pin descriptions.<br>Update 7 Optical characteristics<br>Update 10 Mechanical drawing. |
| 0.2 | Aug, 29, 2007 | Update 6.1 AC characteristics<br>Update 3.1 TFT LCD Panel |
| 0.3 | Sep, 27, 2007 | Update 5.3 Driving Touch Panel (Analog resistance type)<br>Update 10 MECHANICAL DRAWING |
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## 1. FEATURES

The 2.8” LCD module is the active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is applied with vertical and horizontal drivers built on the panel.

Both of horizontal and vertical scan are reversible and controlled by the serial interface commands.

The product is designed for the requirement of the green product, and the specification complies with TPO’s “Green Product Chemical Substance Specification Standard Hand Book”.

## 2. GENERAL SPECIFICATIONS

| Item | Description | Unit |
|---|---|---|
| Display Size (Diagonal) | 2.8 | Inch |
| Aspect ratio | 3:4 | - |
| Display Type | Transmissive | - |
| Active Area (HxV) | 43.2 x 57.6 | mm |
| Number of Dots (HxV) | 240 x RGB x320 | Dot |
| Dot Pitch (HxV) | 0.06 x 0.18 | mm |
| Color Arrangement | RGB Stripe | - |
| Color Numbers | 262K | - |
| Outline Dimension (HxVxT) | 52.9 x 71.7 x 3.85(Max) | mm |
| Weight | 30(Max) | G |

## 3. INPUT/OUTPUT TERMINALS

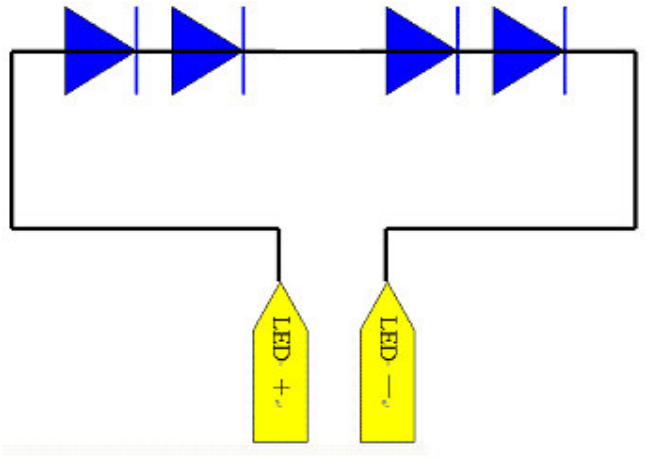
### 3.1TFT LCD Panel

Recommend connector: **FH23-39S-0.3SHW(05)/HIROSE**

| Pin | Symbol | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | LED+ | - | High Voltage Power Supply for LED | Note 3-1 |
| 2 | LED- | - | Low Voltage Power Supply for LED | Note 3-1 |
| 3 | DVDD | - | Power Supply of Digital | |
| 4 | AVDD | - | Input to DC/DC | |
| 5 | VSS | - | Ground | |
| 6 | YU | - | Touch Panel Y(12 Clock Side) | Note 3-2 |
| 7 | XL | - | Touch Panel X(Left Side) | Note 3-2 |
| 8 | YL | - | Touch Panel Y(6 Clock Side) | Note 3-2 |
| 9 | XR | - | Touch Panel X(Right Side) | Note 3-2 |
| 10 | SPI_CS | I | SPI Chip Select | Reserved for Register Setup |
| 11 | SPI_SDA | I/O | SPI Serial Data Input/Output | Reserved for Register Setup |
| 12 | VSS | - | Ground | |
| 13 | SPI_SCL | - | SPI Clock | Reserved for Register Setup |
| 14 | SD | I | Auto power on/of sequence enable input | |
| 15 | RST | I | RESET(L: Reset, H: Active) | |
| 16 | B0/ID1 | I | BLUE data Bit B0(LSB)/ LCM ID Pin 1 (Pull-high 10K to DVDD by Resistor) | |
| 17 | B1 | I | BLUE data Bit B1 | |
| 18 | B2 | I | BLUE data Bit B2 | |
| 19 | B3 | I | BLUE data Bit B3 | |
| 20 | B4 | I | BLUE data Bit B4 | |
| 21 | B5 | I | BLUE data Bit B5(MSB) | |
| 22 | G0/ID2 | I | GREEN data Bit G0(LSB)/ LCM ID Pin 2 (Pull-down 10K to VSS by Resistor) | |
| 23 | G1 | I | GREEN data Bit G1 | |
| 24 | G2 | I | GREEN data Bit G2 | |
| 25 | G3 | I | GREEN data Bit G3 | |
| 26 | G4 | I | GREEN data Bit G4 | |
| 27 | G5 | I | GREEN data Bit G5(MSB) | |

| | | | | |
|---|---|---|---|---|
| 28 | R0/ID0 | I | RED data Bit R0(LSB)/ LCM ID Pin 0<br>(Pull-down 10K to VSS by Resistor) | |
| 29 | R1 | I | RED data Bit R1 | |
| 30 | R2 | I | RED data Bit R2 | |
| 31 | R3 | I | RED data Bit R3 | |
| 32 | R4 | I | RED data Bit R4 | |
| 33 | R5 | I | RED data Bit R5(MSB) | |
| 34 | VSS | - | Ground | |
| 35 | DCK | I | Data Sampling Clock Signal | |
| 36 | VSS | - | Ground | |
| 37 | VSYNC | I | Vertical sync signal | |
| 38 | HSYNC | I | Horizontal sync signal | |
| 39 | DE | I | Data Enable | |

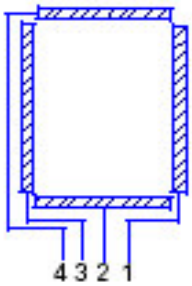
Note 3-1: The figure below shows the connection of backlight LED.




Note 3-2: Touch panel Pin

| Touch Panel Pin | Module Pin | Symbol | Description | Remark |
|---|---|---|---|---|
| 1 | 9 | XR | Touch Panel Right Side | |
| 2 | 8 | YL | Touch Panel Lower Side | |
| 3 | 7 | XL | Touch Panel Left Side | |
| 4 | 6 | YU | Touch Panel Upper Side | |

Pin Assignment for Touch panel



## 4. ABSOLUTE MAXIMUM RATINGS

Ta = 25℃, GND=0V

| Item | Symbol | MIN | MAX | Unit | Remark |
|---|---|---|---|---|---|
| Logic Supply Voltage | DVDD | -0.3 | 3.6 | V | |
| Analog Supply Voltage | AVDD | -0.3 | 3.6 | | |
| Touch Panel Operation Voltage | $V_{Touch}$ | - | 5 | V | |
| Input Signal Voltage | DE, VSYNC, HSYNC, DCK, RESETB, R[0:7], G[0:7], B[0:7], | VSS | DVDD | V | |
| Back Light Forward Current | $I_{LED}$ | -- | 20 | mA | |
| Operating Temperature | $T_{OPR}$ | -20 | 60 | ℃ | |
| Storage Temperature | $T_{STG}$ | -30 | 70 | ℃ | |

## 5. ELECTRICAL CHARACTERISTICS

### 5.1. Driving TFT LCD Panel

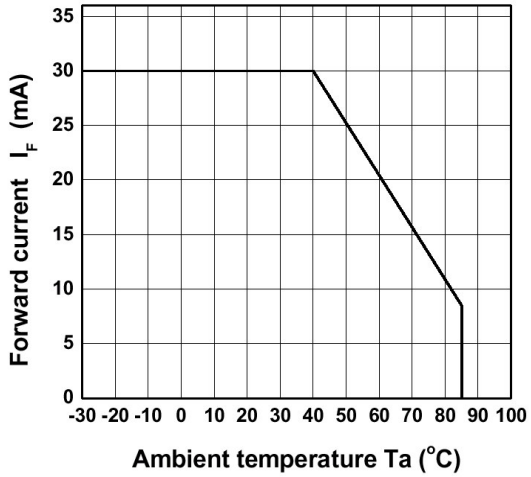
GND=0V, Ta=25℃

| Item | | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Logic Supply Voltage | | DVDD | 1.6 | 2.8 | 3.6 | V | |
| Analog Supply Voltage | | AVDD | 2.4 | 2.8 | 3.6 | V | |
| Input Signal Voltage | Low Level | $V_{IL}$ | VSS | - | 0.2x DVDD | V | Input Signal Voltage |
| | High Level | $V_{IH}$ | 0.8x DVDD | - | DVDD+0.3 | V | |
| Panel Power Consumption | | $W_P$ | - | 8.8 | 9.9 | mA | |

### 5.2 Driving Backlight

Ta=25℃

| Item | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|
| Forward Current | $I_F$ | -- | 20 | -- | mA | |
| Forward Current Voltage | $V_F$ | -- | 3.3 | -- | V | |
| Backlight Power Consumption | $W_{BL}$ | -- | 330 | -- | mW | |



5.3 Driving Touch Panel (Analog resistance type)

Ta=25℃

| Item | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|
| Resistor between terminals (XR-XL) | Rx | 200 | - | 1300 | Ω | |
| Resistor between terminals (YU-YL) | Ry | 200 | - | 1300 | Ω | |
| Operation Voltage | $V_{Touch}$ | - | 5 | 7 | V | DC |
| Line Linearity (X direction) | - | -1.5 | - | +1.5 | % | Note |
| Line Linearity (Y direction) | - | -1.5 | - | +1.5 | % | |
| Chattering | - | - | 10 | - | ms | |
| Surface Hardness | - | 3 | - | - | H | JIS K 5600 |
| Minimum tension for detecting | - | - | - | 80 | g | |
| Insulation Resistance | Ri | 20 | - | - | MΩ | At DC 25V |

Note. The minimum test force is 80 g.

The TP vendors are S/W and efast.

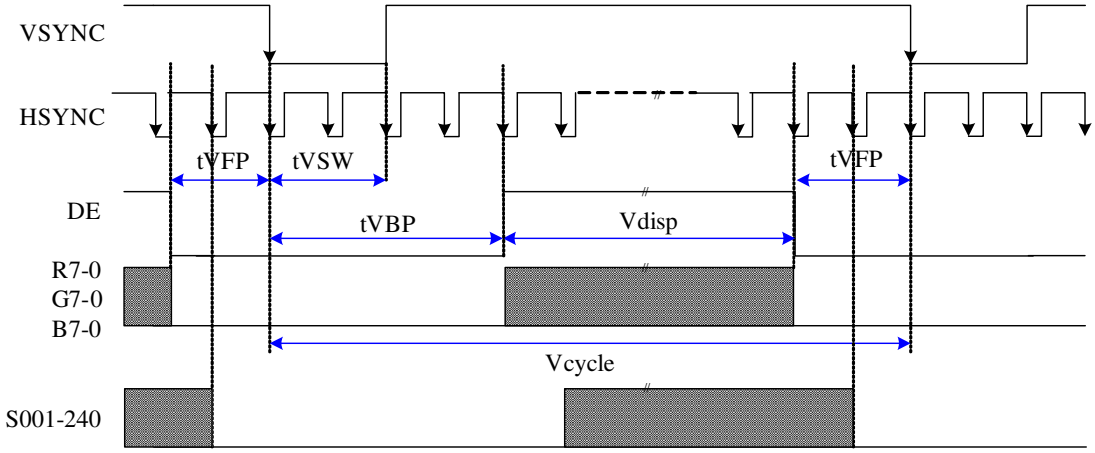
## 6. TIMING CHART

### 6.1 AC CHARACTERISTICS

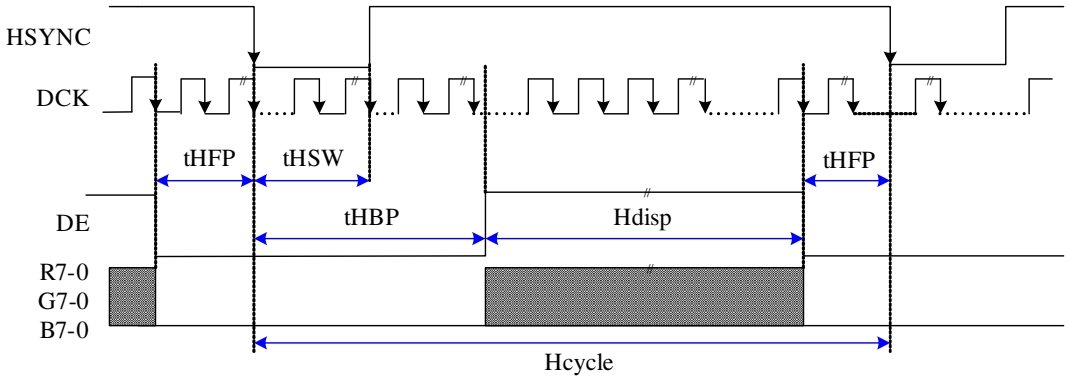
| Display Mode | Parameter | Symbol | Conditions | Ratings | | | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | | |
| Normal | Vertical Cycle | Vcycle | | 432 | 435 | 439 | HSYNC | |
| | VSYNC Pulse Low Width | tVSW | | - | 2 | - | HSYNC | |
| | Vertical Back Porch | tVBP | | - | 4 | 15 | HSYNC | |
| | Vertical Front Porch | tVFP | | 110 | 111 | - | HSYNC | |
| | Vertical Blanking Period | tVBP + tVFP | | 112 | 115 | - | HSYNC | |
| | Vertical Display Area | Vdisp | | - | 320 | - | HSYNC | |
| | Horizontal Cycle | Hcycle | | 272 | 280 | 300 | DCK | |
| | HSYNC Pulse Low Width | tHSW | | - | 10 | - | DCK | |
| | Horizontal Back Porch | tHBP | | - | 30 | 63 | DCK | |
| | Horizontal Front Porch | tHFP | | 2 | 10 | - | DCK | |
| | Horizontal Blanking Period | tHBP + tHFP | | 32 | 40 | - | DCK | |
| | Horizontal Display Area | Hdisp | | - | 240 | - | DCK | |
| | DCK Frequency | fDCK | | 6.8 | 7.3 | 7.5 | MHz | |
| | DCK Period | tDCK | | 147 | 136 | 133 | ns | |
| | VSYNC Set-up Time | tvsys | | 20 | - | - | ns | |
| | VSYNC Hold Time | tvsyh | | 20 | - | - | ns | |
| | HSYNC Set-up Time | thsys | | 20 | - | - | ns | |
| | HSYNC Hold Time | thsyh | | 20 | - | - | ns | |
| | Phase Difference of Sync Signal Falling Edge | thv | | -18 | - | 20 | DCK | |
| | DCK Low Period | tCKL | | 60 | - | - | ns | |
| | DCK High Period | tCKH | | 60 | - | - | ns | |
| | Data Set-up Time | tds | | 20 | - | - | ns | |
| | Data Hold Time | tdh | | 20 | - | - | ns | |
| | DE Set-up Time | teds | | 30 | - | - | ns | |
| | DE Hold Time | tedh | | 30 | - | - | ns | |

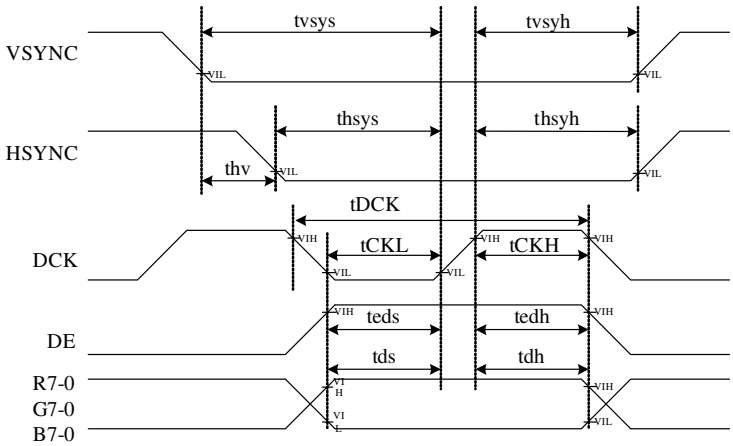
AC CHARACTERISTICS WAVEFORM

VERTICAL TIMING (VIH=0.8DVDD, VIL=0.2DVDD)



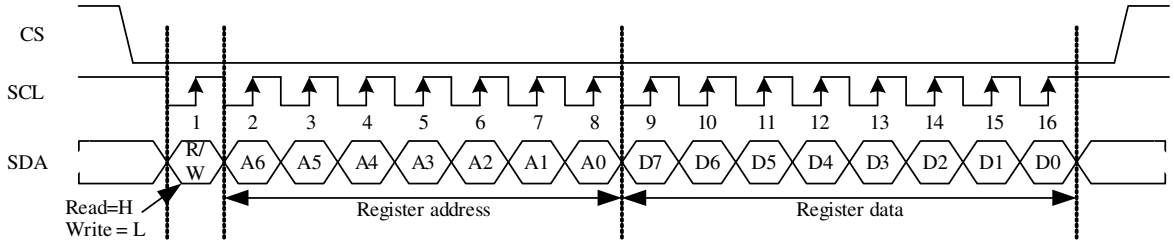

HORIZONTAL TIMING (VIH=0.8DVDD, VIL=0.2DVDD)



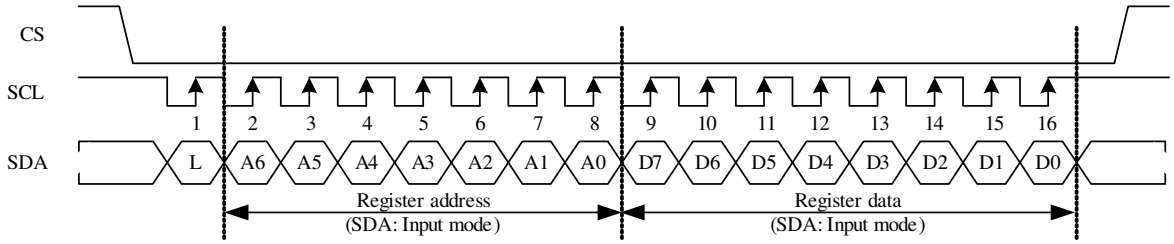



## 6.2 SERIAL INTERFACE

TIMING CHART:




WRITE MODE (RW=L):

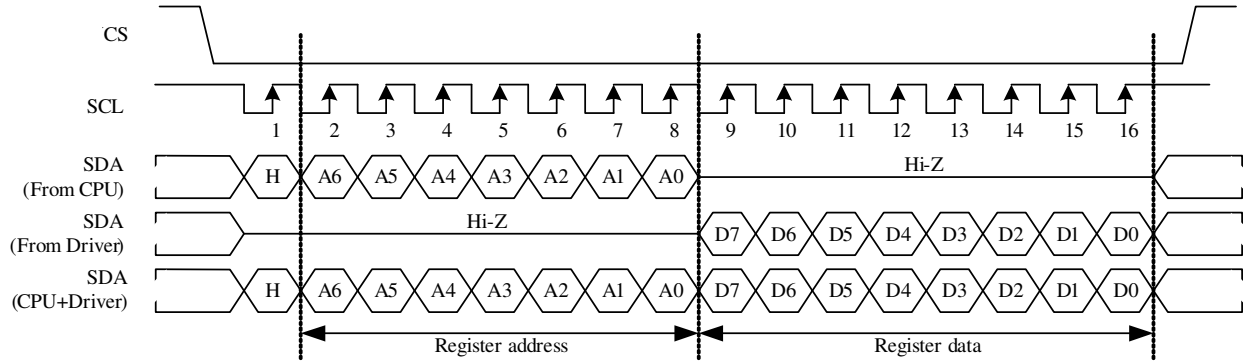



The shift register and counter are reset to their initial values when the chip select signal is inactive. Do not set the chip select signal to inactive between transmission of an 8-bit address and 8-bit data set for the command.

When using SCL wiring, the module has to be designed carefully to avoid any noise coming from reflection or from external sources. We recommend checking operation with the actual module.

If there is a break in data transmission by RESETB or CS pulse, while transferring a Command or Parameter, before Bit D0 of the byte has been completed, then ASIC will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CS) is activated after RESETB have been High state.

READ MODE (RW=H):




The read mode of the interface means that the micro controller reads data from the ASIC.

To do so the micro controller first has to send a command: the read status command.

Then the following byte is transmitted in the opposite direction. After that CS is required to go high.

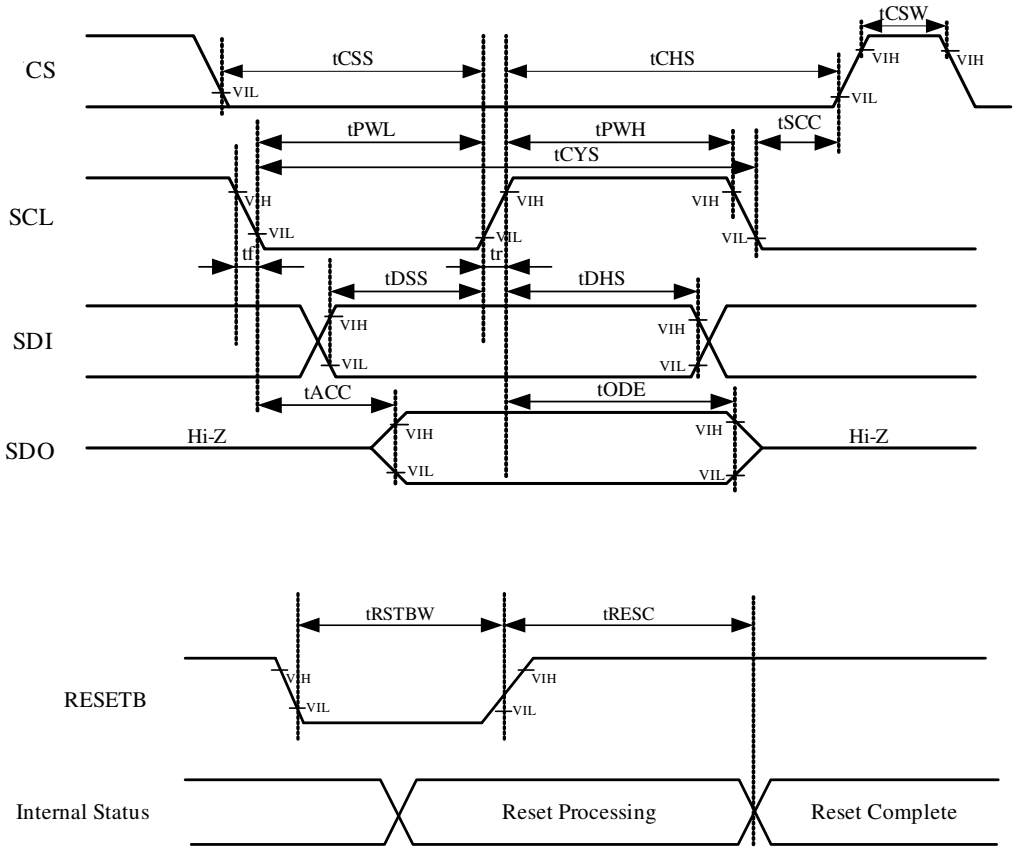
ASIC samples the SDA data input at rising SCL edges, but shifts SDA data output at falling SCL edges.

Thus the micro controller is supposed to read SDA data at rising SCL edges.

After the read status command has been sent, the SDA line must be set to tristate not later then at the rising SCL edge of the last bit.

The ASIC can read data from the register.

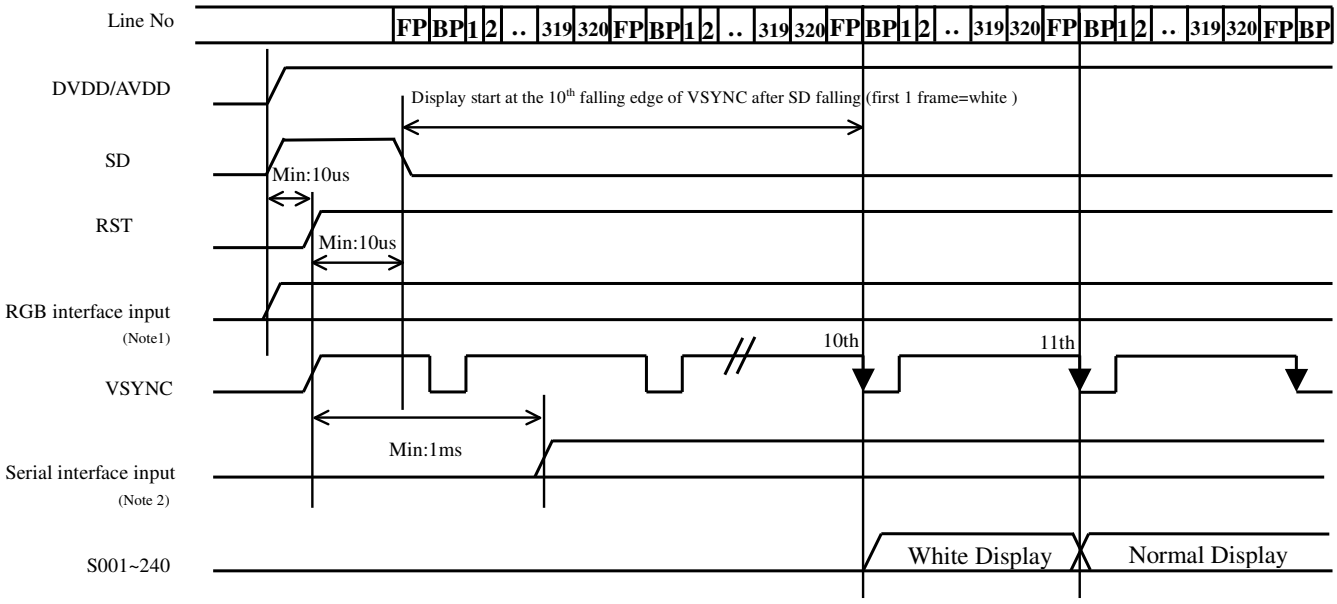
Serial interface and reset waveform (VIH=0.8DVDD，VIL=0.2DVDD)




| Serial interface and Reset | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Clock cycle | tCYS | - | 150 | - | - | ns |
| Clock High Period | tPWH | - | 60 | - | - | ns |
| Clock Low Period | tPWL | - | 60 | - | - | ns |
| Data Set-up Time | tDSS | - | 60 | - | - | ns |
| Data Hold Time | tDHS | - | 60 | - | - | ns |
| CS High width | tCSW | - | 1 | - | - | us |
| CS Set-up Time | tCSS | - | 60 | - | - | ns |
| CS Hold Time | tCHS | - | 70 | - | - | ns |
| SCL to CS | tSCC | - | 40 | - | - | ns |
| Output Access Time | tACC | - | 10 | - | 50 | ns |
| Output Disable Time | tODE | - | 25 | - | 80 | ns |
| RSTB low width | tRSTBW | - | 10 | - | - | us |
| RESET complete time | tRESC | - | - | - | 1000 | ns |

## 6.3 Power On/Off Sequence

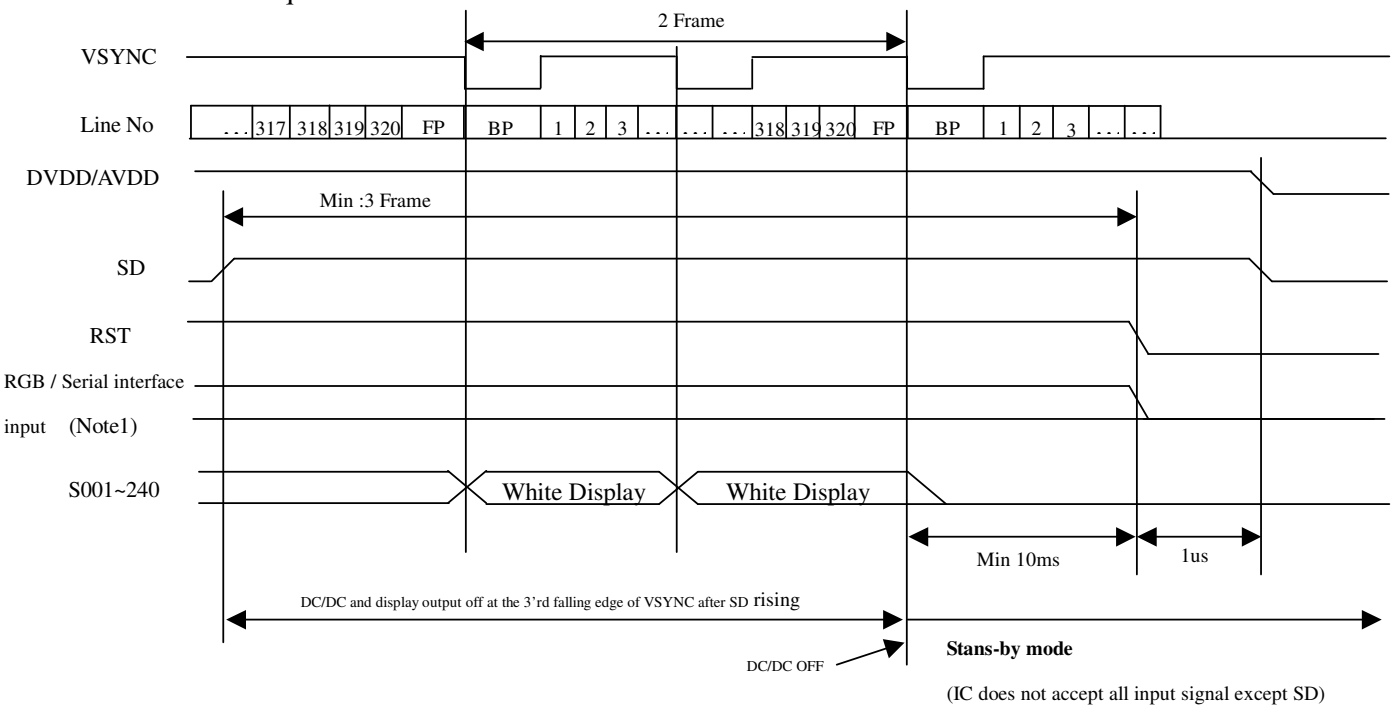
Power on sequence




(Note 1) RGB interface input – VSYNC/HSYNC/DCK/R5-0/G5-0/B5-0/DE

(Note 2) Serial interface input –(0x3f,0x18) ; (0x71,0x1F) ; (0x78,0x93)

Power off sequence




(Note 1) RGB interface input – VSYNC/HSYNC/DCK/R5-0/G5-0/B5-0/DE

## 7. OPTICAL CHARACTERISTICS

### 7.1 Optical Specification

(1) Backlight on /w touch panel

Ta=25℃

| Item | | Symbol | Condition | MIN | TYP | MAX | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Viewing Angles | | Θ11(R) | CR ≥ 10 | 30 | 40 | - | Degree | Note 7-1 |
| | | Θ12(L) | | 30 | 40 | - | | |
| | | Θ21(U) | | 40 | 55 | - | | |
| | | Θ22(D) | | 10 | 15 | - | | |
| Contrast Ratio | | CR | Θ=0° | 200 | 300 | - | | Note 7-2 |
| Response Time | Rising | Tr | | - | 5 | 10 | ms | Note 7-3 |
| | Falling | Tf | | - | 11 | 20 | | |
| Luminance ($I_F$=20mA) | | L | | 180 | 220 | 390 | cd/m$^2$ | Note 7-4 |
| Uniformity | | - | | 75 | 80 | - | % | Note 7-6 |
| Chromaticity | NTSC% | - | | 45 | 50 | - | | |
| | White | x | | 0.275 | 0.310 | 0.345 | - | Note 7-5 |
| | | y | | 0.290 | 0.330 | 0.370 | | |
| | Red | x | | 0.565 | 0.615 | 0.665 | | |
| | | y | | 0.300 | 0.350 | 0.400 | | |
| | Green | x | | 0.290 | 0.34 | 0.390 | | |
| | | y | | 0.509 | 0.559 | 0.609 | | |
| | Blue | x | | 0.096 | 0.146 | 0.196 | | |
| | | y | | 0.062 | 0.112 | 0.162 | | |

(2) Picture Quality

| Category | Item | Description | **Remark** |
|---|---|---|---|
| Picture Quality | Flicker | Quantification need to be <-20 db | |
| | Cross-Talk | Cross Talk Ratio should be less than 2%. | |
| | Hot Spot | There should be no noticeable hot spot and light leakage found on LCD, especially on LED side. | Note 7-6 |
| | Image Stick | There should be no latent image found on full screen white, black and middle gray pattern after 48 hour (room temperature) burn-in by displaying 5 * 5 checkerboard pattern. | |

7.2 Basic Measure Conditions

(1) Driving voltage

Vcc= 5 V

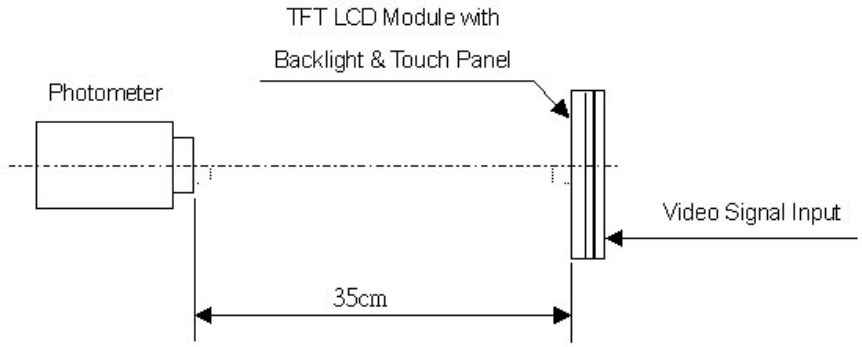
(2) Ambient Temperature: Ta=25℃

(3) Testing Point: Measure in the display center point and the test angle Θ=0°

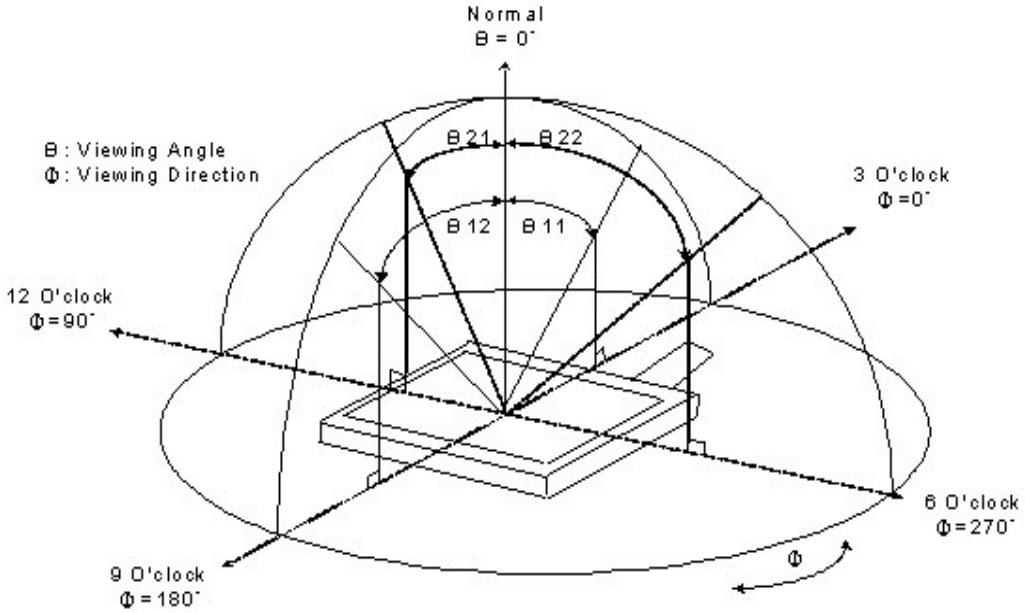
(4) LED Current: $I_F$=20mA.

(5) Testing Facility

Environmental illumination: ≤ 1 Lux




Note 7-1: Viewing angle diagrams:

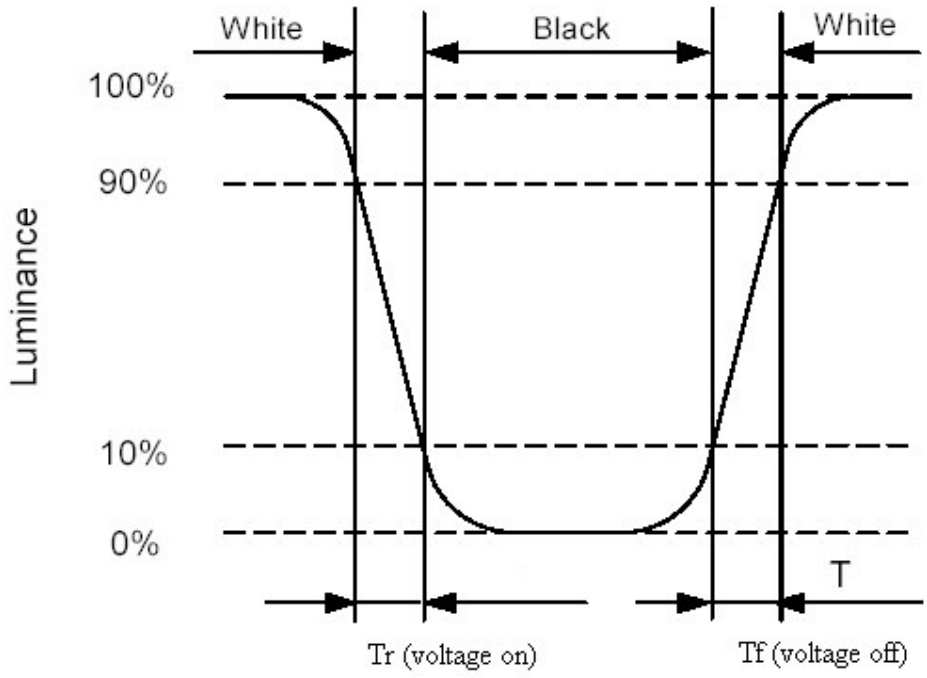



Note 7-2: Contrast Ratio:

Contrast ratio is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 7-3: Definition of response time:




Note 7-4: Luminance:

Test Point: 9 points average of Display (Measured by DMS)

Note 7-5: Chromaticity: The same test condition as Note 7-4.

Note 7-6 : Hot Spot (Curtain Mura) Examination

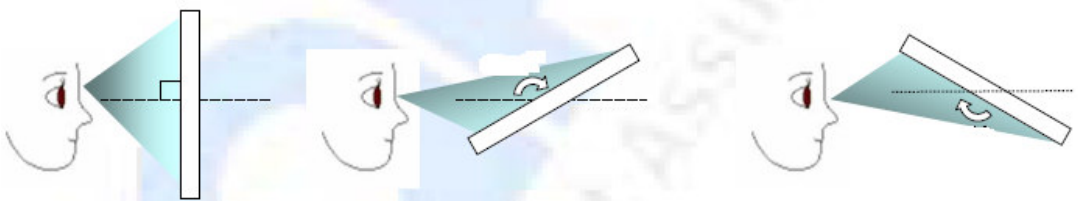
-Test Condition

Dark room with ambient illuminance under 5 lux.

Observation Direction: With up and down 45° vertical or in perpendicular view angle. (Refer to the figure below)

Observation Area: Entire Screen (especially on the side of Back Light Source.)

Back Light Luminance: Tune to be maximum.



**In Perpendicular** **Down 45°** **Up 45°**

Test Pattern: Full screen white pattern

## 8. REILIABILITY

**TBD**

## 9. HANDLING CAUTIONS

### 9.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is.

(2) The machine and working table for the panel should have ESD protection strategy.

(3) In handling the panel, ionized airflow decreases the charge in the environment is necessary.

(4) In the process of assemble the module, shield case should connect to the ground.

### 9.2 Environment

(1) Working environment of the panel should be in the clean room.

(2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionized air to prevent the electrostatic discharge.

### 9.3 Touch panel

(1) The front touch panel is vulnerable to heavy weight, so any input must be done by special stylus or by a finger. Do not put any heavy stuff on it.

(2) When any dust or stain is observed on a film surface, clean it using a glass lens cleaner for something similar.

### 9.4 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface or condensation as panel power on will corrode panel electrode.

(4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

(5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible.

9.5 Design notes on touch panel

(1) Explanation of each boundary of touch panel

A.Boundary of Double-sided adhesive

a. Electrically detectable within this zone.

When holding the touch panel by housing, it needs to be held at outside of this zone.

b. Film is supported by double-sided adhesive tape.

B.Viewing area

a. Cosmetic inspection to be done for this area.

This area is set as inside of boundary of double-sided adhesive with tolerance.

C.Boundary of transparent insulation

a. Purpose is to "Help" to secure insulation.

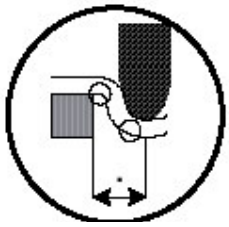
b. Electrical insulation on this area is not guaranteed.

c. We do recommend not to hold this area by something like housing or gasket.

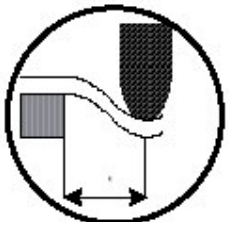
D.Active area

a. This area is where the performance is guaranteed.

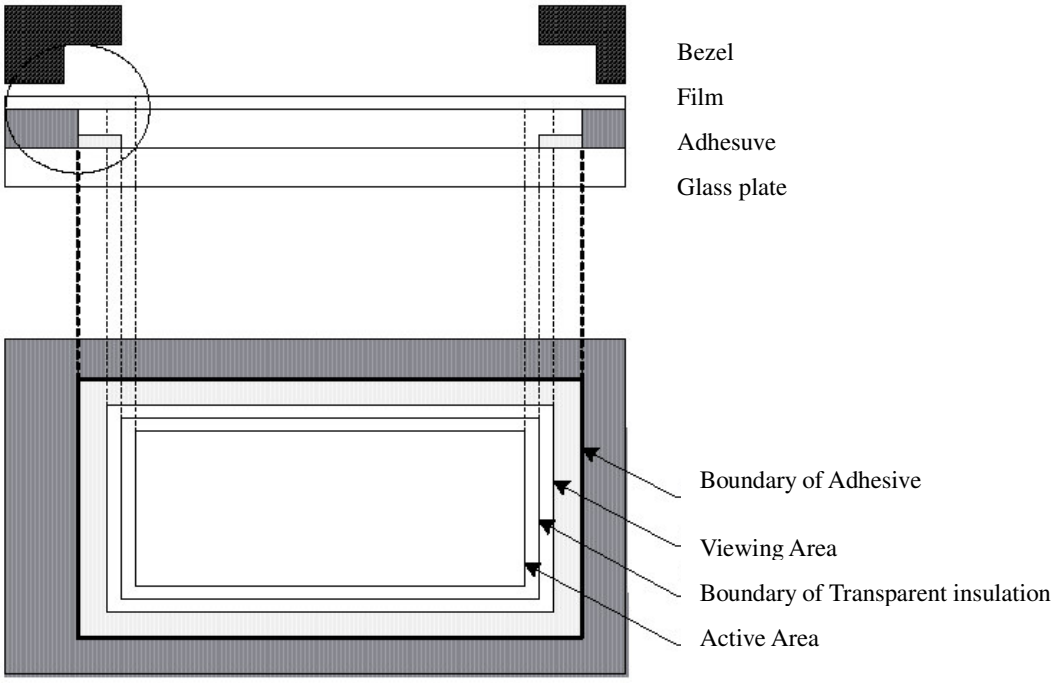
This area set as 2.3mm inside from the boundary area of double-sided adhesive tape since its neighboring area is less durable to writing friction.



There is some possibility to damage ITO



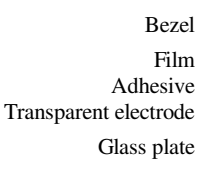
No Damage to ITO



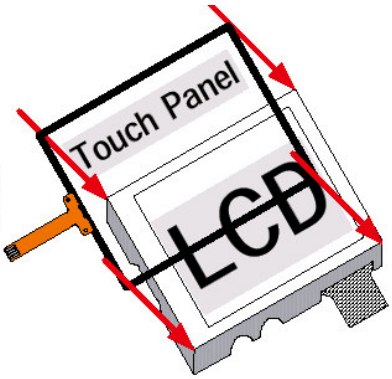

(2) Housing and touch panel

A. Please have clearance between the side of touch panel and any conductive material such as metal frame (Drawing.1). Transparent electrode exists on glass of touch panel from end to end.

B. It is recommended to fix a touch panel on the LCD module chassis rather than the touch panel housing. Clinging at conductive material and side of touch panel might cause the malfunction.

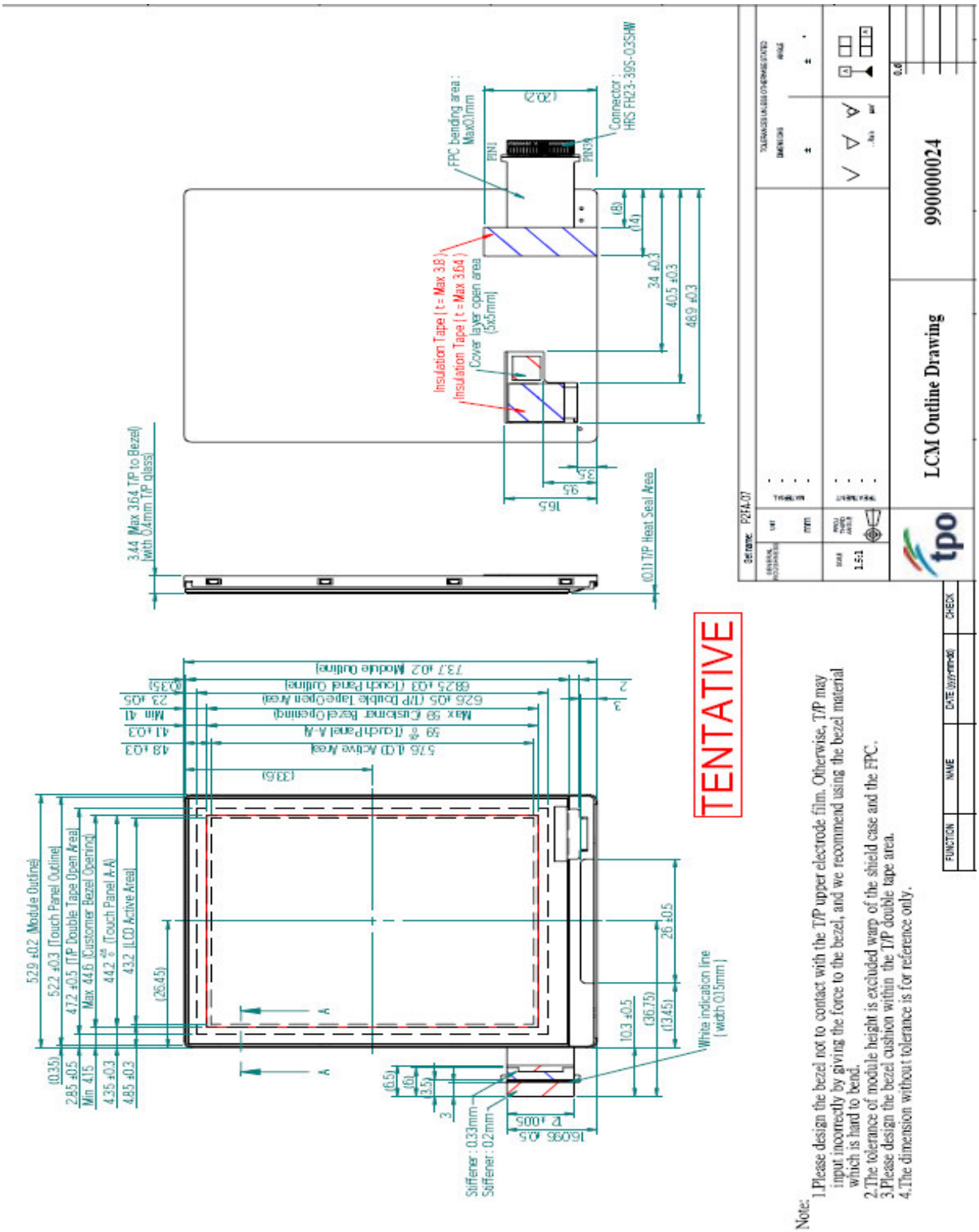


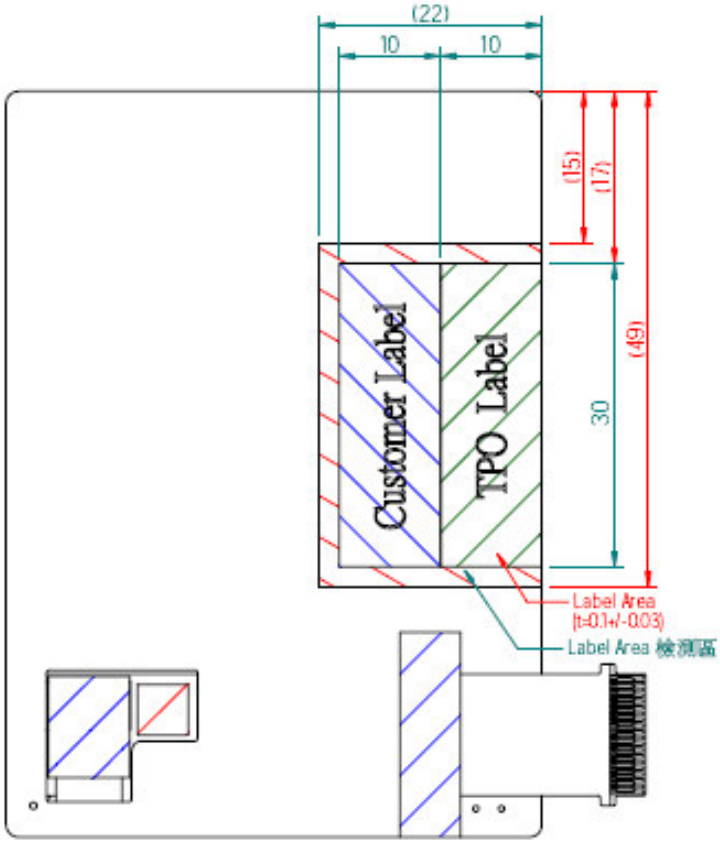

Drawing 1



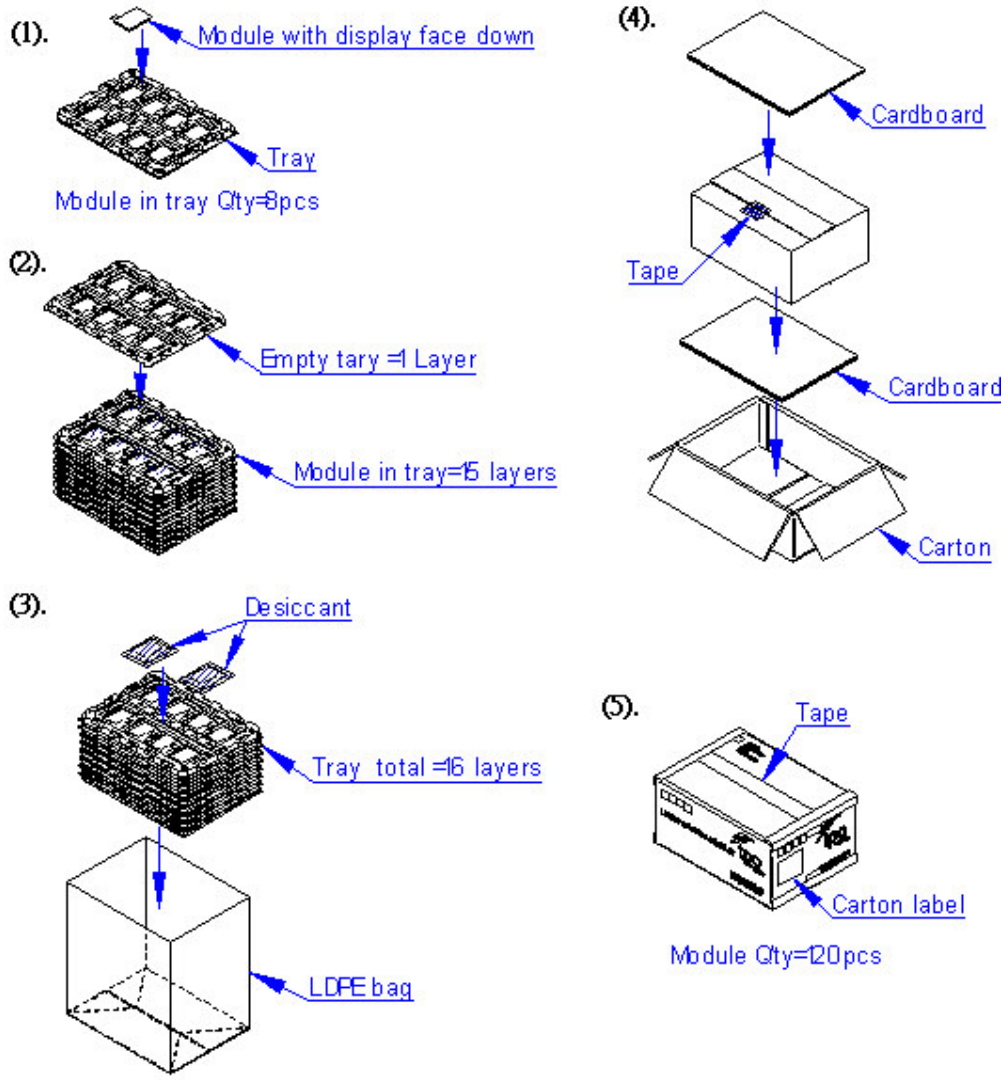

Drawing 2

## 10 MECHANICAL DRAWING





## 11 Packing Drawing




2.8" module (990000024) delivery packing method

(1). Module packed into tray cavity (with Module display face down).

(2). Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.
2pcs desiccant put above the empty tray

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4). Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton.
Put 1pc cardboard above the package unit.

(5). Carton tapping with adhesive tape