TFT LCD Specification

Model NO.: TD035TTEA3

Customer Signature
Date

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Table of Contents

NO.	Item	Page
	Cover Sheet	1
	Table of Contents	2
	Record of Reversion	3
1	Features	4
2	General Specification	4
3	Input / Output Terminals	5
4	Absolute Maximum Ratings	8
5	Electrical Characteristics	9
6	Block Diagram	11
7	Timing Chart	12
8	Power On/Off Sequence	15
9	Optical Characteristics	16
10	Reliability	18
11	Handling Cautions	19
12	Application Note	20
13	Mechanical Drawing	29
14	Packing Drawing	30

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Record of Reversion

Rev	Issued Date	Description
1.0	2006/07/28	New release
1.1	2006/12/27	Changed the product of luminance & transmittance ratio

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1. FEATURES

The 3.5" LCD module is the Transmissive active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is used and its COG design. The LCD module includes touch panel, backlight and TFT LCD panel with minimal external circuits and components required.

2. GENERAL SPECIFICATION

Item		Description	Unit
Display Size (Diagonal)		3.5 inch (8.9cm)	-
Display Type		Transmissive	-
Active Area **(H x V)**		70.08 X 52.56	**mm**
Number of Dots **(H x V)**		320 x RGB x 240	**dot**
Dot Pitch **(H x V)**		0.073 X 0.219	**mm**
Color Arrangement		RGB Stripe	-
Color Numbers		262,144 (6 bits)	-
Outline Dimension **(H x V x T)**		76.9 X 63.9 X 4 w/o FPC	**mm**
Weight		42.15 ±2g	**g**
Power Consumption	LCD Panel + Driver IC	35 (Max.)	**mW**
	Backlight	384 (Typ, I_F= 20mA)	

* Exclude FPC and protrusions.

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3. INPUT/OUTPUT TERMINALS

3.1 TFT LCD module

Pin	Symbol	I/O	Description	Remark
1	LED-	I	LED Cathode	
2	LED-	I	LED_Cathode	
3	LED+	I	LED_Anode	
4	LED+	I	LED_Anode	
5	GND	I/O	Ground	
6	X1	I	X_Right	
7	Y1	I	Y_Bottom	
8	X2	I	X_Left	
9	Y2	I	Y_Up	
10	GND		Ground	
11	NC		NC	
12	NC		NC	
13	NC		NC	
14	RESET	I	Reset	
15	CS	I	Chip Select	
16	SCL	I	Serial Clock	
17	SDI	I	Serial Data	
18	NC		NC	
19	NC		NC	
20	DATA0	I	Blue Data(LSB)	
21	DATA1	I	Blue Data	
22	DATA2	I	Blue Data	
23	DATA3	I	Blue Data	
24	DATA4	I	Blue Data	
25	DATA5	I	Blue Data(MSB)	
26	NC		NC	
27	NC		NC	
28	DATA6	I	Green Data(LSB)	
29	DATA7	I	Green Data	
30	DATA8	I	Green Data	
31	DATA9	I	Green Data	
32	DATA10	I	Green Data	

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33	DATA11	I	Green Data(MSB)	
34	NC		NC	
35	NC		NC	
36	DATA12	I	Red Data(LSB)	
37	DATA13	I	Red Data	
38	DATA14	I	Red Data	
39	DATA15	I	Red Data	
40	DATA16	I	Red Data	
41	DATA17	I	Red Data(MSB)	
42	HSYNC	I	Horizontal Synchronous Signal	
43	VSYNC	I	Vertical Synchronous Signal	
44	DOTCLK	I	Data Colck	
45	NC		NC	
46	NC		NC	
47	VDDIO/VDC	I	Vdigital/ Vanalog power source	Typ=3.3V
48	VDDIO/VDC	I	Vdigital/ Vanalog power source	Typ=3.3V
49	NC		NC	
50	NC		NC	
51	NC		NC	
52	NC		NC	
53	NC		NC	
54	NC		NC	
55	NC		NC	
56	NC		NC	
57	NC		NC	
58	ENABLE	I	Data enabling signal	
59	GND	I/O	Ground	
60	GND	I/O	Ground	

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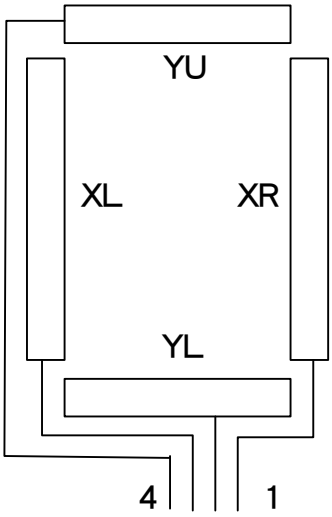
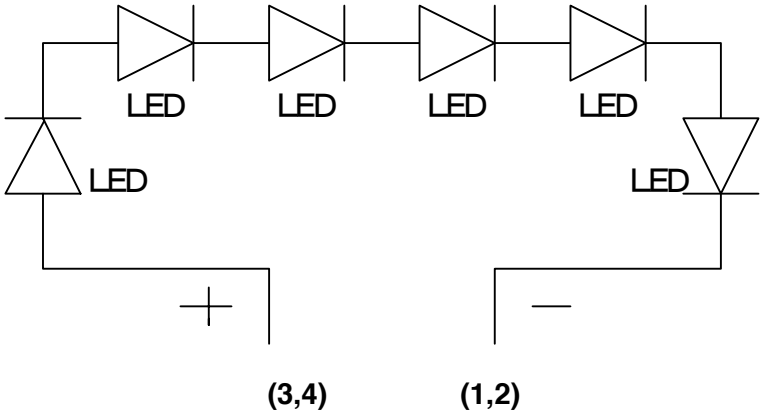
3.2 Touch panel Pin

Touch Panel Pin	Module Pin	Symbol	Description	Remark
1	6	XR	Touch Panel Right Side	
2	7	YL	Touch Panel Lower Side	
3	8	XL	Touch Panel Left Side	
4	9	YU	Touch Panel Upper Side	



3.3 Back light pin assignment



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4. ABSOLUTE MAXIMUM RATINGS

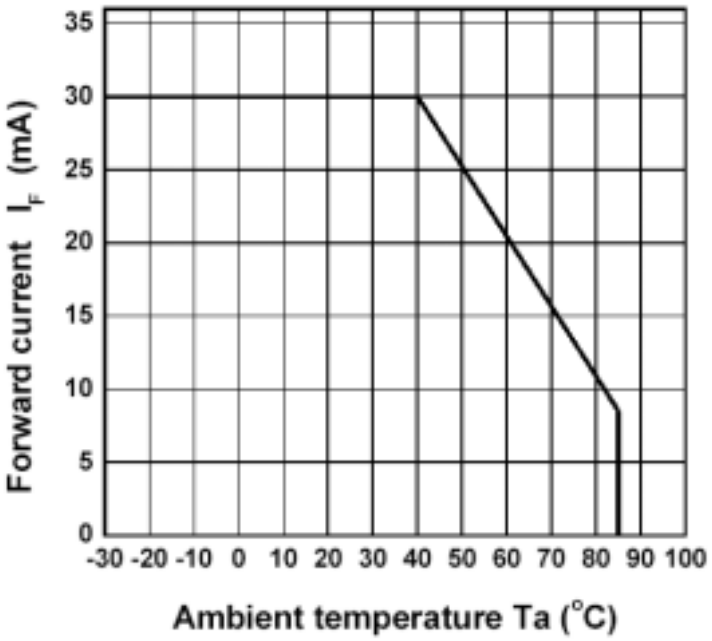
GND=0V

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage	VDDI	-0.3	NIL	+6.5	V	
Analog Supply Voltage	VDC	-0.3	NIL	+6.5	V	
Maximum supply voltage	V_{IN}	-0.3	NIL	VDDI+0.3	V	
	V_{OUT}	-0.3	NIL	VDDI+0.3	V	
Touch Panel Operation Voltage	V_{Touch}	NIL	5	7	V	
Backlight LED forward Voltage	V_F	3.0	3.2	3.3	V	
Backlight LED reverse Voltage	V_R	NIL	NIL	5	V	
Backlight LED forward current (Ta=25℃)	I_F	NIL	20	30	mA	Note 2
Operating Temperature	Topr.	**-20**	**NIL**	**+70**	℃	
Storage Temperature	Tstg.	**-30**	**NIL**	**+80**	℃	

Note 1. Reference voltages must satisfy the following relationship: VDC ≧ VDDIO.

Note 2. Relation between maximum LED forward current and ambient temperature is showed as bellow.

Forward Current Derating Curve



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5. ELECTRICAL CHARACTERISTICS

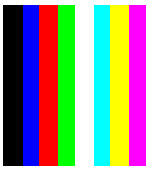
5.1 Driving TFT LCD Panel

Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage		VDDI	+1.65	+3.3	+3.6	V	
		VDD	+2.4	+3.3	+3.6	V	
Input Voltage		VIL	VSS	—	0.3VDDI	V	Note 1
		VIH	0.7VDDI	—	VDDI	V	
Output Voltage		VOL	VSS	—	0.2VDDI		DOUT
		VOH	0.8VDDI	—	VDDI		
Input Current		I_{IL}	-10	—	—	uA	
		I_{IH}	—	—	10	uA	
Supply Current	Normal mode	I_{VDD}	—	9.53	10.11	mA	Note 2 Note 3
Power consumption	Normal mode		—	31.50	33.36	mW	Note 4
	Sleep mode		—	-	-	mW	

Note 1: Related pins: VSYNC, HSYNC, DE, PCLK, OSC1, OSC2, FDONIN, XRES, XCS, SCL, DIN, and PD0-17

Note 2: The supply current specification is measured at the line inversion test pattern (Color bar vertical as the diagram shown below).



Note 3: Based on VDDIO=3.3V, VDC=3.3V

Note 4: LCD Panel + Driver IC

5.2 Driving backlight

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	NIL	20	30	mA	LED/Part

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LED Life Time	-	NIL	5,000	NIL	Hours	I_F: 15mA
Forward Current Voltage	V_F	3.0	3.2	3.3	V	I_F: 20mA, LED/Part

Note: Backlight driving circuit is recommend as the fix current circuit.

5.3 Driving touch panel (Analog resistance type) Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Resistor between terminals (XR-XL)	Rx	100	NIL	1100	Ω	
Resistor between terminals (YU-YL)	Ry	100	NIL	1100	Ω	
Operation Voltage	V_{Touch}	NIL	5.0	7.0	V	DC
Line Linearity (X direction)	-	-1.5	NIL	+1.5	%	Note
Line Linearity (Y direction)	-	-1.5	NIL	+1.5	%	
Chattering	-	NIL	NIL	10	ms	
Surface Hardness	-	3	NIL	NIL	H	JIS K 5600
Minimum tension for detecting	-	NIL	NIL	80	g	(TP AA inside 2mm)
Insulation Resistance	Ri	20	NIL	NIL	MΩ	DC 25V

Note. The minimum test force is 120 g.

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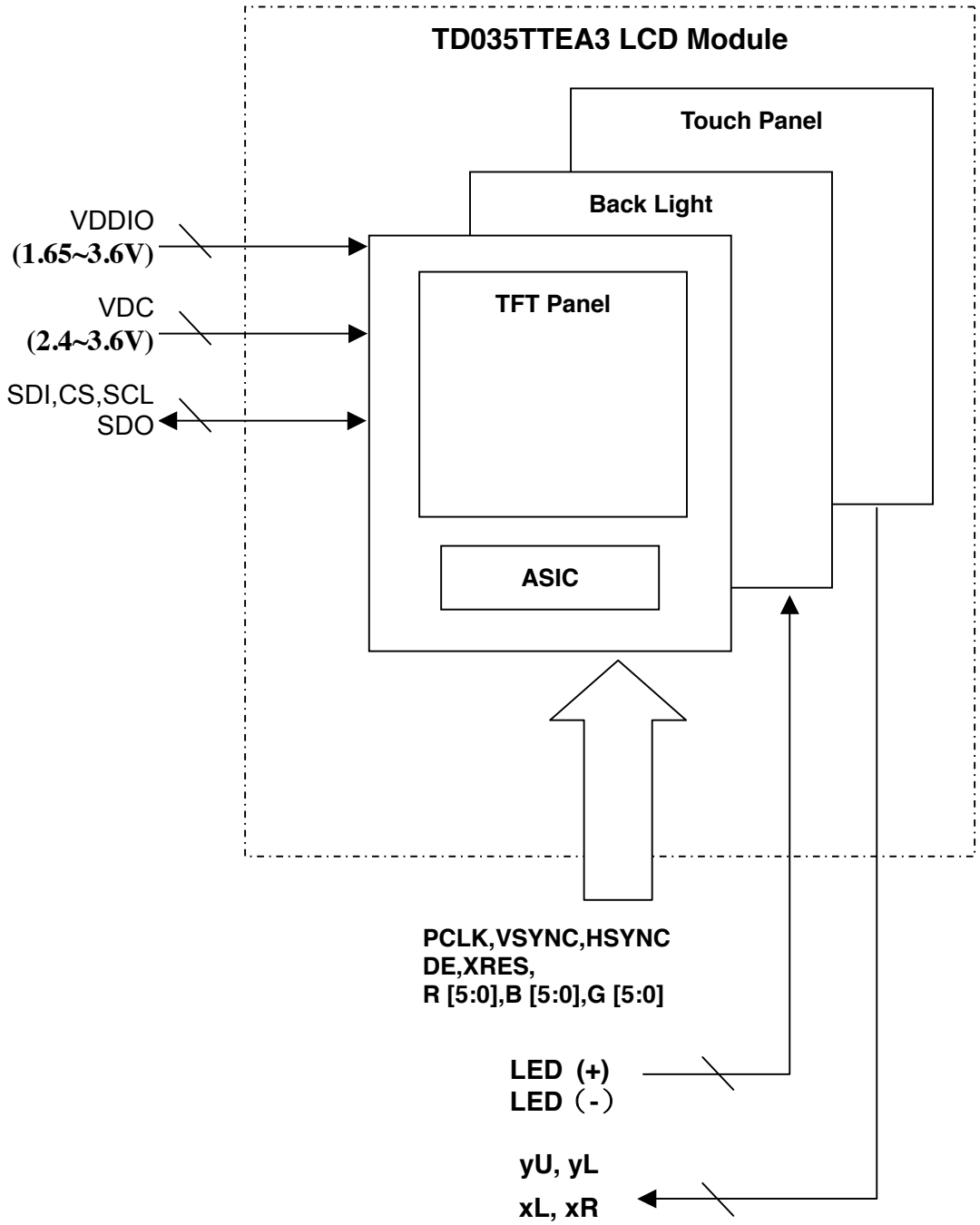
6. BLOCK DIAGRAM



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7. TIMING CHART

7.1 Display timing

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Vertical cycle	VP		246	264	282	Line
Vertical low pulse width	VS		2	8	14	Line
Vertical front porch			2	8	14	Line
Vertical back porch	VBP		2	8	14	Line
Vertical data start	VDS	VS+VBP	4	16	28	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	24	42	Line
Vertical active area	VDISP		NIL	240	NIL	Line
Vertical refresh rate	VRR		50	70	-	Hz
Horizontal cycle	HP		326	440	472	dot
Horizontal Sync Pulse width	HS		2	38	256	dot
Horizontal back porch	HBP		2	40	256	dot
Horizontal front porch	HFP		2	42	256	dot
Horizontal Data start	HDS	HS+HBP	4	72	150	dot
Horizontal blanking period	HBL	HS+HBP+HFP	6	120	152	dot
Horizontal active area	HDISP		NIL	320	NIL	dot
Clock frequency	fclk		4	8	8.65	MHz
	tclk		250	125	115	nS

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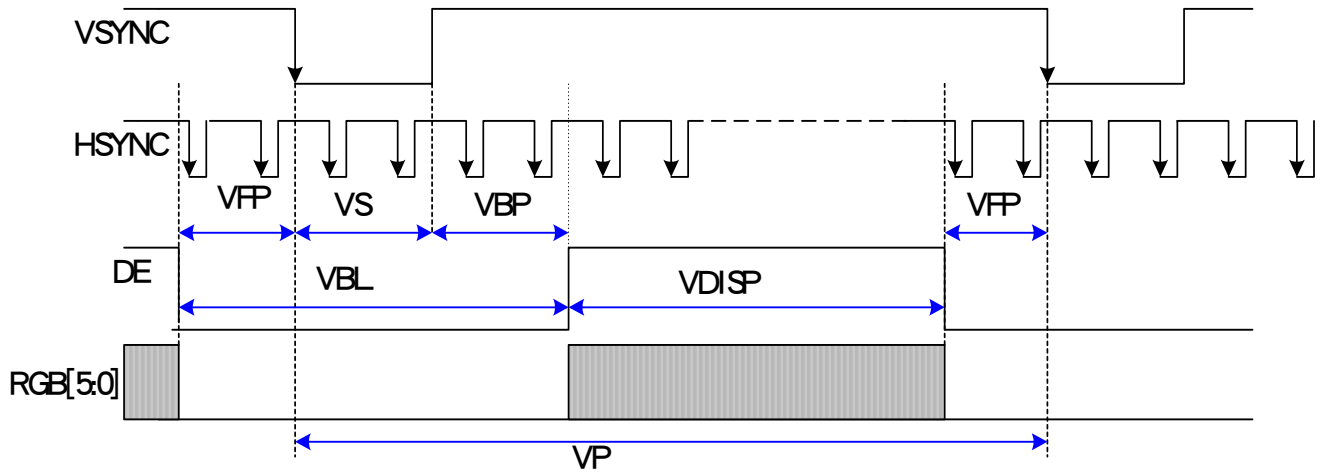
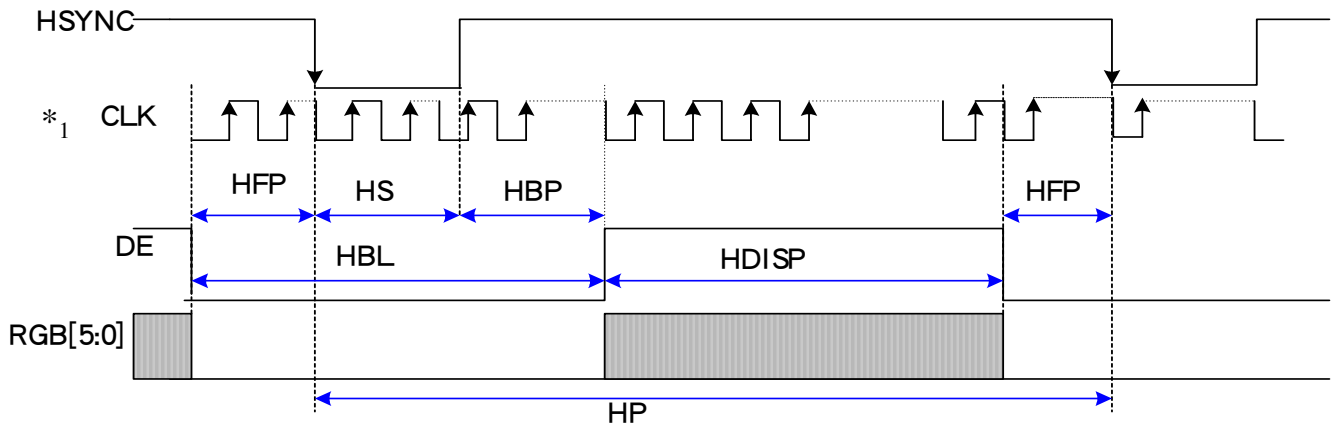
Input timing chart

＜Vertical Timing chart＞



＜Horizontal Timing chart＞



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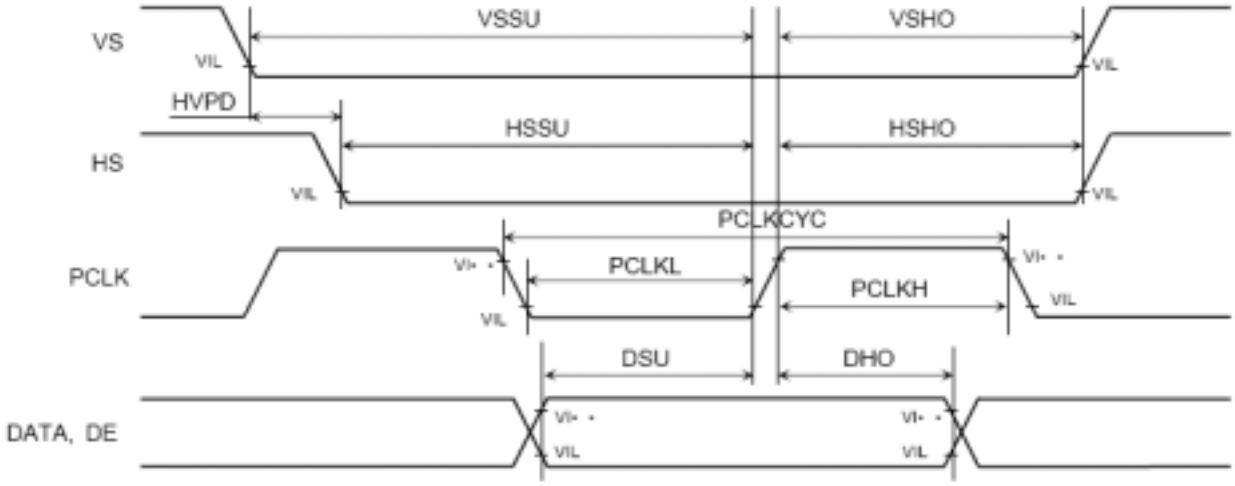
Setup/ Hold Timing chart

RGB Interface



AC Characteristics:

Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
VS setup time	VSSU	—	15	—	—	ns
VS hold time	VSHO	—	15	—	—	ns
HS setup time	HSSU	—	15	—	—	ns
HS hold time	HSHO	—	15	—	—	ns
VS-HS fall time	HVPD	—	0	—	—	ns
PCLK cycle time	PCLKCYC	—	70	—	—	ns
PCLK signal " L " pulse width	PCLKL	—	20	—	—	ns
PCLK signal " H " pulse width	PCLKH	—	20	—	—	ns
Data setup time	DSU	—	15	—	—	ns
Data hold time	DHO	—	15	—	—	ns

Note 1 : Unless otherwise specified, V_{DD} = 2.4 to 3.6 V, V_{DDI} = 1.65 to 3.6 V, V_{SS} = 0 V, Ta = −30 to 80 °C

Note 2 Input signal rise / fall time : tr, tf ≤ 15ns

Note 3 : The threshold voltage of Input singal : VIH = 0.7 × V_{DDI}, VIL = 0.3 × V_{DDI}

8. Power On/Off Sequence

Power On Sequence

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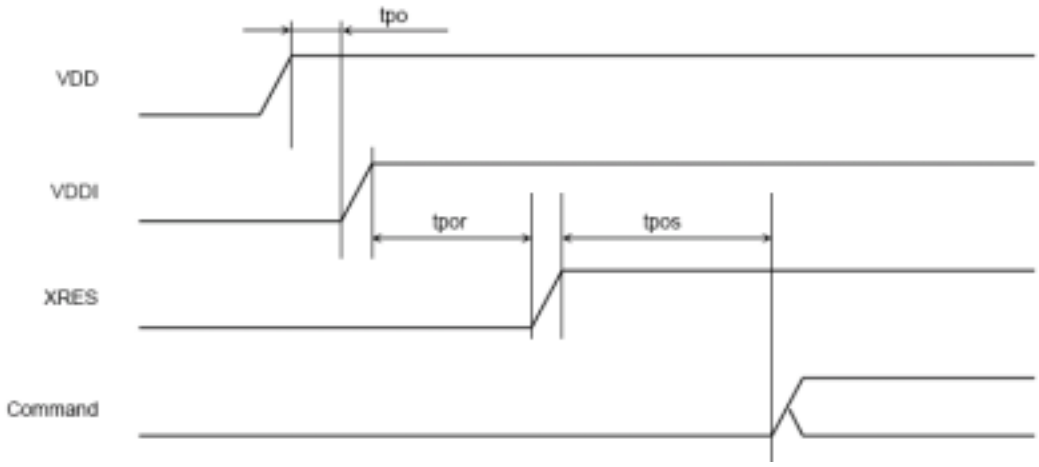
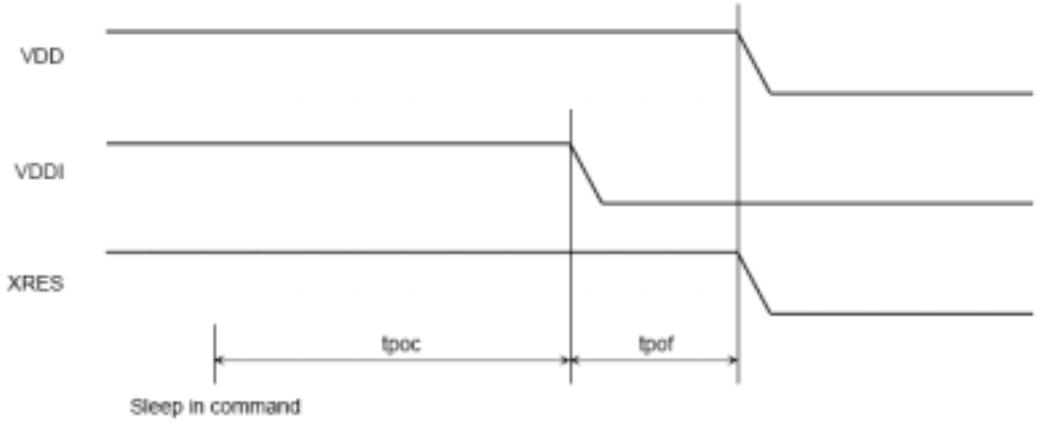


Power Off Sequence



Characteristics	Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
V_{DD} - V_{DDI} power on time	tpo	—	—	—	1	ms
Power on reset time	tpor	—	100	—	—	ns
Reset release time	tpos	—	1	—	—	ms
Sleep mode release time	tpoc	—	250	—	—	ms
V_{DDI} - V_{DD} power off time	tpof	—	—	—	1	ms

Note 1: Unless otherwise specified, V_{DD} = 2.4 to 3.6 V, V_{DDI} = 1.65 to 3.6 V, V_{SS} = 0 V, Ta = −30 to 80 °C

9. Optical Characteristics

9.1 Optical Specification

(1) Transmissive Mode (Back Light On w/i Touch panel， LED current I_F= 20 mA)

Ta=25℃

Item	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	ΘR	CR ≥ 10	-	60	-	Degree	Note 9-1
	ΘL		-	60	-		

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	ΘU			-	60	-		
	ΘD			-	60	-		
Response Time	Tr+Tf		Θ=0°	-	20	-	Ms	Note 9-2
Ratio	CR		Θ=0°	-	300:1	-	-	Note 9-3
Luminance	L		Θ=0° I_F =20 mA	260	290	NIL	cd/m^2	Note 9-4
NTSC	-		-	-	50	-	%	Note 9-4
Uniformity	-		-	-	80	-	%	Note 9-5
Chromaticity	W	X	Θ=0°	0.280	0.330	0.380	NIL	Note 9-6
		Y		0.290	0.340	0.390		
	R	X		0.545	0.595	0.645		
		Y		0.315	0.365	0.415		
	G	X		0.281	0.332	0.382		
		Y		0.518	0.568	0.618		
	B	X		0.092	0.142	0.192		
		Y		0.028	0.079	0.128		

9.2 Basic measure condition

(1) Ambient temperature: Ta=25℃

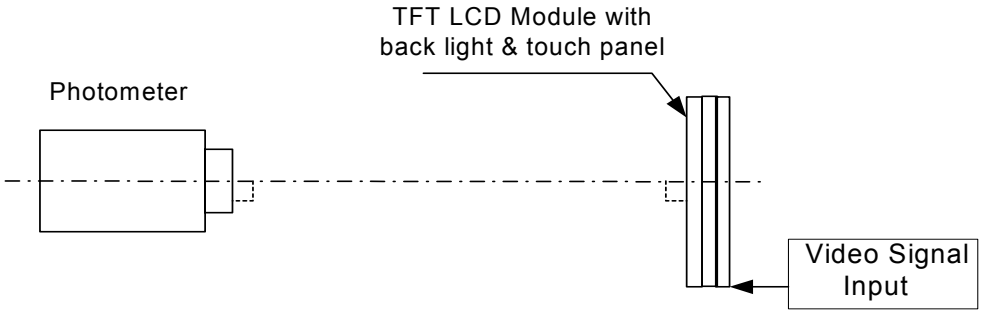
(2) Testing point: measure in the display center point and the test angle Θ=0°

(3) Testing Facility

Environmental illumination: ≤ 1 Lux

(4) Measuring System

a. System A



Note 9-1: Viewing angle diagrams (Measure System A)

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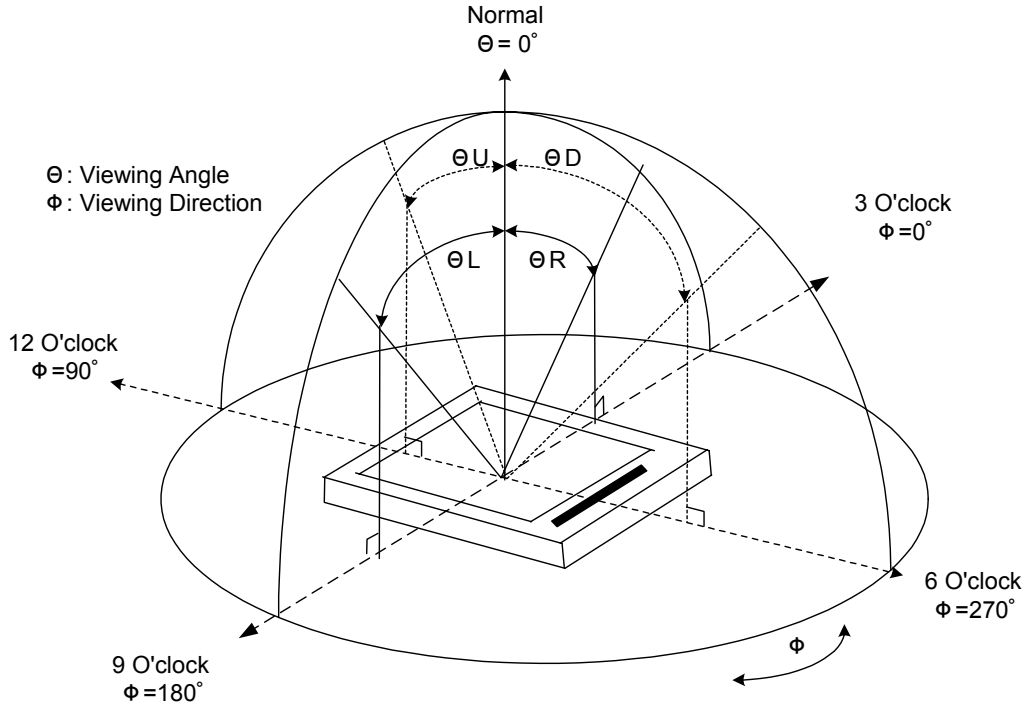
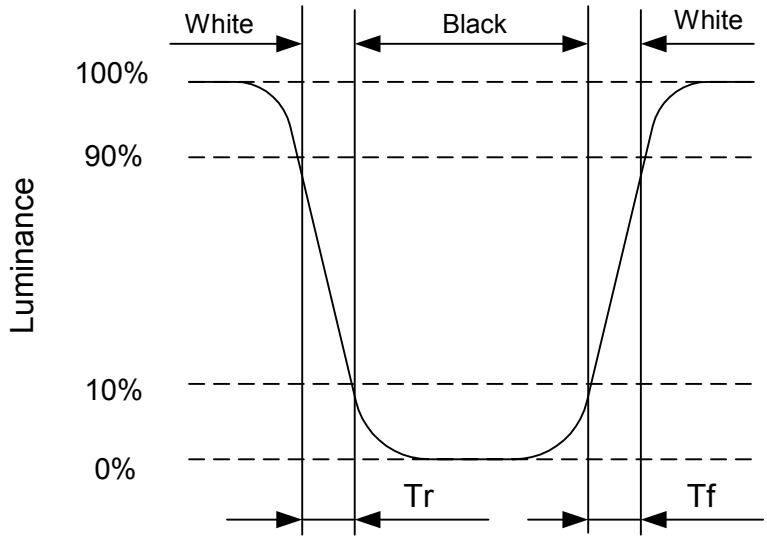


Note 9-2: Definition of response time: (Measure System A)



Note 9-3: Contrast ratio in back light On (Measure System A)

Contrast Ration is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 9-4: Luminance: (Measure System A)

Test Point: Display Center

LED current I_F= TBD mA

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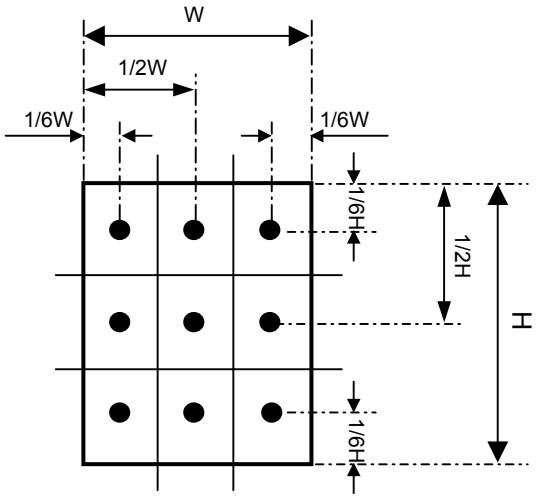
Note 9-5: Uniformity (Measure System A)

The luminance of 9 points as the black dot in the figure shown below are measured and the uniformity is defined as the formula:



Active Area (W x H)

Note 9-6: White chromaticity: The same test condition as Note 9-4.

10. Reliability

No	Test Item	Condition
1	High Temperature Operation	Ta=+70℃, 240hrs **0~60℃(20~90%RH) 61~70℃(20~60%RH)**
2	High Temperature & High Humidity Operation	Ta=+40℃, **95%** RH, 240hrs
3	Low Temperature Operation	Ta= -20℃, 240hrs
4	High Temperature Storage (non-operation)	Ta=+80℃, 240hrs **0~60℃(20~90%RH) 61~80℃(20~60%RH)**
5	Low Temperature Storage (non-operation)	Ta= -30℃, 240hrs
6	Thermal Shock (non-operation)	-20℃(30 min)← → 70℃(30 min),30 cycles
7	**Terminal Discharge (non-operation) (LCD surface)**	C=150pF, R=330 Ω; Discharge: Air: **±15kV**; Contact: **±8kV** 5 times / Point; 5 Points / Panel
8	Shock (non-operation)	Acceleration: 100G; Period: 2.5 ms Directions: ±X, ±Y, ±Z; Cycles: Three times
9	Pin Activation Test (Touch Panel)	Hit **1,000,000** times with a silicon rubber of R8mm, HS 60. Hitting Force: 250g

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		Hitting Speed: 3 time/sec
10	Writing Friction Resistance Test (Touch Panel)	Pen: R0.8mm Polyacetal stylus Load: 250g Speed: 3 Strokes/sec Stroke: 35mm **100,000** times

11. Handling Cautions

11.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.

(2) The machine and working table for the panel should have ESD protection strategy.

(3) In handling the panel, ionized air flowing decrease the charge in the environment is necessary.

(4) In the process of assemble the module; shield case should connect to the ground.

11.2 Environment

(1) Working environment should be clean room.

(2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionized to prevent the electrostatic discharge.

11.3 Touch panel

(1) The front touch panel is vulnerable to heavy weight, so any input must be done by special stylus or by a finger. Do not put any heavy stuff on it.

(2) When any dust or stain is observed on a film surface, clean it using a lens cleaner for glasses or something similar.

11.4 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface when panel is powered on will corrode panel electrode.

(4) Before opening up the packing bag, watch out the environment for the panel storage. High temperature and high humidity environment is prohibited.

(5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and

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soap as soon as possible

12. Application Note

12.1 Design notes on touch panel

(1) Explanation of each boundary of touch panel

A. Boundary of Double-sided adhesive

a. Electrically detectable within this zone.

When holding the touch panel by housing, it needs to be held at outside of this zone.

b. Film is supported by double-sided adhesive tape.

B. Viewing area

a. Cosmetic inspection to be done for this area.

This area is set as inside of boundary of double-sided adhesive with tolerance.

C. Boundary of transparent insulation

a. Purpose is to "Help" to secure insulation.

b. Electrical insulation on this area is not guaranteed.

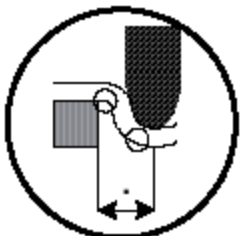
c. We do recommend not to hold this area by something like housing or gasket.

D. Active area

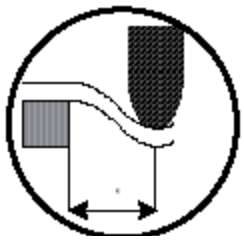
a. This area is where the performance is guaranteed.

This area set as some distance inside from the boundary area of double-sided adhesive tape since its neighboring area is less durable to writing friction.

b. Please refer to the attached module drawing for the bezel opening and window size design.



There is some possibility to damage ITO



No Damage to ITO

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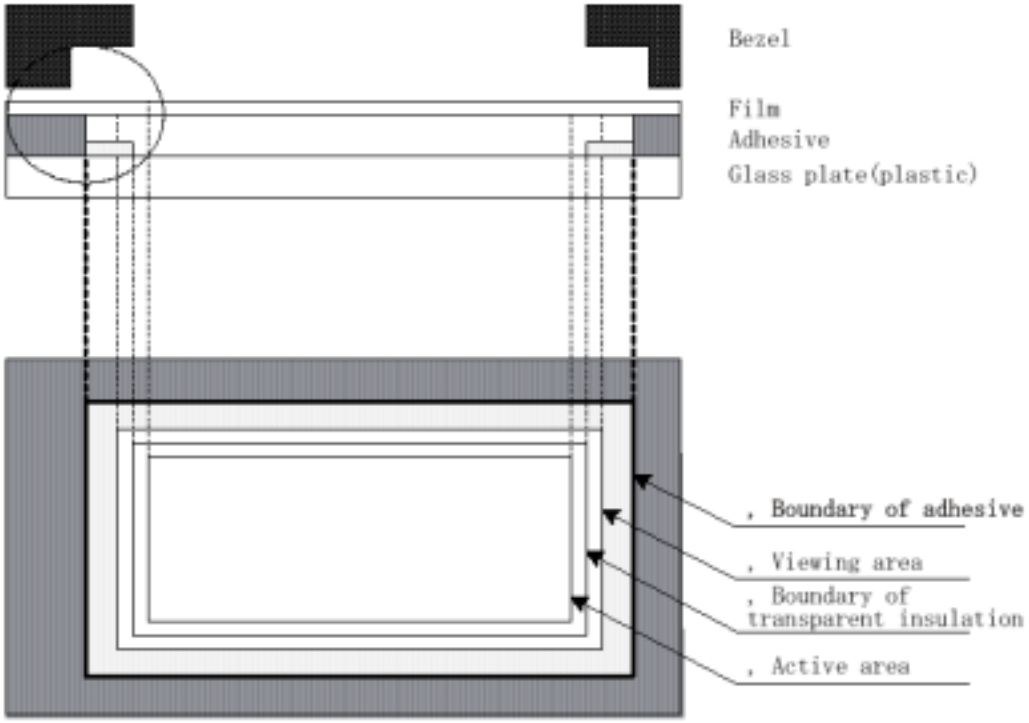
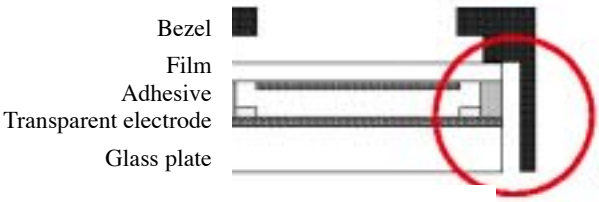


(2) Housing and touch panel

a. Please have clearance between the side of touch panel, and any conductive material such as metal frame.(drawing.1) Transparent electrode exists on glass of touch panel from end to end.

b. It is recommended to fix a touch panel on the LCD module chassis rather than the touch panel housing. Clinging at conductive material and side of touch panel might cause malfunction.



Drawing 1

Drawing 2

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12.2 Note for image discharge circuit

(1) The image will remain on display when the power is suddenly cut off in abnormal condition, ie, unit dropped and battery fell out. The phenomenon is because the electrical charge well be held in pixel, if there is no extra input signal to release it, the residual image occurs.

(2) The imaging discharge circuit is used for clearing the image residual on display. The circuit is designed on panel and customer can input signal to driver the function especially in the case that the battery or power supplier unit are removable.

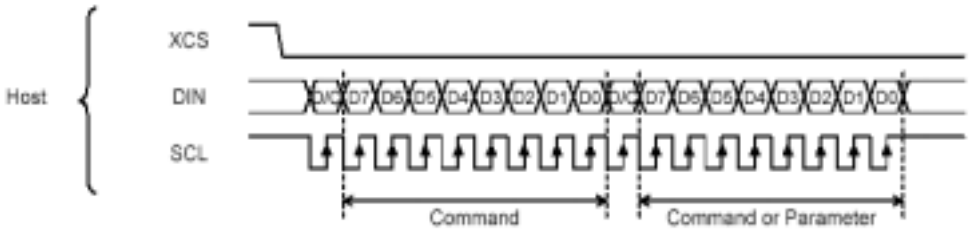
(3) The circuit below is designed on panel to avoid image sticking.

12.3 Note for 3-Wire command

The LCM support the 3-Wire serial interface to set internal register. Read/Write bit D/C, Serial address D7 to D0 (DIN) and serial data D7 to D0 (DOUT) are read at the rising edge of the serial clock, via the serial input pin. This data is synchronized on the rising edge of eighth serial clock and is then converted to parallel data. The serial interface signal timing chart is shown below.

a) Command write instruction

While the XCS signal is low, a zero detected in the DIN signal causes the serial interface controller to recognize the next SCL rising edge as D7 of a command and start fetching data. In the input data, MSB = D7 and LSB = D0. Once the LSB of the command has been input, the serial interface controller expects either a command or parameter data according to the rising edge. If D/C = high, it recognizes the data the host transmits next as a parameter. If D/C = low, it recognizes the next data as a command.



b) Status read

The JBT6K78-AS(PI) allows the host to issue a request (status read instruction) to retrieve the internal chip status and ID information. Status data and ID information are output on the rising edge of SCL. After reading status data and ID information, the host can enable the next command transfer by driving XCS high temporarily and then back low. Note that the status read protocol varies with the operation command type.

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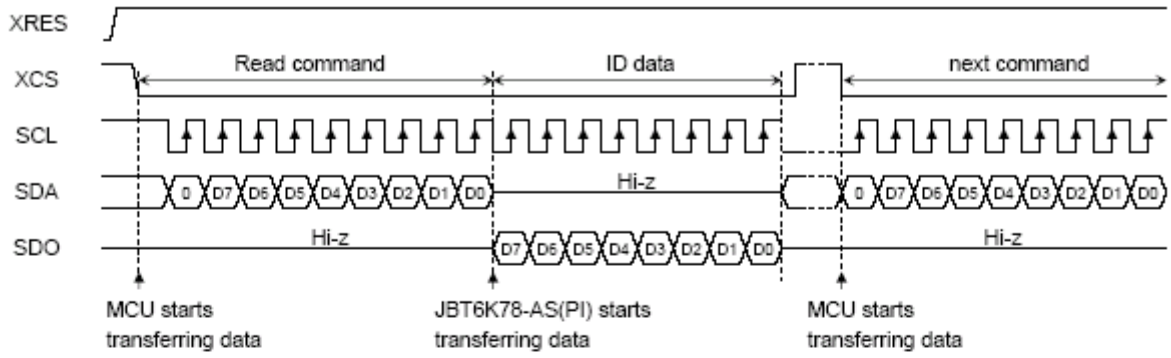
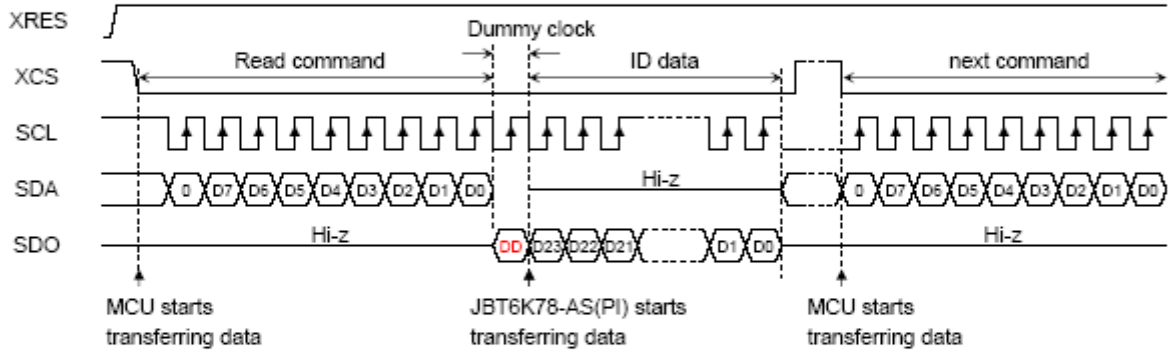
- ••For the 06h, 07h, 08h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, DAh, DBh, and DCh operation commands

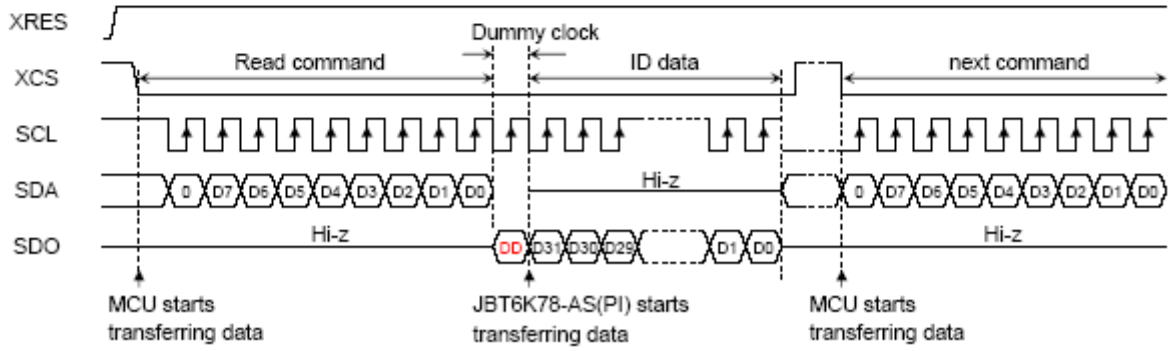


- ••For the 04h operation command



Note 1: The ID data is 24 bits long.

- ••For the 09h operation command



Note 2: The ID data is 32 bits long.

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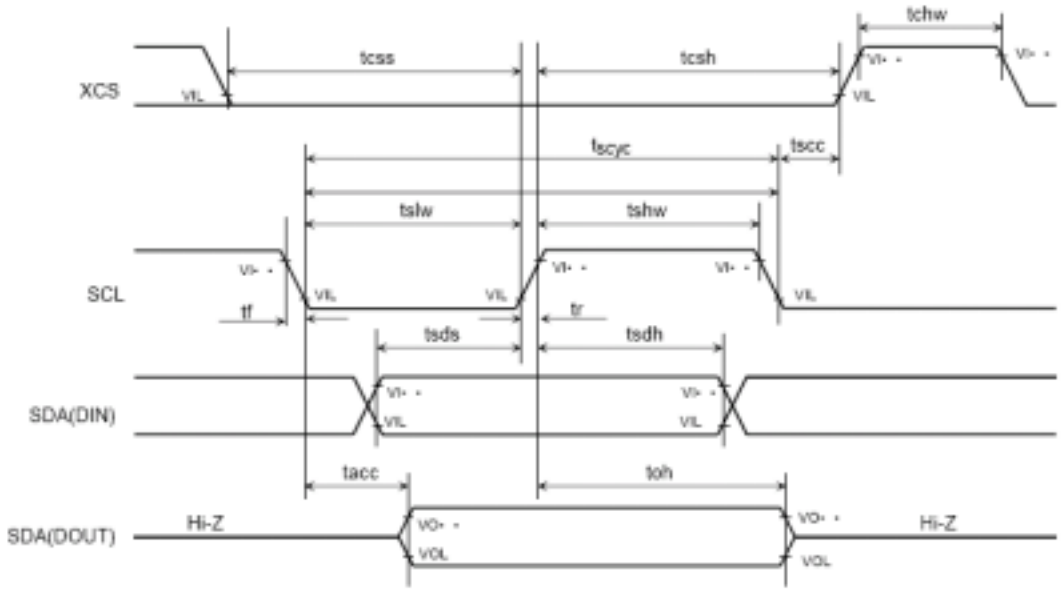
Serial Interface



Characteristics		Symbol	Test Conditions/Circuit	Min	Typ.	Max	Unit
Write mode	Serial clock cycle time	tscyc	—	100	—	—	ns
	SCL signal " H " pulse width	tshw	—	35	—	—	ns
	SCL signal " L " pulse width	tslw	—	35	—	—	ns
	Data setup time	tsds	—	20	—	—	ns
	Data hold time	tsdh	—	20	—	—	ns
Read mode	Serial clock cycle time	tscyc	—	150	—	—	ns
	SCL signal " H " pulse width	tshw	—	60	—	—	ns
	SCL signal " L " pulse width	tslw	—	60	—	—	ns
	Output data delay time	tacc	(Note 3, 5, 6)	10	—	50	ns
	Output data hold time	toh	(Note 3, 5)	15	—	50	ns
XCS signal " L " cancel time		tscc	—	20	—	—	ns
XCS signal " H " pulse width		tchw	—	40	—	—	ns
XCS signal setup time		tcss	—	30	—	—	ns
XCS signal hold time		tcsh	—	35	—	—	ns

Note 1 : Unless otherwise specified, V_{DD} = 2.4 to 3.6 V, V_{DDI} = 1.65 to 3.6 V, V_{SS} = 0 V, Ta = −30 to 80 °C

Note 2 Input signal rise / fall time : tr, tf ≤ 15 ns

Note 3 : SDA(DOUT) signal rise / fall time : tr, tf ≤ 15 ns

Note 4 : The threshold voltage of Input singal : VIH = 0.7 × V_{DDI}, VIL = 0.3 × V_{DDI}

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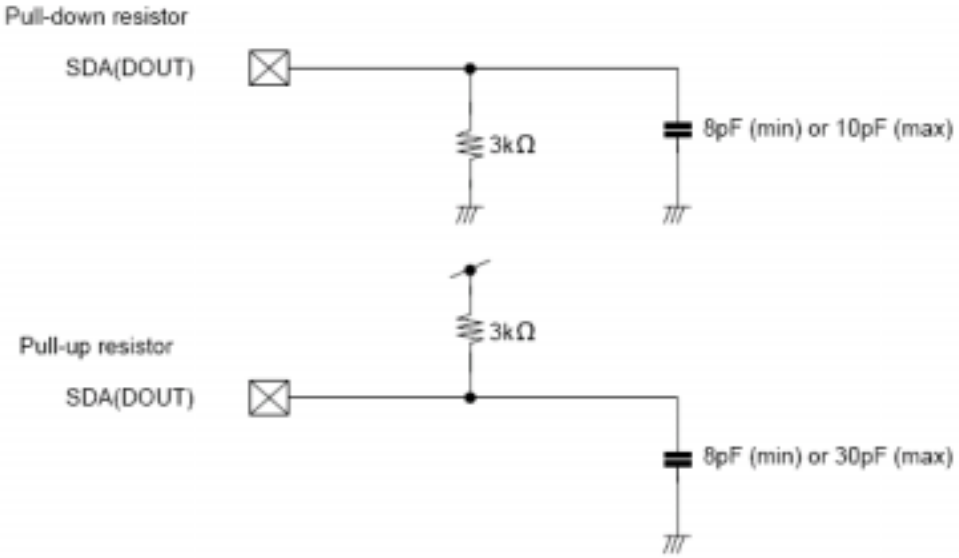
Note 5 : Applied when the following load model is connected.



Note 6 : When measuring the minimum value of tacc, the threshold value of SDA(OUT) is applied to a point 0%(VOL) and 100%(VOH). Moreover, when measuring the maximum value of tacc, the threshold value of SDA(OUT) is applied to a point 20%(VOL) and 80%(VOH).

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Summary of Operation Command:

Operation Code	Function	Instruction	Byte	Initial		FR Sync.
				HW-Reset	SW-Reset	
00h	No operation**	NOP	0	-	-	
01h	Software reset**	SWRESET	0	-	-	
04h	Read display identification information	RDDIDIF	3	000015h	000015h	
06h	Read red color**	RDRED	1	00h	00h	
07h	Read green color**	RDGREEN	1	00h	00h	
08h	Read blue color**	RDBLUE	1	00h	00h	
09h	Read Display Status**	RDDST	4	00610000h	00 maintained 0040h	
0Ah	Read Display Power Mode**	RDDPM	1	08h	08h	
0Bh	Read Display MADCTL **	RDDMADCTL	1	00h	maintained	
0Ch	Read Display Pixel Format**	RDDCOLMOD	1	60h	maintained	
0Dh	Read Display Image Mode**	RDDIM	1	00h	00h	
0Eh	Read Display Signal Mode**	RDDSM	1	00h	maintained	
10h	Sleep In**	SLPIN	0	Enable		
11h	Sleep Out**	SLPOUT	0	Disable		
12h	Partial Mode On**	PTLON	0	Disable		
13h	Normal Display Mode On**	NORON	0	Enable		
20h	Display Inversion off**	INVOFF	0	Enable		*
21h	Display Inversion on**	INVON	0	Disable		*
26h	Gamma Set**	GAMSET	1	01h	01h	*
28h	Display Off**	DISPOFF	0	Enable		
29h	Display On**	DISPON	0	Disable		
2Ah	Column Address Set**	CASET	4	0000015Fh	0000015Fh	*
2Bh	Page Address Set**	PASET	4	00000031h	00000031h	*
2Ch	Memory Write**	RAMWR	ANY	maintained	maintained	
30h	Partial area**	PTLAR	4	00000031h	00000031h	*
36h	Memory Access Control**	MADCTL	1	00h	maintained	*
3Ah	Interface Pixel Format**	COLMOD	1	60h	maintained	*
3Bh	Image scaling**	IMASCA	1	00h	00h	*
DAh	Read ID1**	RDID1	1	xx	xx	
DBh	Read ID2**	RDID2	1	xx	xx	
DCh	Read ID3**	RDID3	1	15h	15h	

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Operation Code	Function	Instruction	Byte	Initial		FR Sync.
				HW-Reset	SW-Reset	
B0h••	Blanking period control (1)••	BLANK1	1••	01h	Maintained	*
B1h••	Blanking period control (2)••	BLANK2	2••	0202h	Maintained	*
B2h••	Power supply circuit ON / OFF control	POW	1••	0Eh	Maintained	*
B3h••	Full color / 8 colors mode switching	COLS	1••	01h	Maintained	*
B4h••	Display mode setup••	DISPMOD	1••	00h	Maintained	
B5h••	VCS voltage adjustment••	AJVCS	1••	20h	Maintained	*
B6h••	Output control••	OCONT	2••	FFFDh	Maintained	
B7h••	DCCK, DCEV timing setup••	DCTIM	1••	13h	Maintained	*
B8h••	Reserved register••	—	2••	0000h	Maintained	*
B9h••	VCOM voltage adjustment••	AJVCOM	1••	40h	Maintained	
BAh••	Booster operation setup••	DCFUN	1••	48h	Maintained	
BBh••	Booster mode setup••	DCMOD	1••	33h	Maintained	*
BCh••	Booster frequency setup••	DCF	1••	0Ah	Maintained	*
BDh••	Regulator and operational amplifier capability setup••	REGSET	1••	55h	Maintained	*
BEh••	ASW signal slew rate adjustment••	ASWSR	1••	12h	Maintained	*
BFh••	CKV timing control ON/OFF••	ADDOFF	1••	01h	Maintained	*
C0h••	CKV1,2 timing control••	CKVTIMC	2••	0C12h	Maintained	*
C1h••	Reserved register••	—	2••	0000h	Maintained	*
C2h••	OEV timing control (1)••	OEVTIMC	2••	0C12h	Maintained	*
C3h••	Reserved register••	—	2••	0000h	Maintained	*
C4h••	ASW timing control (1)••	ASWTIMC1	2••	1236h	Maintained	*
C5h••	ASW timing control (2)••	ASWTIMC2	1••	0Dh	Maintained	*
C6h••	Sleep out FR count setup (A)••	SLPOFRA	1••	11h	Maintained	*
C7h••	Sleep out FR count setup (B)••	SLPOFRB	1••	11h	Maintained	*
C8h••	Sleep out FR count setup (C)••	SLPOFRC	1••	11h	Maintained	*
C9h••	Sleep in FR count setup (D)••	SLPILD	2••	2040h	Maintained	*
CAh••	Sleep in FR count setup (E)••	SLPILE	2••	3060h	Maintained	*
CBh••	Sleep in FR count setup (F)••	SLPILF	2••	1020h	Maintained	*
CCh••	Sleep in FR count setup (G)••	SLPILG	2••	60C0h	Maintained	*
CDh••	White data insertion count setup for ×2 scaling••	SCALWIN	1••	00h	Maintained	*
CEh••	Gamma 1 fine tuning (1)••	AJGAM11	2••	3344h	Maintained	
CFh••	Gamma 1 fine tuning (2)••	AJGAM12	1••	44h	Maintained	
D0h••	Gamma 1 inclination adjustment••	AVGAM13	1	33h	Maintained	
D1h••	Gamma 1 blue offset adjustment••	AVGAM14	1••	00h	Maintained	
D2h••	Gamma 2 fine tuning (1)••	AJGAM21	2••	3344h	Maintained	
D3h••	Gamma 2 fine tuning (2)••	AJGAM22	1••	44h	Maintained	
D4h••	Gamma 2 inclination adjustment••	AVGAM23	2••	33h	Maintained	
D5h••	Gamma 2 blue offset adjustment••	AVGAM24	1••	00h	Maintained	
D6h••	Gamma 3 fine tuning (1)••	AJGAM31	2••	3344h	Maintained	
D7h••	Gamma 3 fine tuning (2)••	AJGAM32	1••	44h	Maintained	

380Ch

33h

27h

1235h

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Operation Code	Function	Instruction	Byte	Initial		FR Sync.
				HW-Reset	SW-Reset	
D8h	Gamma 3 inclination adjustment	AVGAM33	2	33h	Maintained	
D9h	Gamma 3 blue offset adjustment••	AJGAM34	1	00h	Maintained	
DEh••	Gamma 4 fine tuning (1)••	AJGAM41	2••	3344h	Maintained	
DFh••	Gamma 4 fine tuning (2)••	AJGAM42	1••	44h	Maintained	
E0h••	Gamma 4 inclination adjustment••	AVGAM43	2••	33h	Maintained	
E1h••	Gamma 4 blue offset adjustment••	AJGAM44	1••	00h	Maintained	
E2h••	Built-in oscillator ON / OFF••	OSCONF	1••	01h	Maintained	
E3h••	Built-in oscillator frequency division setup••	OSCFS	1••	00h	Maintained	*
E4h••	Built-in oscillator clock count setup••	PTL1HC	1••	1Bh	Maintained	*
E5h••	CKV timing control for using built-in oscillator••	PTLHCTIM	2••	011Bh 011Ah	Maintained	*
E6h••	OEV timing control for using built-in oscillator••	PTLHOTIM	2••	011Bh 011Ah	Maintained	*
E7h••	DCEV timing control for using built-in oscillator••	PTLDCW	1••	01h	Maintained	*
E8h••	ASW1-6 timing control for using built-in oscillator••	PTLASW1	2••	0102h 0103h	Maintained	*
E9h••	ASW1-6 interval control for using built-in oscillator••	PTLASW2	1••	01h	Maintained	*
EAh••	Booster clock setup for using built-in oscillator••	PTLDCCF	1••	10h	Maintained	*
EBh••	Refresh interval setup for using built-in oscillator••	PTLWCTL	1••	02h	Maintained	*
ECh••	Vertical blanking count setup for using built-in oscillator••	PTLVB	2••	0404h	Maintained	*
EDh••	Valid display lines setup for using built-in oscillator	VHDOTSET	1••	10h	Maintained	*
EEh	Total number of horizontal clock cycles••	HTTLCNT	2••	01B8h	Maintained	

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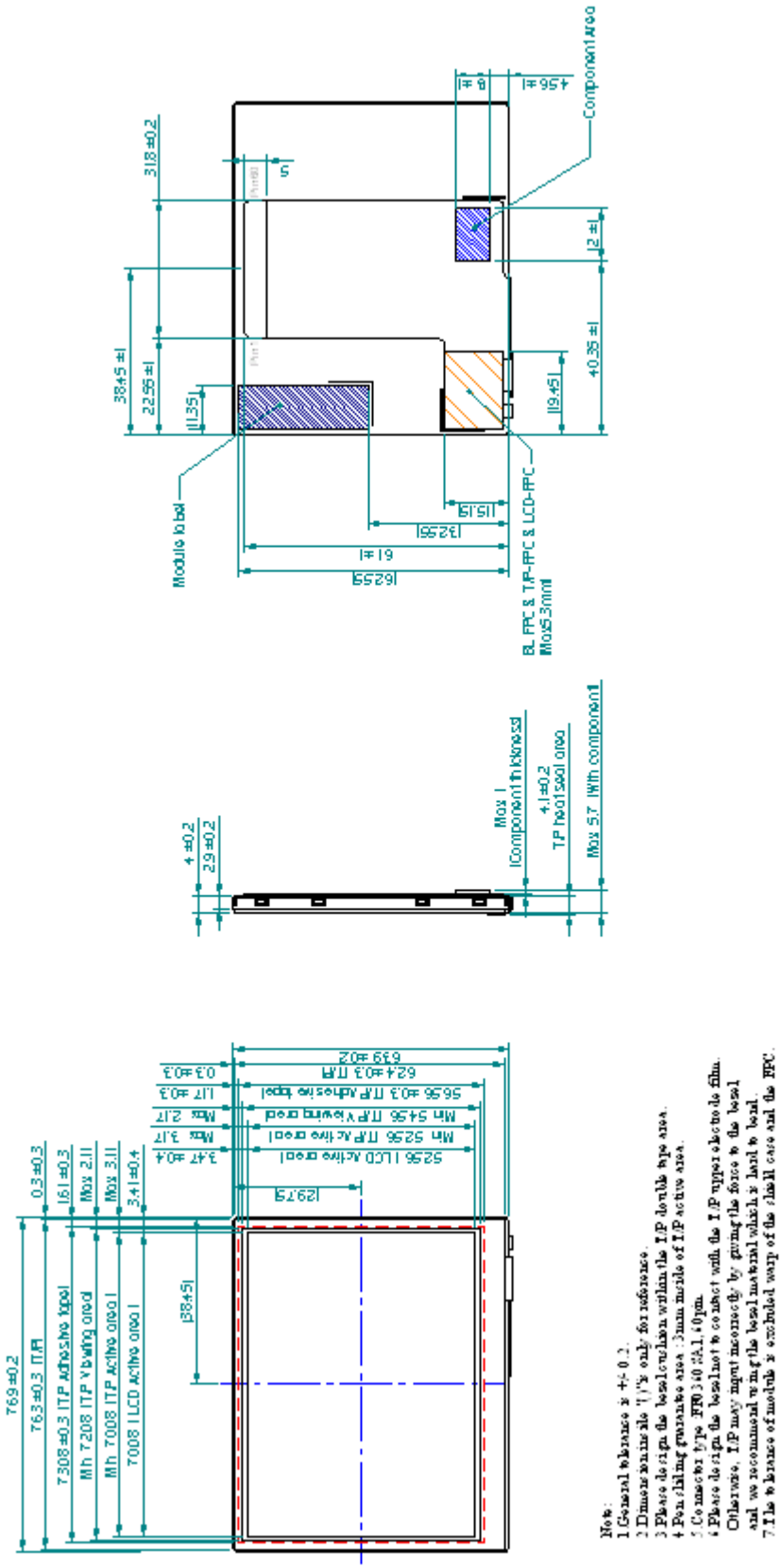
13. Mechanical Drawing



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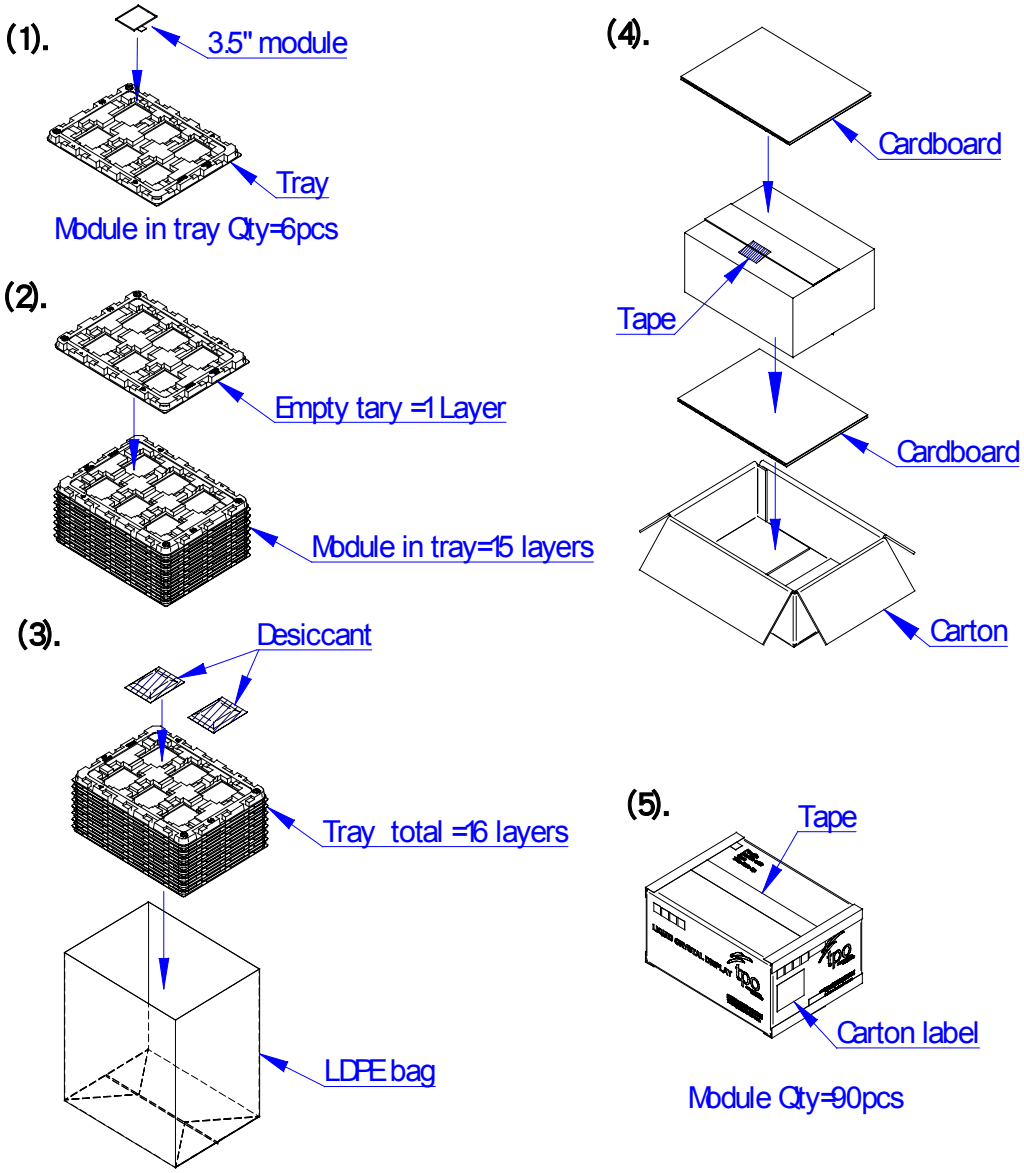
14. Packing Drawing



3.5" module (TD035TTEA3) delivery packing method

(1). Module packed into tray cavity (with Module display face down).

(2). Tray stacking with 15 layers and with 1 empty tray above the stacking tray unit.2pcs desiccant put above the empty tray

(3). Stacking tray unit put into the LDPE bag and fixed by adhesive tape.

(4). Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton. Put 1pc cardboard above the package unit.

(5). Carton tapping with adhesive tape.

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