UNIPAC OPTOELECTRONICS CORPORATION

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TFT-LCD CONTROLLER LSI (UPS015)
PRELIMINARY SPECIFICATION

MODEL NAME: UPS015

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Approved by	Checked by	Prepared by
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Contents:

A.General description:

This timing controller is a synchronizing signal controlling CMOS array LSI for Unipac LCD module. It provides all the necessary control timing signals to the LCD source and gate drivers. With external VCO as the master clock, the controller has built-in phase locked loop system which can synchronize the master clock with the horizontal and vertical Sync. signals from a classical TV system.
The applicable Unipac' s TFT-LCD modules are SM261D series, UP20D01,UP25D01, UP40D01 , UP68D01.

B. Feature:

* Programmable resolution mode.
* Low Power Consumption.
* Single Supply : +5.0 Volts.
* 48 pins TQFP.
* Shift Clocks Signal for the Source Driver. (3 - ϕClock)
* Line Inversion Driving Scheme.
* NTSC TV Standard System .
* Master Clock Frequency : 26 MHz max.
* Provides Timing Scan Signals for Left / Right and Up / Down Shift Control.
* Display Timing Range = 49.6μs

C.Pin description:

Pin no	Symbol	I/O	Description	Remark
1	INV/O	O	Inverter output	
2	INV/I	I	Inverter input	
3	OEH	O	Output enable control signal for source driver	
4	OEV	O	Output enable control signal for source driver	
5	TEST			Note 1
6	TEST			Note 1
7	GND		Ground	
8	Q1HA	O	Sample & hold sequence control signal for source driver	
9	A18	I	Resolution mode selecting pin I	Note 2
10	STV1	O	Gate driver start pulse. when (1).UDC=H, STV1 is output pin of start pulse. (2).UDC=L, STV1 is in high impedance state.	
11	STV2	O	Gate driver start pulse. when (1).UDC=H, STV2 is in high impedance state. (2).UDC=L, STV2 is output pin of start pulse.	
12	VCC			
13	STHL	O	Source driver start pulse. when (1).LRC=H, STHL is in high impedance state. (2).LRC=L, STHL is output pin of start pulse.	
14	STHR	O	Source driver start pulse. when (1).LRC=H, STHR is output pin of start pulse. (2).LRC=L, STHR is in high impedance state.	
15	NPD	O	Negative polarity phase detector output.	
16	CKV	O	Gate driver shift clock.	
17	CK1A	O	Source driver shift clock ϕ1 .	
18	CK2A	O	Source driver shift clock ϕ2 .	
19	CK3A	O	Source driver shift clock ϕ3 .	
20	TEST			Note 1
21	TEST			Note 1
22	RC1	I	Resolution mode selecting pin LI	Note 2
23	GND		Ground	
24	VCC			
25	OSC/O	O	Inverted OSC signal output	
26	OSC/I	I	Master system clock input. This input pin is connected to the external VCO output for system clock timing & synchronization to the TV sync. signals through the phase locked loop block.	

Pin no	Symbol	I/O	Description	Remark
27	VSY / O	O	Negative polarity vertical sync. output	
28	TEST			Note 1
29	GR	I	Global reset. It should be connected to V_{CC} in normal operation. If connected to GND, the controller is in reset state.	
30	VSY/I	I	Vertical synchronization signal input from the sync. separator of a TV system. It should be a negative polarity.	
31	UD	O	Inverted UDC signal output.	
32	GND		Ground	
33	RC2	I	Resolution mode selecting pin III .	
34	HSY/O	O	Negative polarity horizontal sync. output.	
35	Csync	I	Positive polarity composite sync. input.	
36	GND		Ground	
37	UDC	I	Up / Down scan control pin.	
38	TEST			Note 1
39	LRC	I	Left / Right scan control pin.	
40	LRA	O	Inverted LRC signal output.	
41	TEST			Note 1
42	TEST			Note 1
43	NPC	I	It should be pulled to Vcc in normal operation.	
44	PFRP	O	Polarity alternating signal for V_{com}	
45	TEST			
46	CP/O	O	Compare pulse output.	
47	CP/I	I	Compare pulse input.	
48	VCC			

Note 1 : All the test pins should be electrically opened.
Note 2 : Resolution setting :

A18	RC1	RC2	Resolutiion mode (VXH)	Appicable Unipac' s LCD
L	L	H	220 X 528	UP20D01
L	H	H	220 X 280	SM261D series
H	L	H	234 X 960	
H	H	H	234 X 480	UP25D01 , UP40D01
H	L	L	234 X 1152	UP68D01

This chip can drive different Unipac' s LCD according to the above table.

D.DC characteristics

1.Absolute maximum ratings:

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power supply	-0.3 to 6.0	V
V_{IN}	Input voltage	-0.3 to VCC + 0.3	V
V_{OUT}	Output voltage	-0.3 to VCC + 0.3	V
T_{STG}	Storage temperature	-40 to 125	°C

2.Recommended operating conditions:

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power supply	4.5	5.0	5.5	V
V_{IN}	Input voltage	0	-	V_{CC}	V
T_{OPR}	Operating temperature	-20	-	85	°C

3.General DC characteristics:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	Remark
I_{IL}	Input low current	no pull-up or pull-down	-1	-	1	μA	
I_{IH}	Input high current	no pull-up or pull-down	-1	-	1	μA	
I_{OZ}	Tri-state leakage current		-10	-	10	μA	
C_{IN}	Input capacitance		-	3	-	pF	
C_{OUT}	Output capacitance		3	-	6	pF	
V_{IL}	Input low voltage	CMOS	-	-	0.3Vcc	V	
V_{SIL}	Schmitt input low voltage	CMOS	-	1.76	-	V	Note 1
V_{IH}	Input high voltage	CMOS	0.7Vcc	-	-	V	
V_{SIH}	Schmitt input high voltage	CMOS	-	3.2	-	V	Note 1
V_{OL}	Output low voltage	I_{OL}=4mA	-	-	0.4	V	
V_{OH}	Output high voltage	I_{OH}=4mA	3.5	-	-	V	
R_I	Input pull up/down resistance	V_{IL}=0V or V_{IH}=V_{CC}	-	50	-	KΩ	

Note 1: The applicable pins are A18, OSC/I, GR, VSY/I, Csync, CP/I.

4.Current consumption for 5 volts operating:

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Loading
I_{IN}	Current consumption	Vcc=5V	3	5	7	mA	SM261D series
			5	8	11	mA	UP20D01
			4	7	10	mA	UP25D01
			4	7	10	mA	UP40D01
			8	13	18	mA	234 X 960 mode
			9	15	21	mA	UP68D01

E. AC characteristics

1.Timing condition

(i) 220 X 280 resolution mode.

a.Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
OSC/I period	t_{OSC}	150	166	183	ns	
Csync period	t_H	61.5	63.5	65.5	μs	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μs	
Csync rising time	t_{Cr}	-	-	300	ns	
Csync falling time	t_{Cf}	-	-	300	ns	
VSY/I pulse width	t_{VSY}	1	3	5	t_H	
VSY/I rising time	t_{Vr}	-	-	700	ns	
VSY/I falling	t_{Vf}	-	-	700	ns	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY/O pulse width	t_{HSY}	-	9	-	t_{CPH}	
OEH pulse width	t_{OEH}	-	2	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	16	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	10	-	t_{CPH}	
CKV pulse width	t_{CKV}	-	11	-	t_{CPH}	
CP/O period	t_{CP}	-	1	-	t_H	
CP/O pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY/O-OEH timing difference	t_1	-	5	-	t_{CPH}	
HSY/O-CKV timing difference	t_2	-	4	-	t_{CPH}	
HSY/O-OEV timing difference	t_3	-	3	-	t_{CPH}	
HSY/O-CP/O timing difference	t_4	-	6	-	t_{CPH}	

STV setup time	t_{SUV}	-	2	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSY/O-STV1 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY/O-STV2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
OEH-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

(ii) 234 X 480 resolution mode.

a.Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
OSC/I period	t_{OSC}	94	104	114	ns	
Csync period	t_H	61.5	63.5	65.5	μs	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μs	
Csync rising time	t_{Cr}	-	-	300	ns	
Csync falling time	t_{Cf}	-	-	300	ns	
VSY/I pulse width	t_{VSY}	1	3	5	t_H	
VSY/I rising time	t_{Vr}	-	-	700	ns	
VSY/I falling	t_{Vf}	-	-	700	ns	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY/O pulse width	t_{HSY}	-	15	-	t_{CPH}	
OEH pulse width	t_{OEH}	-	3	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	27	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	13	-	t_{CPH}	
CKV pulse width	t_{CKV}	-	20	-	t_{CPH}	

CP/O period	t_{CP}	-	1	-	t_H	
CP/O pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY/O-OEH timing difference	t_1	-	8	-	t_{CPH}	
HSY/O-CKV timing difference	t_2	-	6	-	t_{CPH}	
HSY/O-OEV timing difference	t_3	-	2	-	t_{CPH}	
HSY/O-CP/O timing difference	t_4	-	10	-	t_{CPH}	
STV setup time	t_{SUV}	-	3	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSY/O-STV1 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY/O-STV2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
OEH-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

(iii) 220 X 528 resolution mode.

a.Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
OSC/I period	t_{OSC}	85	94	103	ns	
Csync period	t_H	61.5	63.5	65.5	μs	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μs	
Csync rising time	t_{Cr}	-	-	300	ns	
Csync falling time	t_{Cf}	-	-	300	ns	
VSY/I pulse width	t_{VSY}	1	3	5	t_H	
VSY/I rising time	t_{Vr}	-	-	700	ns	
VSY/I falling	t_{Vf}	-	-	700	ns	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	

STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY/O pulse width	t_{HSY}	-	18	-	t_{CPH}	
OEH pulse width	t_{OEH}	-	5	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	27	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	14	-	t_{CPH}	
CKV pulse width	t_{CKV}	-	24	-	t_{CPH}	
CP/O period	t_{CP}	-	1	-	t_H	
CP/O pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY/O-OEH timing difference	t_1	-	8	-	t_{CPH}	
HSY/O-CKV timing difference	t_2	-	7	-	t_{CPH}	
HSY/O-OEV timing difference	t_3	-	1	-	t_{CPH}	
HSY/O-CP/O timing difference	t_4	-	12	-	t_{CPH}	
STV setup time	t_{SUV}	-	4	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSY/O-STV1 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY/O-STV2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
OEH-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

(iv) 234 X 960 resolution mode.

a.Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
OSC/I period	t_{OSC}	47	52	57	ns	
Csync period	t_H	61.5	63.5	65.5	μs	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μs	
Csync rising time	t_{Cr}	-	-	300	ns	
Csync falling time	t_{Cf}	-	-	300	ns	
VSY/I pulse width	t_{VSY}	1	3	5	t_H	
VSY/I rising time	t_{Vr}	-	-	700	ns	
VSY/I falling	t_{Vf}	-	-	700	ns	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{OSC}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY/O pulse width	t_{HSY}	-	30	-	t_{CPH}	
OEH pulse width	t_{OEH}	-	7	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	54	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	26	-	t_{CPH}	
CKV pulse width	t_{CKV}	-	40	-	t_{CPH}	
CP/O period	t_{CP}	-	1	-	t_H	
CP/O pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY/O-OEH timing difference	t_1	-	14	-	t_{CPH}	
HSY/O-CKV timing difference	t_2	-	12	-	t_{CPH}	
HSY/O-OEV timing difference	t_3	-	4	-	t_{CPH}	
HSY/O-CP/O timing difference	t_4	-	20	-	t_{CPH}	
STV setup time	t_{SUV}	-	6	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSY/O-STV1 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY/O-STV2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
OEH-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

(v) 234 X 1152 resolution mode.

a.Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
OSC/I period	t_{OSC}	39	43	47	ns	
Csync period	t_H	61.5	63.5	65.5	μs	
Csync pulse width	t_{CSYN}	4	4.7	5.4	μs	
Csync rising time	t_{Cr}	-	-	300	ns	
Csync falling time	t_{Cf}	-	-	300	ns	
VSY/I pulse width	t_{VSY}	1	3	5	t_H	
VSY/I rising time	t_{Vr}	-	-	700	ns	
VSY/I falling	t_{Vf}	-	-	700	ns	
Horizontal lines per field		256	262.5	268	line	Note 1

Note 1: Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b.Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{osc}	CK1A~CK3A
Clock pulse duty	t_{CWH}	40	50	60	%	CK1A~CK3A
3ϕ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /2	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HSY/O pulse width	t_{HSY}	-	36	-	t_{CPH}	
OEH pulse width	t_{OEH}	-	9	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	62	-	t_{CPH}	
OEV pulse width	t_{OEV}	-	40	-	t_{CPH}	
CKV pulse width	t_{CKV}	-	50	-	t_{CPH}	
CP/O period	t_{CP}	-	1	-	t_H	
CP/O pulse duty	t_{WCP}	-	1/2	-	t_H	
HSY/O-OEH timing difference	t_1	-	18	-	t_{CPH}	
HSY/O-CKV timing difference	t_2	-	14	-	t_{CPH}	
HSY/O-OEV timing difference	t_3	-	12	-	t_{CPH}	
HSY/O-CP/O timing difference	t_4	-	26	-	t_{CPH}	
STV setup time	t_{SUV}	-	8	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	

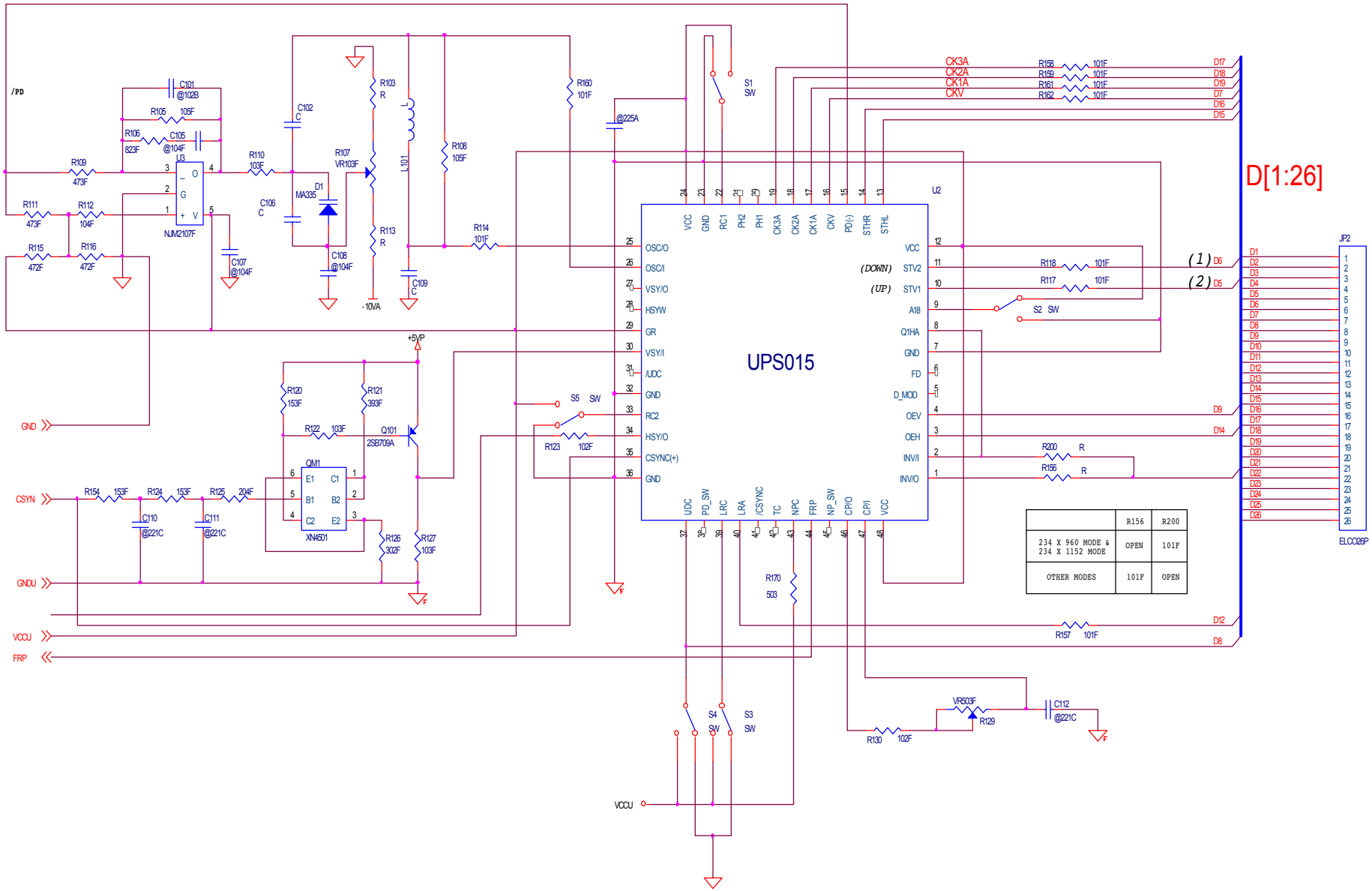
VSY/O-STV1 timing difference(UDC="H")	t_{VS1}	-	19	-	t_H	
VSY/O-STV2 timing difference(UDC="L")	t_{VS2}	-	19	-	t_H	
OEH-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

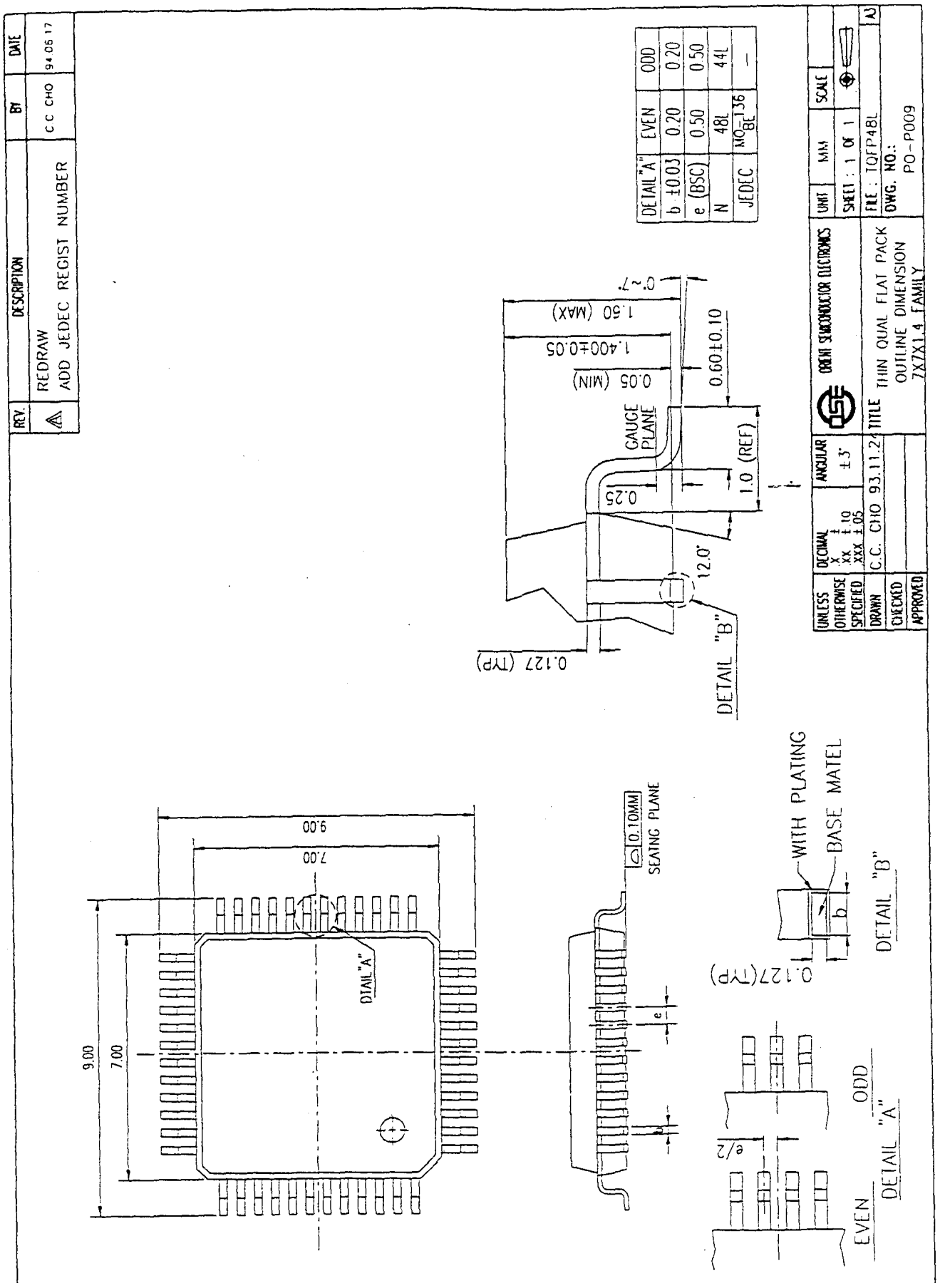
2.Timing diagram

Please refer to the attached drawing. from Fig.1 to Fig.4-(b).

F. Test circuit



G. Package information



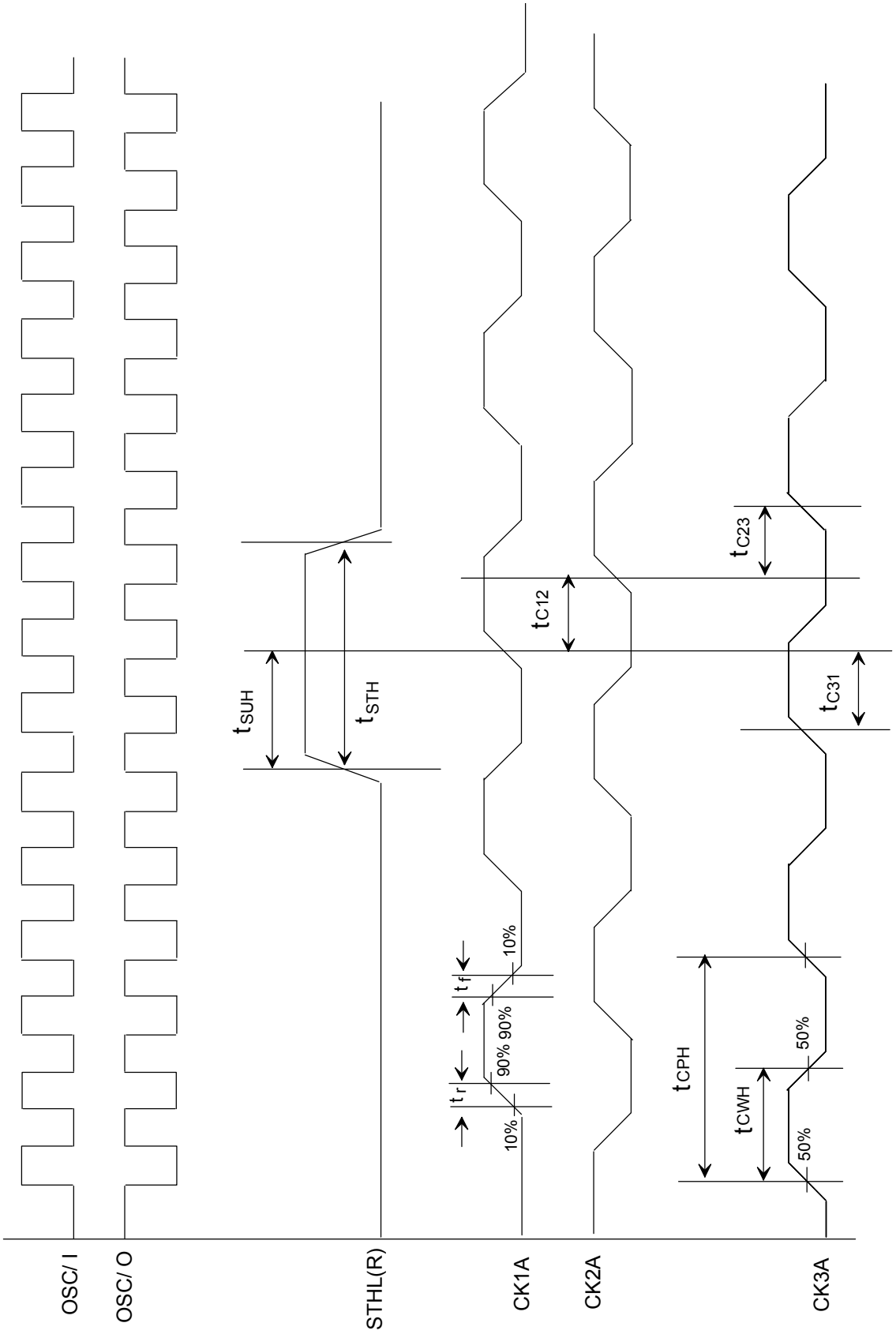
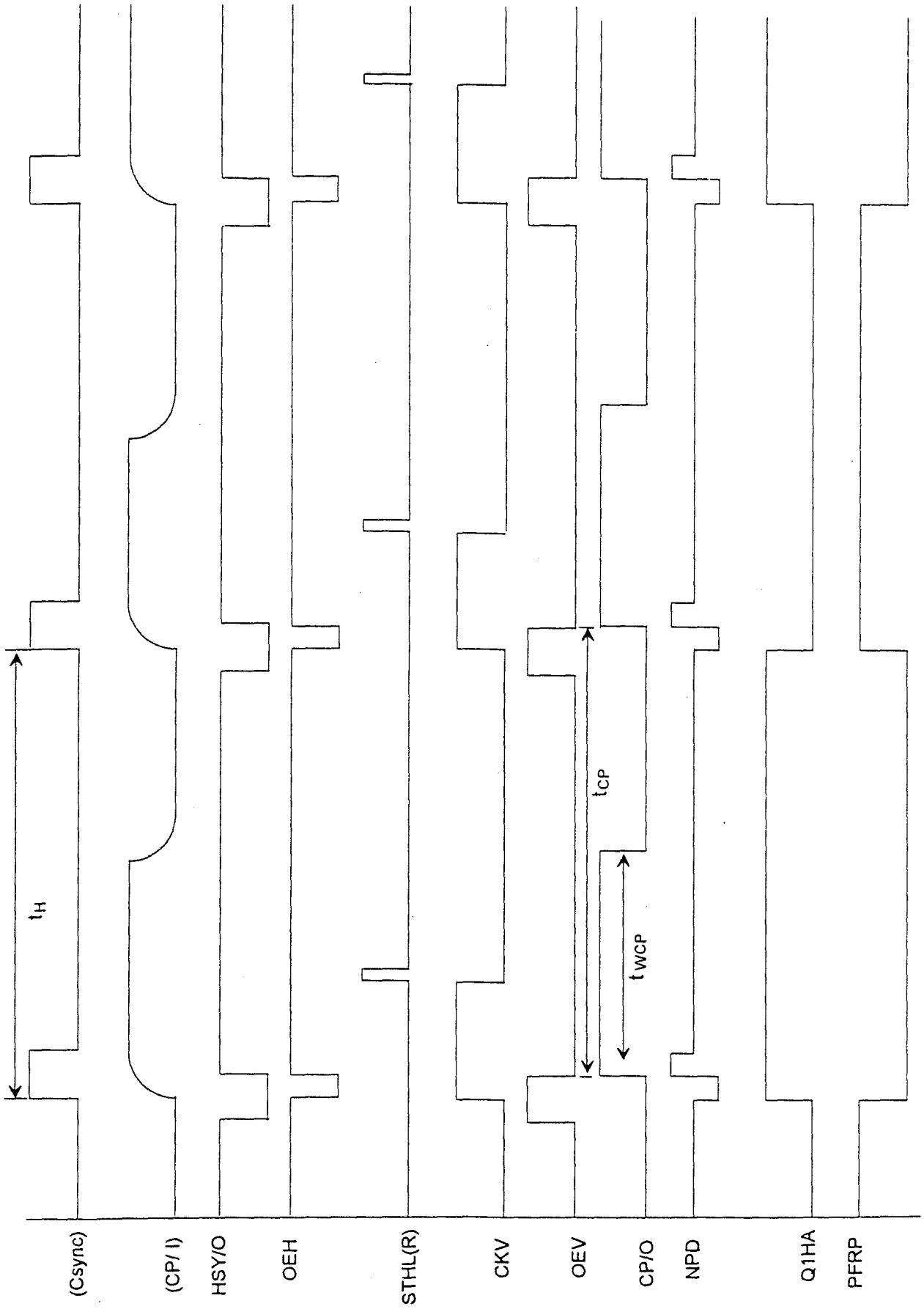
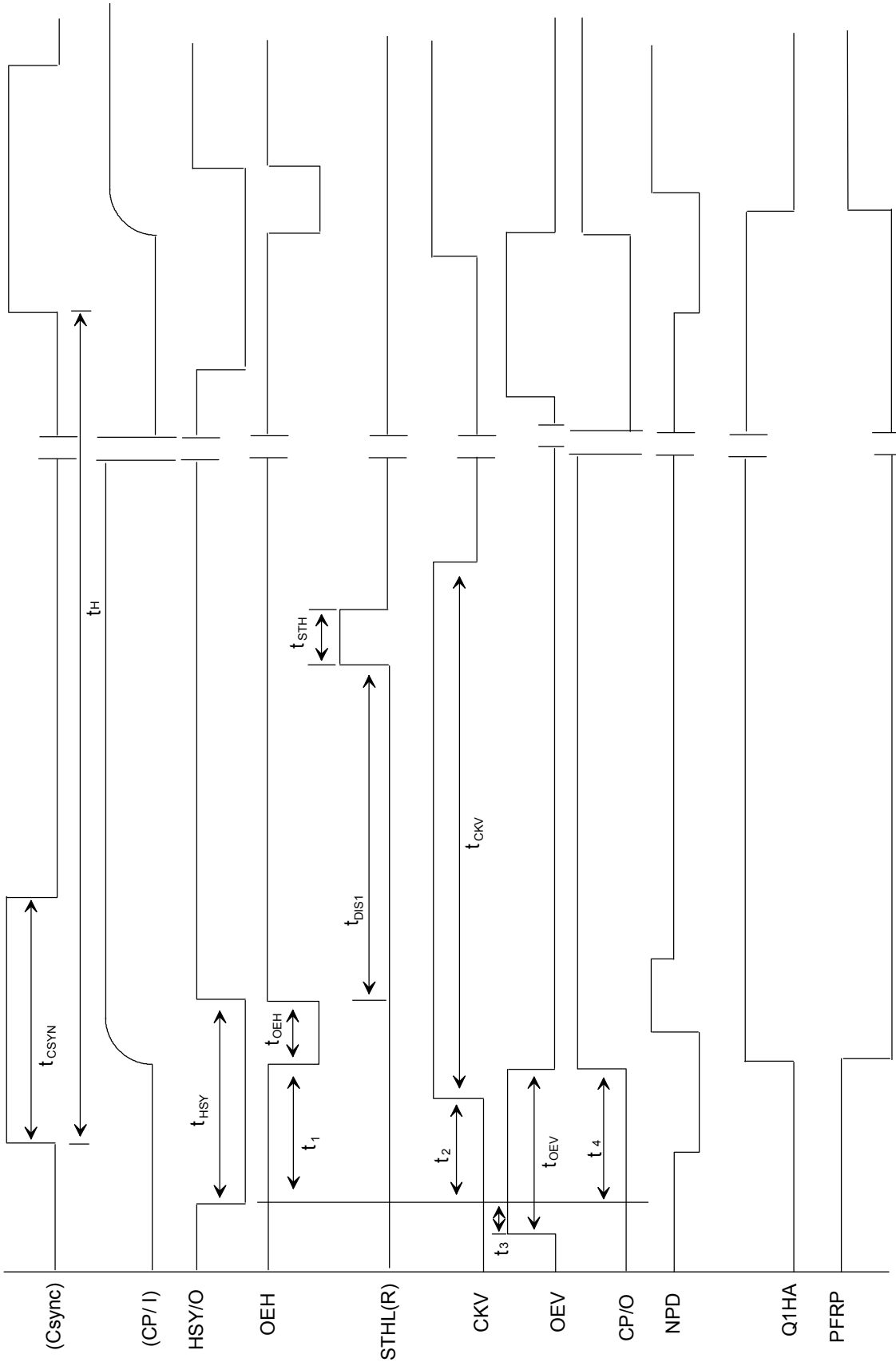


Fig.1 Sampling clock timing



※ In 234 X 960 & 234 X 1152 resolution mode , Q1HA always keeps low.

Fig.2-(a) Horizontal timing



¡ In 234 x 960 & 234 x 1152 resolution mode , Q1HA always keeps low.

Fig.2-(b) Detail horizontal timing

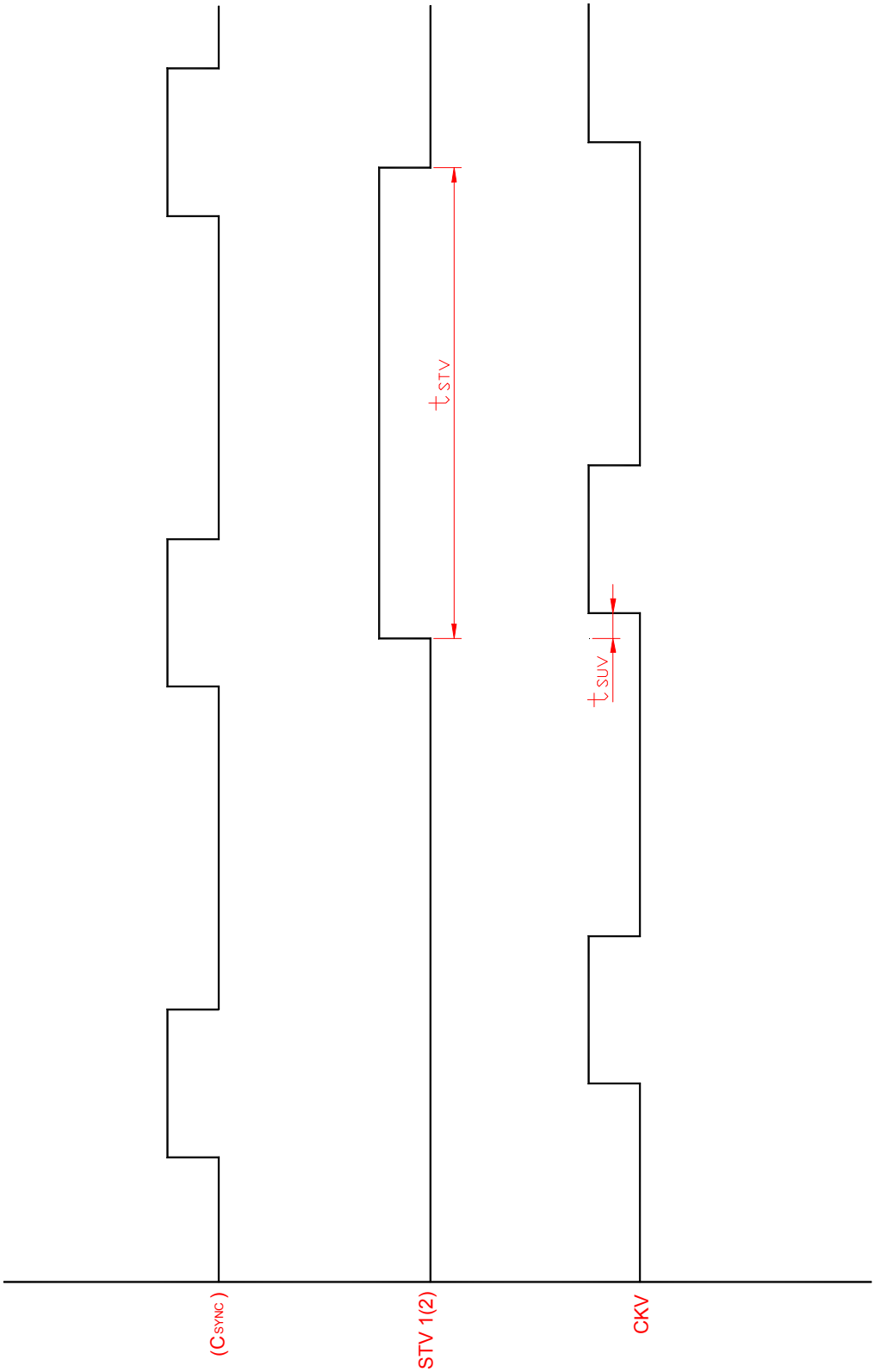


Fig.3 Vertical shift clock timing

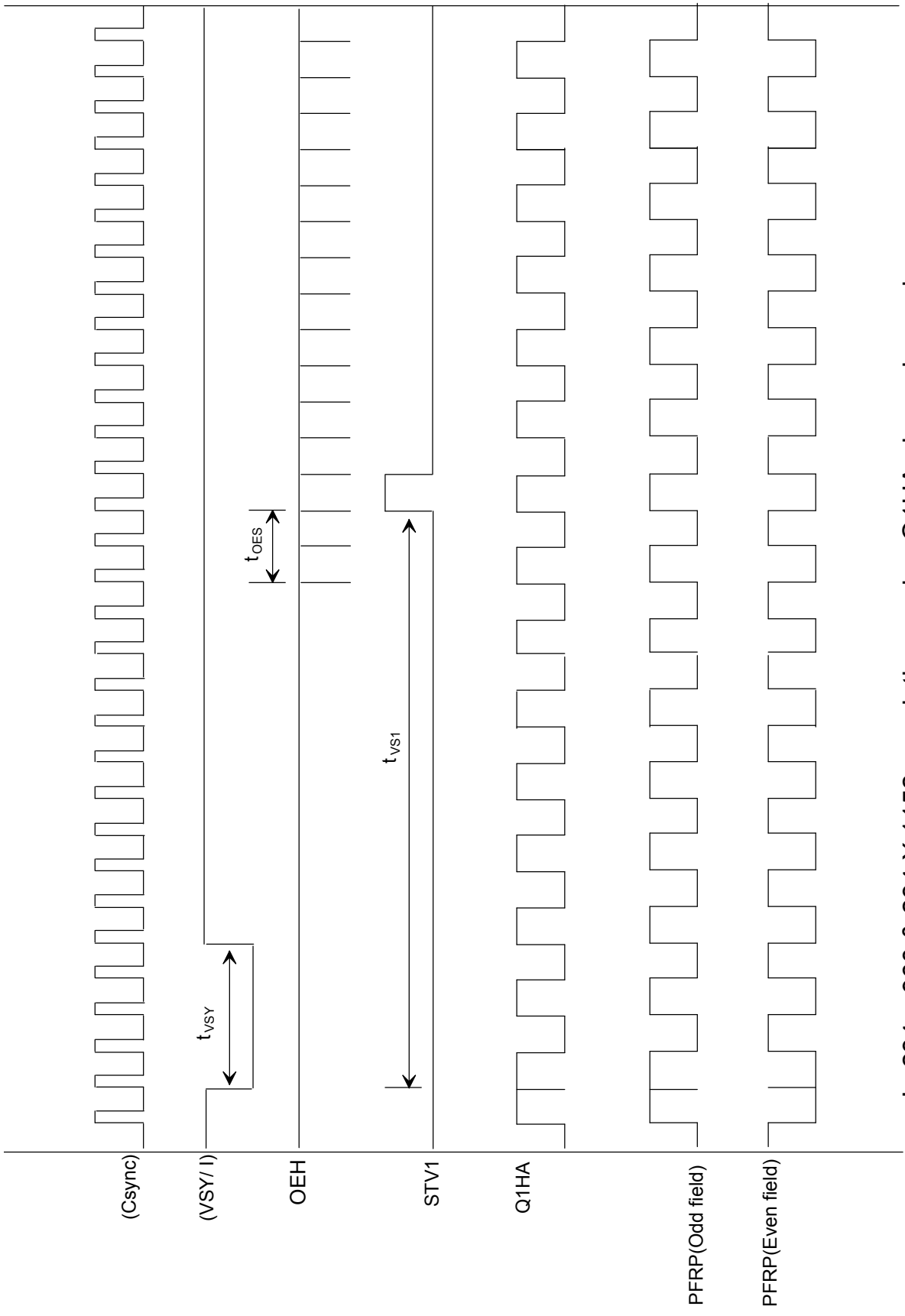
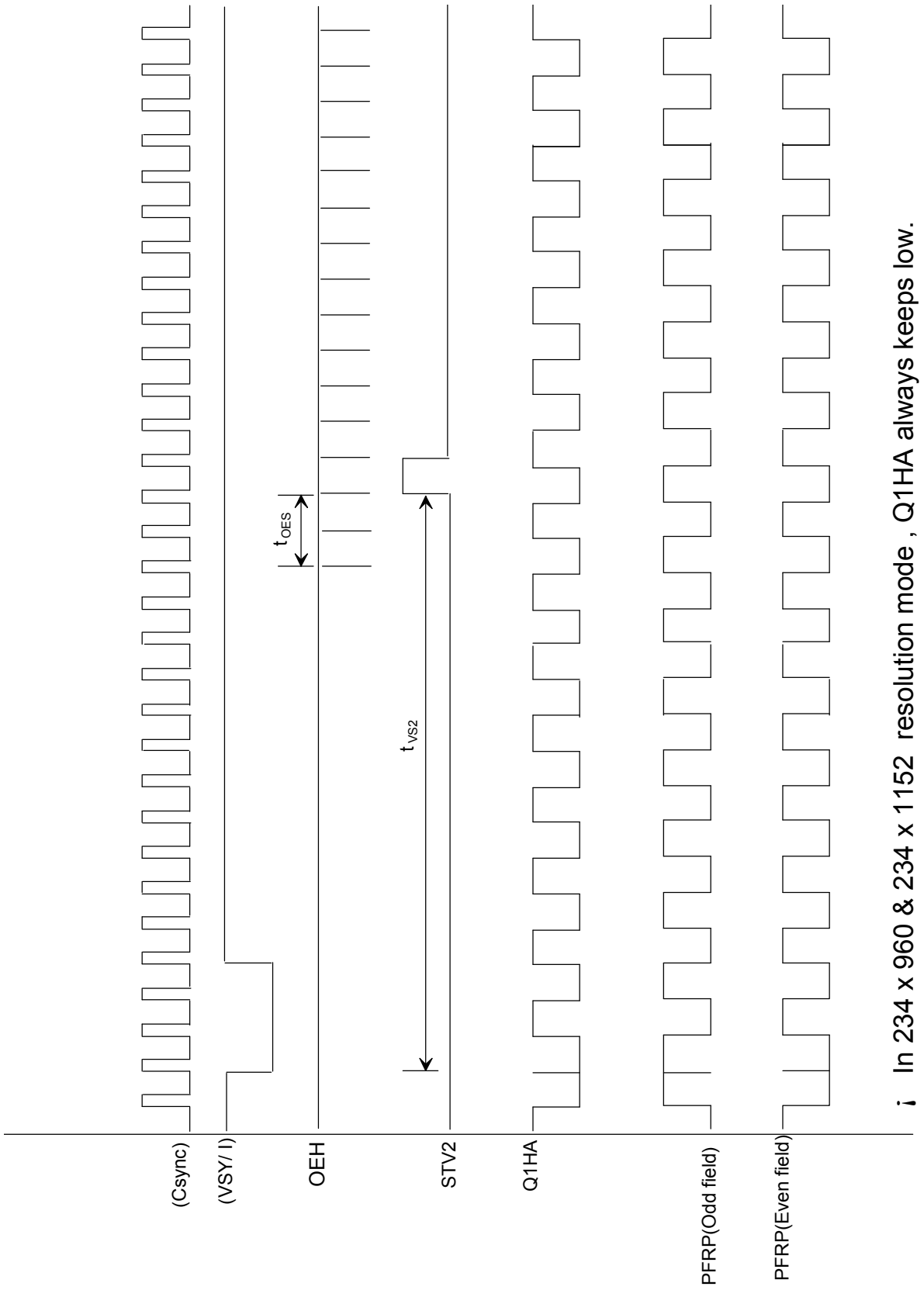


Fig.4-(a) Vertical timing (UDC="H")

i In 234 x 960 & 234 X 1152 resolution mode , Q1HA always keeps low.



i In 234 x 960 & 234 x 1152 resolution mode , Q1HA always keeps low.

Fig.4-(b) Vertical timing (UDC="L")

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TERMS AND CONDITIONS OF SALE
(Revision: January 1996)

These Terms and Conditions of Sale apply to all items designed and/or made by Unipac Optoelectronics Corporation ("Unipac"), and Buyer agrees they apply to all such items.

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THIS FORM WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

a. Delivery will be made Free Carrier (Incoterms), Unipac's warehouse, Science-Based Industrial Park, Taiwan.

b. Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.

c. Shipments are subject to availability. Unipac shall make every reasonable effort to meet the date (s) quoted or acknowledged; and if Unipac makes such effort, Unipac will not be liable for any delays.

3. TERMS OF PAYMENT

a. Terms are as stated on Unipac's quotation, or if none are stated, net forty-five (45) days. Accounts past due will incur a monthly charge at the rate of one and one-half percent (1.5%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.

b. Unipac reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

a. Unipac warrants that the goods sold will be free from defects in material and workmanship and comply with Unipac's applicable published specifications for a period of sixty (60) days from the date of Unipac's shipment.

b. Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications(unless specifically stated in a writing signed by Unipac).

c. No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Unipac from all claims, damages and liabilities arising out of any such uses.

d. This Paragraph 4 is the only warranty by Unipac with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Unipac.

e. Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Unipac is not responsible for such things.

f. EXCEPT AS PROVIDED ABOVE, UNIPAC MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND UNIPAC EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

a. Unipac will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date (s)for Unipac's performance will be deemed extended for a period equal to any delay resulting.

b. THE LIABILITY OF UNIPAC ARISING OUT OF THIS CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR (WITH UNIPAC'S PRIOR WRITTEN CONSENT) REPAIR OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO UNIPAC FREIGHT PRE-PAID).

c. Buyer will not return any goods without first obtaining a customer return order number.

d. AS A SEPARATE LIMITATION, IN NO EVENT WILL UNIPAC BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITAIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

e. No action against Unipac, whether for breach, indemnification,contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Unipac has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.

f. BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Unipac may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Unipac reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

a. This contract may not be canceled by Buyer except with written consent by Unipac and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Unipac, and a reasonable profit).

b. In no event will Buyer have rights in partially completed goods.

8. INDEMNIFICATION

Unipac will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Unipac under this purchase order infringe any valid, enforceable, unexpired R.O.C. patent, copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Unipac, (ii) permits Unipac to participate and to defend if Unipac requests to do so, and (iii) gives Unipac all needed information, assistance and authority. However, Unipac will not be responsible for infringements resulting from anything not entirely manufactured by Unipac, or from any combination with products, equipment, or materials not furnished by Unipac. Unipac will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Unipac makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement.

Except as to claims Unipac agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS UNIPAC FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Unipac shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

a. These terms and conditions are the entire agreement between Unipac and Buyer, and no addition, deletion or modification shall be binding on Unipac unless expressly agreed to in a writing signed by an officer of Unipac.

b. Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

This contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of Taiwan, Republic of China, without reference to conflict of laws principles and excluding the U.N. Convention on Contracts for the International Sale of Goods. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder.

12. JURISDICTION AND VENUE

The courts located in Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to this contract or any sale of goods hereunder, and Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving the enforcement or interpretation of this contract.