UNIPAC OPTOELECTRONICS CORPORATION

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TFT-LCD CONTROLLER LSI (UPS051)

PRELIMINARY SPECIFICATION

MODEL NAME: UPS051

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Appendix

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A. General description:

This timing controller is a synchronizing signal controlling CMOS LSI for Unipac COG type LCD module. It accepts the digital signal and provides all the necessary control timing signals to the LCD source and gate drivers. This controller converts the digital input data to the analog alternated and amplified signals for the driving of the TFT-LCD panel. This controller also supports different resolution modes.

B. Feature:

* Single power supply : +5.0 Volts.
* Low power consumption.
* 64 pins LQFP.
* Built-In PWM circuit.
* Built-In polarity inverted circuit.
* Provides timing scan signals for Left / Right and Up / Down shift control.
* Built-In GAMMA correction function.
* Multi-resolution modes.
* Optional 3.3V input level.
* NTSC/PAL system timing

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C. Pin description:

Pin-no	Symbol	I/O	Description	Remark
1	DCLK	I	Data clock input.	
2	STHR	O	Source driver start pulse. When (1).H_DIR=L, STHR is output pin of start pulse. (2).H_DIR=H, STHR is high impedance state.	
3	STHL	O	Source driver start pulse. When (1).H_DIR=L, STHL is high impedance state. (2).H_DIR=H, STHL is output pin of start pulse.	
4	STVR	O	Gate driver start pulse. When (1).V_DIR=L, STVR is output pin of start pulse. (2).V_DIR=H, STVR is high impedance state.	
5	STVL	O	Gate driver start pulse. When (1).V_DIR=L, STVL is high impedance state. (2).V_DIR=H, STVL is output pin of start pulse.	
6	VOE_OUT	O	Gate driver output enable control signal.	
7	V_CK	O	Gate driver shift clock.	
8	HOE_OUT	O	Source driver output enable control signal.	
9	VCC1	-	Power pin for digital circuits.	
10	VCI	I	Test pin, pull to ground.	
11	GND1	-	Ground pin for digital circuit.	
12	GME	I	Gamma correction enable control signal. (Normally pulled-up)	Note 1
13	HSD	I	Horizontal synchronization signal, negative polarity.	
14	VSD	I	Vertical synchronization signal, negative polarity.	
15	Q1H_OUT	O	Source driver sample & hold sequence control signal.	
16	PFRP_OUT	O	Polarity alternating signal for Vcom.	
17	GND2	-	Ground pin for PWM circuits.	
18	VCC2	-	Power pin for PWM circuits.	
19	PWM_OUT3	O	PWM output.	
20	FBK3	I	Reference voltage feedback.	
21	GND3	-	Ground pin for PWM circuits.	
22	VCC3	-	Power pin for PWM circuits.	
23	PWM_OUT2	O	PWM output.	
24	PWM_OUT1	O	PWM output.	
25	FBK1	I	Reference voltage feedback.	
26	FBK2	I	Reference voltage feedback.	
27	RSC	I	Resolution mode selection pin. (Normally pulled-up)	Note 2
28	UD_OUT	O	Inverted V_DIR signal output.	
29	LR_OUT	O	Inverted H_DIR signal output.	
30	V_DIR	I	Up/Down scan control pin. (Normally pulled-up)	
31	H_DIR	I	Left/Right scan control pin. (Normally pulled-up)	

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Pin-no	Symbol	I/IO	Description	Remark
32	IN1	I	Test pin, pull to ground.	
33	VCC4	-	Power pin for digital circuits of DAC.	
34	VIN	I	Test pin, pull to ground.	
35	NPC	I	NTSC/PAL system setting pin (Normally pulled-up , NTSC)	Note 3
36	GND4	-	Ground pin for digital circuit of ADC and DAC.	
37	IOUT	O	DAC setting pin.	
38	VTEST	I	Vertical timing test mode selection. (Normally pulled-up)	
39	GR_IN	I	Global reset. It should be connected to Vcc in normal operation. If connected to GND, the controller is in reset state. (Normally pulled-up)	
40	VOUT3	O	Alternated, amplified video output.	
41	RSB	I	Resolution mode selection pin. (Normally pulled-up)	Note 2
42	VOUT2	O	Alternated, amplified video output.	
43	RSA	I	Resolution mode selection pin. (Normally pulled-up)	Note 2
44	VOUT1	O	Alternated, amplified video output.	
45	VCC5	-	Power pin for analog circuits of DAC.	
46	GND5	-	Ground pin for analog circuits of DAC.	
47	VG	I	Setting pin of DAC.	
48	VREF	I	Reference voltage setting pin of DAC.	
49	IREF	I	Reference current setting pin of DAC.	
50	DDX0	I	Digital data input, LSB.	
51	DDX1	I	Digital data input.	
52	DDX2	I	Digital data input.	
53	DDX3	I	Digital data input.	
54	GND1	-	Ground pin for digital circuits.	
55	VCC3IO	-	Power pin for 3.3V input optional.	Note 4
56	VCC1	-	Power pin for digital circuits.	
57	DDX4	I	Digital data input	
58	DDX5	I	Digital data input	
59	DDX6	I	Digital data input	
60	DDX7	I	Digital data input, MSB.	
61	CPH3_OUT	O	Source driver shift clock .	
62	CPH2_OUT	O	Source driver shift clock .	
63	CPH1_OUT	O	Source driver shift clock .	
64	DEM	I	Data enable control signal. (Normally pulled-up)	

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Note 1: GME=H , Gamma correction (Normally pulled-up)
GME=L , No gamma correction
Note 2: Use RSA , RSB and RSC to select different resolution modes :

Resolution mode	RSA	RSB	RSC
220× 280	L	L	L
220 × 528	H	H	L
234× 480 (2.5")	H	H	H
234× 480 (4.0")	L	L	H
234× 960	H	L	H
234× 1152	L	H	L
234× 1440	L	H	H

Note 3: NPC=H , NTSC System (Normally pulled-up)
NPC=L , PAL System

Note 4: When connected to 3.3V , the input level of I/Ps (DEM , DCLK , HSD , VSD , V_DIR , H_DIR , DDX0 ~ DDX7) is 3.3V , and when connected to 5.0V , the input level of I/Ps are 5.0V .

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D. DC characteristics

a. Absolute maximum ratings:

Symbol	Parameter	Rating	Units	Remark
V_{CC}	Power supply	-0.3 to 6.0	V	Note 1
V_{IN}	Input voltage	-0.3 to VCC + 0.3	V	
V_{OUT}	Output voltage	-0.3 to VCC + 0.3	V	
T_{STG}	Storage temperature	-40 to 95	℃	

Note 1: For all V_{CC} inputs, including V_{CC1}, V_{CC2}, V_{CC3}, V_{CC4}, V_{CC5} and V_{CC3IO} .

b. Recommended operating conditions:

Symbol	Parameter	Min	Typ	Max	Units	Remark
V_{CC}	Power supply	4.75	5.0	5.25	V	Note 1
V_{IN}	Input voltage	0	-	V_{CC}	V	
T_{OPR}	Operating temperature	0	25	85	℃	

Note 1: For all V_{CC} inputs, including V_{CC1}, V_{CC2}, V_{CC3}, V_{CC4} , V_{CC5} and V_{CC3IO} .

c. General DC characteristics:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IL}	Input leakage current	no pull-up or pull-down	-1	-	1	μA
I_{OZ}	Tri-state leakage current		-10	-	10	μA
C_{IN}	Input capacitance		-	3	-	pF
C_{OUT}	Output capacitance		3	-	6	pF
C_{BID}	Bi-directional buffer capacitance		3	-	6	pF

d. DC electrical characteristics for 3.3V operation:
(Under recommended operating conditions and V_{CC}=3.0V～3.6V, Tj= 0℃ to +115℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Remark
V_{IL}	Input Low voltage	CMOS	-	-	0.3× V_{CC}	V	Note 1
V_{IH}	Input High voltage	CMOS	0.7× V_{CC}	-	-	V	Note 1
V_{t-}	Schmitt trigger negative going threshold voltage	CMOS	-	1.22	-	V	
V_{t+}	Schmitt trigger positive going threshold voltage	CMOS	-	2.08	-	V	
V_{OL}	Output low voltage	I_{OL}=2,4,8,12, 16,24mA	-	-	0.4	V	
V_{OH}	Output high voltage	I_{OH}=2,4,8,12, 16,24mA	2.4	-	-	V	
R_I	Input pull up/down resistance	Vil=0V or Vih=V_{CC}	-	75	-	KΩ	

Note 1: The applicable pins are DEM, DCLK, HSD, VSD, V_DIR, H_DIR DDX0 ～ DDX7.

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e. DC electrical characteristics for 5V operation:

(Under recommended operating conditions and V_{CC}=4.75V～5.25V, Tj= 0℃ to +115℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low voltage	CMOS	-	-	0.3× V_{CC}	V
V_{IH}	Input High voltage	CMOS	0.7× V_{CC}	-	-	V
V_{t-}	Schmitt trigger negative going threshold voltage	CMOS	-	1.84	-	V
V_{t+}	Schmitt trigger positive going threshold voltage	CMOS	-	3.22	-	V
V_{OL}	Output low voltage	I_{OL}=2,4,8,12,16,24mA	-	-	0.4	V
V_{OH}	Output high voltage	I_{OH}=2,4,8,12,16,24mA	3.5	-	-	V
R_I	Input pull up/down resistance	Vil=0V or Vih=V_{CC}	-	50	-	KΩ

f. Current consumption for different resolution modes:

1. 280 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	5.5	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	2.5	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	1	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	39	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

2. 480 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	8.5	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	2.6	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	1.5	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	40	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

3. 528 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	9	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	2.7	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	1.3	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	41	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

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4. 1152 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	19.6	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	3.6	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	3.6	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	41	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

5. 960 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	17.0	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	3.2	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	3.2	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	41	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

6. 1440 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	24	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	4.0	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	4.0	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	41	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

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E. AC characteristics

a. Input signal characteristics

Timing diagrams of input signal are shown in Fig 1 and Fig 2.

1. 280 mode

1-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	5.67	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	360	-	CLK	
	Display period	THd	-	49.4	-	μs	
			280			CLK	
	Pulse width	THp	5	25	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	
VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	13.97	-	ms	
			220			TH	
	Pulse width	TVp	3	-	-	TH	
DATA R0~R7 G0~G7 B0~B7	CLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

1-2. Horizontal display position

1-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	288	-	CLK	
Hsync-Enable signal timing		THe	33	-	57	CLK	

1-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C62(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

1-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		25		H	NTSC
			34		H	PAL

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2. 480 mode

2-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	9.70	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	617	-	CLK	
	Display period	THd	-	49.4	-	μs	
			480			CLK	
	Pulse width	THp	5	44	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	
VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	14.83	-	ms	
			234			TH	
	Pulse width	TVp	3	-	-	TH	
DATA	CLK-DATA timing	Tds	10	-	-	ns	
R0~R7	DATA-CLK timing	Tdh	10	-	-	ns	
G0~G7 B0~B7	Rising time Falling time	Tdrf	-	-	10	ns	

2-2. Horizontal display position

2-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	480	-	CLK	
Hsync-Enable signal timing		THe	60	-	105	CLK	

2-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C106(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

2-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		18		H	NTSC
			27		H	PAL

3. 528 mode

3-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	10.7	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	679	-	CLK	
	Display period	THd	-	49.4	-	μs	
			528			CLK	
	Pulse width	THp	5	48	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	

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VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	13.97	-	ms	
			220			TH	
	Pulse width	TVp	3	-	-	TH	
DATA	CLK-DATA timing	Tds	10	-	-	ns	
R0~R7 G0~G7 B0~B7	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

3-2. Horizontal display position

3-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	576	-	CLK	
Hsync-Enable signal timing		THe	57	-	90	CLK	

3-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C118(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

3-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		25		H	NTSC
			34		H	PAL

4. 1152 mode

4-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	23.3	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	1482	-	CLK	
	Display period	THd	-	49.4	-	μs	
			1152			CLK	
	Pulse width	THp	5	109	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	
VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	14.83	-	ms	
			234			TH	
	Pulse width	TVp	3	-	-	TH	
DATA	CLK-DATA timing	Tds	10	-	-	ns	
R0~R7 G0~G7 B0~B7	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

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4-2. Horizontal display position

4-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	1152	-	CLK	
Hsync-Enable signal timing		THe	108	-	243	CLK	

4-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C247(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

4-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		18		H	NTSC
			27		H	PAL

5. 960 mode

5-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	19.4	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	1235	-	CLK	
	Display period	THd	-	49.4	-	μs	
			960			CLK	
	Pulse width	THp	5	91	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	
VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	14.83	-	ms	
			234			TH	
	Pulse width	TVp	3	-	-	TH	
DATA R0~R7 G0~G7 B0~B7	CLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

5-2. Horizontal display position

5-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	960	-	CLK	
Hsync-Enable signal timing		THe	97	-	204	CLK	

5-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C207(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

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5-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		18		H	NTSC
			27		H	PAL

6. 1440 mode

6-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	29.1	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	1853	-	CLK	
	Display period	THd	-	49.4	-	μs	
			1440			CLK	
	Pulse width	THp	5	137	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	
VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	14.83	-	ms	
			234			TH	
	Pulse width	TVp	3	-	-	TH	
DATA R0~R7 G0~G7 B0~B7	CLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

6-2. Horizontal display position

6-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	1440	-	CLK	
Hsync-Enable signal timing		THe	145	-	305	CLK	

6-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C309(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

6-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		18		H	NTSC
			27		H	PAL

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b. Output signal characteristics

1. 280 mode

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	3	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	11	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	5	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	5	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	8	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	6	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	2	-	t_{CPH}	
STV setup time	t_{SUV}	-	3	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

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2. 480 mode (2.5")

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_ OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_ OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	6	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	17	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	10	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	7	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	12	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	11	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	2	-	t_{CPH}	
STV setup time	t_{SUV}	-	8	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

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3. 480 mode (4.0")

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_ OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_ OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	4	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	14	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	14	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	25	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	17	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	10	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	2	-	t_{CPH}	
STV setup time	t_{SUV}	-	7	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

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4. 528 mode

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	6	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	11	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	11	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	13	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	14	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	9	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	2	-	t_{CPH}	
STV setup time	t_{SUV}	-	6	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

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5. 1152 mode

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	12	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	24	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	39	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	60	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	46	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	22	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	4	-	t_{CPH}	
STV setup time	t_{SUV}	-	15	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

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6. 960 mode

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	8	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	29	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	28	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	50	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	33	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	19	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	3	-	t_{CPH}	
STV setup time	t_{SUV}	-	15	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

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7. 1440 mode

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	12	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	42	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	42	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	75	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	49	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	28	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	4	-	t_{CPH}	
STV setup time	t_{SUV}	-	15	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

c. Video signal output characteristics(refer to the attached drawing Fig.7)

Item	Symbol	Min.	Typ.	Max.	Unit.	Remark
Video signal amplitude (Vout1, Vout2, Vout3)	V_{IAC}	-	3.5	-	V	AC Component
	V_{IDC}	-	3.15	-	V	DC Component

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F. Color sequence for different resolution modes:

a. Delta type arrangement color filter :

Due to the “Delta” type arrangement of LCD’s color filter, the R.G.B data are different in odd lines and even lines. Please follow the corresponding sequence under different conditions which are shown in Tab.1

Tab.1 Color sequence for different resolution modes. (Delta type)

Scanning direction control setting	V_DIR (Note 1)	Low	Low	High	High
Display modules	H_DIR (Note 2)	High	Low	High	Low
4”: 480× 234 (UP40DXX)	Odd Line	B R G	G R B	G B R	R B G
	Even Line	G B R	R B G	B R G	G R B
1.8”: 280× 220 (SM26X Series) 2.0”: 528× 220 (UP20DXX) 2.5”: 480× 234 (UP25DXX)	Odd Line	R G B	B G R	G B R	R B G
	Even Line	G B R	R B G	R G B	B G R

Note 1: V_DIR is an Up/Down scanning direction control pin of UPS051.
When V_DIR is high , the scanning direction control is from “ Down to Up “.
When V_DIR is low , the scanning direction control is from “ Up to Down “.

Note 2: H_DIR is a Left/Right scanning direction control pin of UPS051.
When LR is high, the scanning direction is from “left to Right”.
When LR is low, the scanning direction is from “right to Left”.

Note 3: The sequence specified in each column represents the order of data which should be sent to UPS051 for cycle #1, 2, 3, 4, 5, ・・・・

Note 4: The Q1H_OUT (Pin 15) signal can be used as the index to specify odd line or even line for users.

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b. Stripe type arrangement color filter

The R.G.B sequences are same in odd line and even line in stripe type arrangement color filter.

Tab.2 Color sequence for different resolution modes. (Stripe type)

Display module	H_DIR	High	Low
6.8" : 1152× 234 (UP68DXX) 5.6" : 960× 234 (UP056DXX) 7.0" : 1440× 234 (UP070DXX)	Odd line Even line	R G B	B G R

G. Reliability test item:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta = 80℃ 240H	
2	Low temperature storage	Ta = -25℃ 240H	
3	High temperature operation	Ta = 60℃ 240H	
4	Low temperature operation	Ta = 0℃ 240H	
5	High temperature and high humidity	Ta = 60℃ • 95%RH 240H	Operation
6	Heat shock	-25℃～+80℃/50 cycles 2H/cycle	Non-operation
7	Electrostatic discharge	± 200V,200pF(0Ω),once for each terminal	Non-operation

Note : Ta is the Ambient temperature.

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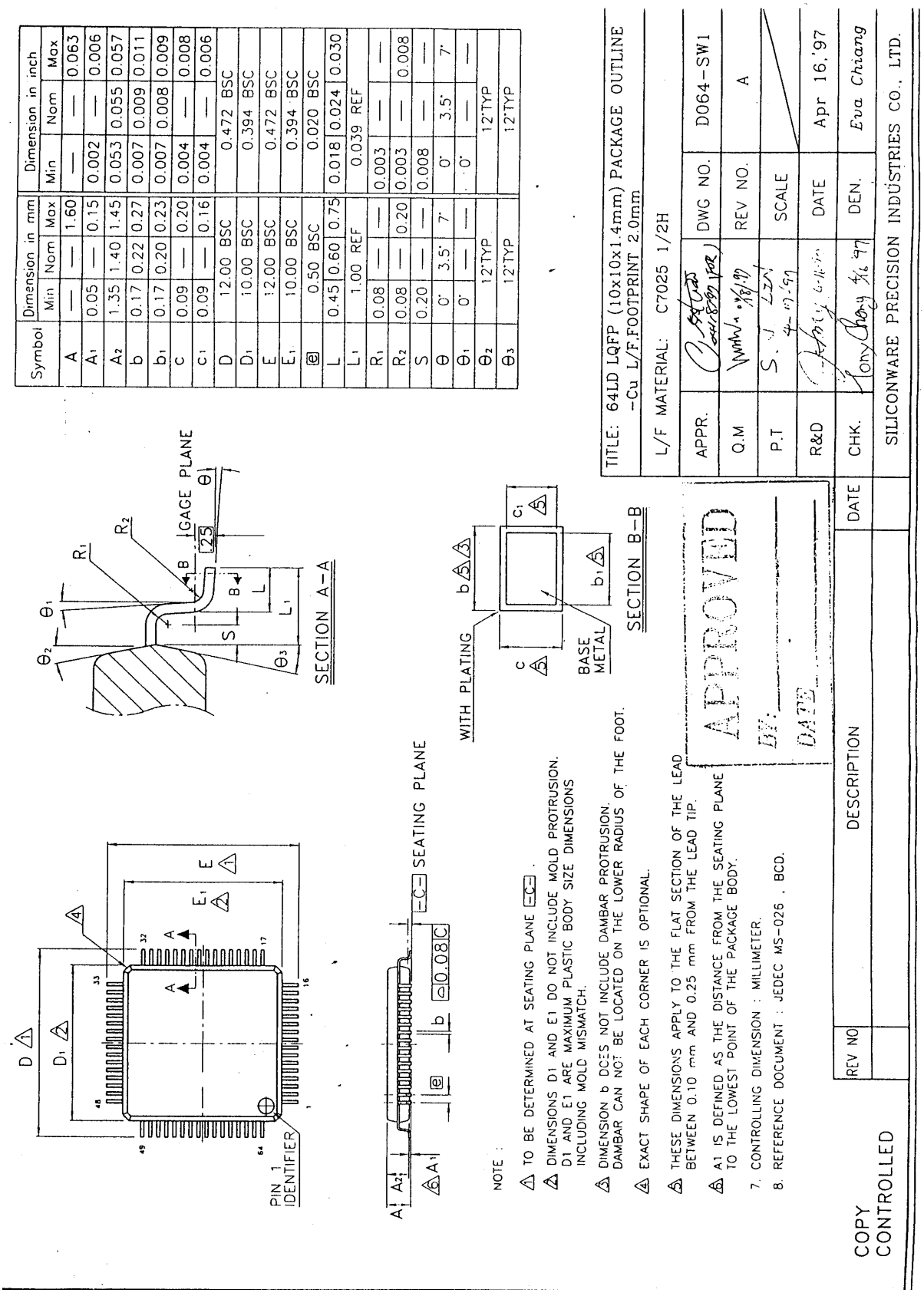
H. Package information



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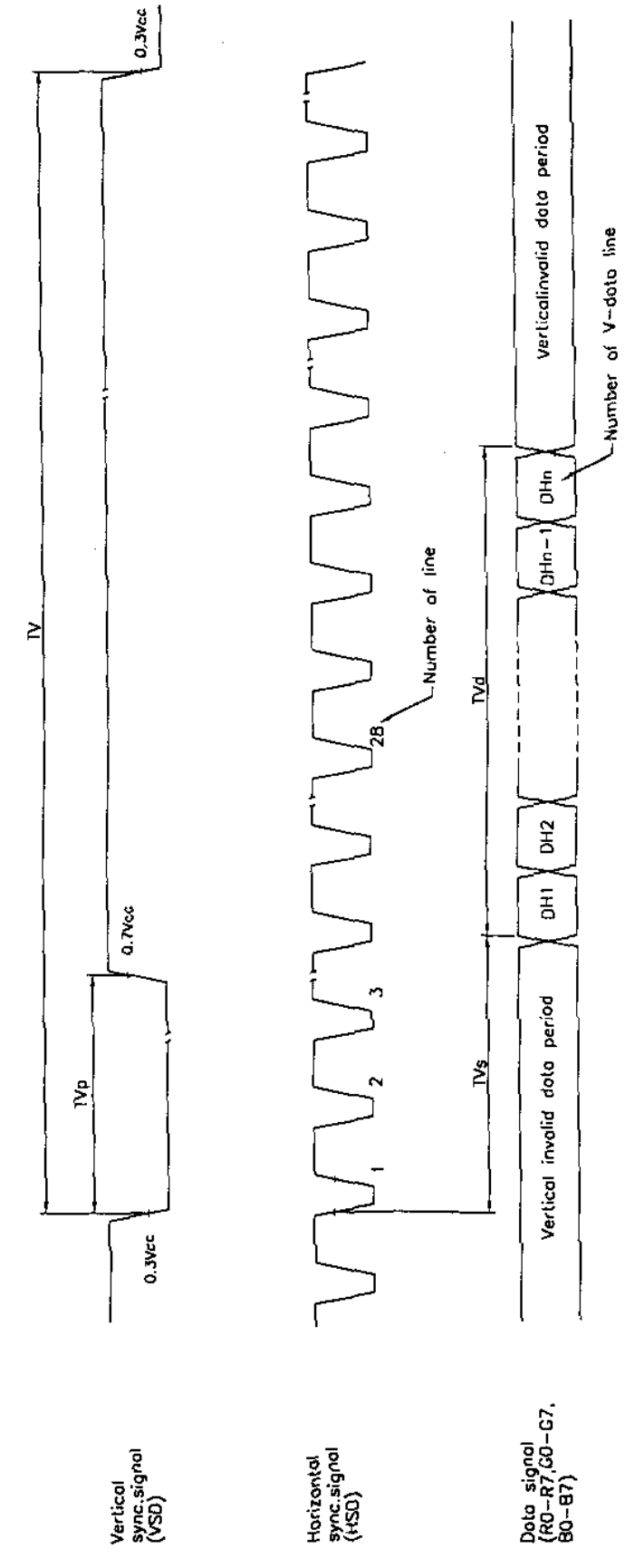

Fig.1 Input Vertical timing

File:f:\PDMEM0606\UP20DTC.dwg

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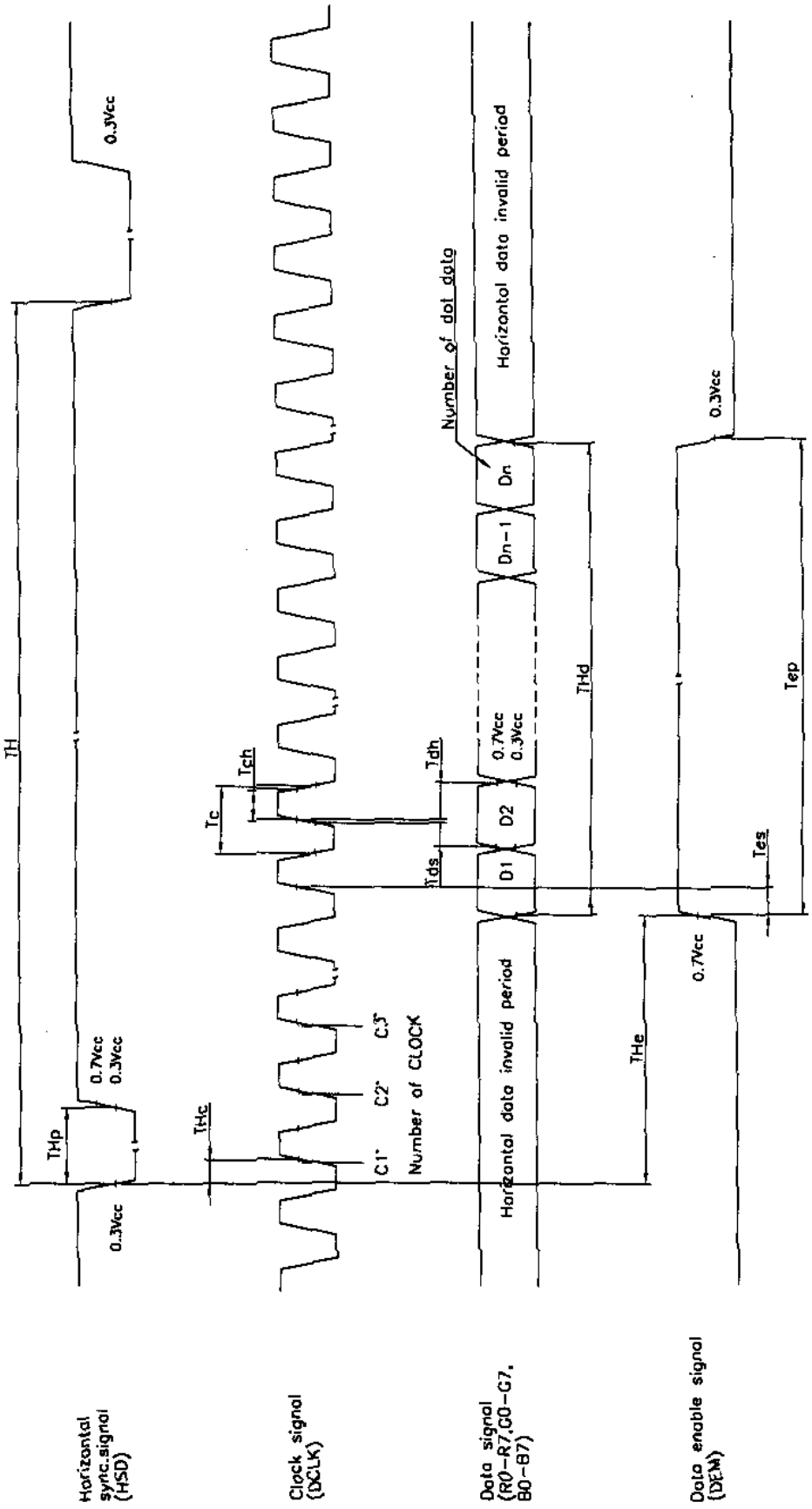

Fig.2 Input horizontal timing

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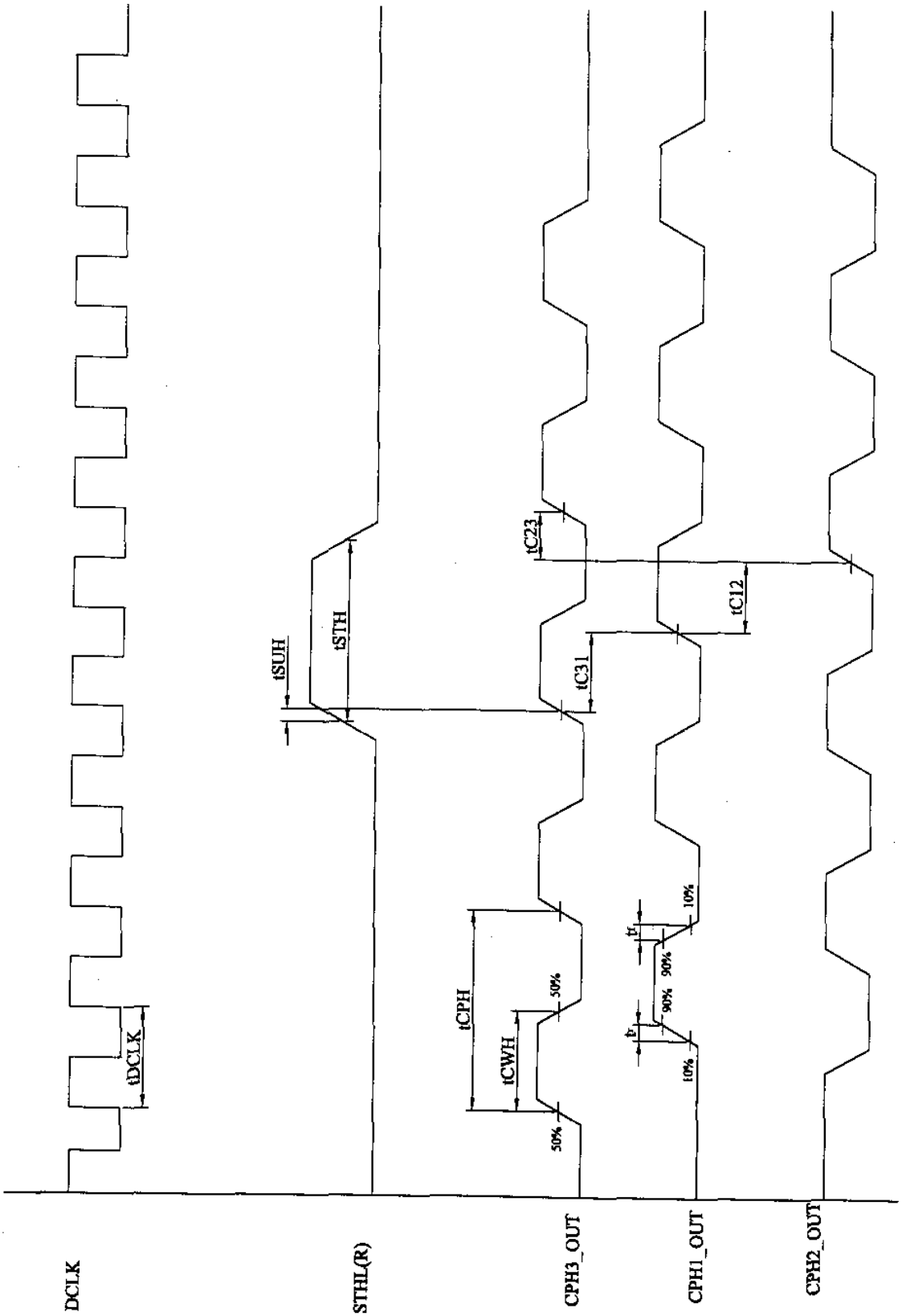

Fig.3 Sampling clock timing

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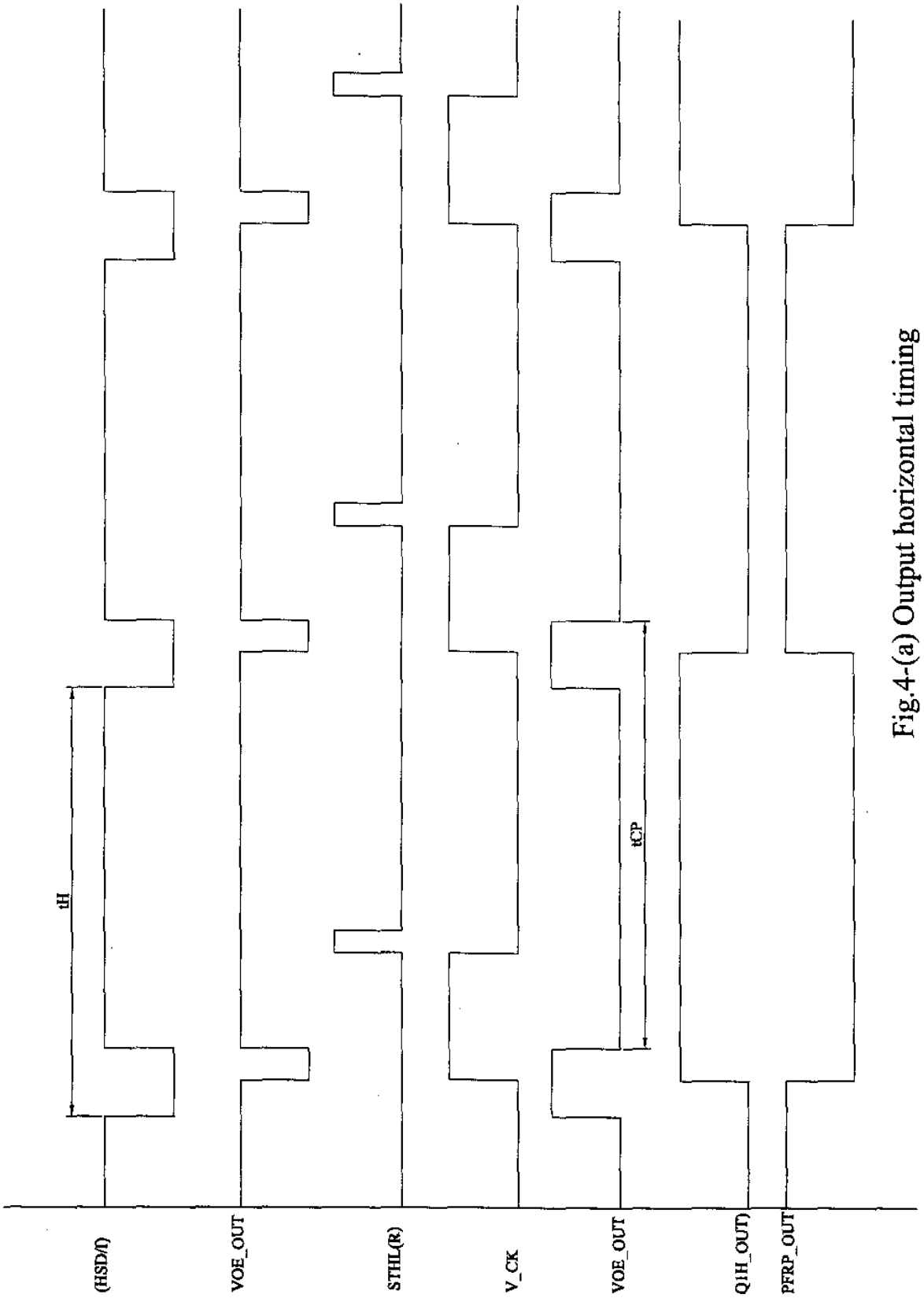

Fig.4-(a) Output horizontal timing

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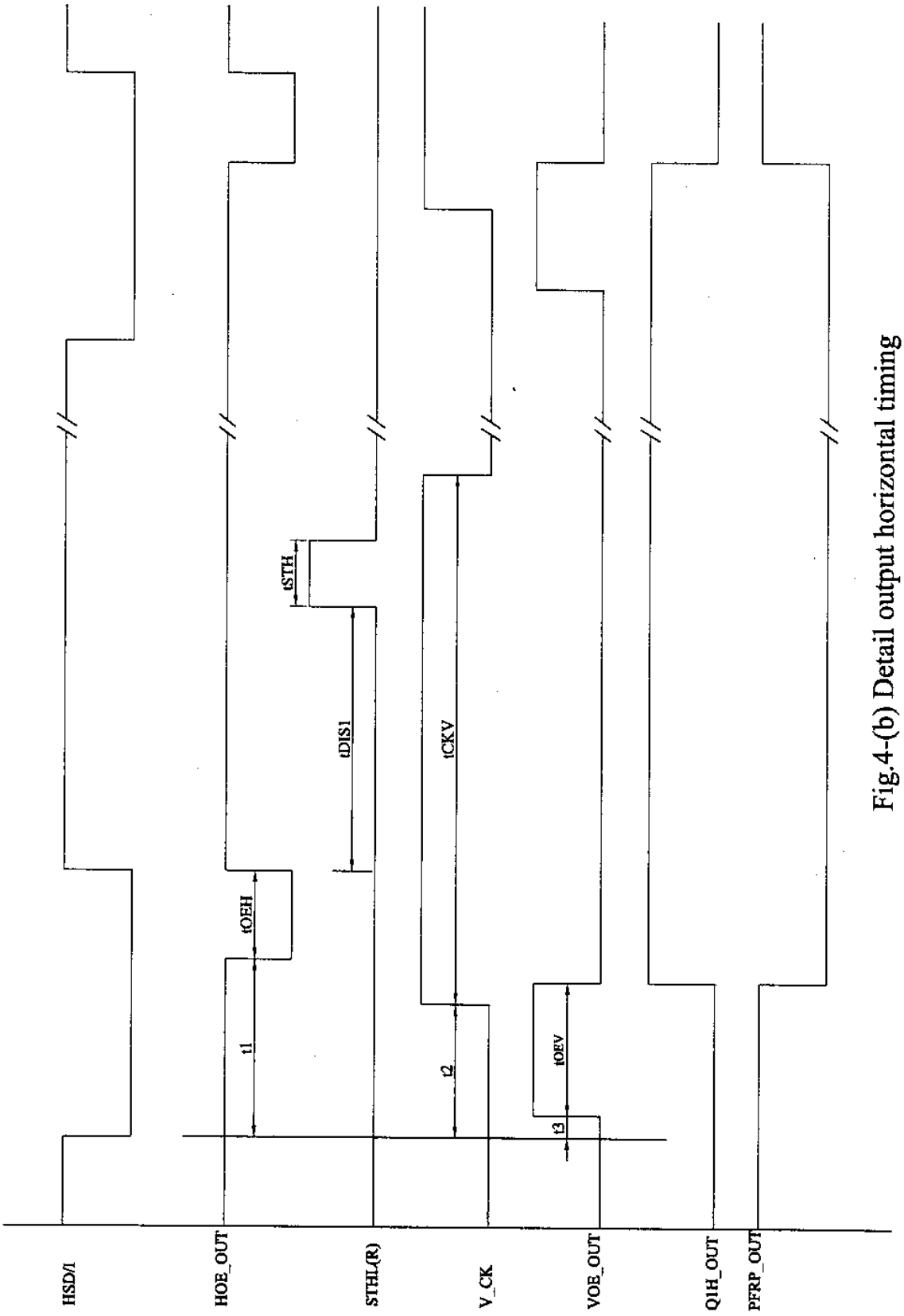

Fig.4-(b) Detail output horizontal timing

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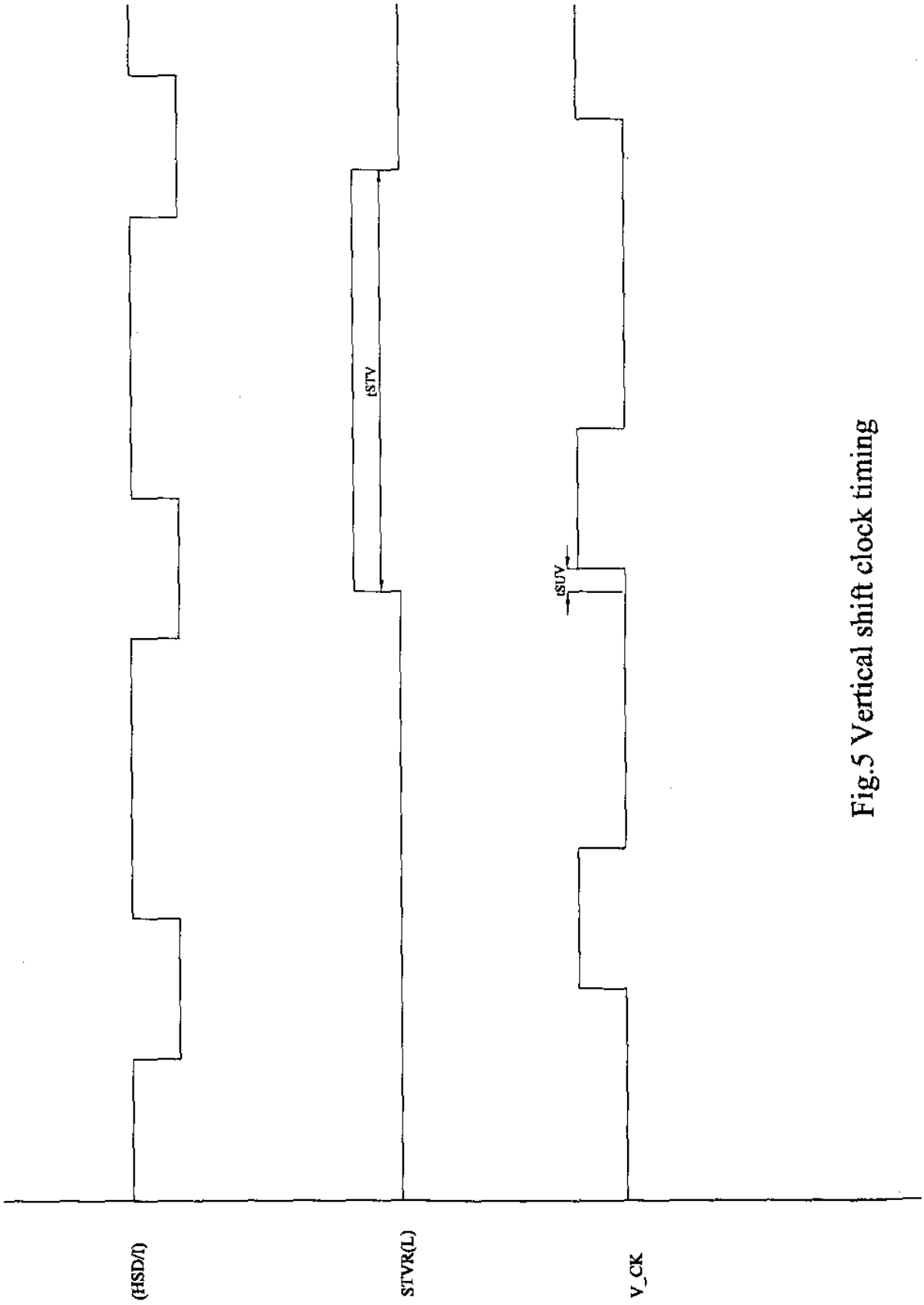

Fig.5 Vertical shift clock timing

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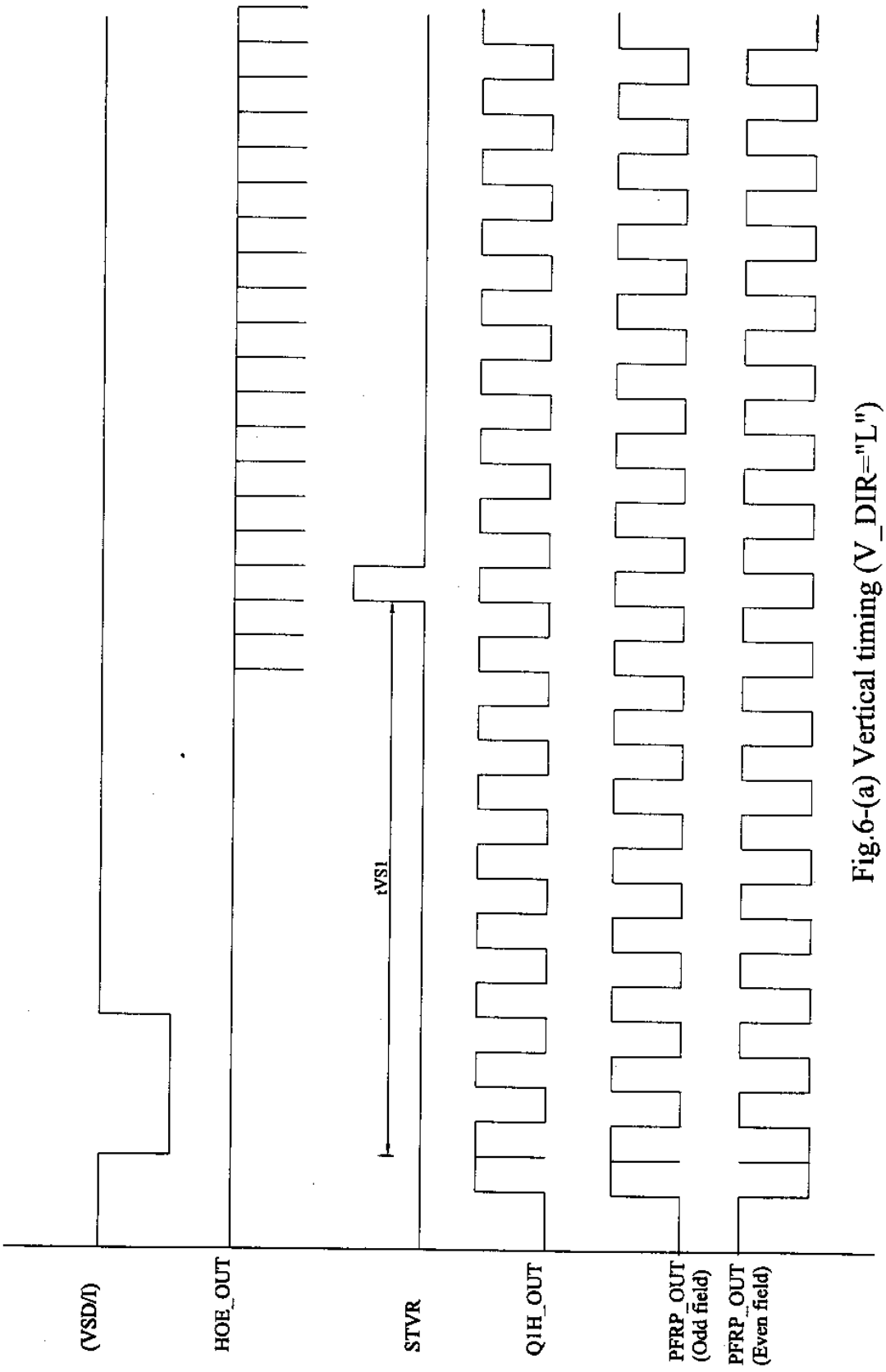

Fig.6-(a) Vertical timing (V_DIR="L")

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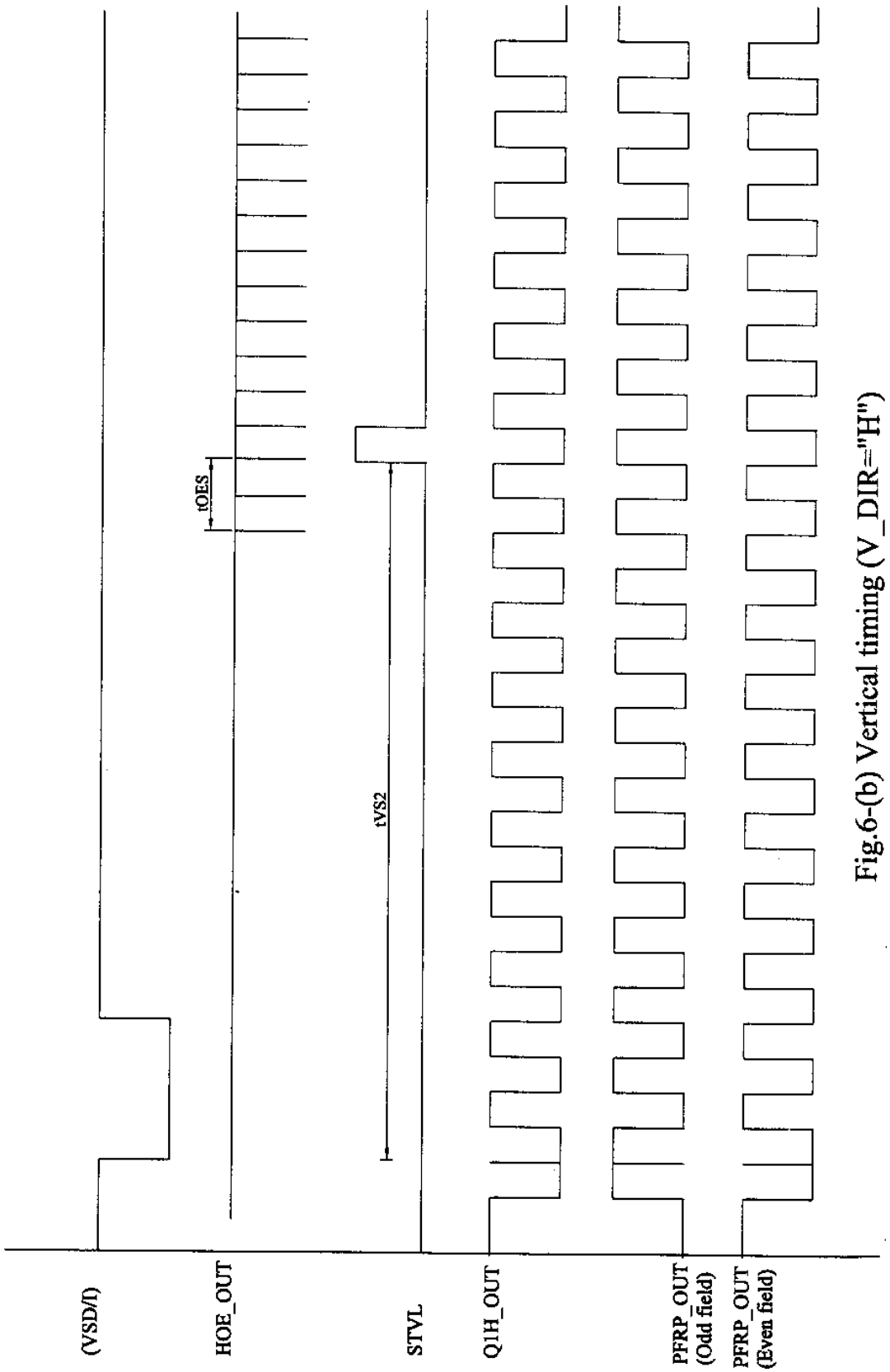

Fig.6-(b) Vertical timing (V_DIR="H")

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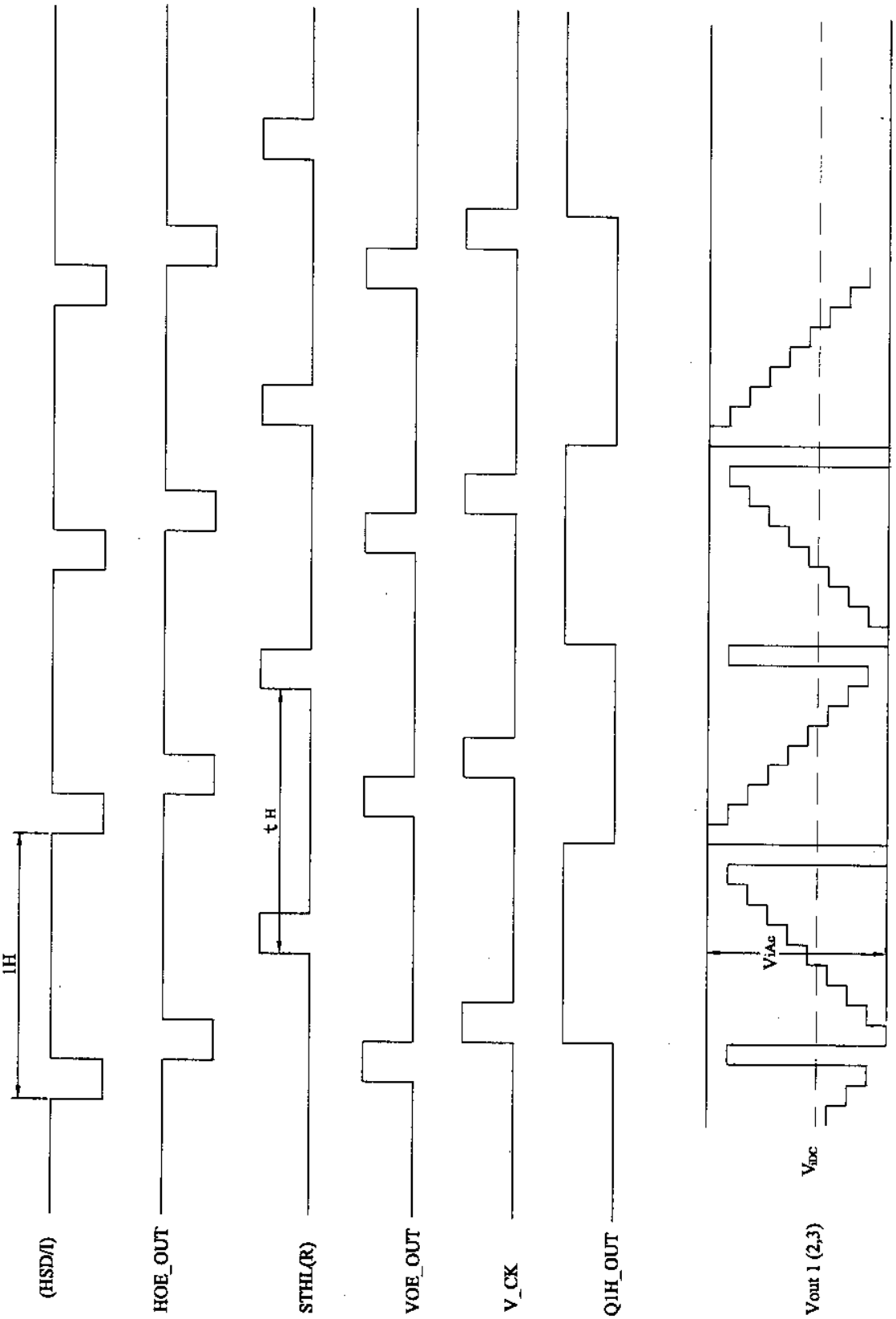

Fig.7 Vout 1(2,3) amplitude

ALL RIGHTS STRICTLY RESERVED. ANY PORTION OF THIS PAPER SHALL NOT BE REPRODUCED, COPIED, OR TRANSFORMED TO ANY OTHER FORMS WITHOUT PERMISSION FROM UNIPAC OPTOELECTRONICS CORP.

UNIPAC OPTOELECTRONICS CORPORATION
TERMS AND CONDITIONS OF SALE

These Terms and Conditions of Sale apply to all items designed and/or made by Unipac Optoelectronics Corporation ("Unipac"), and Buyer agrees they apply to all such items.

1 ACCEPTANCE OF TERMS. BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS SUPPLIED BY UNIPAC WITHIN 5 DAYS OF THEIR DELIVERY.

2 DELIVERY

2.1 Delivery will be made Free Carrier (Incoterms 1990), Unipac's warehouse, Science-Based Industrial Park, Taiwan to a carrier designated in writing by Buyer, or if Buyer fails to designate a carrier, to a carrier designated by Unipac.

2.2 Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.

2.3 Shipments are subject to availability. Unipac shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Unipac makes such effort, UNIPAC WILL NOT BE LIABLE FOR ANY DELAYS.

3 TERMS OF PAYMENT

3.1 Unless otherwise stated on Unipac's quotation, all shipments shall be T/T in advance, by Letter of Credit at Sight, or pursuant to agreed prepayment terms. Unipac reserves the right to change credit terms at any time in its sole discretion.

3.2 Buyer guarantees prompt payment of all obligations accrued pursuant to purchase orders issued by Buyer.

4 LIMITED WARRANTY

4.1 Unipac warrants that the goods sold will be free from defects in material and workmanship and comply with Unipac's applicable published specifications for a period of sixty (60) days from the date of Unipac's shipment.

4.2 Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in writing signed by Unipac). Unipac shall not be responsible for defects or claims caused by acts not performed by Unipac; or by combination of goods with other things.

4.3 No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation, weaponry or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Unipac from all claims, damages and liabilities arising out of any such uses.

4.4 This Article 4 is the only warranty by Unipac with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Unipac.

4.5 Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Unipac is not responsible for such things.

4.6 REGARDLESS OF CAUSE OR REASON FOR DAMAGE (WHETHER ACCIDENT, NEGLIGENCE, OR OTHERWISE) UNIPAC SHALL HAVE NO LIABILITY (DIRECT, CONSEQUENTIAL OR OTHER) FOR, IN CONNECTION WITH OR ARISING FROM PROPERTY FURNISHED FOR USE AT OR LEFT AT UNIPAC; and by delivering or entrusting property to Unipac, Buyer expressly confirms this limitation. Notwithstanding this limitation, Unipac will replace, or pay the reasonable retooling costs to replace, masks damaged or destroyed as a result of Unipac's gross negligence or fault.

4.7 EXCEPT AS PROVIDED ABOVE, UNIPAC MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND UNIPAC EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5 LIMITATION OF LIABILITY

5.1 Unipac will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, material shortage or labor conditions. In any such event, the date(s) for Unipac's performance will be deemed extended for a period equal to any delay resulting.

5.2 THE LIABILITY OF UNIPAC ARISING OUT OF THIS AGREEMENT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR (WITH UNIPAC'S PRIOR WRITTEN CONSENT) REPAIR OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO UNIPAC FREIGHT PRE-PAID); OR IN THE EVENT OF A FAILURE OR BREACH BY UNIPAC REGARDING DELIVERY, AN AMOUNT EQUAL TO THE TOTAL PURCHASE PRICE OF THE GOODS THAT HAVE NOT BEEN DELIVERED DUE TO SUCH FAILURE.

5.3 Buyer will not return any goods without first obtaining a customer return order number.

5.4 AS A SEPARATE LIMITATION, IN NO EVENT WILL UNIPAC BE LIABLE (i) FOR COSTS OF SUBSTITUTE GOODS, (ii) FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL, RELIANCE OR INDIRECT DAMAGES, OR (iii) FOR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, GOODWILL AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OR OF ANY FAILURE OR INADEQUACY OF ANY REMEDY. THIS AGREEMENTSTATES THE ONLY AND EXCLUSIVE REMEDY FOR ANY AND ALL CLAIMS MADE AGAINST UNIPAC UNDER ANY AGREEMENT AND/OR WITH RESPECT TO PANELS, COMPONENTS, SERVICES AND/OR GOODS.

5.5 No action or proceeding may be commenced by either party against the other (other than to collect money due for goods delivered or services rendered), whether for breach, indemnification, contribution or otherwise, more than one year after delivery of the goods to the carrier; and no claim may be brought unless the non-claiming party has first been given commercially reasonable notice, a full written explanation of all pertinent details (including copies of all materials), and a good faith opportunity to resolve the matter.

5.6 BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF ARTICLES 5, 8 AND 9 AND TO THEIR REASONABLENESS.

5.7 The exclusions and limitations of Articles 5, 8 and 9 will survive the termination of the applicable Agreements, and shall apply notwithstanding any claim of a failure of any one or more remedies to accomplish their purpose, and THE PARTIES EXPRESSLY WAIVE AND RELINQUISH ANY CONTRARY RIGHTS UNDER ANY AGREEMENT, AND/OR LAW, DECISION, CUSTOM OR PRACTICE.

6 SUBSTITUTIONS AND MODIFICATIONS

Unipac may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Unipac reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing. Other changes to process and/or specifications by Unipac shall be pursuant to Unipac's standard ECN procedures.

7 CANCELLATION

7.1 This Agreement may not be canceled by Buyer except with written consent by Unipac and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Unipac, and a reasonable profit).

7.2 In no event will Buyer have rights in partially completed goods.

8 INDEMNIFICATION

8.1 Unipac will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Unipac under this purchase order infringe any valid, enforceable, unexpired R.O.C. patent, copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Unipac, (ii) permits Unipac to participate and to defend if Unipac requests to do so, and (iii) gives Unipac all needed information, assistance and authority. However, Unipac will not be responsible for infringements resulting from anything not entirely manufactured by Unipac, or from any combination with products, equipment, or materials not furnished by Unipac. Unipac will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

8.2 Except as expressly stated in this Article 8 or in another writing signed by an authorized officer, Unipac makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement.

8.3 Except as to claims Unipac agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS UNIPAC FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9 NO CONFIDENTIAL INFORMATION

Unipac shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10 ENTIRE AGREEMENT

These terms and conditions are the entire agreement between Unipac and Buyer, and no addition, deletion or modification shall be binding on Unipac unless expressly agreed to in a writing signed by an officer of Unipac. Buyer is not relying upon any warranty or representation except for those specifically stated here.

11 APPLICABLE LAW

This Agreement and all performance and disputes arising out of or relating to goods involved will be governed by the laws of Taiwan, Republic of China, without reference to conflict of laws principles and excluding the U.N. Convention on Contracts for the International Sale of Goods. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder.

12 DISPUTE RESOLUTION

12.1 Buyer and Unipac shall cooperate and attempt in good faith to resolve any and all disputes arising out of and/or relating to this Agreement and/or goods furnished pursuant to this Agreement.

12.2 Any disputes relating to and/or arising out of any Agreement and/or goods furnished pursuant to this Agreement that cannot be so resolved will be decided exclusively by binding arbitration. Such arbitration shall take place in Taipei, Taiwan pursuant to the Rules for International Arbitrations under the American Arbitration Association.

12.3 Notwithstanding anything to the contrary, any party may apply to any court of competent jurisdiction for interim injunctive relief with respect to irreparable harm which cannot be avoided and/or compensated by such arbitration proceedings, without breach of this Article 12 and without any abridgment of the powers of the arbitrators.

13 ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving the enforcement or interpretation of this Agreement.